CS244 Reproducing Network Research Proposal
Spring 2017

Primary Proposal

Students:
Kate Stowell <kstowell@stanford.edu>
Travis Lanham <tlanham@stanford.edu>

Paper:
The iSLIP Scheduling Algorithm for Input-Queued Switches.
IEEE/ACM TRANSACTIONS ON NETWORKING, VOL. 7, NO. 2, APRIL 1999.

Author:
Nick McKeown, Stanford University

Description:
The paper outlines an algorithm for input-queued switch scheduling that the author calls iSLIP. The algorithm is designed to achieve high throughput while solving arrival burstiness issues found in PIM, a previous iterative switch scheduling algorithm.

Result to Reproduce:
The main result of the paper is the performance of iSLIP versus other switch scheduling algorithms, particularly those that also address the issue of head of line blocking (e.x. PIM). We intend to reproduce the performance graph (Figure 5) that shows how iSLIP outperforms PIM and RRM.

Implementation Plan:
For implementation, we intend to rely on a simulator for switch scheduling that will allow provide performance data for each of the scheduling algorithms. We have not been able to find available simulators that provide the scheduling abstraction we are looking for so we anticipate that the bulk of our work will be in creating the simulator.

Mininet does not allow for control over the scheduling algorithm that the virtual switches use; similarly, other emulators/simulators that target networks allow for reconfigurable topologies but not at the switch design level itself. It seems likely that industrial quality simulators exist for modeling switch scheduling behavior but are proprietary to switch makers since network operators care about switch performance but not implementation. Similarly, programmable data plane abstractions like p4 provide programmability for packet processing but not how the switch itself works.

Backup Proposal

Paper:
A Quantitative Comparison of Iterative Scheduling Algorithms for Input-Queued Switches.
http://yuba.stanford.edu/~nickm/papers/Comparison.pdf

Authors:
Nick McKeown (Stanford University), Thomas E. Anderson (The University of California at Berkeley)

Description:
The paper performs a quantitative comparison of iterative switch scheduling algorithms. The main result is an examination of the performance of the iLRU scheduling algorithm against iSLIP, PIM, theoretical maximal match, theoretical output queuing, and FIFO. These are iterative algorithms designed to be easily implemented in hardware to achieve high throughput. The authors focuses on input-queued switches for performance reasons to achieve 100s of millions of scheduling decisions per second.

Result to Reproduce:
The focus will be to reproduce the results from the paper's comparison of matchings made based on randomness, iterative round robin matching, and least recently used output. In particular, we intend to reproduce figure 10, which compares iLRU to several algorithms (FIFO, PIM, maximum size matching, output queueing) under uniform workload and Bernoulli arrivals.

Implementation Plan:
Since the papers address similar experimental results, our implementation plan is almost identical to the primary proposal. We would build a software switch simulator (similar to mininet but with a small subset of features focused on emulating switch behavior with a modular, replaceable scheduling policy). Again, we have not been able to find switch simulators that provide a scheduling abstraction, instead most focus on the network topology abstraction.