Version: 2.0

Technical Specification

MODEL NO: VD1405-FOA (ED060XCG)

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approved By 黃禎華

Confirmed By 莊博鈞

Prepared By 黃志彬

Revision History

Rev.	Issued Date	Revised Contents
1.0	2020-08-05	New
2.0	2021-06-07	Electrical Characteristics: remove VDD 1.8V

TECHNICAL SPECIFICATION

CONTENTS

1. Application

VD1405-FOA is a reflective electrophoretic E Ink® technology display module. It is based on active matrix TFT substrate. It has 6” active area, the display is capable to display images at 2-16 gray levels (1-4 bits) depending on the display controller and the associated waveform file it used.

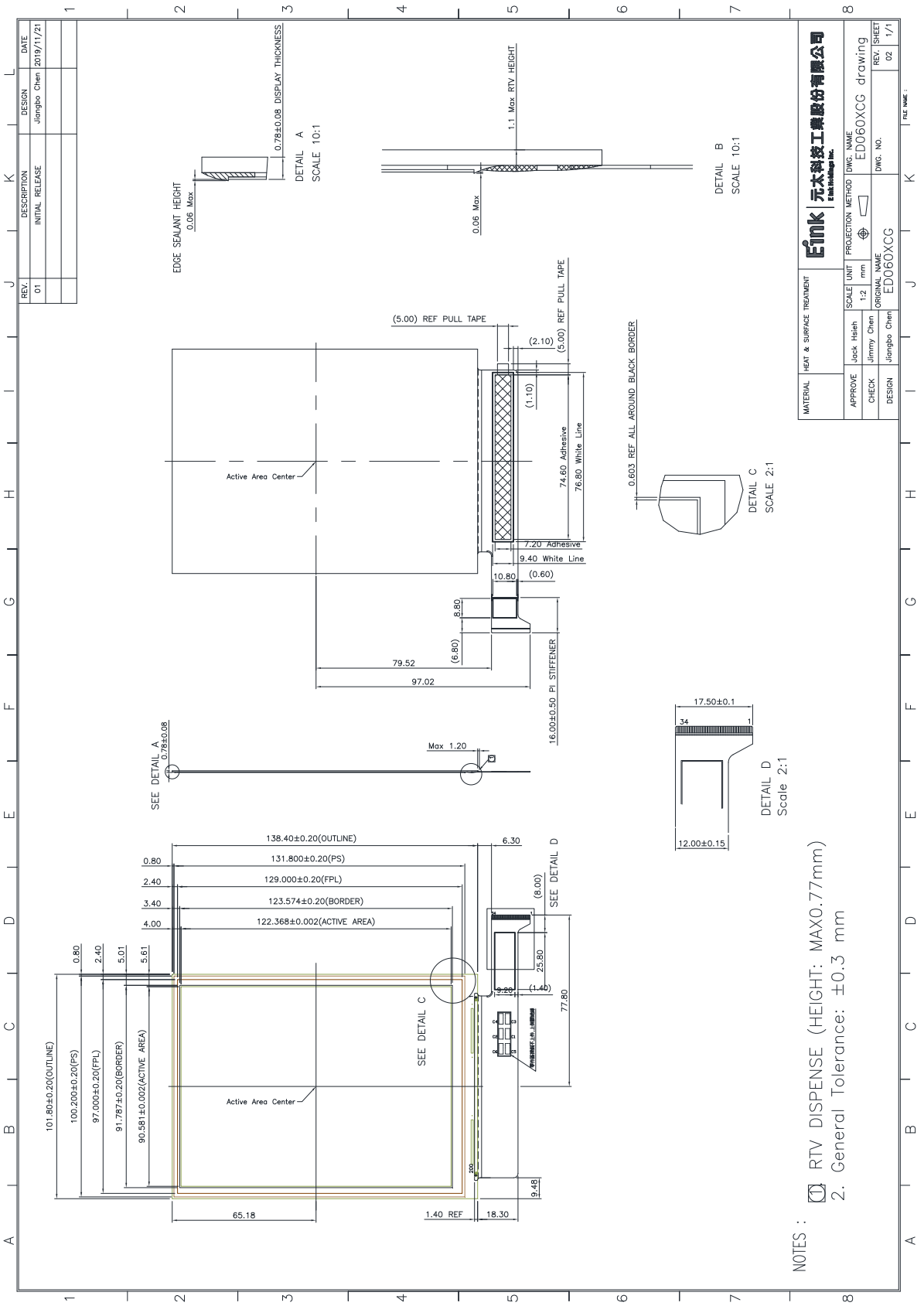
2. Features

- High contrast reflective/electrophoretic technology
- Bi-stable
- Glass TFT
- Wide viewing angle
- Low power consumption
- Pure reflective mode
- Portrait and landscape mode
- Commercial temperature range

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	6 (3:4 diagonal)	Inch	
Display Resolution	758 (H)×1024 (V)	Pixel	212dpi
Active Area	90.581 (H)×122.368 (V)	mm	
Pixel Pitch	0.1195 (H)x0.1195 (V)	mm	
Outline Dimension	101.8 (W)×138.4 (H)×0.78 (D)	mm	
Module Weight	23.09± 2.3	g	
Number of Gray	16 Gray Level (monochrome)		

4. Mechanical Drawing of EPD Module



5. Output Interface

5-1) Recommended Connector Type of Panel

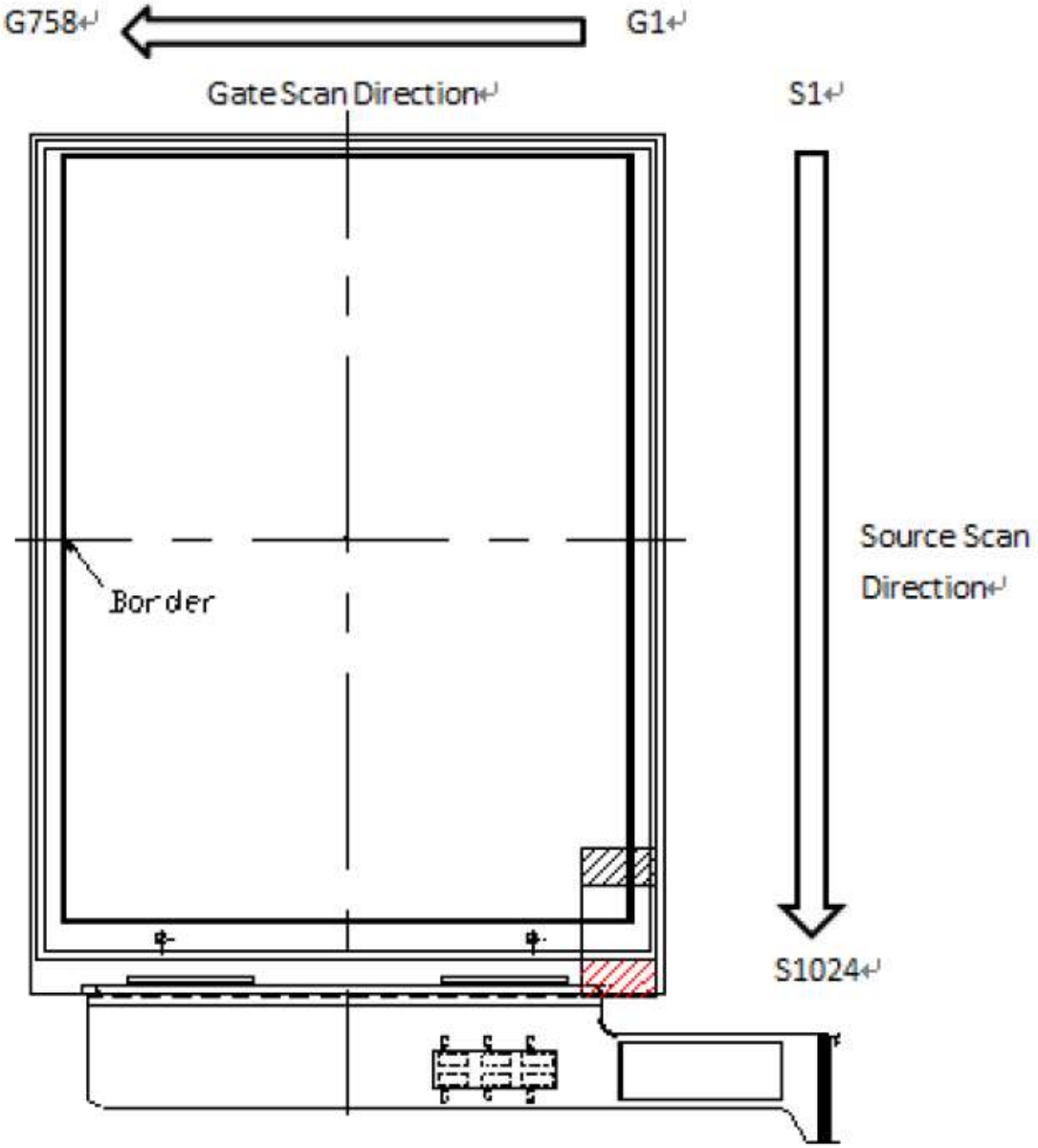
FH34S-34S-0.5SH(50)-Hirose

5-2) Pin Assignment of Panel

Pin #	Signal	I/O	Description	Remark
1	VSL	P	Negative power supply source driver	Note1
2	VGL	P	Negative power supply gate driver	Note1
3	VSS	P	Ground	Note1
4	NC	-	No Connection	
5	NC	-	No Connection	
6	VDD	P	Digital power supply drivers	Note1
7	VSS	P	Ground	Note1
8	CKH	I	Clock source driver	
9	VSS	P	Ground	Note1
10	LEH	I	Latch enable source driver	
11	OEH	I	Output enable source driver	
12	SPH	I	Start pulse source driver	
13	D0	I	Data signal source driver(LSB)	
14	D1	I	Data signal source driver	
15	D2	I	Data signal source driver	
16	D3	I	Data signal source driver	
17	D4	I	Data signal source driver	
18	D5	I	Data signal source driver	
19	D6	I	Data signal source driver	
20	D7	I	Data signal source driver(MSB)	
21	VCOM	P	Common voltage	Note1
22	NC	-	No Connection	
23	NC	-	No Connection	
24	NC	-	No Connection	
25	NC	-	No Connection	
26	VSS	P	Ground	Note1
27	OEV	I	Output mode selection gate driver	
28	CKV	I	Clock gate driver	
29	SPV	I	Start pulse gate driver	
30	NC	-	No Connection	
31	Border	I	Border connection	
32	VSS	P	Ground	Note1
33	VSH	P	Positive power supply source driver	Note1
34	VGH	P	Positive power supply gate driver	Note1

Note1: P Power pin

5-3) Panel Scan Directions



5-4) The relationship of input data and output

Output	S1	S2	S3	S4
Data	D7	D5	D3	D1
	D6	D4	D2	D0

6. Electrical Characteristics

6-1) Absolute Maximum Ratings of panel only:

Parameter	Symbol	Rating	Unit	Remark
Logic Supply Voltage	VDD	-0.3 to +5.0	V	--
Positive Supply Voltage	V_{SH}	-0.3 to +18.0	V	--
Negative Supply Voltage	V_{SL}	+0.3 to -18.0	V	--
Max .Drive Voltage Range	$V_{SH} – V_{SL}$	36.0	V	--
Supply Voltage	VGH	-0.3 to VGL+50.0	V	--
Supply Voltage	VGL	-25.0 to +0.3	V	--
Supply Range	VGH-VGL	10.0 to +45.0	V	--
Operating Temp. Range	TOTR	0 to +50	℃	--
Storage Temperature	TSTG	-25 to +70	℃	--

6-2) Panel DC Characteristics (Note. 1)

Parameter	Symbol	Conditions	Min	Typ(Note 3)	Max(Note 2)	Unit
Signal ground	VSS		-	0.0	-	V
Logic Voltage supply	VDD		3	3.3	3.6	V
	I_{VDD}	VDD=3.3V	-	3.7	4.4	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}	VGL = -20V	-	3.2	9.8	mA
Gate Positive supply	VGH		21	22	23	V
	I_{GH}	VGH = 22V	-	2.7	3.9	mA
Source Negative supply	VSL		-15.4	-15	-14.6	V
	I_{SL}	VSL = -15V	-	10.4	55.9	mA
Source Positive supply	VSH		14.6	15	15.4	V
	I_{SH}	VSH = 15V	-	10.3	59.9	mA
Border supply	VCOM		-4	Adjusted	-0.2	V
Asymmetry source	V_{Asym}	VSH+VSL	-800	0	800	mV
Common voltage	VCOM		-4	Adjusted	-0.2	V
	I_{COM}		-	1.4	-	mA
Panel Power	P			446.2	2033.4	mW
Standby power panel (Note 4)	P_{STBY}		-	-	0.4	mW

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	ISH	VSH = 15V	-		250.4	mA
	ISL	VSL = -15V	-		221.0	mA
	IGH	VGH = 22V	-		58.0	mA
	IGL	VGL =-20V	-		145.6	mA
	ICOM	--	-		148.8	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input “H” voltage	VIH	--	0.8VDD		VDD	V
Digital Input “L” voltage	VIL	--	GND		0.2VDD	V

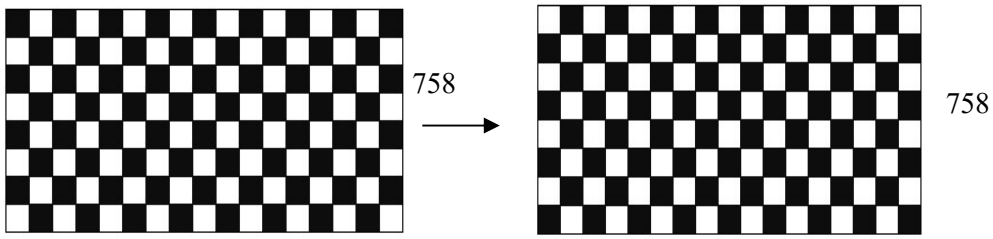
Note :

1. The power consumption in this field is provided for the purpose as the follows:
   1-1. The selection of suitable PMIC in the market to drive EPD normally.
   1-2. Estimation of voltage-drop at input side of PMIC for setting of threshold-voltage of battery.
2. The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
3. The Typical average current for power consumption is measured using 85 Hz waveform with following pattern transition:
   3-1. For displaying with grayscale image, it is from horizontal 4 gray scale pattern to vertical 4 gray scale pattern without dithering process. (Note 6-2)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using 85 Hz waveform with following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform provided by E Ink.
7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3054)

Note6-1

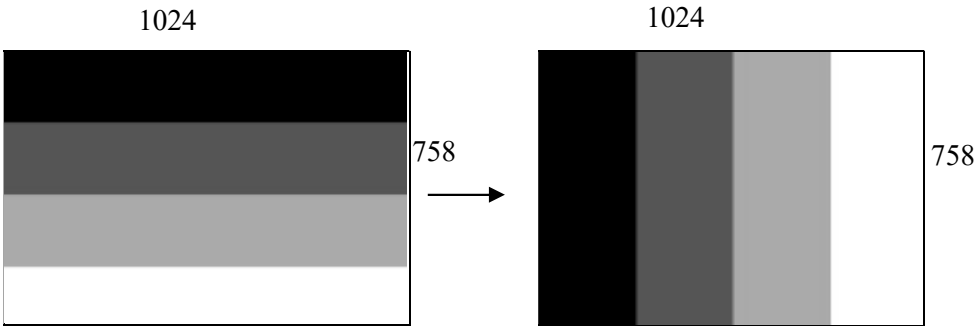
The maximum average current and Maximum Currents for B/W

1024 1024



Note6-2

The typical power consumption for B/W display



Note6-3

The decoupling capacitors on each power rail for Max. Currents

Power rail	Capacitors suggested (uF / Tolerance)
ISH	4.7uF x 2pcs / ±10%
ISL	4.7uF x 2pcs / ±10%
IGH	2.2 uF x 1 pcs / ±10%
IGL	4.7uF x 1 pcs / ±10%
IDD	4.7uF x 1 pcs / ±10%

6-3) Panel DC Characteristics for Device Battery-Life Estimation (Note.1)

Parameter	Symbol	Conditions	Min	Typ(Note 3)	Max(Note 2)	Unit
Signal ground	VSS		-	0.0	-	V
Logic Voltage supply	VDD		3	3.3	3.6	V
	I_{VDD}	V_{DD}=3.3V	-	3.7	2.4	mA
Gate Negative supply	VGL		-21	-20	-19	V
	I_{GL}	VGL = -20V	-	3.2	6.3	mA
Gate Positive supply	VGH		21	22	23	V
	I_{GH}	VGH = 22V	-	2.7	1.3	mA
Source Negative supply	VSL		-15.4	-15	-14.6	V
	I_{SL}	V_{SL} = -15V	-	4.2	24.5	mA
Source Positive supply	VSH		14.6	15	15.4	V
	I_{SH}	V_{SH} = 15V	-	3.4	25.9	mA

Border supply	VCOM		-4	Adjusted	-0.2	V
Asymmetry source	V_{Asym}	V_{SH}+VSL	-800	0	800	mV
Common voltage	VCOM		-4	Adjusted	-0.2	V
	I_{COM}		-	1.4	-	mA
Panel Power	P			249.7	918.6	mW
Standby power panel (Note 4)	P_{STBY}		-	-	0.4	mW

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Currents (Note 5)	ISH	V_{SH} = 15V	-		250.4	mA
	ISL	V_{SL} = -15V	-		221.0	mA
	IGH	V_{GH} = 22V	-		58.0	mA
	IGL	V_{GL} =-20V	-		145.6	mA
	ICOM	--	-		148.8	mA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Digital Input “H” voltage	VIH	--	0.8VDD		VDD	V
Digital Input “L” voltage	VIL	--	GND		0.2VDD	V

Note :

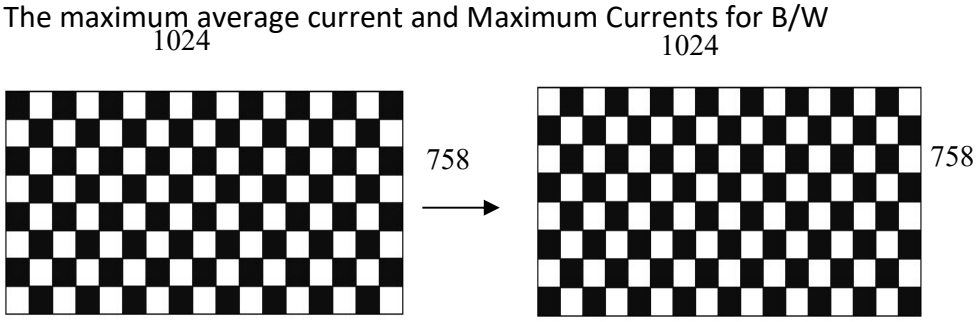
1. The power consumption in this field is measured in whole updated time by 350ms (at 25 degree C) for device battery life estimation.
2. The maximum average Currents for power consumption are measured using 85 Hz waveform with following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
3. The Typical average current for power consumption is measured using 85 Hz waveform with following pattern transition:
   3-1. For displaying with grayscale image, it is from horizontal 4 gray scale pattern to vertical 4 gray scale pattern without dithering process. (Note 6-2)
4. The standby power is the consumed power when the panel controller is in standby mode.
5. The Maximum Currents are measured using 85 Hz waveform with following pattern transition in both B/W: from black and white single checker pixel pattern to inversed black and white single checker pixel pattern. (Note 6-1)
   - It is performed with decoupling capacitors on each power rail as below table (Note 6-3).
   - The minimum value in table of Maximum current is produced by charging mechanism between decoupling capacitors.
6. The listed electrical/optical characteristics are only guaranteed under the controller and waveform

provided by E Ink.

7. Vcom is recommended to be set in the range of assigned value ± 0.1 V
8. Use of measuring instruments: Oscilloscope (Model: Tektronix MDO3054)

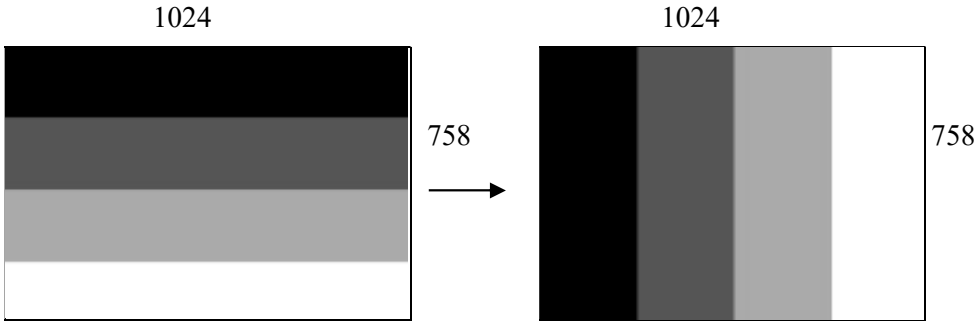
Note6-1

The maximum average current and Maximum Currents for B/W



Note6-2

The typical power consumption for B/W display



Note6-3

The decoupling capacitors on each power rail for Max. Currents

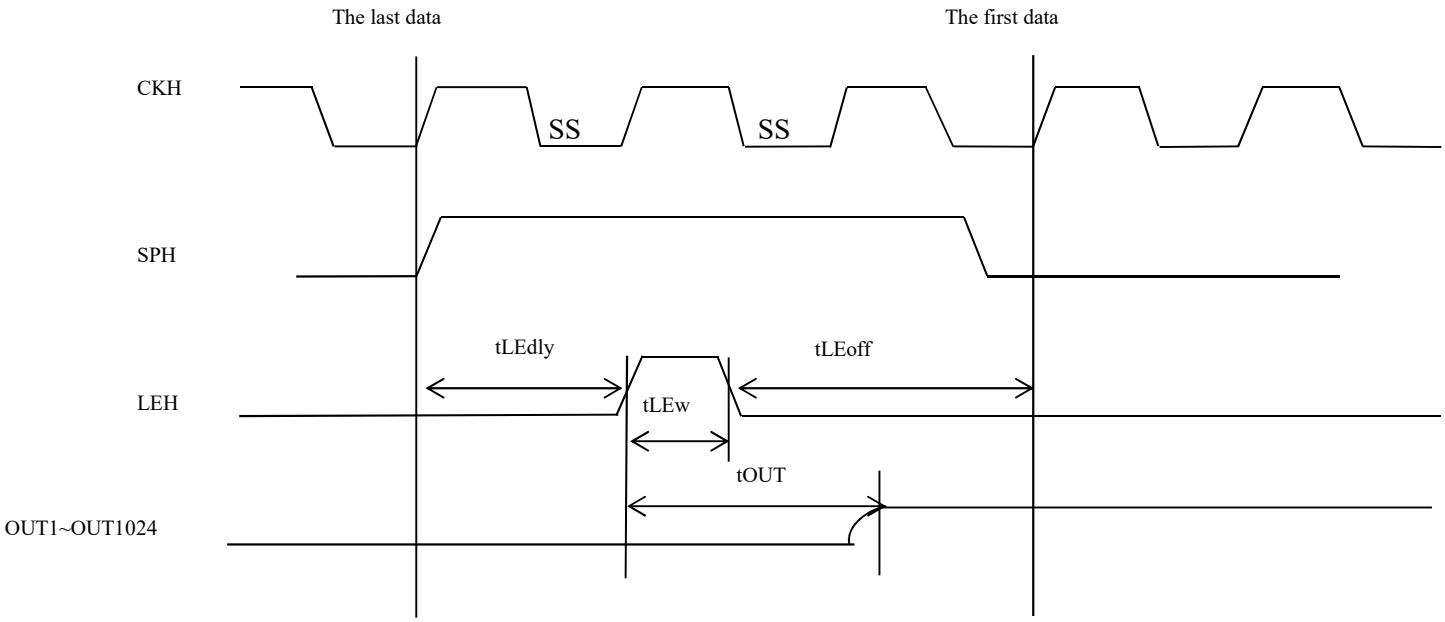
Power rail	Capacitors suggested (uF / Tolerance)
ISH	4.7uF x 2pcs / ±10%
ISL	4.7uF x 2pcs / ±10%
IGH	2.2 uF x 1 pcs / ±10%
IGL	4.7uF x 1 pcs / ±10%
IDD	4.7uF x 1 pcs / ±10%

6-4) Panel AC characteristics:

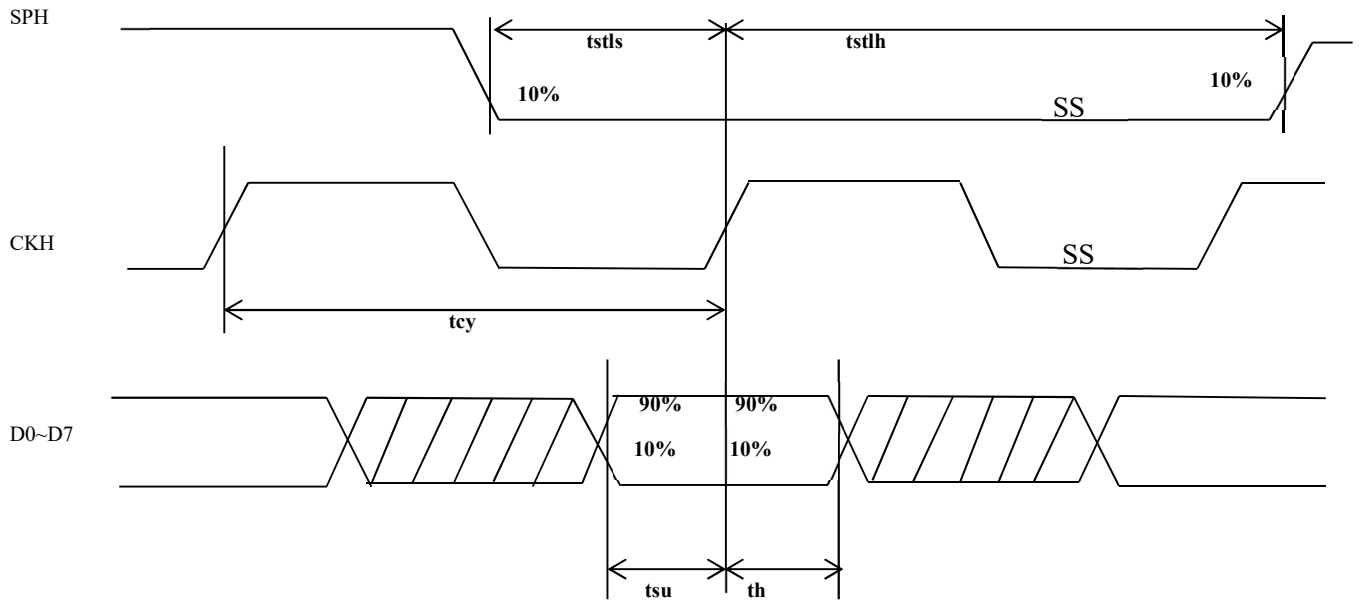
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
Clock frequency	fckv	-	-	200	kHz
Minimum “L” clock pulse width	twL	0.5			us
Minimum “H” clock pulse width	twH	0.5			us
Clock rise time	trckv	-	-	100	ns
Clock fall time	tfckv	-	-	100	ns
SPV setup time	tSU	100	-	twH-100	ns

SPV hold time	tH	100	-	twH-100	ns
Pulse rise time	trspv	-	-	100	ns
Pulse fall time	tfspv	-	-	100	ns
Clock CKH cycle time	tcy	16.6	-	-	ns
D0 .. D7 setup time	tsu	8	-	-	ns
D0 .. D7 hold time	th	8	-	-	ns
SPH setup time	tstls	8	-		ns
SPH hold time	tstlh	8	-		ns
LEH on delay time	tLEdly	40	-	-	ns
LEH high-level pulse width (When VDD=3.0V to 3.6V)	tLEw	150	-	-	ns
LEH off delay time	tLEoff	200	-	-	ns
Output setting time to +/- 30mV(C_{load}=200pF)	tout	-	-	12	us

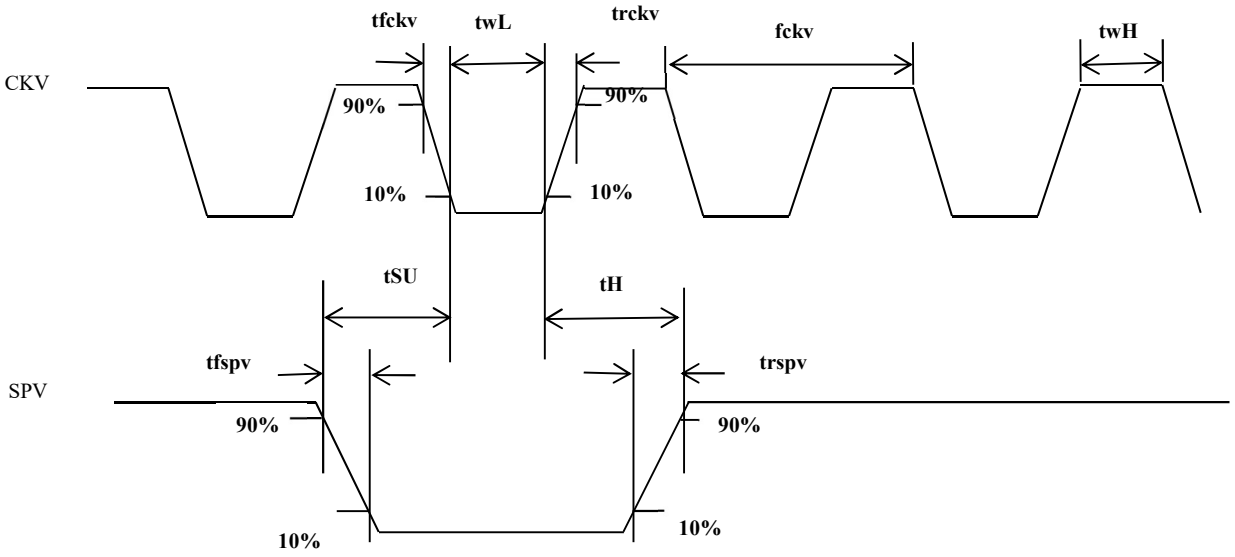
OUTPUT LATCH CONTROL SIGNALS



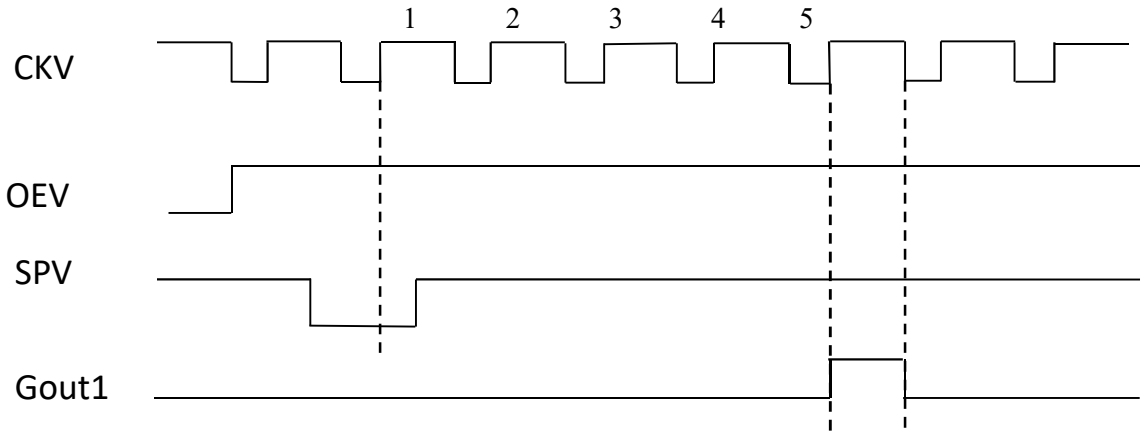
CLOCK & DATA TIMING



CKV & SPV TIMING



GATE OUTPUT TIMING



Note：The 1st Gate line(Gout1) is output based on above timing of "GATE OUTPUT TIMING"

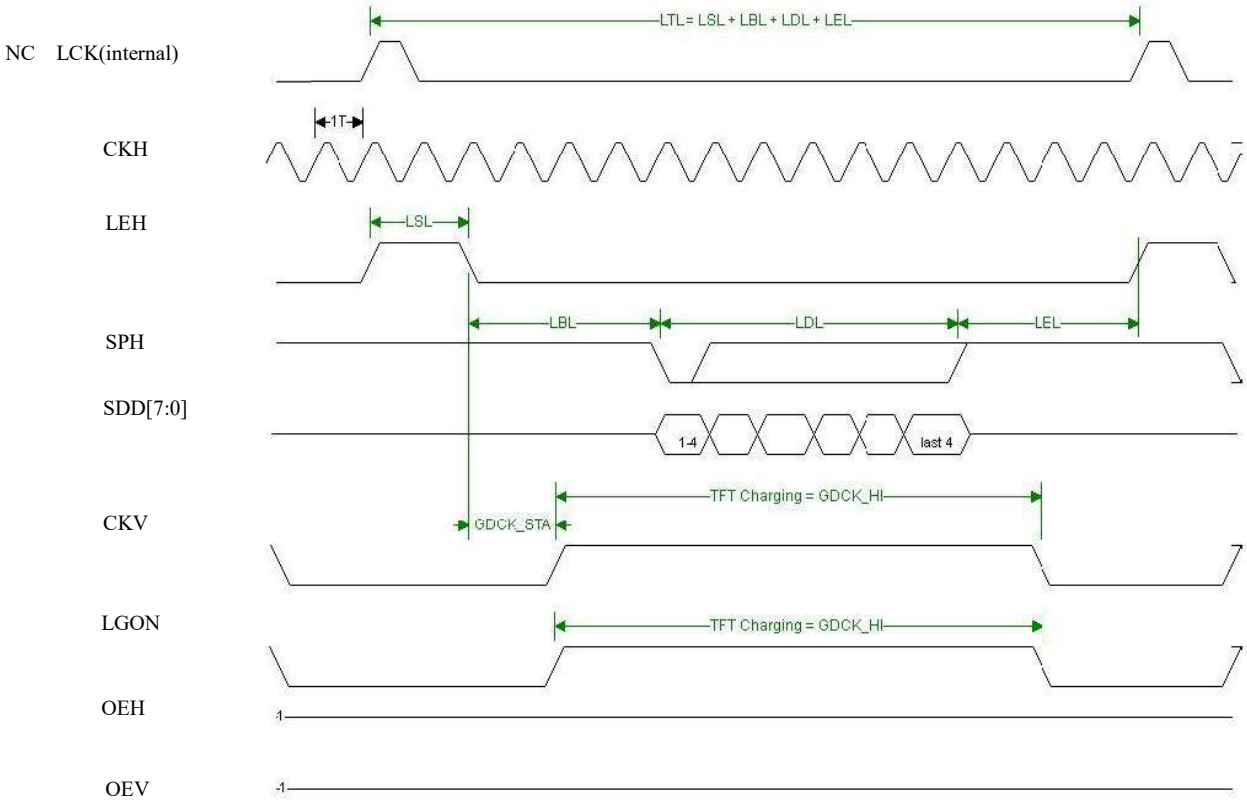
6-5) Refresh Rate

The module applied at a maximum refresh rate of 85 Hz.

	Min	Max
Refresh Rate	-	85 Hz

6-6) Controller Timing

This timing mode is depicted on Figure 1 and Figure 2 and it refers to timing of Source Driver Output Enable (OEH) and Gate Driver Clock (CKV). Note, that in this mode LGON follows CKV timing



Note: LCK is an internal signal and it is shown for reference only

Figure 1

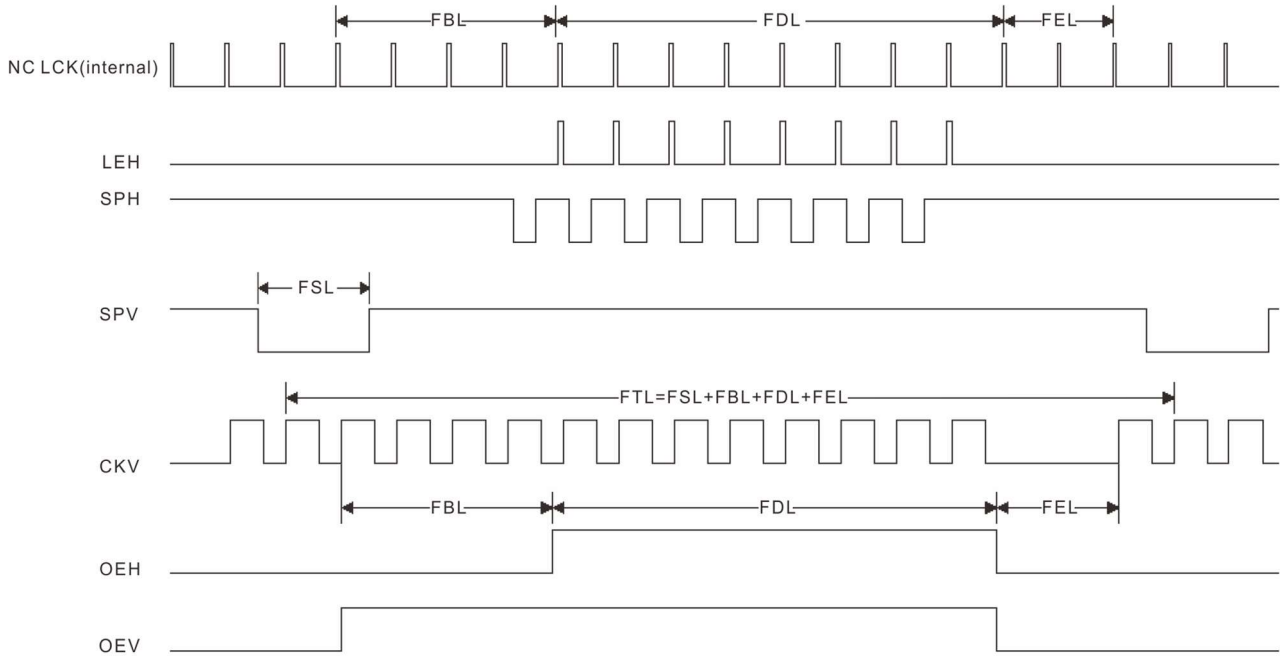


Figure 2

Timing Parameters Table

Mode	3	Resolution 1024x758				
SDCK [MHz]	20					
Pixels Per SDCK	4					
Line	LSL	LBL	LDL	LEL	GDCK_STA	LGONL
Parameters[SDCK]	6	6	256	38	4	262
Line	-	-	-	-	-	-
Parameters[us]	0.3	0.3	12.8	1.9	0.2	13.10
Frame	FSL	FBL	FDL	FEL	-	FR [Hz]
Parameters [lines]	2	4	758	5	-	84.99
Frame					-	-
Parameters [us]	30.60	61.20	11597.4	76.50	-	-

Note:

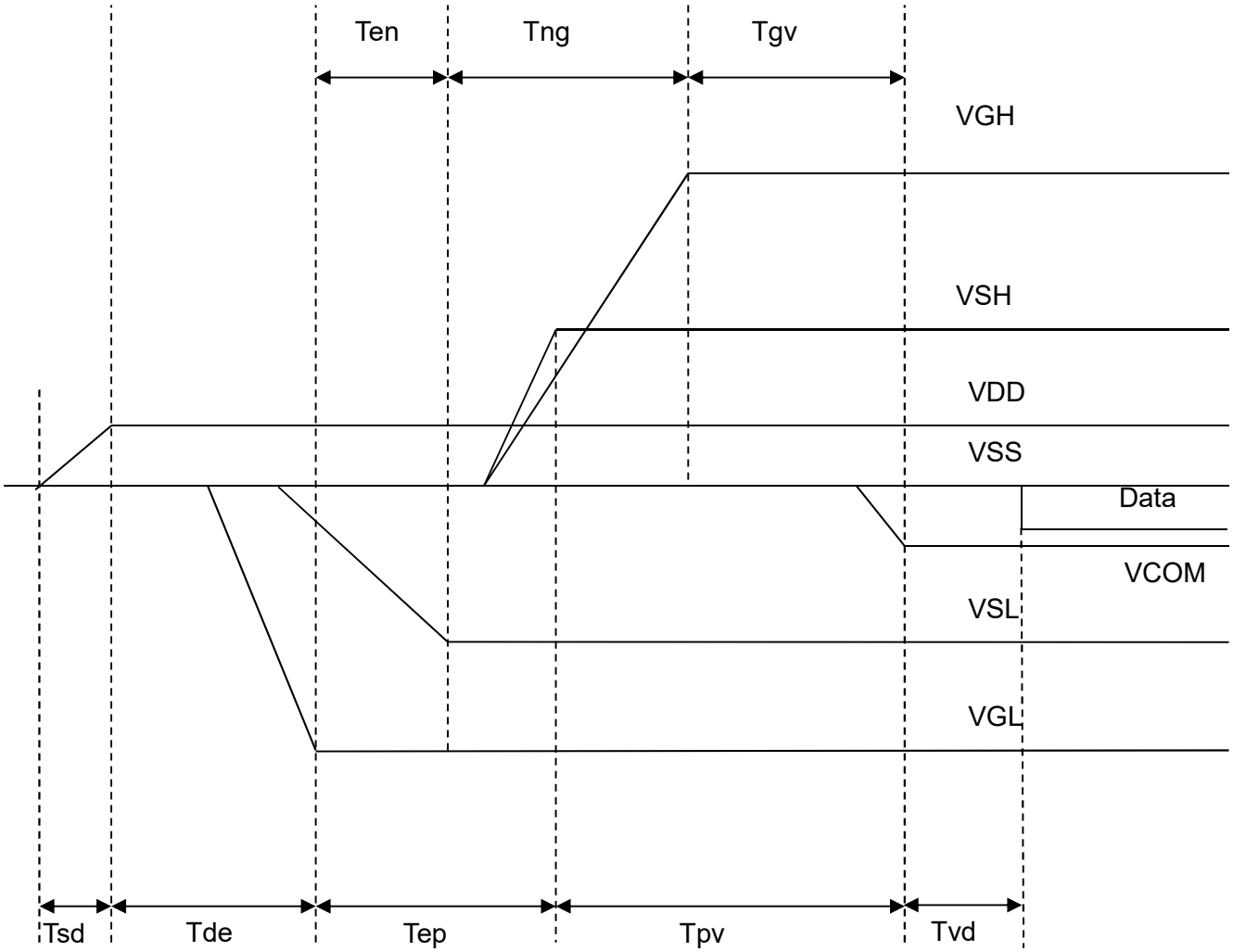
1. For parameters definition, see above Figure 1 and Figure 2.
2. For NXP SoC GDOE Low pulse represent FSL and GDSP pulses with the first period of FBL
3. The mapping of pins between controller timing and pin-assignment of panel:

7. Power Sequence

Power Rails must be sequenced in the following order：

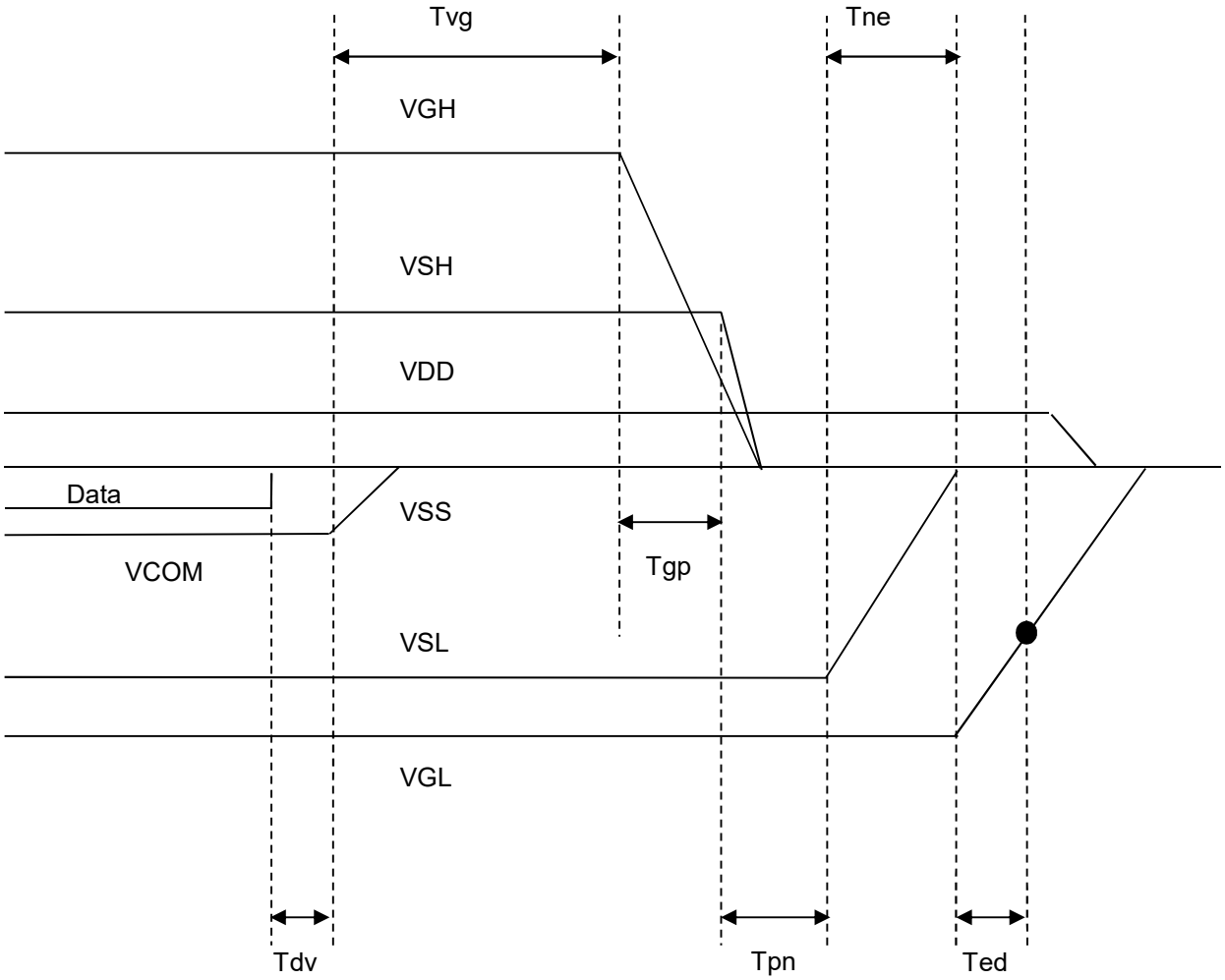
1. VSS → VDD → VSL → VSH (Source driver) → VCOM
2. VSS → VDD → VGL → VGH (Gate driver)

POWER ON



	Min	Max
Tsd	30us	-
Tde	100us	-
Tep	1000us	-
Tpv	100us	-
Tvd	100us	-
Ten	0us	-
Tng	1000us	-
Tgv	100us	-

POWER OFF



	Min	Max	Remark
Tdv	100µs	-	-
Tvg	0µs	-	-
Tgp	0µs	-	-
Tpn	0µs	-	-
Tne	0µs	-	-
Ted	0.5s	-	Discharged point @ -7.4 Volt

Note:

1. Supply voltages decay through pull-down resistors.
2. VGL must remain negative of Vcom during decay period

8. Optical Characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	32	40	-	%	Note 9-1
Gn	N_{th} Grey Level	-	-	DS+(WS-DS) ×n/(m-1)	-	L*	-
CR	Contrast Ratio	-	12	17	-		-

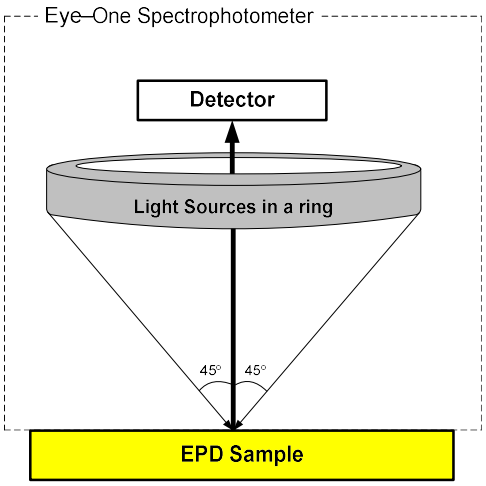
WS: White state , DS: Dark state, Gray state from Dark to White :DS、G1、G2…、Gn…、Gm-2、WS
m:4、8、16　when 2、3、4 bits mode

Note 9-1: Luminance meter:　Eye – One Pro Spectrophotometer

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd):

CR = Rl/Rd



8-3) Reflection Ratio

The reflection ratio is expressed as:

$R = \text{Reflectance Factor}_{\text{white board}} \times (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area (R=G=B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. Handling, Safety and Environmental Requirements and Remark

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains formal product specifications.
Limiting values	

Data sheet status
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and does not form part of the specification.

REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

10. Reliability Test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T = +50°C, RH = 30% for 240 hrs	IEC 60 068-2-2Bp	
2	Low-Temperature Operation	T = 0°C for 240 hrs	IEC 60 068-2-2Ab	
3	High-Temperature Storage	T = +70°C, RH=40% for 240 hrs Test in white pattern	IEC 60 068-2-2Bp	
4	Low-Temperature Storage	T = -25°C for 240 hrs Test in white pattern	IEC 60 068-2-1Ab	
5	High-Temperature, High-Humidity Operation	T = +40°C, RH = 90% for 168 hrs	IEC 60 068-2-3CA	
6	High Temperature, High- Humidity Storage	T = +60℃, RH=80% for 240hrs Test in white pattern	IEC 60 068-2-3CA	
7	Temperature Cycle	-25℃→+70℃, 100 Cycles 30min 30min Test in white pattern	IEC 60 068-2-14	
8	Solar radiation test	765 W/m^2 for 168hrs,40℃ Test in white pattern	IEC60 068-2-5Sa	
9	Package Vibration	1.04G, Frequency: 10~500Hz Direction: X,Y,Z Duration: 1 hours in each direction	Full packed for shipment	
10	Package Drop Impact	Drop from height of 100 cm on concrete surface. Drop sequence: 1 corner, 3 edges, 6 faces One drop for each.	Full packed for shipment	
11	Electrostatic Effect (non-operating)	(Machine model)+/− 250V 0Ω, 200pF	IEC 62179, IEC 62180	

Actual EMC level to be measured on customer application

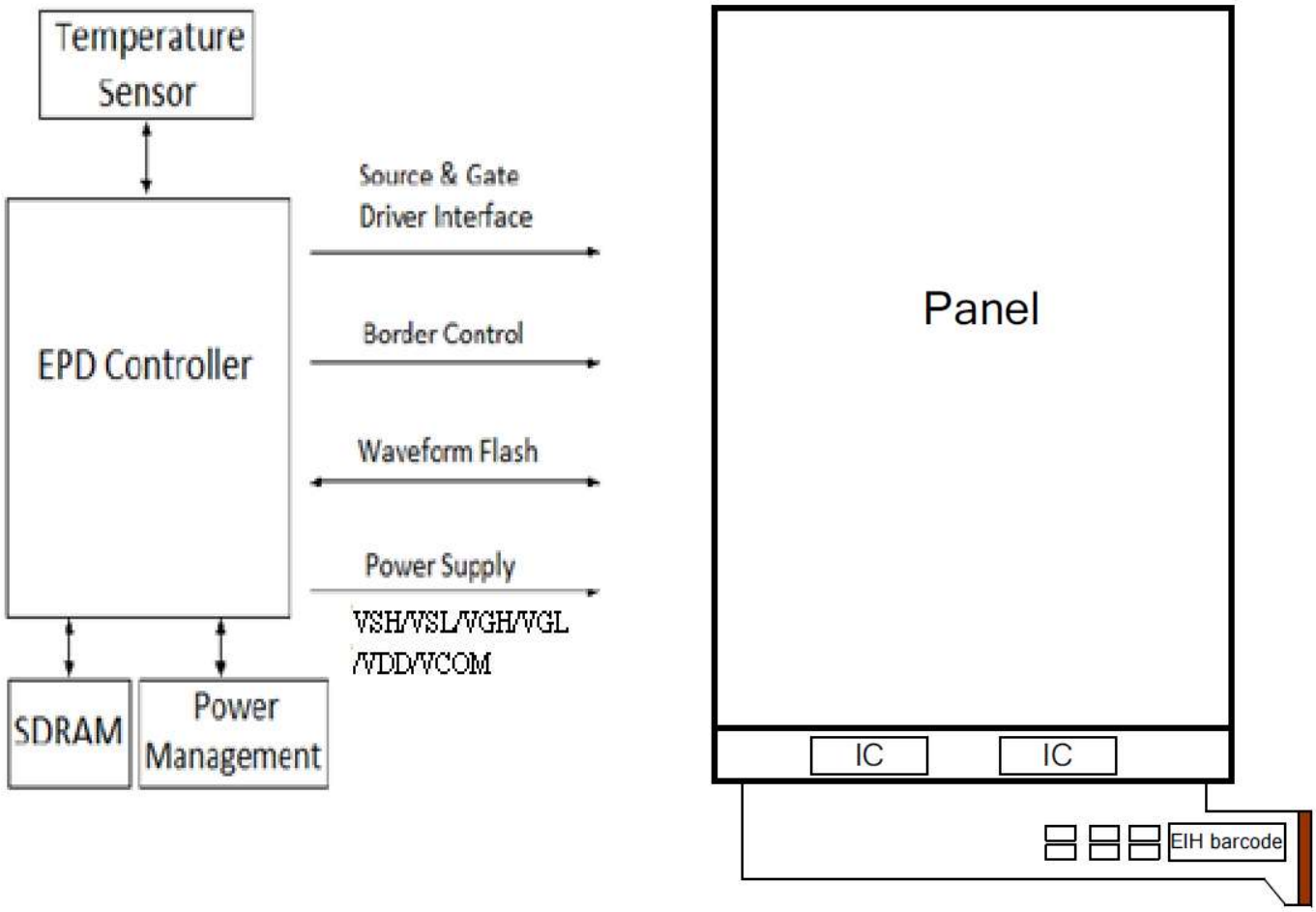
Note: The protective film must be removed before temperature test.

< Criteria >

In the standard conditions, there is not display function NG issue occurred.

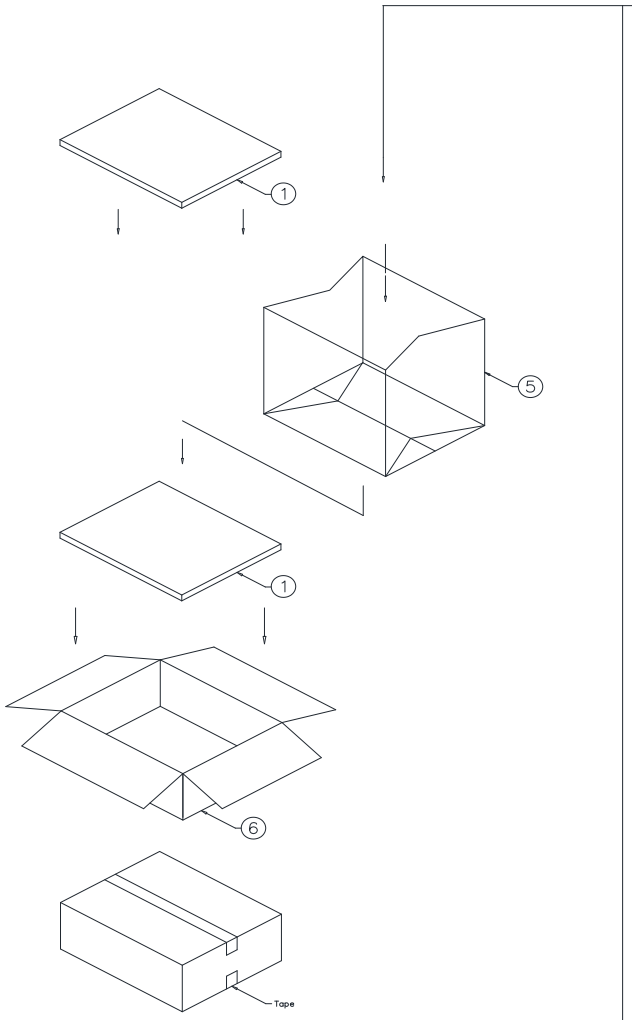
(Including：line defect, no image) All the cosmetic specification is judged before the reliability stress.

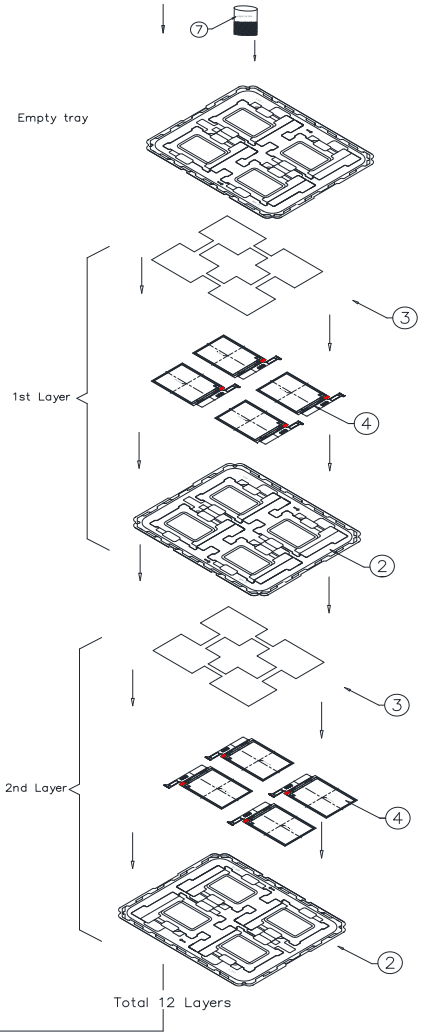
11. Block Diagram



12. Packing

REV	DESCRIPTION	DESIGN	DATE
01	INITIAL RELEASE	Jiangbo	2020/01/17





NOTE:
1. One layer include: 1 piece of cushion sheet, 4 pcs module & 1 piece of tray.
2. Q'TY: 48 pcs panel/carton.
3. Dimension: 445*365*170mm
4. Make sure tray stacked with 180° rotation. We can check this by lateral side view.

ITEM	DESCRIPTION	QTY	REMARK
7	30g加厚複合紙袋碳酸鹽73*95mm	2	
6	CARTON INTERNAL	1	
5	摺口袋450*380*700mm	1	抗靜電
4	ED060XCF&XCG	48	
3	EPE CUSHION SHEET	12	抗靜電
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司 E Ink Holdings Inc.

			SCALE	UNIT	SHEET	DWG.TITLE
APPROVE	Jack Hsieh	2020/01/17	1:1	mm	1 OF 1	ED060XCG PACKING
CHECK	Jimmy Chen	2020/01/17				
DESIGN	Jiangbo Chen	2020/01/17				

MTL.NO.	DWG.NO.	REV.	A4 SIZE
		01	