

UM2088
DPHA User Manual
Rev. 3 - 03 June 2013

Purpose of this Manual

This User Manual contains the full description of Digital Pulse Height Analyzer for 724 series. The description is compliant with DPP-PHA firmware release **4.1_128.26**, and DPP-PHA Control Software release **1.2.3**. For future release compatibility check in the firmware and software revision history files.

Change Document Record

Date	Revision	Changes
16 February 2012	00	Initial release
07 June 2012	01	Updated Chapter 7
29 January 2013	02	Fully revised for DT5780 support
03 June 2013	03	Revised Chapters 4, 5, and 6. Removed Register Chapter(*).

(*) A new document unifying the registers descriptions of CAEN digitizers is in progress; the user can temporarily refer to the document "DPHA Registers Description" at the DPP-PHA page in the documentation tab .

Symbols, abbreviated terms and notation

ADC	Analog to Digital Converter
CSP	Charge Sensitive Preamplifier
DAQ	Data Acquisition
DPHA	Digital Pulse Height Analyzer
DPP	Digital Pulse Processing
DPP-CI	DPP for Charge Integration
DPP-PHA	DPP for Pulse Height Analysis
DPP-PSD	DPP for Pulse Shape Discrimination
HPGe	High Purity Germanium
MCA	Multi-Channel Analyzer
OS	Operating System
PC	Personal Computer
PHA	Pulse Height Analysis
PMT	Photo Multiplier Tube
TTF	Trigger and Timing Filter
USB	Universal Serial Bus

Reference Documents

[RD1]	GD2783 – First Installation Guide to Desktop Digitizers & MCA
[RD2]	GD2512 – CAENUpgrader QuickStart Guide
[RD3]	AN2508 – CAEN Digital Pulse Height Analyzer - a digital approach to Radiation Spectroscopy
[RD4]	UM1935 – CAENDigitizer User & Reference Manual
[RD5]	GD2827 - How to make coincidences with CAEN digitizers COMING SOON
[RD6]	AN2086 – Synchronization of CAEN digitizers in multi board acquisition systems

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1 Introduction

The **Digital Pulse Height Analyzer** (hereafter called **DPHA**) is a Multi-Channel Analyzer for Gamma and X-ray spectroscopy. It is ideally suited for high energy resolution detectors, such as **HPGe**, connected to the output of a Charge Sensitive Preamplifier (CSP), but it can also properly work with PMT-based detectors like **NaI**. The DPHA operates as a traditional spectroscopy acquisition chain made of Shaping Amplifier plus Peak Sensing ADC, thus representing a digital replacement of that modules. In some cases, it can also replace Discriminators, TDCs, Scalers and Coincidence Units. It is possible to apply the digital algorithm used in the DPHA also to signals that are not coming from a CSP (for instance the output of a PMT), but for this type of detector CAEN recommends solutions based on faster digitizers (such as the 720 or 751 series) running specific algorithms for the digital Charge Integration (DPP-CI) or Pulse Shape Discrimination (DPP-PSD).

From the hardware point of view, the DPHA is a 2, 4, or 8-channel, 14-bit, 100 MS/s waveform Digitizer according to the form factor:

- **V1724**: 8-channel VME module (single unit, 6U) with VME 32/64-bit and Optical Link readout
- **DT5724, N6724**: 2 or 4-channel Desktop or NIM module with USB and Optical Link readout
- **DT5780**: 2-channel Desktop module with USB and optical link readout, completed by a 2-channel High Voltage (up to 5 KV, 300 uA) and Low Voltage (± 12 V, ± 24 V) power supply for the detector and the preamplifier.

Fig. 1.1 represents a simplified block diagram of the module.

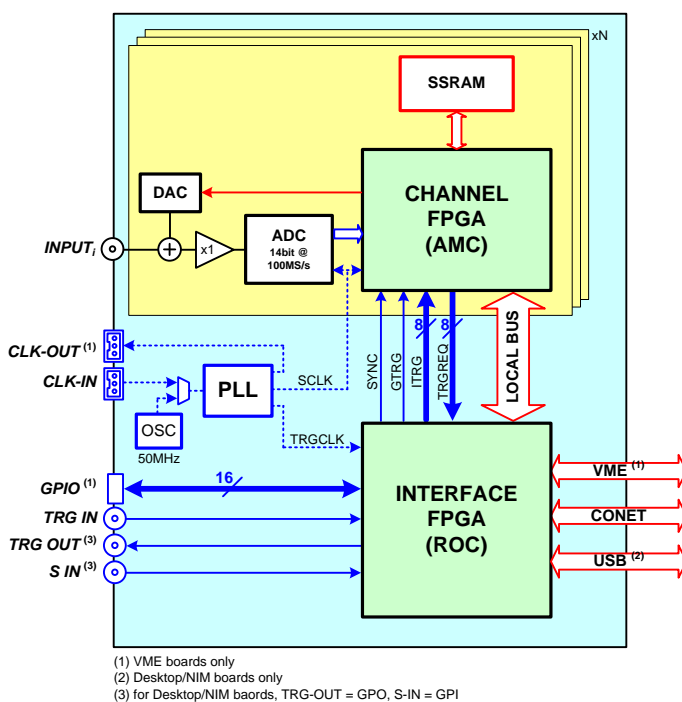


Fig. 1.1: Simplified block diagram of the Digitizer

The Digitizer is a dead-timeless acquisition system, meaning that the analog input signal is continuously converted into a stream of digital samples and on-line processed by the Channel FPGA (AMC). The AMC purpose is to perform the on-line Digital Pulse Processing to implement a Pulse Height Analysis MCA (**DPP-PHA**). The algorithms implemented in the DPP-PHA firmware are based on the trapezoidal filter (Moving Window Deconvolution) for the calculation of the pulse height.

The **DPP-PHA firmware** transforms the waveform Digitizer into a spectroscopy acquisition system providing energy (i.e. pulse height) and timing information as well as portions of the waveform for debugging, monitoring and further off-line pulse shape analysis.

The system also includes the **DPP-PHA Control Software** that allows the user to set the parameters for the acquisition, to configure the hardware and to perform the data readout, the histogram collection and the spectrum or waveform plotting and saving. The program can be easily interfaced to software tools for the spectroscopy analysis. Drivers, libraries and demo source codes are also available for users that need to integrate the DPP-PHA into their DAQ programs, or simply to modify the program and tailor it to a specific application.

The hardware has been designed to operate as a scalable multi-channel acquisition system: the front panel clock, the trigger and the general purpose I/Os make easy to synchronize several boards and to run them simultaneously; the advanced trigger logic and the event time stamping allow for the implementation of coincidences and anti-coincidences among multiple detectors.

This following list summarizes what you can do with the PDHA:

- receive the signals coming from a Charge Sensitive Preamplifier (CSP) and adapt the dynamic range (programmable DC offset and, in the DT5780 model, also programmable Gain);
- detect input pulses and generate a local trigger on them;
- calculate the time of arrival of the trigger and the pulse height by means of digital shaping filters (trapezoidal filters);
- build an event made of a configurable combination of Trigger Time Stamp, Pulse Height (energy) and raw waveforms (i.e. series of ADC samples belonging to a programmable size acquisition window);
- detect pile-up conditions and manage the count loss (dead-time);
- implement coincidences and anti-coincidences among channels within the same board;
- save events (list) into a memory buffer and manage the readout through the Optical Link, USB or VME;
- accumulate the histograms (up to 16K channels), compensate for the dead-time and plot the spectra acquired from each channel (histogram mode);
- plot the waveforms of the input signals as well as of the internal filters. The user can adjust the parameters of the acquisition and immediately get a feedback by looking at the waveforms (oscilloscope mode);
- generate output files (lists, histograms or waveforms) in a binary or ASCII format.

2 Getting Started

Scope of the chapter

This chapter is intended to provide a quick start guide of the DPP-PHA Control Software. The proposed setup is intended only to provide an example of gamma ray detection, to get the user familiar with a DPHA system.

System Overview

CAEN's DPHA system proposed in the chapter consists of the following CAEN products:

- DT5724, 4-channel 14-bit 100 MS/s Desktop Digitizer
- DPP-PHA firmware running on the Digitizer.
- DPP-PHA Control Software running on the host station.

The description is compliant with DT5780 as well.

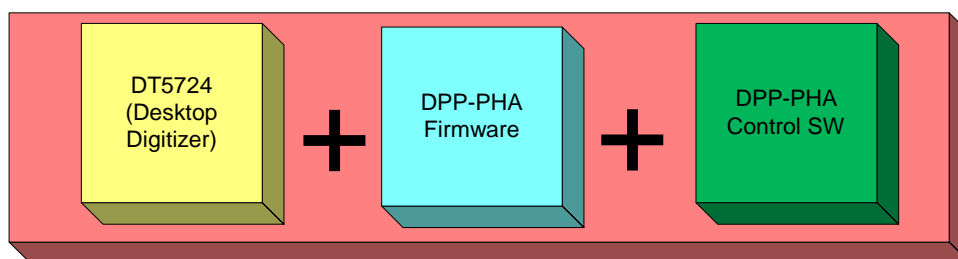


Fig. 2.1: CAEN DPHA System components

Hardware Setup

The DPHA system receives on channel 0 the signal from a Charge Sensitive Preamplifier CSP (CAEN N914 board) elaborating the analog output of a NaI(Tl) detector coupled with a PMT. The CAEN N1470 (a 4-channel, HV Programmable Power Supply board) provides the power supply to the detector ($V_{bias} = 800\text{ V}$). A Cobalt-60 (^{60}Co) gamma ray source (counting rate $\sim 1\text{ KHz}$) is used. A computer equipped with a Microsoft Windows 7 Professional 64-bit OS acts as host station. The communication protocol between the computer and the Digitizer is USB (2.0 version).

The use of DT5780 can substitute the power supply and the DT5724 digitizer.

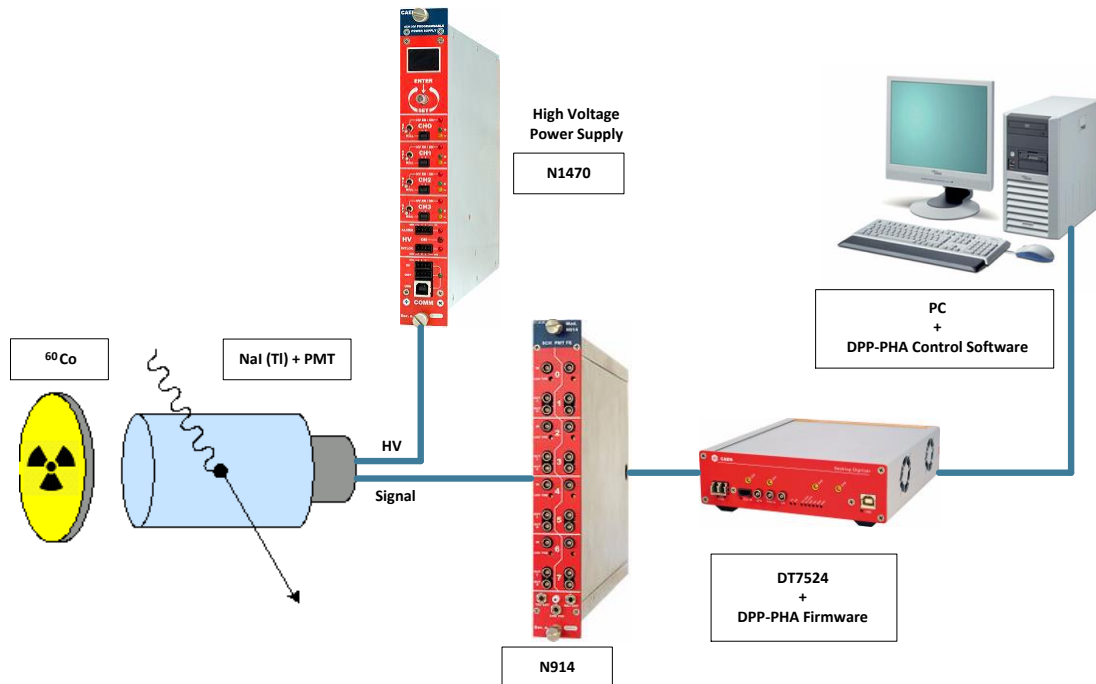


Fig. 2.2: The hardware setup including the DPHA used for the practical application

Drivers and Software Installation

In order to manage the DPHA System, the host station needs either Windows or Linux OS, and the third-party software **Java Runtime Environment 6** or later (trademark of Oracle, Inc, downloadable from <http://www.java.com>). Linux users must also take care of proper installation of **gnuplot** graphical tool, as well as of **CAEN Libraries**. The latter can be downloaded from CAEN website (login required before to download).

According to the preferred way of connection to the digitizer, users must also take care of proper installation of USB or optical drivers. In our case we are going to describe the procedure for USB connection.

✓ DRIVER

- **USB 2.0 CAEN driver.**



Note: If you're using a different communication interface (i.e. Optical Link or VME), the related driver is required.



Note: It is recommended to install the driver before to connect the hardware.



Note: More details about USB driver installation are in [RD1].

How to install the driver (Windows)

Download the latest release of the **USB driver** for Windows on CAEN website in the 'Software/Firmware' area at the DT5724 page.

Unpack the **driver package**.

Power on the **Digitizer** and **plug** the **USB cable** in a USB port on your computer.

Windows will try to find drivers and, in case of failure (the message "**Device driver software was not successfully installed**" may be displayed), the driver needs to be installed manually:

Go to the system **Device Manager** through the Control Panel and **check** for the **CAEN DT5xxx USB1.0** unknown device.

Right click and **select Driver software update** in the scrolling menu.

Select the option to **browse my computer for driver software**.

Point to the **driver folder** and **finalize** the installation.

How to install the driver (Linux)

Download the latest release of the **USB driver** for Linux on CAEN website in the 'Software/Firmware' area at the DT5724 page.

Unpack the **driver package** (tar -zxf CAENUSBDrvB-xxx.tgz).

Go to the driver **folder** (cd CAENUSBDrvB-xxx).

Follow the **instructions** on the **Readme.txt** file.

Type: make

sudo make install

Reboot your machine

✓ SOFTWARE

- **DPP-PHA Control Software** for Windows OS.

Download the standalone **DPP-PHA Control Software 1.2.3** full installation package on CAEN website in the 'Download' area at the DPP-PHA Control Software page (**login is required before the download**).

Unpack the **installation package**, **launch** the **setup file** and **complete** the **Installation wizard**.

- **DPP-PHA Control Software** for Linux OS.

Download the DPP-PHA_ControlSoftware-1.2.3.tar.gz package on CAEN website in the 'Download' area at the DPP-PHA Control Software page (**login is required before the download**).

Unpack the **installation package** (tar -zxf DPP-PHA_ControlSoftware-1.2.3.tar.gz).

Follow the instruction on **Setup/Linux/Readme.txt**

Type: ./configure

make

sudo make install

Launch the Control Software typing **DPP-PHA_ControlSoftware**



Note: in the Linux environment it is required to first install CAENVME, CAENComm and CAENDigitizer. You can find those libraries in the CAEN web page. In the Windows environment all libraries come within the control software package itself.

Firmware and Licensing

The DPHA works with the **DPP-PHA Firmware** common to the 724 series of CAEN digitizers and to the DT5780 Digital MCA.

✓ How to install the firmware

Download the **DPP-PHA Firmware (.cfa)** on CAEN website in the 'Download' area at the DPP-PHA page.

Download the **CAENUpgrader** software required to upload the firmware on your board. The program full installation package for Windows OS is available on CAEN website in the 'Download' area at the CAENUpgrader page.

Unpack the **installation package**, **launch** the **setup file** and **complete** the **Installation wizard**.

Run the **CAENUpgrader GUI** by one of the following options:

- The **desktop icon** for the program
- The **Quick Launch icon** for the program

- The **.jar file** in the *bin* folder from the installation path on your host

Select **'Upgrade Firmware'** in the **'Available actions'** scroll box menu of the **'Board Upgrade'** tab.

Select the **model** of your board in the **'Board Model'** scroll box menu.

Enter the **.cfa file** in the **'Firmware binary file'** text box by the **'Browse'** button.

Set **'USB'** in the **'Connection Type'** scroll box menu.

Set **'0'** as **'Link number'** setting.

Check **'Standard Page'** in the **'Config Options'**.

Press the **'Upgrade'** button to perform the upload; after few seconds, a pop up message will inform you about the successful upgrade.

Power cycle the **board**.

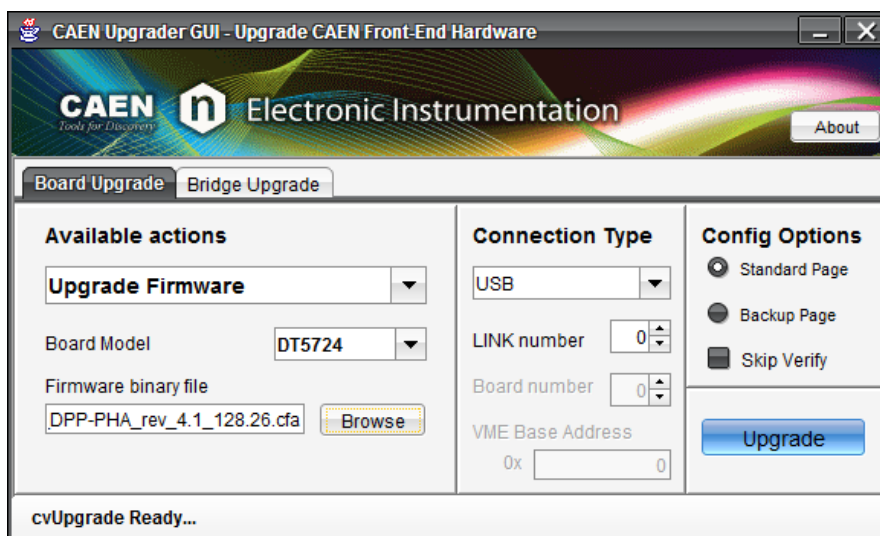


Fig. 2.3: CAENUpgrader settings for DPP-PHA firmware upgrade.

Note that when running the DPP-PHA Control Software, the program checks for the firmware loaded in the target Digitizer. If no license is found, a pop-up warning message shows up and reports the time left before the acquisition is stopped (trial version). In order to unlock the DPP firmware and use it without any time limitation, you need to purchase a license from CAEN. Refer to **[RD2]** for detailed instructions on how to use CAENUpgrader and on the licensing procedure.



Note: The DT5780 is an exception, since it is delivered already running a licensed version (i.e. not time limited) of the DPP-PHA Firmware. This means that no license needs to be bought by the user when purchasing a DT5780

Practical Use

The following step-by-step procedure shows how to use the DPP-PHA Control Software (see Chapter 5) in a typical application of gamma ray detection by setting the relevant DPP parameters, by plotting the signals (Oscilloscope mode) and the energy histogram (Histogram mode), finally by saving the acquired data.

Check that the whole hardware in your setup is properly connected and powered on.



Note: After typing the value of a parameter in a box menu, press the “Enter” key on your keyboard to activate the setting.

1. Run the software.

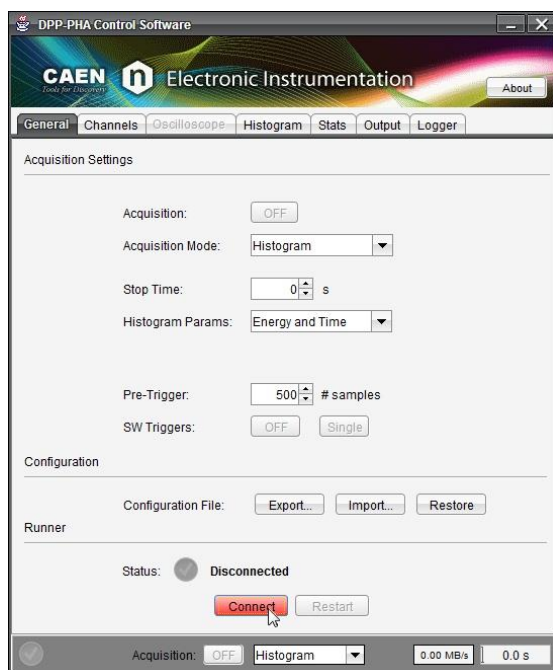
Run the **DPP-PHA Control Software GUI**, according to the options selected in the installation wizard, choosing one of the following options:

- The **desktop icon** for the program
- The **Quick Launch icon** for the program
- The **.bat file** in the main folder from the installation path on your host

2. Connect to the Digitizer.

Path1: Tab **GENERAL** → Section **RUNNER**

Action1: click the button **CONNECT**. The “Connection” window will appear.



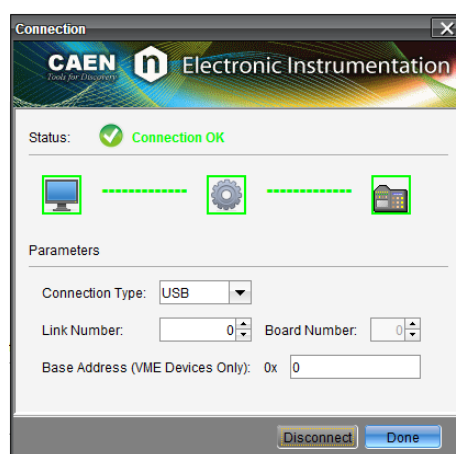
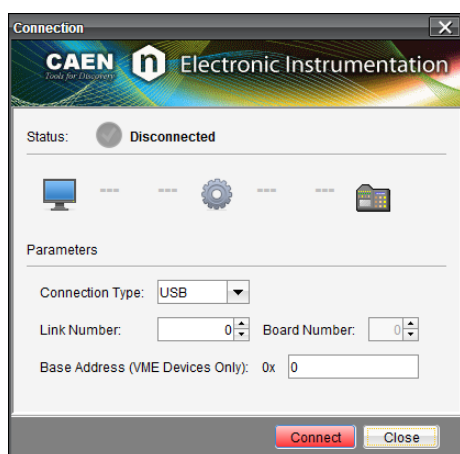
Action2: set the connection parameters values. Using a USB communication link with a Desktop digitizer, the correct settings are: **Connection Type** = “USB”, **Link Number** = “0” and **Base Address** = “0”. **Tab. 2.1** shows the setting values for common communication channels and Digitizers. Further examples are in **Tab. 6.4**.

Connection chain	Type	Link	Board	Address
PC → USB → DT5724 / N6724 / DT5780	USB	0	0	0
PC → USB → V1718 → VME → V1724	USB	0	0	32100000*
PC → PCI/PCIe → A2818/A3818 → CONET → DT5724 / N6724 / DT5780	PCI	0	0	0
PC → PCI/PCIe → A2818/A3818 → CONET → V1724	PCI	0	0	32100000*

Tab. 2.1: Examples of connection settings

(*)How to read the Base Address of a VME Digitizer is described in the digitizer’s User Manual.

Action3: click the button **CONNECT** and verify that the connection Status turns to green (i.e. Connection OK), then click the button **DONE**.

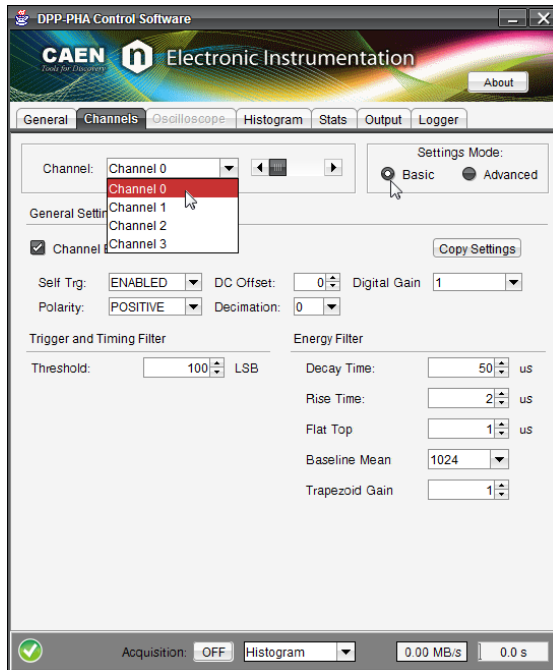


3. Enable Channel 0 and Basic Settings mode, set Oscilloscope mode and the Pulse Polarity

Path1: Tab **CHANNELS** → Section1 **CHANNEL** → Section2 **SETTINGS MODE**

Action1: enable “**Channel 0**” using the scroll menu box or the side bar.

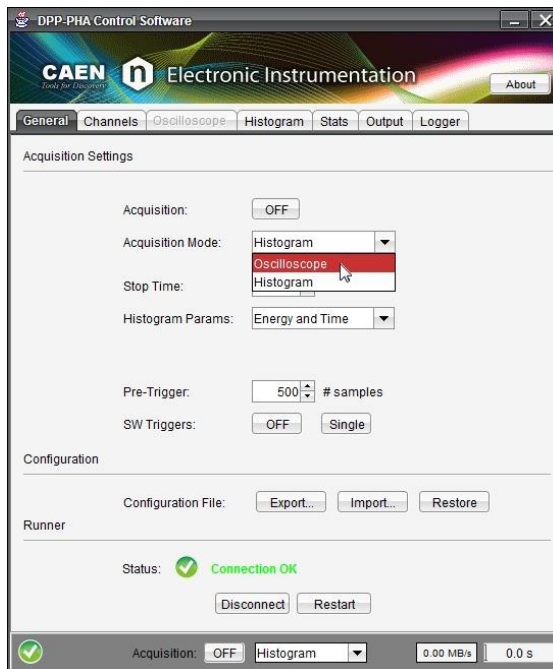
Action2: check the “**Basic**” option as **SETTINGS MODE**.



Make sure that the board’s self-trigger is active (**SELF TRG = ENABLED**).

Path2: Tab: **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: set **ACQUISITION MODE** on “**Oscilloscope**” using the scroll menu box.

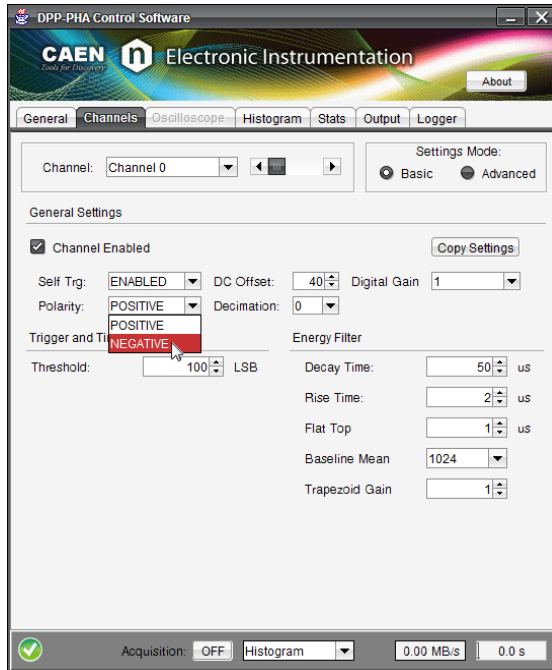


Path3: Tab **CHANNELS** → Section **GENERAL SETTINGS**

Action1: set the pulse **POLARITY** on "**Negative**".



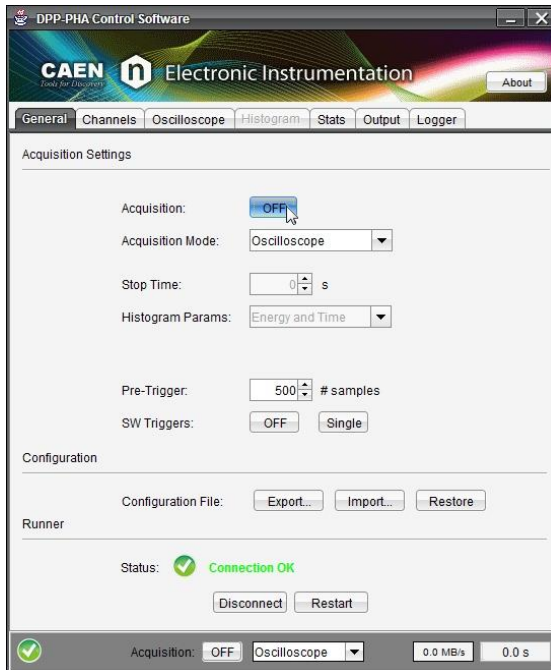
Note: The trapezoidal algorithm of the DPP-PHA is designed to work properly with a positive input, that is usually the polarity of the CSPs' output. In the specific hardware setup, the N914 preamplifier is an exception, providing out a negative pulse. It is so possible, by the **POLARITY** option, to invert the signal at firmware level before it enters the FPGA.



4. Start acquisition and check RUN LED on the front panel

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: click the **ACQUISITION “ON/OFF”** button in order to set the acquisition **ON** and start the Run. Check that the “Run” green LED on the Digitizer’s front panel lights on.

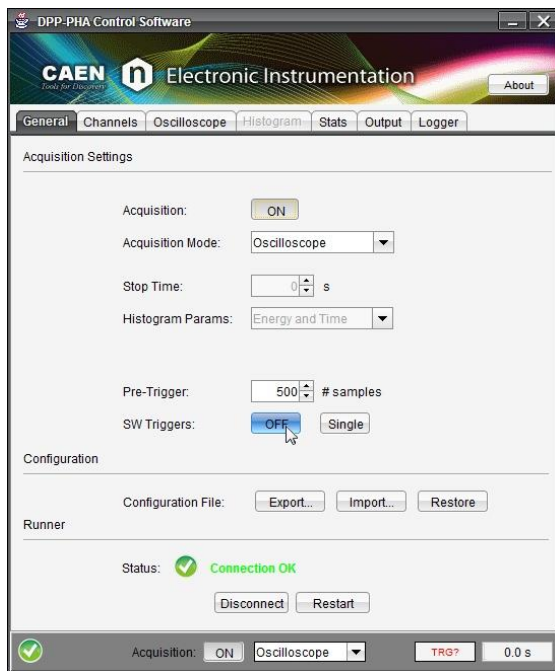


5. Enable SW trigger, adjust the DC offset, set the threshold for self triggering

With the acquisition on, since it is not guaranteed that the channel is properly triggering on the input pulses because trigger threshold and DC offset are not tuned yet, the software trigger is used to force the acquisition and see the waveforms. It is so possible to adjust the baseline of the input signal (DC offset) according to the Digitizer's dynamic range and the trigger threshold according to the noise level of the RC-CR² signal.

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: enable the software trigger to be continuously issued by clicking the **SOFTWARE TRIGGERS "ON/OFF"** button.



Path2: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action1: set “Channel 0” in the **CHANNEL** list.

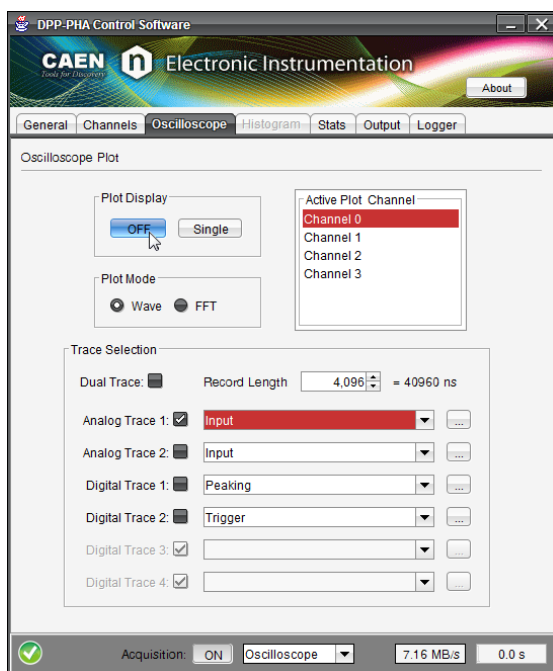
Action2: check the “Wave” box as **PLOT MODE**.

Action3: disable **DUAL TRACE** displaying.

Action4: check **ANALOG TRACE 1** and select “Input” in the scroll box. The input pulse from the Charge Sensitive Preamplifier will be plotted.

Action5: disable **ANALOG TRACE 2**, **DIGITAL TRACE 1** and **DIGITAL TRACE 2**.

Action6: enable the continuous plotting by clicking the **PLOT DISPLAY “ON/OFF”** button.



Action7: look at the input pulse baseline (DC offset) in the plot in order to check if an adjustment is needed according to the Digitizer’s ADC dynamic range. In the specific case, a reasonable value of DC offset is around **2000** (counts). If the plotted signal doesn’t fit this setting, go to **path3** right below.

Note: The value in the “DC Offset” menu is expressed in percentage of the Digitizer’s ADC input dynamics and ranges between -50 and +50 (%). In theory, the value of 0 (DC Offset = “0”) means the input pulse baseline is set at half the ADC dynamics (i.e. 8192 counts for the 14-bit and 2.25 V input range DT5724 Digitizer), the value of “50” (DC Offset = “50”) sets the baseline at the upper dynamics border (i.e. 16384 counts), while the value of “-50” (DC Offset = “-50”) sets the baseline at the lower dynamics border (i.e. 0 counts). The real DC offset adjustment implemented in the DPP-PHA firmware is shown in **Fig. 2.4**: in order to preserve from saturation the input signals near the dynamics borders, setting the DC offset to +50 or -50 puts the signal baseline respectively a step up the upper border and a step under the lower border.

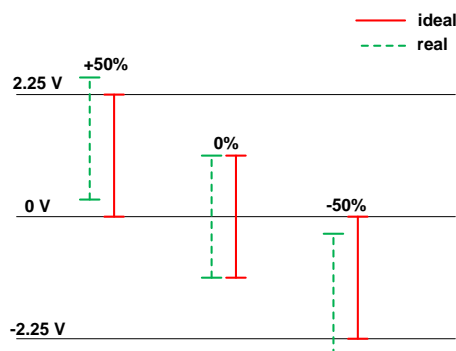
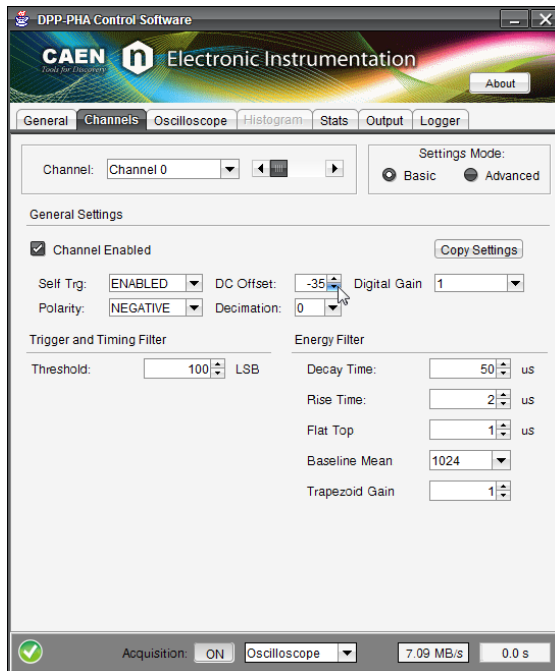


Fig. 2.4: Input signal DC offset adjustment description

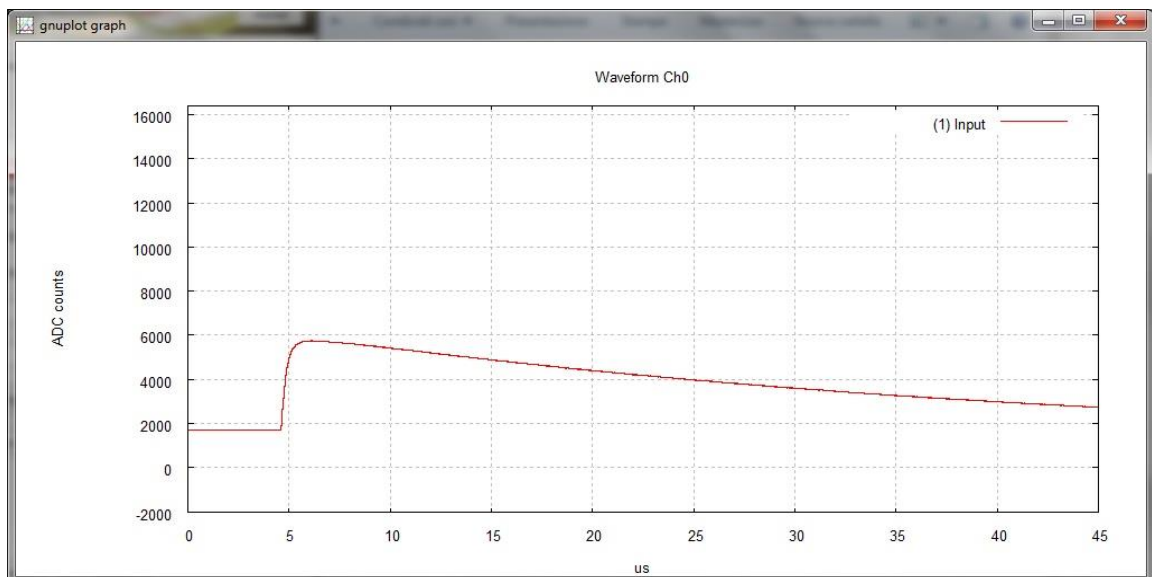
Path3: Tab **CHANNELS** → Section **GENERAL SETTINGS**

Action1: verify that the **CHANNEL ENABLED** box is checked.

Action2: set the DC offset value using the **DC OFFSET** box menu, then press “Enter” on your keyboard to activate the setting. In the example, the value of “-35” has been set, that is negative according to the negative pulses coming from the N914 preamplifier.



Action3: check the effect of the setting in the plot window. Repeat **Action2** if a further DC offset adjustment is needed.



Next step is to fix the trigger threshold over the noise level of the RC-CR² signal, so that the channel is able to self trigger on the input pulses. For this reason, it is useful to display both the threshold and the RC-CR² signal and zoom the RC-CR² baseline to help setting the correct threshold level.

Path4: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

Action1: enable **DUAL TRACE** displaying by clicking the related check box. This will allow the second analog trace (ANALOG TRACE 2) to be plotted.

Action2: select “**RC-CR2**” in the scroll box as **ANALOG TRACE 1**. The bipolar signal coming out from the Trigger and Timing Filter will be plotted.

Action3: check **ANALOG TRACE 2** and select “**Threshold**” in the scroll box in order to display the trigger threshold level.

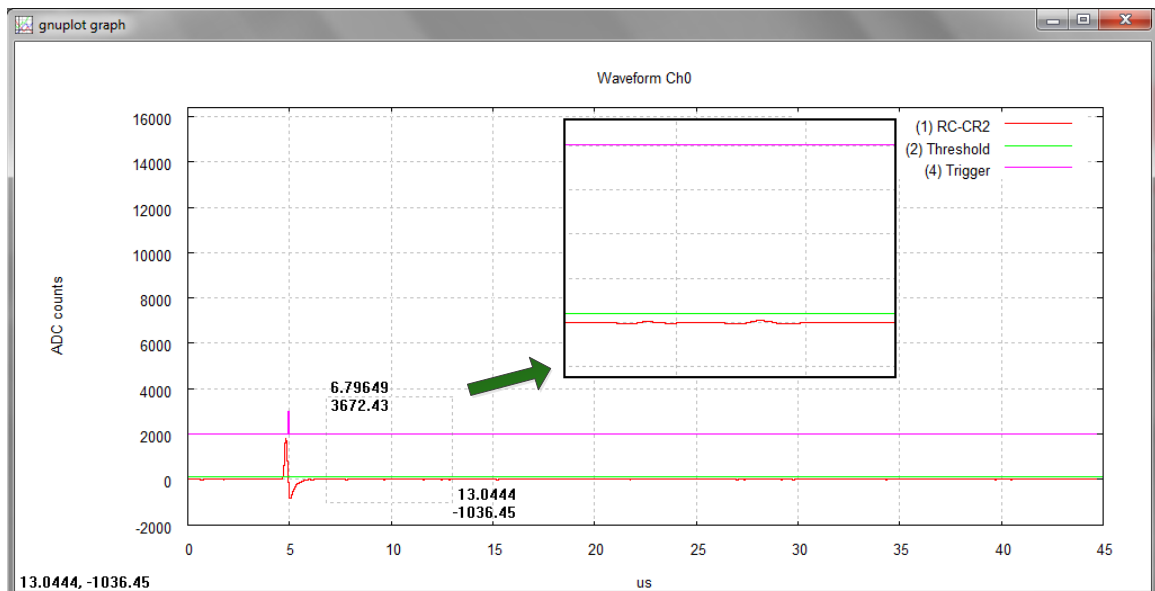
Action4: leave **DIGITAL TRACE 1** unchecked, then check **DIGITAL TRACE 2** and select “**Trigger**” in the scroll box to display the occurring triggers.

Action5: set the “**Threshold**” and the “**RC-CR2**” traces’ DC offset to “**0**” (counts) and the “**Trigger**” trace well distanced, at “**2000**” (counts) for example. To do that, click on the “...” button at the side of each trace scroll box and adjust the DC offset value through the appearing “**Trace Settings**” window interface.

Action6: Use the zoom to highlight the “**Threshold**” signal with respect to the “**RC-CR2**” and choose the trigger threshold value. In the example of this section, the threshold has been finally set to **100** (LSB).

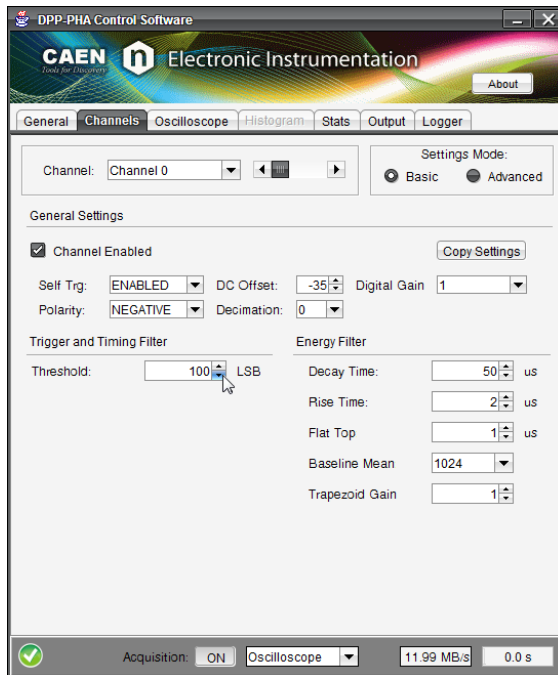


Note: In order to zoom, right click on the plot in a point near a portion of the RC-CR² baseline, then release the mouse button, move to a point on the opposite corner and left click. Press “**u**” key on the keyboard to un-zoom (or press “**a**” to auto scale).



Path5: Tab **CHANNELS** → Section **TRIGGER AND TIMING FILTER**

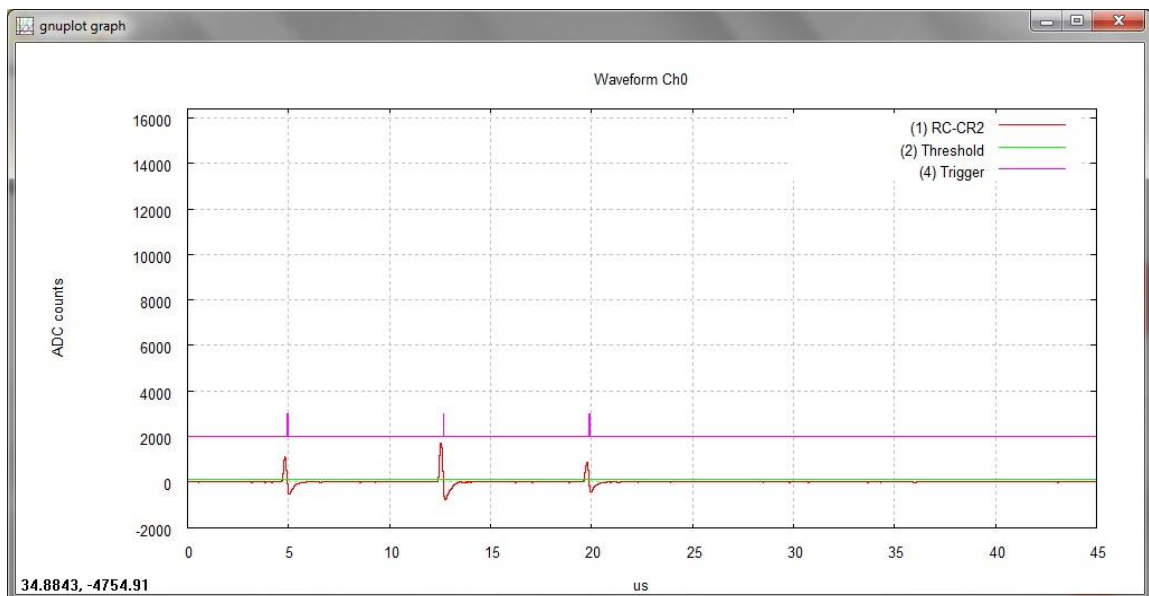
Action1: type the threshold value of “100” (LSB) in the **THRESHOLD** box and press “Enter” on your keyboard to activate the setting.



Path6: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: Disable the software trigger by the **SOFTWARE TRIGGERS “ON/OFF”** button.

Action2: Look that the Digitizer goes on triggering and plotting waveforms, and check the triggers appearing in correspondence of RC-CR² signal exceeding the threshold.



6. Set Energy Filter parameters

At this step, the basic energy filter parameters will be set, taking into account issues like the pile-up occurrence, the ballistic deficit effect in the charge collection, the energy resolution. The numeric values here proposed have been chosen for the specific practical example described in this chapter. Once you have typed the parameter's value, press **"Enter"** on your keyboard to activate the setting.

Path1: Tab **CHANNELS** → Section **ENERGY FILTER**

The decay time parameter (expressed in μs) refers to the time constant of the exponential decay of the input pulse coming from the Preamplifier. It is to be set according to this value in order to perform the pole-zero cancellation in the Trapezoid signal. For a better setting, the plotting of the input pulse and the trapezoid signal is recommended together with the help of the zoom option (see **Fig. 6.8** in Chapter 5).

Action1: type the value of **"40"** into the **DECAY TIME** box menu.

The rise time (expressed in μs) refers to the Trapezoid signal and affects the resolution and the pile-up probability. The longer is the rise time, the better is the resolution (especially for low counting rates), while the probability of pile-up events increases. A trade-off value has usually to be found.

Action2: type the value of **"5"** into the **RISE TIME** box menu.

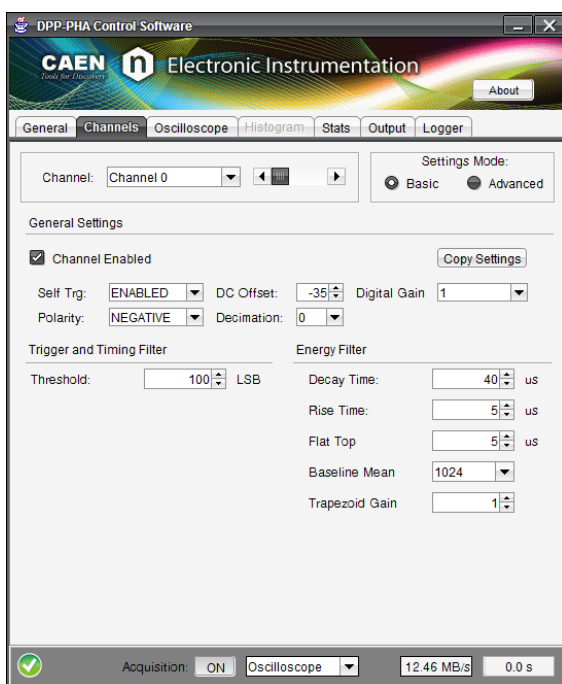
The flat top parameter is related to the Trapezoid plateau length (expressed in μs). The value ought to be not too small (short plateau) in order to compensate the ballistic deficit error and not to affect the precision in the Trapezoid peak calculation, and not too big (long plateau) in order to reduce the pile-up occurrence and for a fast refresh of the baseline value.

Action3: type the value of **"5"** (usually 1 μs is also correct) into the **FLAT TOP** box menu.

The baseline mean parameter is the number of samples of the Trapezoid baseline to be averaged in order to obtain the reference for the Trapezoid height calculation (i.e. the energy).

Action4: type the value of **"1024"** into the **BASELINE MEAN** box menu.

Action5: type **"1"** into the **TRAPEZOID GAIN** box menu. This means no software gain applied to the Trapezoid signal.



In order to verify the effect of the settings, it worth setting the plot to simultaneously monitor a maximum of four (4) significant signals.

Path2: Tab **OSCILLOSCOPE** → Section **OSCILLOSCOPE PLOT**

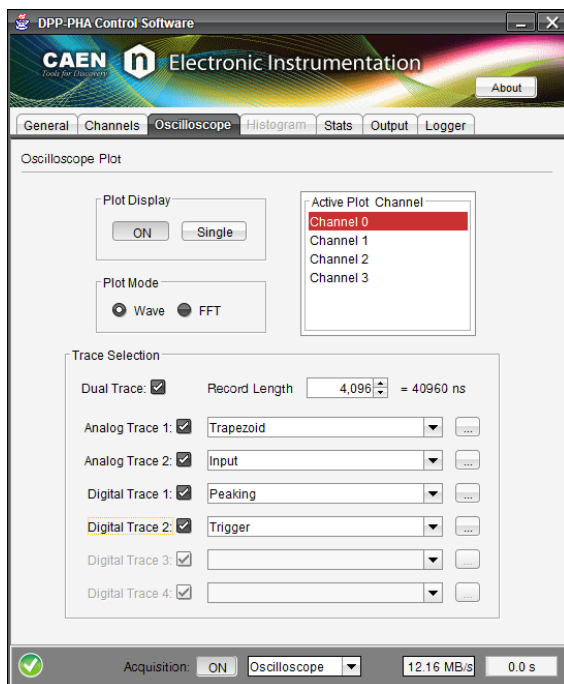
Action1: enable **ANALOG TRACE 1** check box and select “**Trapezoid**” in the scroll menu.

Action2: enable **ANALOG TRACE 2** check box and select “**Input**” in the scroll menu.

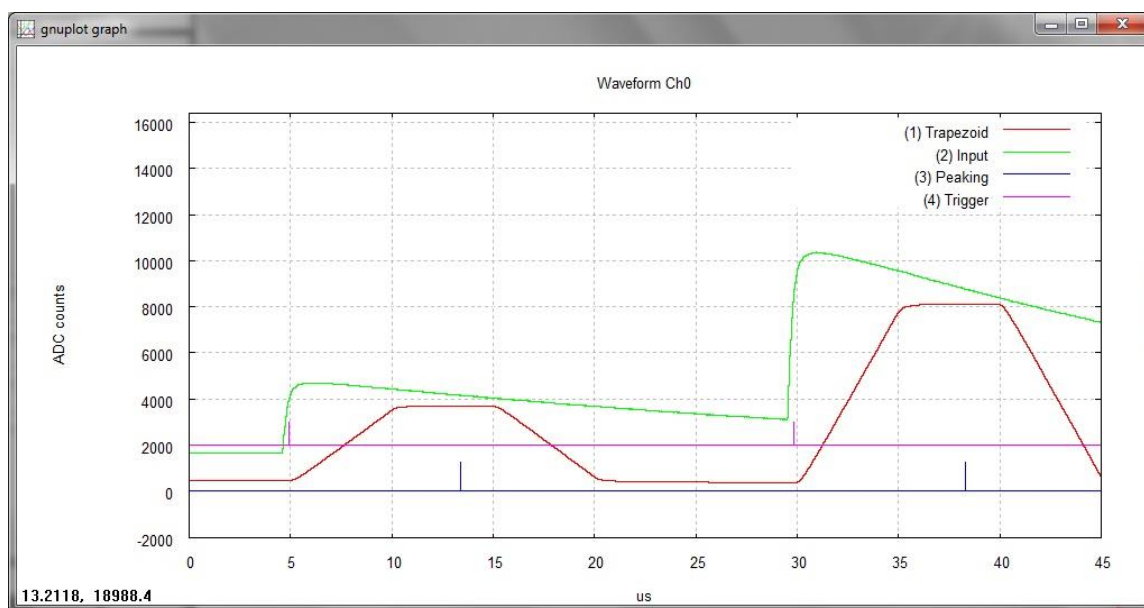
Action3: enable **DIGITAL TRACE 1** check box and select “**Peaking**” in the scroll menu.

Action4: enable **DIGITAL TRACE 2** check box and select “**Trigger**” in the scroll menu.

Action5: if needed, adjust the DC offset and/or the gain of every trace through the “**Trace Settings**” window interface appearing once you click on the “...” button.



Action6: inspect the plotted signals.



Action7: once the parameters configuration has been set, stop the acquisition (you can use the **ACQUISITION “ON/OFF”** button duplicated in the deep grey stripe at the bottom of the GUI) and the plotting (in the **OSCILLOSCOPE** tab).

7. Switch from Oscilloscope to Histogram mode and plot the energy spectrum

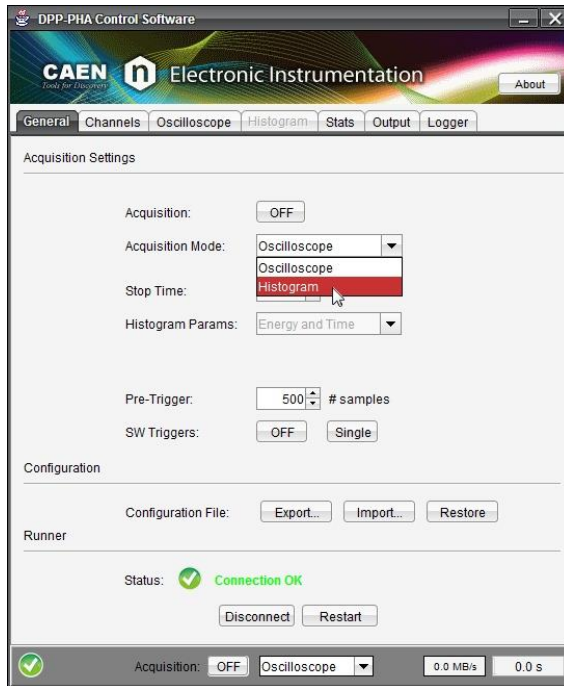
This step leads the user to plot the histogram of energies, i.e. the energy spectrum of the gamma ray source ^{60}Co .

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: set **ACQUISITION MODE** on “Histogram” using the scroll menu box.



Note: In Histogram mode, the overall data throughput of the Digitizer reduces significantly, as only the energy and time parameters are transmitted, while the windowed waveforms are not interested. When the acquisition starts, this is confirmed by the lighting off of the “**BUSY**” red LED on the Digitizer front panel.



Path2: Tab **HISTOGRAM** → Section **HISTOGRAM PLOT**

Action1: set “Channel 0” in the **CHANNELS** box menu.

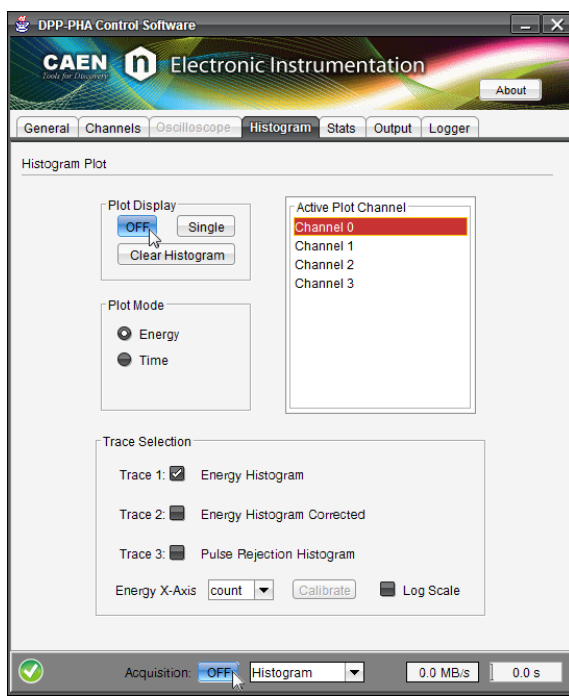
Action2: check “Energy” as **PLOT MODE**.

Action3: check **TRACE 1** to select the “Energy Histogram”.

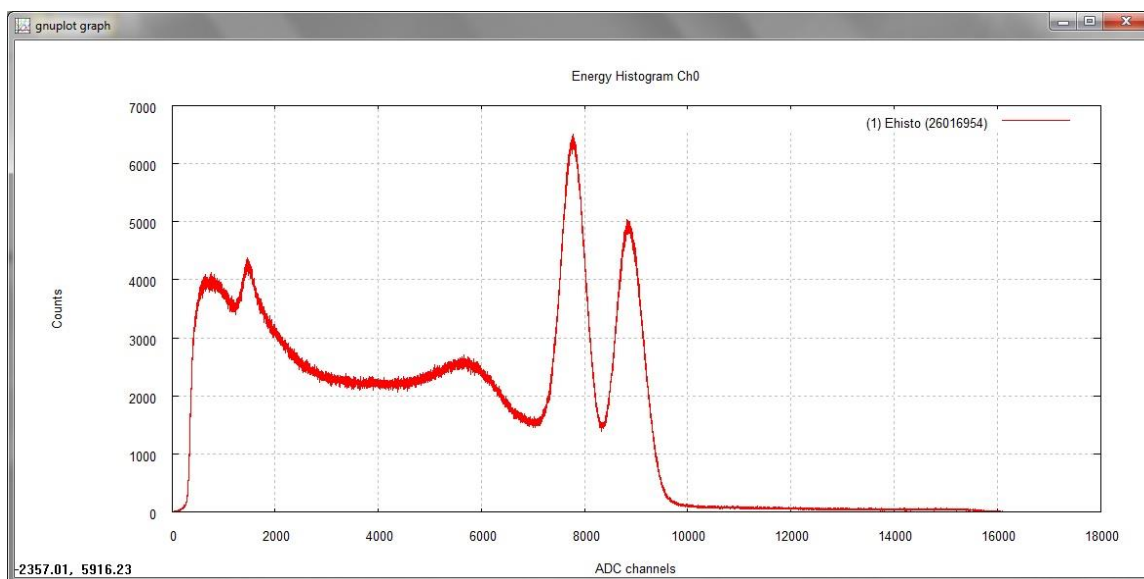
Action4: select “count” as **ENERGY X-AXIS** (not calibrated energy spectrum).

Action5: press the **ACQUISITION “ON/OFF”** button in the deep grey stripe at the bottom of the GUI to start the acquisition.

Action6: press the **PLOT DISPLAY “ON/OFF”** button to enable the histogram plotting.



Action7: check that the plot window is updated with the Energy Histogram being dynamically represented.



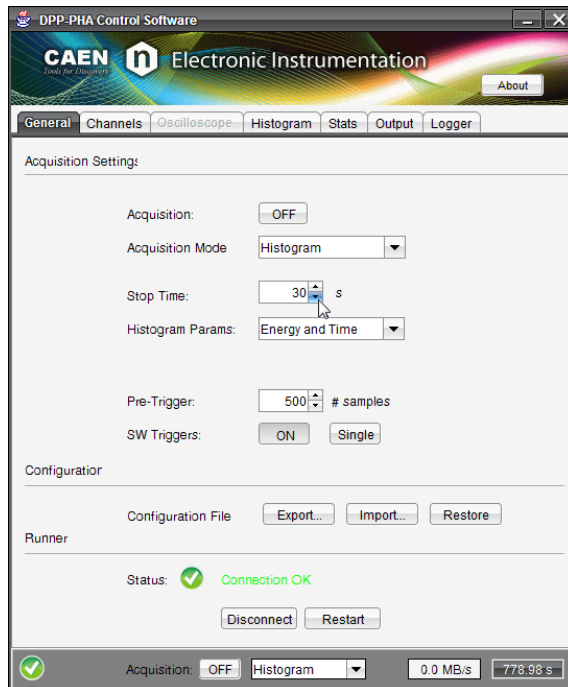
8. Generate the output file and save the histogram data

The steps below allow to save the energy histogram data of a time programmed acquisition run into an output file on the host disk.

Stop the current acquisition run before to start with the followings actions.

Path1: Tab **GENERAL** → Section **ACQUISITION SETTINGS**

Action1: type the **STOP TIME** parameter value (expressed in seconds) to the desired duration of the acquisition run, for example to “30”.



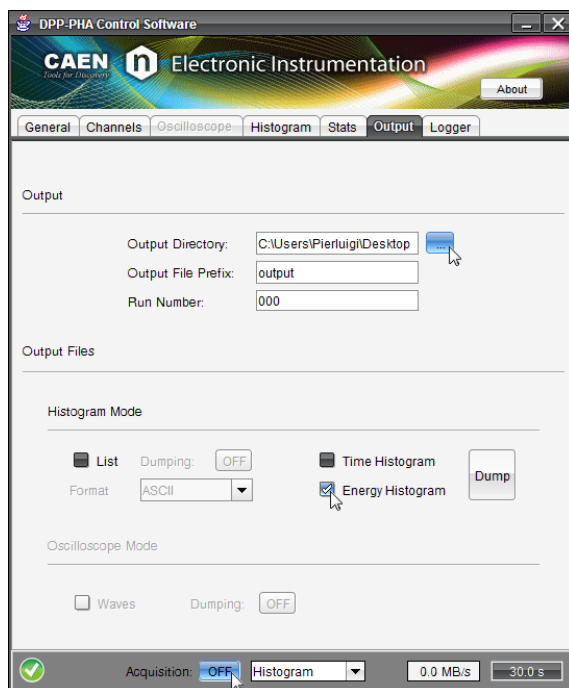
Path2: Tab **OUTPUT** → Section1 **OUTPUT** → Section2 **OUTPUT FILES**

Action1: use the **OUTPUT DIRECTORY** “...” button to browse a specific destination path, different from the default one, where to save the output file on the host disk. In the example, it is the “**Desktop**” folder.

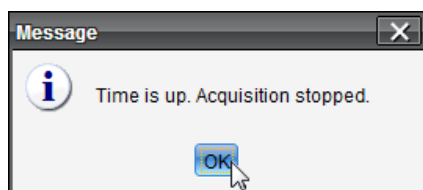
Action2: in the **OUTPUT FILE PREFIX** text box, type a name for the prefix of the output file (“**output**”, in the example) different from the default one, and press “**Enter**” on your keyboard.

Action3: click on the **ENERGY HISTOGRAM** checkbox to enable the saving option.

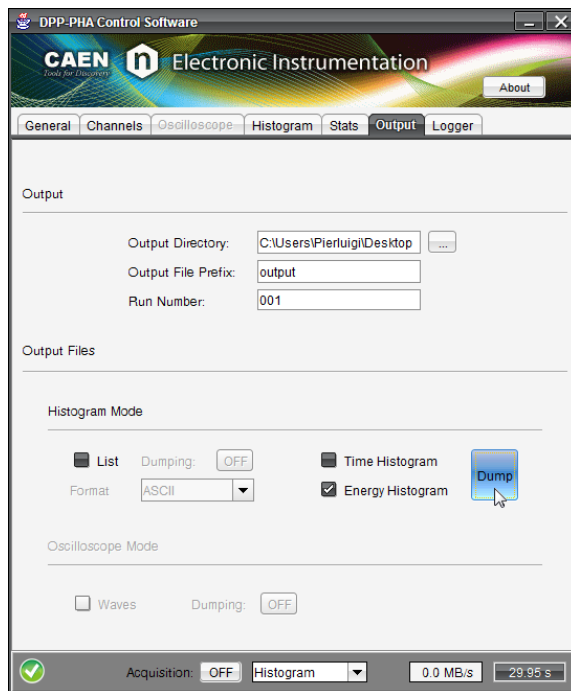
Action4: start the acquisition run by the **ACQUISITION** button in the bottom bar. Note that the **RUN NUMBER** value updates (this is an incremental number identifying the actual run).



The end of the time programmed run is signaled by a pop-up message window and the acquisition is automatically stopped.



Action5: press the **DUMP** button to generate the output data file.



Check the file saved in the selected destination folder. The file format for the acquisition data in the example is: **output_001_eh_0.dat**, where “**output**” is the chosen prefix, “**001**” is the identifier for the actual run session, “**eh**” stands for “energy histogram” and “**0**” is the channel number. The file is a 2-column file with the x-variable values (i.e. the bin number) on the first column and the y-variable values (i.e. the energy histogram value) on the second.

3 Principle of Operation

Traditional Analog Approach

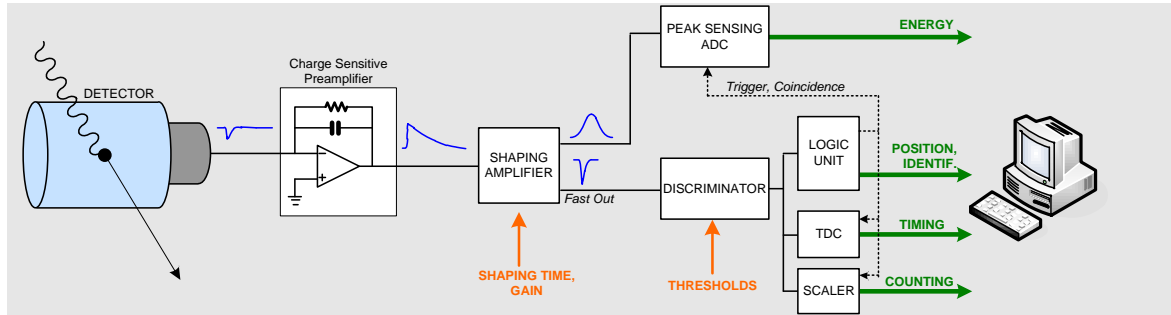


Fig. 3.1: Block Diagram of a traditional Spectroscopy System

The traditional acquisition system for Radiation Spectroscopy is usually made of an almost all-analog chain, where the electronics rely upon three fundamental devices: the Charge Sensitive Preamplifier, the Shaping Amplifier and the Peak Sensing ADC.

Usually, the result of a particle interaction within the detector's sensitive volume is the excitation of the absorber medium, e.g. scintillators, or the release of an observable burst of charge proportional to the energy lost by the particle in the interaction, e.g. semiconductors. In some cases, the value of this charge is sufficient to be managed by the front-end electronics, but in many applications, typically where a semiconductor detector is required, a preamplification stage is mandatory. In order to minimize the noise, it is wise to amplify the signal as close to the detector as possible, and sometimes to insert the very first stage of the preamplifier in the detector's architecture, as it happens in HPGe detectors.

The Charge Sensitive Preamplifier (**Fig. 3.2**) integrates the signal coming from the detector, thus converting the collected charge into a voltage step. Ideally, it is just a simple capacitor; however, in order to avoid saturation, the integrating capacitor is put in parallel with a discharging resistor, so that the preamplifier output will have pulses with a fast rise time and a long exponential tail with decay time τ . The charge information (proportional to the energy released by the particle in the detector) is here represented by the pulse height.

The charge-amplitude proportionality is set by the capacitor value $V_{out} = \frac{Q}{C}$ and the decay time of the output signal is $\tau = RC$.

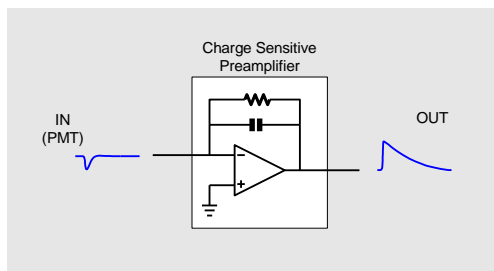


Fig. 3.2: Simplified schematic of a RC-type Charge Sensitive Preamplifier

In order to have a good charge-amplitude conversion and to minimize the noise, the decay time τ is much larger than the width of the detector signal, typically 50-100 μ s, and for this reason pile-up of different particle detections can arise (**Fig. 3.3**)

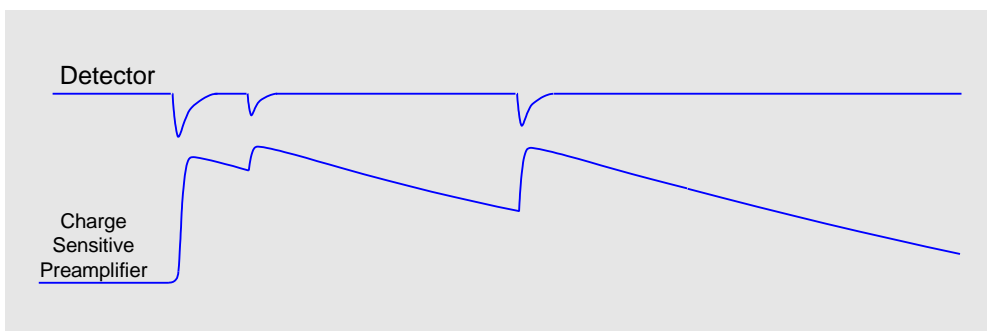


Fig. 3.3: Pile-up of detector signals due to the large decay time of the Preamplifier output

Another issue with the output signal of the Charge Sensitive Preamplifier is when the peak is too sharp for the Peak Sensing ADC to be detected with the required precision.

In order to avoid these problems in a traditional analog acquisition chain a Shaping Amplifier is requested. This amplifier receives the signal from the Preamplifier output and provides a quasi-Gaussian output whose width can be changed selecting different shaping time. The height is still proportional to the energy released by the detected particle.

In this way it's possible to reduce the pile-up and feed the Peak Sensing ADC with a smooth signal.

Finally, the Peak Sensing ADC is capable to evaluate and digitize the height of the pulses output by the Shaping Amplifier, filling a histogram with these values, i.e. an energy spectrum.

In order to preserve the timing information, the fast component of the signal (rising edge) is usually treated by a Fast Amplifier (or Timing Amplifier) that derivates the signal; the output of the fast amplifier usually feeds a chain made out of a Discriminator (CFD), a TDC and/or a Scaler for the timing/counting acquisition. Further modules can be present in order to implement logic units, make coincidences (giving the position and the trajectory of the particles), generate triggers or give information about the pulse shape (time over threshold, zero crossing, etc.) for the particles identification. Usually the Fast Amplifier is included into the Shaping Amplifier module and the relevant signal is provided as a separate fast output (or timing output).

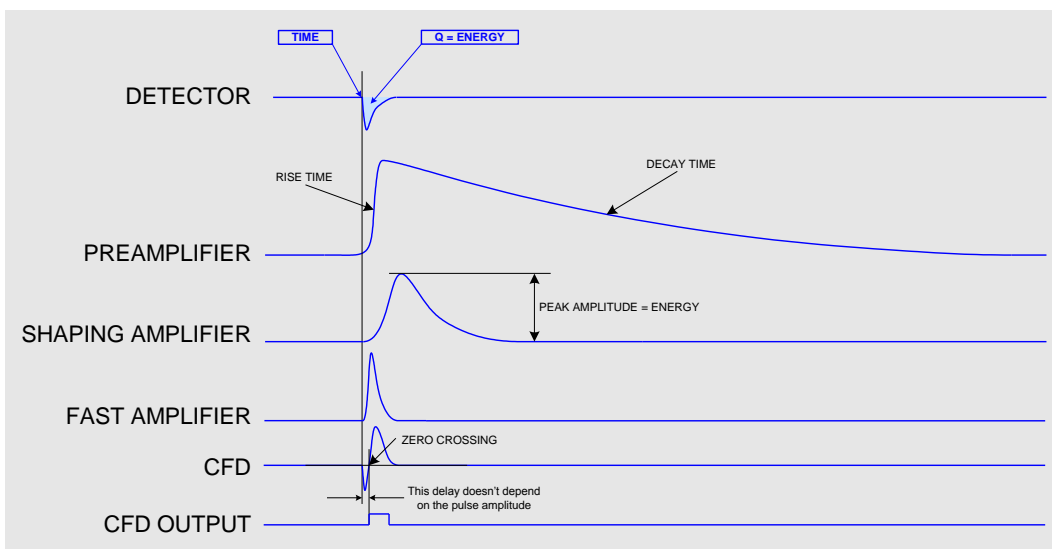


Fig. 3.4: Signals in the traditional analog chain

CAEN Digital Approach

As mentioned in the **Introduction**, the DPHA is a waveform Digitizer with on-line Digital Pulse Processing capabilities (DPP-PHA Firmware) managed by the DPP-PHA Control Software. Unlike the traditional acquisition chains for spectroscopy, in which the signal is treated by a certain number of analog blocks and then converted to digital at the end of the chain, in a digital MCA this approach has been reversed: the A/D conversion is performed at the input of the module by a flash ADC (in this case 14-bit @100 MSPs) whose output data (a continuous stream of digital samples) are managed by an FPGA that applies filters and algorithms for the extraction of the quantities of interest, such as the pulse height for the energy calculation, the baseline, the time stamp, etc.. The benefits of the digital approach are great stability and reproducibility, ability to reprogram and tailor the algorithms to the application, ability to preserve the information of the signal along the entire acquisition chain, flexibility, better correction of unwanted effect such as baseline fluctuation, pile-up, ballistic deficit, etc.. All this in a single board.

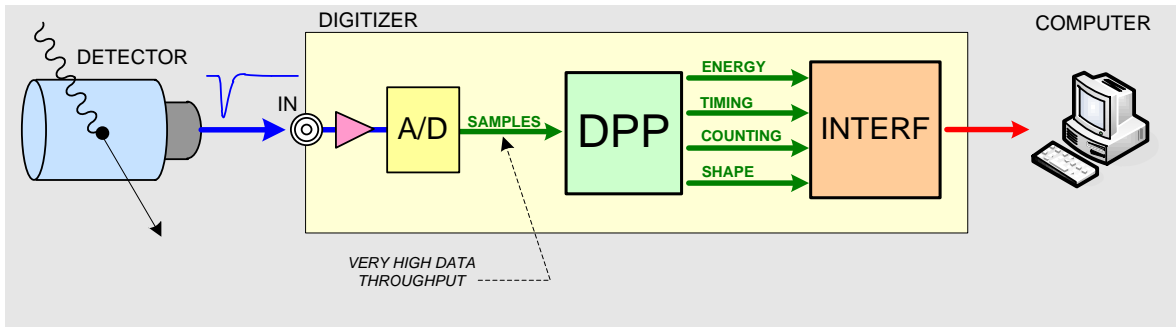


Fig. 3.5: Block Diagram of a Digitizer-based Spectroscopy System

Fig. 3.6 shows the block diagram of the filters implemented inside the FPGA.

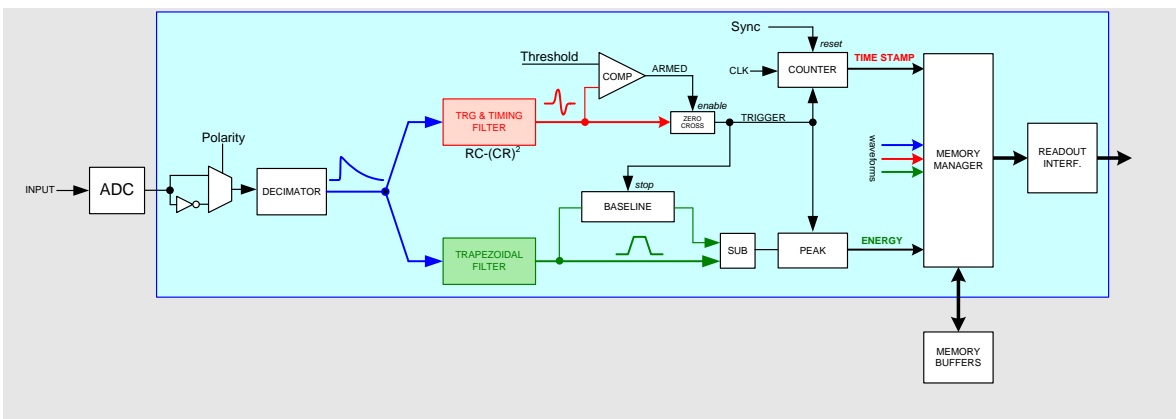


Fig. 3.6: Block Diagram of the processing chain programmed into the Digitizer's FPGA

Referring to the analog approach, in the DPHA the Digitizer replaces both the Shaping Amplifier and the Peak Sensing ADC, operating on the signals generated by the CSP; these are characterized by pulses with a relatively fast rise time (typ. 100 ns – 1 μ s) and a slow exponential decay time (typ. 50 μ s time constant). The pulses are assumed to be positive; in case of negative output, the DPHA is able to digitally invert the input and make it positive.

Decimator

The first block after the polarity selector is a decimator filter; this can be used in the case the signal is particularly slow, hence it is necessary to set values for the DPP time parameters that are not within the allowed range. The effect of the decimator is to scale down the sampling frequency of a factor 2, 4 or 8; it might have also benefits in terms of noise, since it averages a certain number of samples to make a new sample for the data stream.

Trigger and Timing Filter

After the decimator, there are two parallel branches: one for timing and triggering, the other one for the energy. The aim of the Trigger and Timing Filter (TTF) is to identify the input pulses, generate a trigger on them and calculate the time stamp by means of a kind of “constant fraction discriminator”. To make an analogy with an analog system, the TTF is like a RC-CR² filter: the integrative component is a smoothing filter based on a moving average filter that reduces the high frequency noise and prevent the trigger logic to generate false triggers on spikes or fast fluctuation of the signals. Instead, the purpose of the derivative component is to subtract the baseline, so that the trigger threshold is not affected by the low frequency fluctuation and, that is more important, by the pile up. As a result of the double derivation (CR²), the output signal of the TTF is bipolar and the zero crossing is independent of the pulse amplitude. This is the same principle of the CFD, although the algorithm is different. The trigger logic uses the threshold to get armed, then waits for the zero crossing to generate the trigger signal. It is worth noticing that the digital derivation is obtained by the difference between two samples separated by a programmable gap: $D_i = S_i - S_{i-k}$, where k is the gap that can be programmed by means of the *Delay* parameter (defined in the **GUI Description** section of Chapter 5); usually, in order to maximize the amplitude of the TTF output, k is set to a value between one and two times the rising edge of the input signal.

Trapezoidal Filter (Energy Filter)

The trapezoidal filter (TF) for the energy calculation has the same purpose of the Shaping Amplifier in the analog MCA: it transforms the long exponential decay of the signal into a trapezoidal shaped signal whose amplitude is proportional to the input pulse height (energy). In order to reduce the pile-up, the duration of the trapezoid is usually much shorter than the input exponential pulse; the user can program the rise time of the trapezoid (that is always equal to the fall time) as well as the width of the flat top. In analogy with the shaping time of the analog systems, choosing the rise time of the trapezoid is a compromise between resolution and pile-up rejection (dead time). It is also possible to program the position on the flat top where the peak is calculated; this setting is particularly important for large volume detectors in which the ballistic deficit causes a significant error in the energy calculation; this error can be corrected by delaying the time at which the trapezoid peak is sampled, thus waiting for the full charge collection.

The trapezoid, like the Gaussian pulse of the shaping amplifier, requires an accurate pole-zero cancellation in order to guarantee the correct return to the baseline at the end of the falling edge; in theory, when the pole-zero compensation is perfect, after a finite and deterministic time equal to $2T_R + T_F$ (where T_R is the rise/fall time and T_F is the flat top) the output of the trapezoidal filter goes back to the baseline. This is a great advantage of the digital filter compared to the analog shaping amplifier in which the tail of the pulse is unlimited, at least from the mathematical point of view.

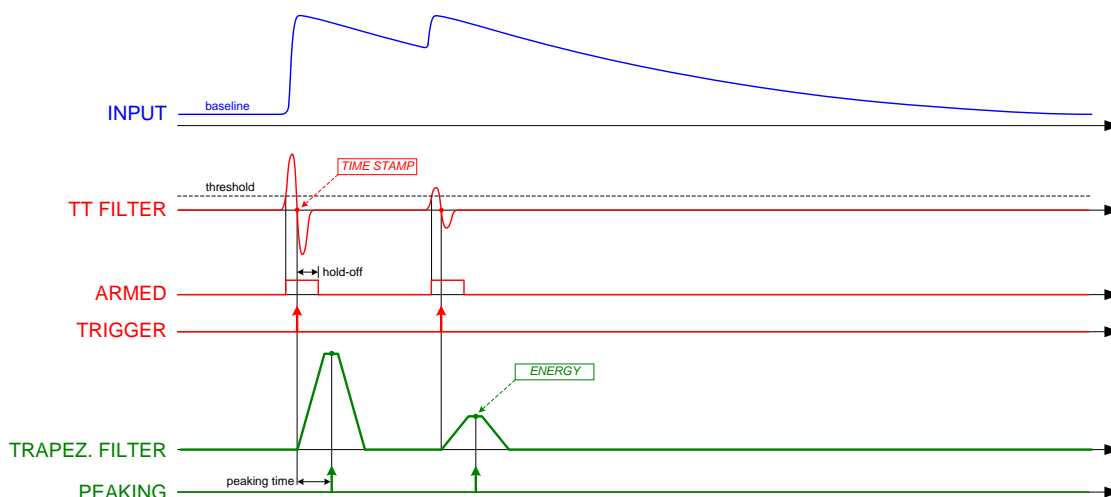


Fig. 3.7: Simplified signals perspective of the two parallel processing branches

Baseline Restorer

The energy filter includes also a baseline restorer; this operates on the trapezoidal filter output and calculates the baseline by averaging a programmable number of points before the start of the trapezoid. The baseline is then frozen during the ramp up and used in the height calculation. Once the trapezoid is returned to the baseline (ramp down), the averaging restarts to run.

The pulse height (i.e. the trapezoid amplitude) is given by the distance between the flat top and the baseline taken in the programmed position; in order to further reduce the fluctuation of this distance due to the noise, it is possible to average a certain number of points in the flat top before subtracting the baseline.

Pile-up Rejector and Live Time correction

If two pulses are separated by less than the trapezoid duration ($2T_R + T_F$), then the relevant trapezoids overlap. There are three different cases (Fig. 3.8):

- 1) the rising edge of the 2nd trapezoid overlaps the falling edge of the 1st one ($T_R + T_F < \Delta T < 2T_R + T_F$); in this case, the amplitude of both trapezoids is not affected by the pile-up and the energy can be calculated for both them.
- 2) the 2nd trapezoid starts on the rising edge or on the flat top of the 1st one ($\Delta T < T_{PK}$); in this case, the amplitude of both the trapezoid is corrupted and the relevant energies cannot be calculated. The firmware saves, in the time stamp and energy "list" of the board RAM, a zero value for the energy. According to a specific register value, the event can also be tagged as pile-up event (see bit "PU" in Fig. 5.1).
- 3) The two pulses are so close that the trigger filter is unable to resolve the double pulse condition ($\Delta T < \text{Input Pulse Rise Time}$). In this case, the pile-up cannot be recognized and the two pulses are threaded as a single pulse, thus giving only one time stamp and one energy, whose value is about the sum of the two energies (this effect is often clearly visible as a phantom 'sum peak' in the spectrum). The Rise Time Discriminator is a technique that increases the probability of double pulse detection even when they are very close.

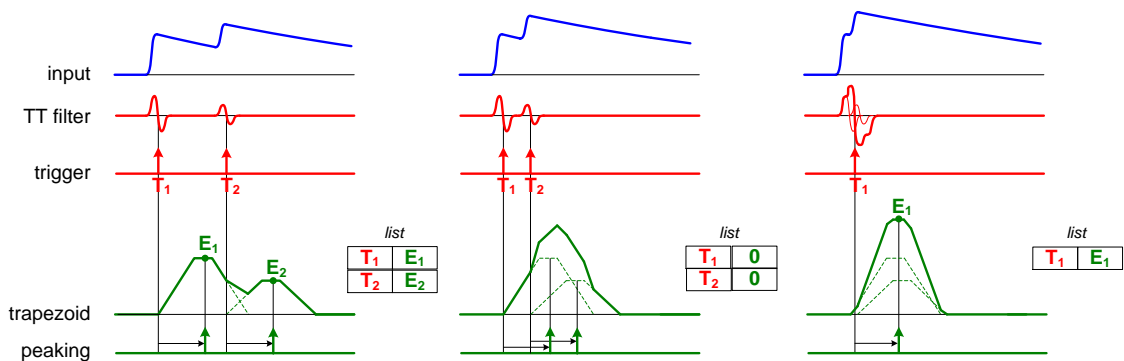


Fig. 3.8: The effect of trapezoids overlapping in three main cases: 1) The second trapezoid starts on the falling edge of the first one (left). 2) The second trapezoid starts on the rising edge ($\Delta T < T_{PK}$) of the first one (center). 3) The second trapezoid starts on the rising edge of the first and $\Delta T < T_R$

Except for the case 3, the DPFA is therefore able to save into the memory buffer all the incoming events, including the piling-up pulses; for these pulses, only the time stamp is available, while the energy is meaningless. During the readout of the event list, these events won't be accumulated into the histograms (that are calculated in the software), although they participate the total count, thus giving an accurate estimation of the activity (Input Count Rate). Furthermore, the energy spectrum can be corrected run-time by a statistical redistribution of the missed energies over the spectrum acquired within a specific time slot.

As already said, the acquisition in the PDFA is continuous and dead-timeless (there is not any conversion time), although the pile-up can occur also in a digital MCA and it causes, like in the analog chains, loss of energy values. The difference is that for a digital system, the amount of missed events is known, while for the analog systems the count loss is calculated on a statistical base. For an analog MCA, the dead-time is the amount time during which the system is not able to record events; therefore, at the end of the acquisition, the energy spectrum and the total count rate are rescaled with a factor equal to dead-time/total-time. For a digital MCA, in analogy with the analog ones, the dead-time can be defined as the ratio between the energy calculated and the total number of events.

A description of the capability of the 724 series (14 bit, 100MSps) to perform Pulse Height Analysis in Radiation Spectroscopy is reported in [RD3].

4 Acquisition Modes

The DPPHA allows for three main acquisition modes: Oscilloscope, List and Mixed.

1. **Oscilloscope Mode:** this acquisition mode is mainly intended to debug and to set the DPP parameters. For each trigger (internal or external), the digitizer saves a portion of the waveform (i.e. a sequence of samples within the acquisition window) into a local memory buffer. Running in Oscilloscope Mode, the user can view the input signal, the baseline, and other control signals (such as the trigger, the gate, the trigger hold-off, etc...) in the same plot. This makes easier to adjust the parameters for the acquisition. Running in oscilloscope mode implies a very high data throughput, due to the huge amount of samples saved into the board memory and then read out by the DAQ software.
2. **List Mode:** this is the mode where the DPP algorithm is applied runtime by the FPGA on the input signals. Once the parameters are properly set in the Oscilloscope Mode, the acquisition can be switched to the List Mode (histogram mode in the DPP Control Software). The waveform recording is disabled, while time stamp and integrated charge are calculated and saved into the local memory buffer for each triggered pulse. As soon as the list reaches a certain size, it is made available for readout and the acquisition continues in another buffer. This feature assures an acquisition with *no dead time*. Being the size of the event very small (typically few bytes), the throughput is extremely reduced.
3. **Mixed Mode:** in some applications, the simple charge/time stamp information is not enough and it is necessary to save also few samples (as raw waveforms) belonging to a specific region of interest. This is useful in sophisticated pulse shape analyses, as pulse fitting, that cannot be implemented on-line by the FPGA. Another example is when, to increase the timing resolution (10 ns for the x724 module) it is required to interpolate the samples around the threshold and evaluate the crossing timing. In all these cases, it is possible to read the charge, the baseline and the time stamp information together with a portion of the waveform, so that the user can retrieve further information and use it off-line, still keeping a reasonable level of throughput bandwidth.



Note: Mixed Mode is not managed by the DPP-PHA Control Software.

Trigger Modes

The general operating principle of a digitizer running with DPP-PHA firmware is summarized in **Fig. 4.1**. Each channel of the board can trigger on the input pulse independently from the other channels. When the input is over-threshold the channel FPGA sends a “Trigger Request” (TRG_REQ) signal, that enables the event building.

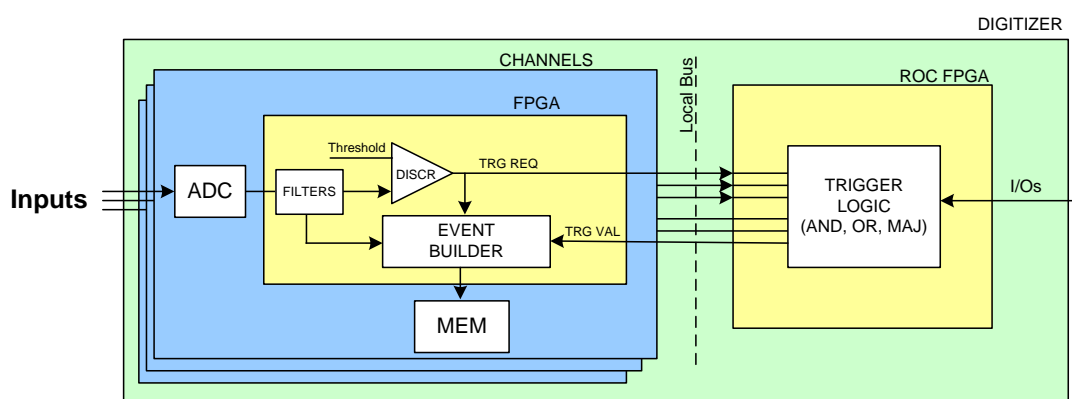


Fig. 4.1: Schematic chain of the trigger architecture of a DPP system

There are three possible ways to acquire the events and save the information on the board memory (**Fig. 4.1**). In the simplest case each channel acquires through its individual TRG_REQ independently from the other channels. This is the “Normal (Individual) trigger mode”.

Otherwise, in the “Coincidence/Anticoincidence Trigger Mode” all the trigger requests can be sent to the common “ROC FPGA” for the coincidence evaluation. The ROC can be programmed to look for triggers within a programmable window, through the Individual Trigger Logic (ITL) that can perform the logic operation of AND, OR, or Majority. When the coincidence condition is met, the ROC sends back a “trigger validation” signal, one per channel. The coincidence

logic is individual, so that it is possible to program different coincident conditions for each channel. The trigger validation enables the data saving into the memory buffer. In this way the channel uses its local trigger for the event building (time stamp, gate, etc..) but only those events having the validation are saved into the memory.

The last way is called “*Neighbour Trigger Mode*”. In this case the event building can be enabled with a TRG_VAL signal only, even if no TRG_REQ has been occurred for that channel. This may happen when a “neighbour” channel is over-threshold and generates a TRG_REQ. Then its previous and consecutive channels receive a TRG_VAL signal too, and they can start the event building with the TRG_VAL signal as reference. This is particularly useful in case of strip detector where you want to read data not only from the channel that triggered, but also from its “neighbours”.

Normal (Individual) Trigger Mode

In the normal (individual) trigger mode each channel can trigger on the input pulse independently from the other channels.

Referring to **Fig. 4.2** the input signal is discriminated if over-threshold (OVTH). After the discrimination, through a multiplexer, it is possible to select the output itself, or a logic pulse of adjustable time width T_{ST} . This is the *shaped trigger* that enables the “trigger request” (TRG_REQ) for data acquisition. Unlike the Coincidence or Neighbour acquisition modes, the TRG_VAL signal is always set to 1, so the event builder is activated when either a TRG_REQ, or an Individual Trigger (ITRG), or a Global Trigger (GTRG) signal arrive.

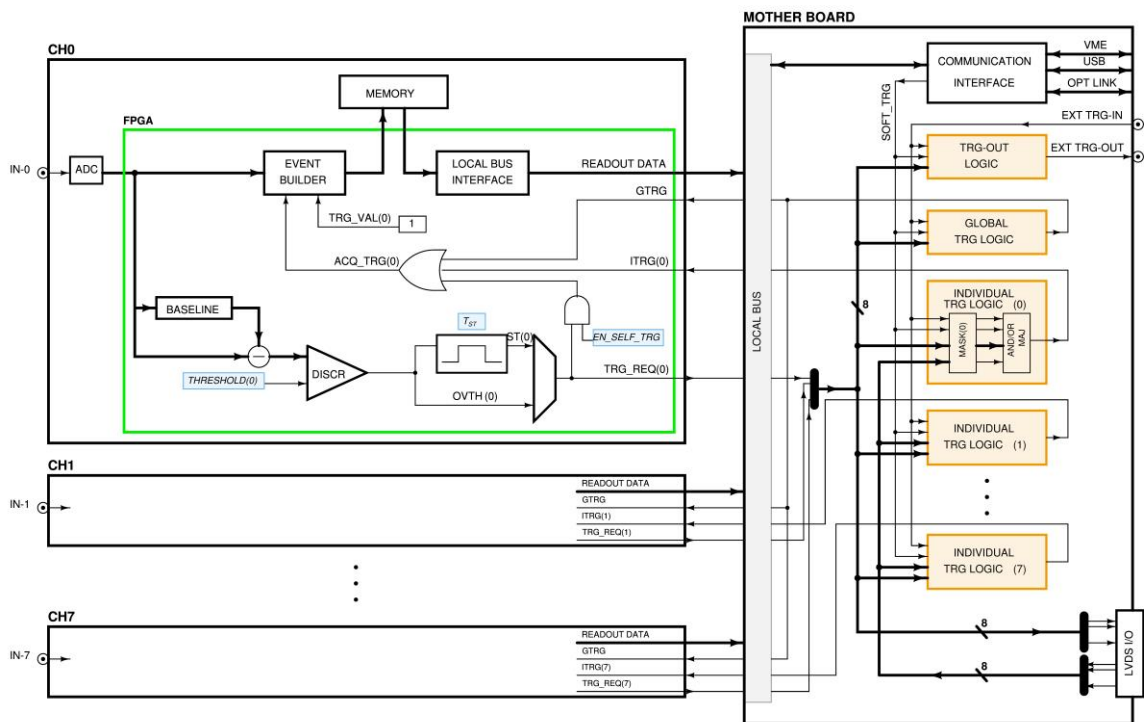


Fig. 4.2: Block diagram of the Trigger Architecture in a DPHA board

In the DPHA the input pulse is fed into a Trigger and Timing Filter for the proper trapezoid calculation. When its output exceeds the programmed threshold, the trigger logic gets armed (the signal “armed” goes high), then it waits until the zero crossing to fire the Trigger Request TRG_REQ (**Fig. 4.3**). It is also possible to enable the Rise Time Discriminator whose purpose is to detect double pulses the pile-up on the rising edge; in fact, in this case, the rise time of the input signal gets longer. The user can define an acceptance window RTDwin timed by the armed signal; if no TRG_REQ (zero crossing) occurs within that window, then the trigger logic assumes that two or more pulses are piling up and two triggers are issued. The RTD is disabled when $Trtdw = 0$.

After the TRG_REQ, it is possible to program a trigger hold-off time window to prevent a new trigger to be generated on the tail of the RC-CR2 signal. This might happens especially when the input pulses have an over-shoot that causes a small end pulse at the output of the timing filter. Another reason for using the trigger hold-off is to create a known dead-time in the acquisition.

When TRG_REQ is generated, the energy filter goes into the run state ($pkrun = 1$) and the calculation of the trapezoid baseline is frozen ($baseline_off = 1$). Note that there is a small delay (16 clock cycles) between the TRG_REQ and the start of the trapezoid; this prevents the baseline to be frozen when the trapezoid already started.

The peaking time T_{pk} defines the position on the flat top where the energy is calculated; in this trigger mode, T_{pk} starts with the TRG_REQ. Starting from the peaking time T_{pk} , it is possible to average a certain number of points on the flat top (Tpkavg).

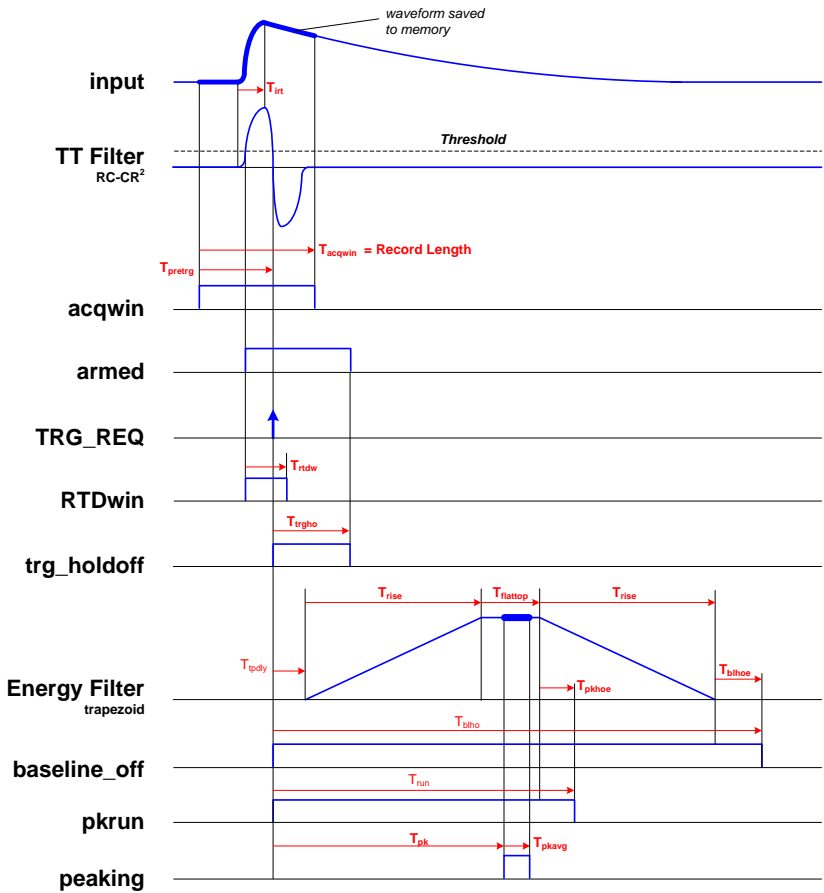


Fig. 4.3: Timing diagram (Normal Trigger Mode)

According to the theory of the trapezoid filter, it is possible to accept a new trigger as soon as the flat top of the previous one is finished. However, it is always better to keep some safety margin (T_{pkhoe}); the effect of this parameter is to increase the width of the $pkrun$ window. If a new TRG_REQ arrives within that window, then this event is identified as pile-up. There are three different cases, as shown in the following pictures:

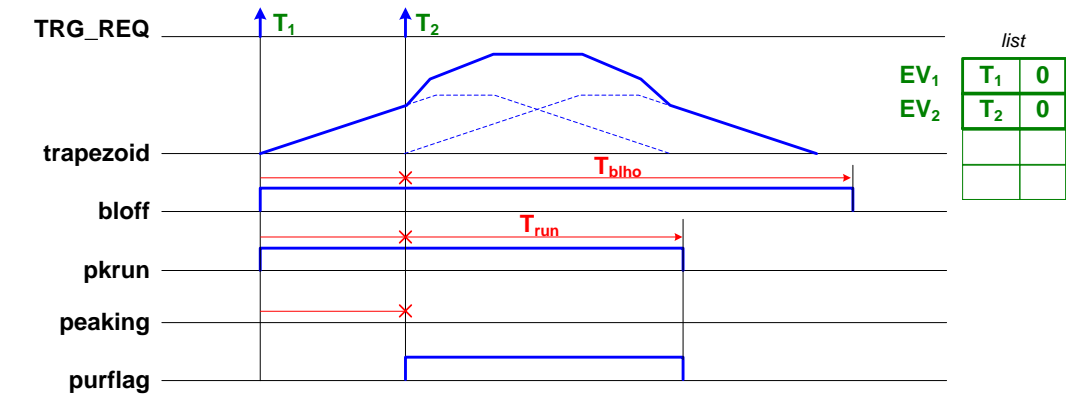


Fig. 4.4: Pile-up occurred before the peaking time

When the second TRG_REQ occurs before the peaking time (**Fig. 4.4**), then the energy filter output becomes meaningless and the pile-up inspector rejects both TRs. In this case, the event builder saves two time stamps and zero for the relevant energies (see the memory content represented in green). Notice that the second TRG_REQ restarts the timer for Trun and Tblho while Tpk is aborted (red crosses).

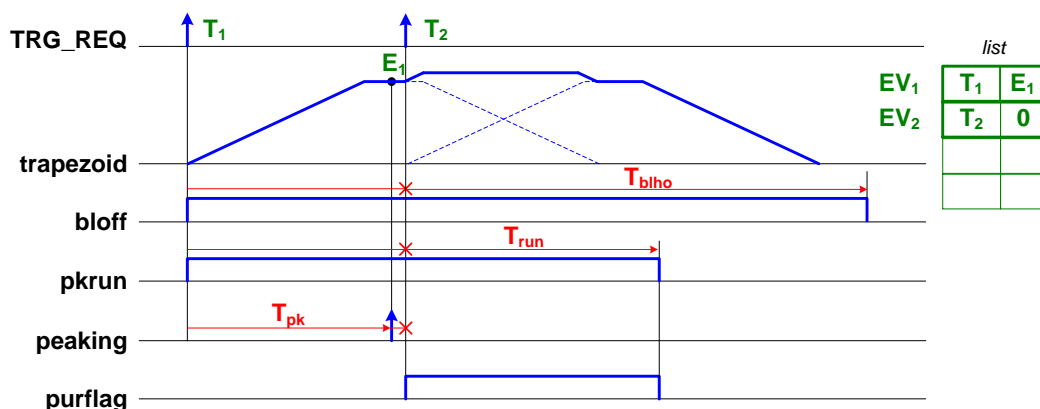


Fig. 4.5: Pile-up occurred after the peaking time

If the second TRG_REQ occurs after the energy of the previous has been saved (but still before the end of pkrun), then only the second TRG_REQ will be rejected (see **Fig. 4.5**).

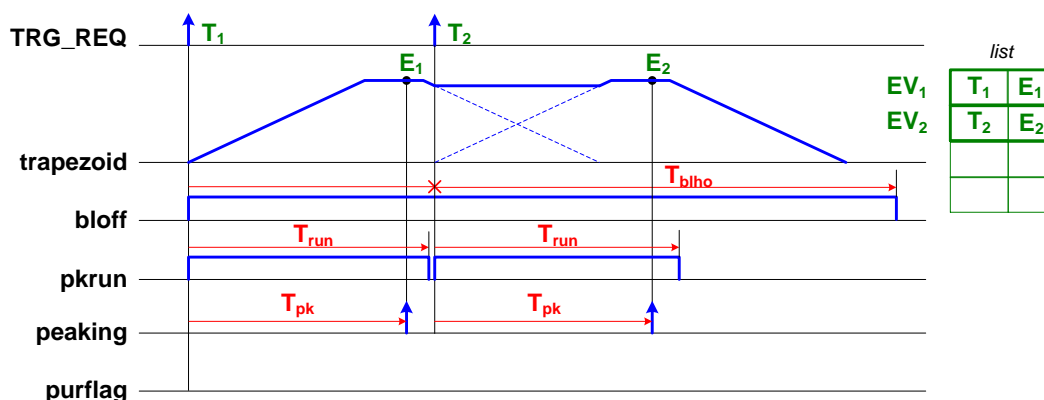


Fig. 4.6: Overlapped trapezoids that don't cause pile-up rejection

If instead the second TRG_REQ occurs outside the pkrun window, although the two trapezoids are piled-up, both energies can be calculated and there is no pile-up rejection. However, in this case, the baseline of the second trapezoid cannot be recalculated, thus the same baseline calculated for the first trapezoid will be used for the second one too (see **Fig. 4.6**).

When the counting rate is high, it might happen that the baseline is kept off for many subsequent pulses and this can significantly worsen the energy resolution. In this case, it is possible to increase Tpkhoe and make pkrun longer than the full trapezoid width or even more. Doing that, the pile-up inspector will reject all the pulses but those that are well separated, thus allowing the baseline to be properly calculated for every pulse. By default, the baseline calculation starts again at the end of the trapezoid but it is possible to delay it by the Tblhoe value.

Coincidence Trigger Mode

Acquiring coincident events is a common task in physics, and the DPP-PHA firmware allows you to make online coincidences among channels. As already introduced, the TRG_REQ signal can be sent to the ROC FPGA (mother board) that makes a programmable Individual Trigger Logic (ITL) calculation among the logic AND, OR, or Majority¹ (Fig. 4.7). The ITL has the same multiplicity of the number of channel, and each ITL can be programmed with a different logic function. Moreover the ITL can receive as input not only the TRG_REQ from all channels, but also the signal from the front panel output GPIO (line 0 to 7 of the LVDS I/O connector – VME only), the software trigger (SOFT_TRG), and the external trigger (EXT TRG-IN).

The user has the possibility to rather program a Global Trigger Logic (GTL) or a “TRG_OUT logic”. The GTL and the TRG_OUT logic can receive as inputs the TRG_REQ from all channels, the EXT TRG-IN and the SOFT TRG. They cannot receive the inputs from the LVDS I/O. At the moment these logic units can perform only the OR operation. There is one GTL for all channels, since its output triggers all channels simultaneously, while the TRG_OUT logic allows to send the trigger request outside the board.

Either the ITRG and the GTRG can generate the TRG_VAL signal. To save the event into the memory the TRG_VAL signal has to arrive within a programmable time window TVAW (Trigger Validation Acceptance Window). If the TRG_VAL signal is outside the TVAW than the event is rejected.

In this trigger mode, all timings are referred to TRG_REQ, and the TRG_VAL never causes pile-up.

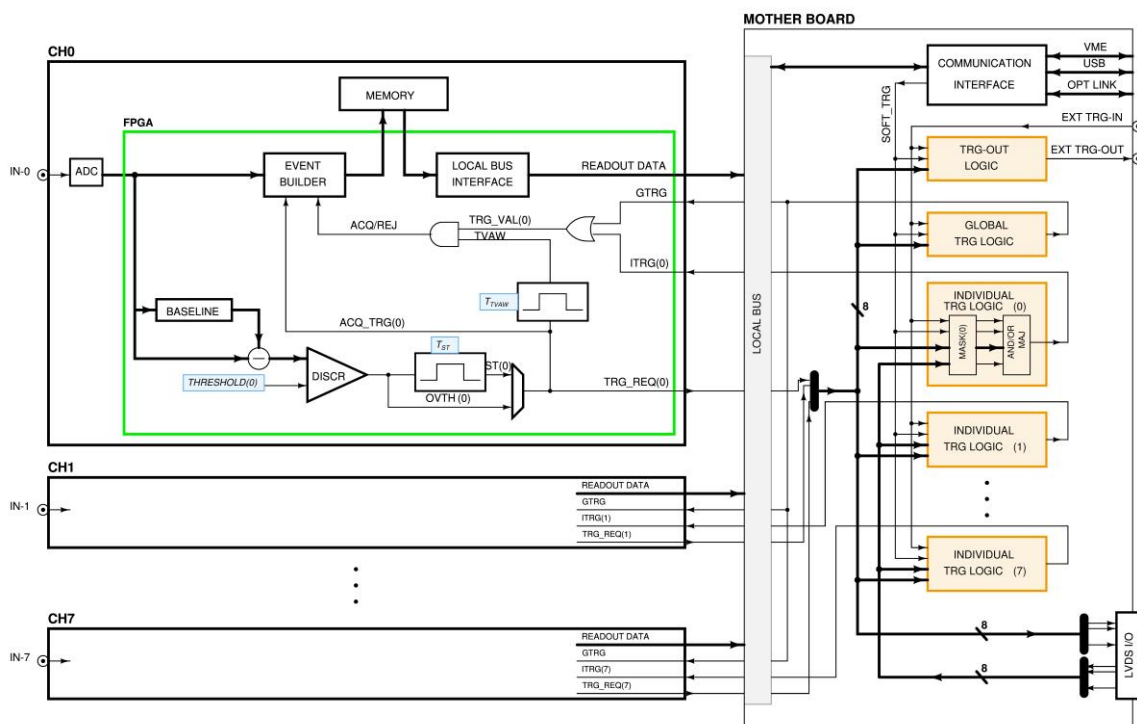


Fig. 4.7: Block diagram of the Trigger Architecture in a DPHA board

More information and detailed instructions on how to make coincidences among channels of the same board can be found in [RD5].

Anti-coincidence Trigger Mode

The structure of the anti-coincidence trigger mode is exactly the same of the coincidence one, the only difference being the logic operation performed between the TRG_VAL signal and the TVAW. Indeed the event is saved into memory when no TRG_VAL signal arrives within the TVAW window.

Refer to [RD5] for more information and detailed instructions on how to make anti-coincidences among channels of the same board.

¹ The Majority is true when at least a programmable “majority level” number of enabled inputs are in coincidence.

Neighbour Trigger Mode

In the neighbour trigger mode, each channel still self-trigger on the input pulse. Moreover its TRG_REQ generates a TRG_VAL signal that enables the data writing of the channel itself and of the “neighbour” channels, i.e. the previous and the consecutive.



Note: The neighbor trigger mode is particularly useful with strip detectors.

In order to have the same peaking times and the same waveform acquisition window in both cases (channel triggered by TRG_REQ or by TRG_VAL), Tpk and Tpretrg are referred to TRG_VAL instead of TRG_REQ. For this reason, the trigger logic that generates TRG_VAL must keep the jitter between TRG_REQ and TRG_VAL as low as possible. Also the time stamp saved in the event data is that one of TRG_VAL.

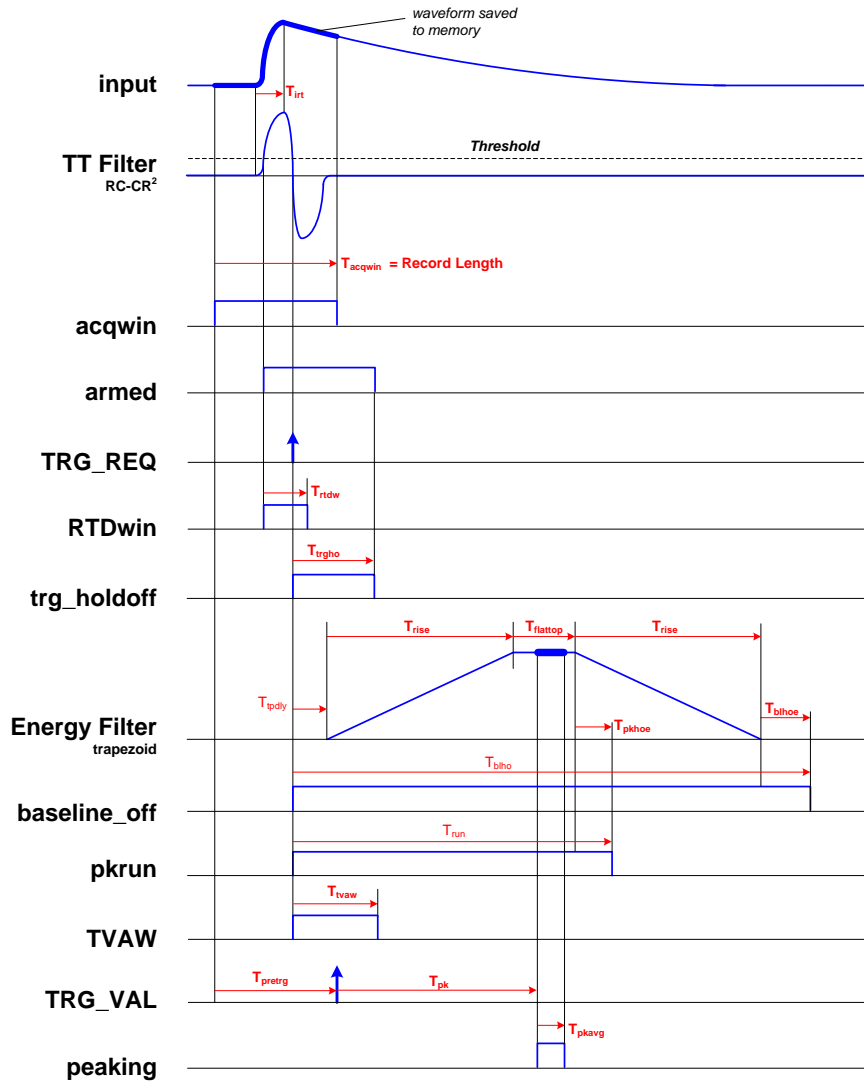


Fig. 4.8: Timing diagram (Neighbour Trigger Mode)

If TRG_VAL signal arrives outside the TVAW window (see Fig. 4.9), then the event will have the pile-up flag. Indeed TRG_VAL is not related to the event that caused the TRG_REQ in that channel and the calculated energy value is not properly evaluated.

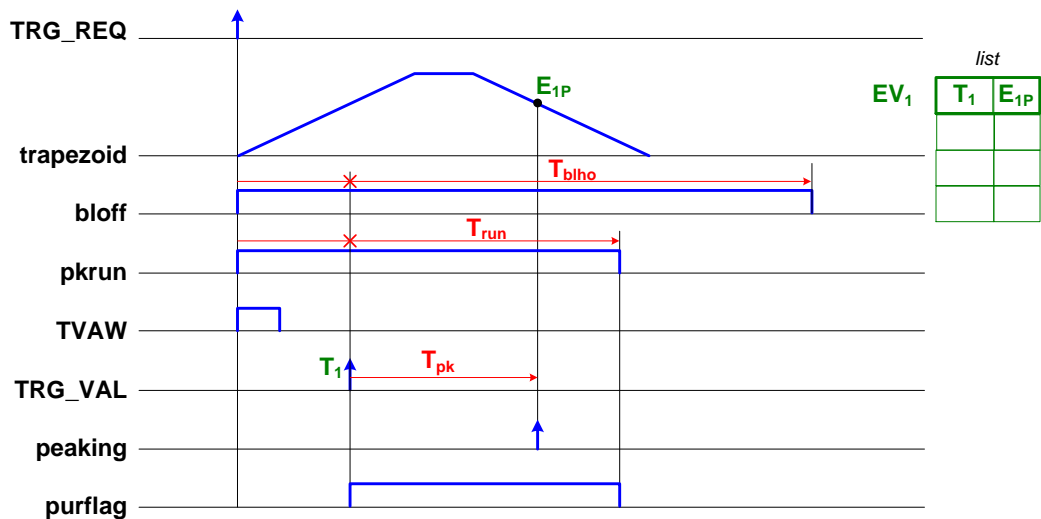


Fig. 4.9: TRG_VAL outside the acceptance window

If a “neighbour” channel triggers and gets a valid TRG_VAL signal, then also the neighbour channels, even if they do not have enough charge to enable their own TRG_REQ, they receive the same TRG_VAL signal (see Fig. 4.10). Please note that, unlike in the Normal Trigger Mode, the energy value latched at Tpk is saved into the memory with bit[15] = 1 (see **Channel Aggregate Data Format for 724 series**) indicating the pile-up condition. When the neighbour channel receives the TRG_VAL signal it starts its Tpk and Trun counters even though the value measured will be probably close 0.

Refer to [RD5] for detailed instructions on how to enable this trigger mode with DPHA.

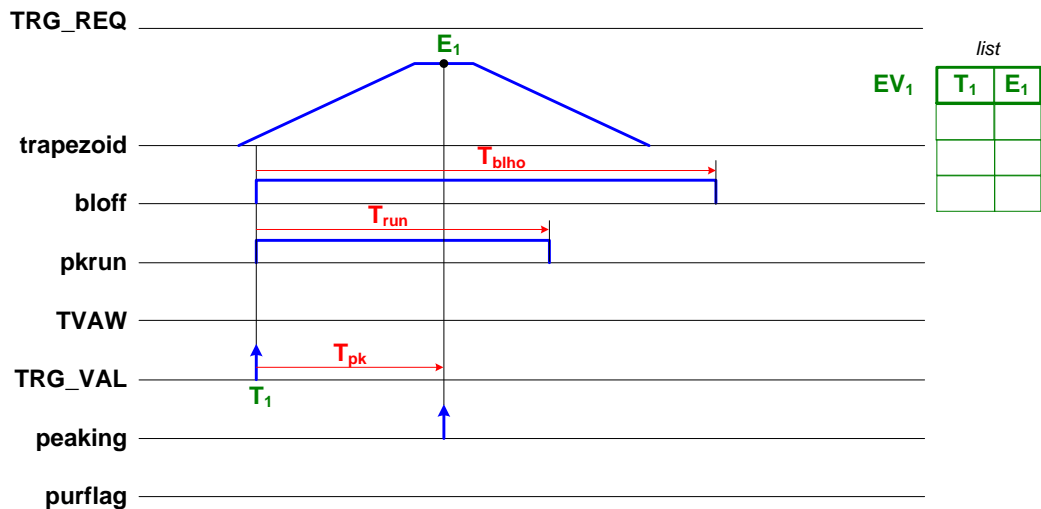


Fig. 4.10: TRG_VAL without TRG_REQ

The TRG_REQ pile-up condition for the Neighbour Trigger Mode is similar to Normal Trigger Mode (see the following figures).

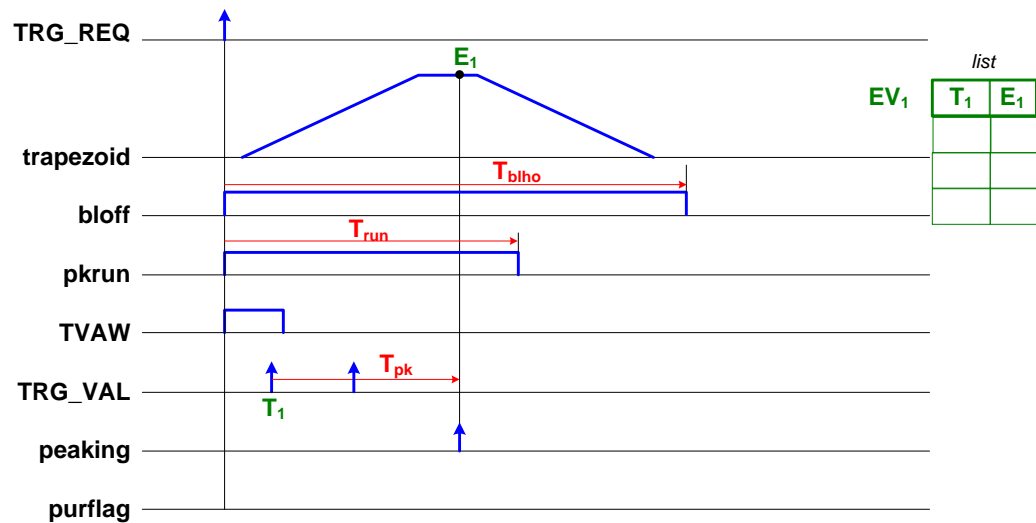


Fig. 4.11: Second TRG_VAL occurring within pkrun

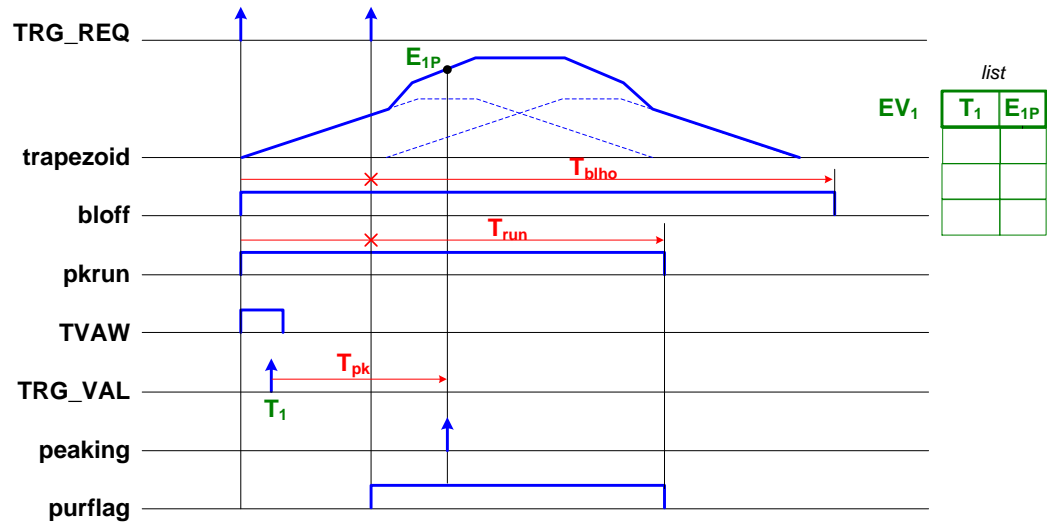


Fig. 4.12: Pile-up occurred before the peaking time (Neighbour Trigger Mode)

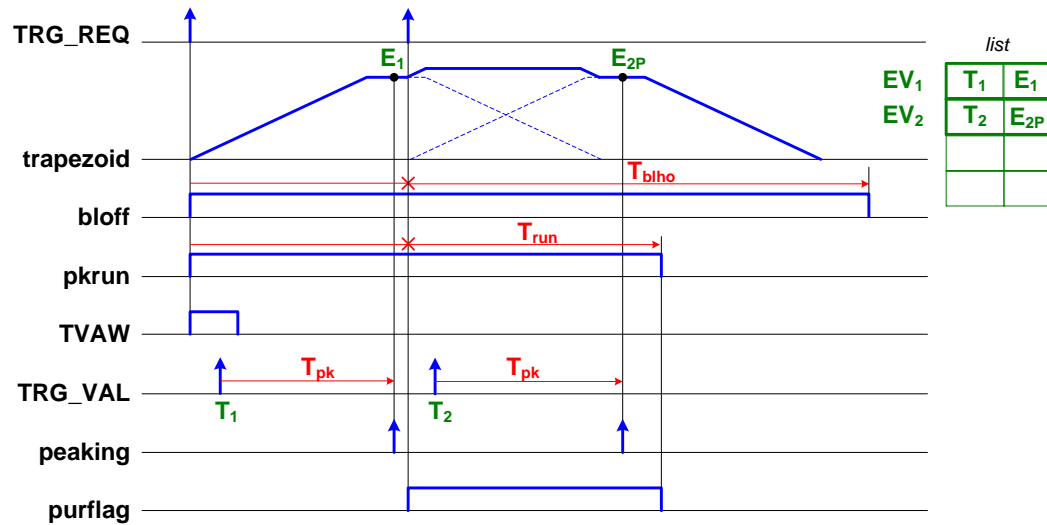


Fig. 4.13: Pile-up occurred after the peaking time (Neighbour Trigger Mode)

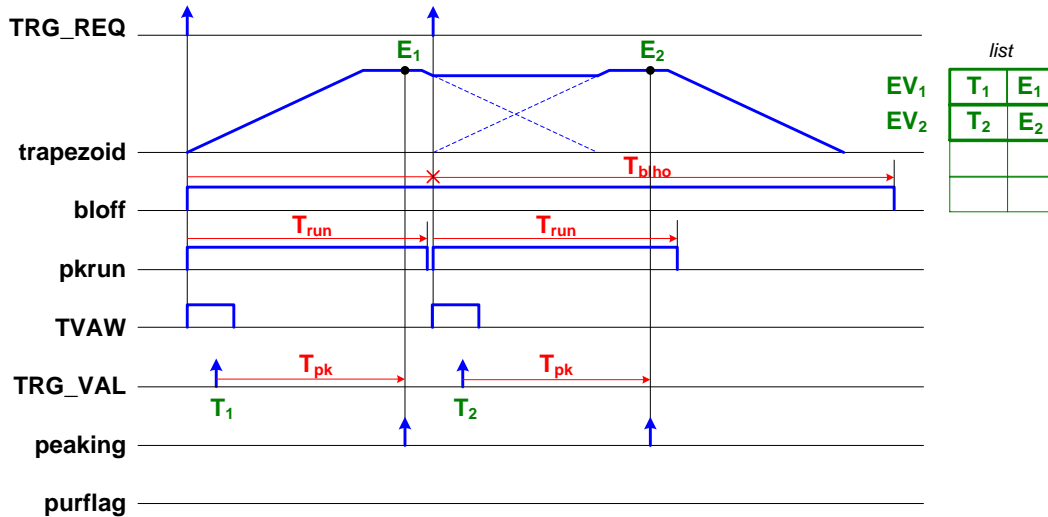


Fig. 4.14: Overlapped trapezoids that do not cause pile-up rejection (Neighbour Trigger Mode)

Synchronization among different boards

In cases when multi-board systems are involved in the experiment, it is necessary to synchronize different boards. In this way the user can acquire from N boards with Y channel each, like if they were just one board with (N x Y) channels.

The main issue in the synchronization of a multi-board system is to propagate the sampling clock among the boards. This is made through input/output daisy chain connections among the digitizers. One board has to be chosen to be the “master” board that propagates its own clock to the others. A programmable phase shift can adjust possible delays in the clock propagation. This allows to have both the same ADC sampling clock, and the same time reference for all boards. Having the same time reference means that the acquisition starts/stops at the same time, and that the time stamps of different boards is aligned to the same absolute time.

There are several ways to implement the trigger logic. The synchronization tool allows to propagate the trigger to all boards and acquire the events accordingly. Moreover in case of busy state of one or more boards, the acquisition is inhibited for all boards.

Refer to [RD6] for more details on how to synchronize CAEN digitizers.

5 Memory organization

The DPP-PHA firmware manages two acquisition modes: the oscilloscope and the list mode (see also Chapter **Acquisition Modes**). In the first case the firmware saves into the board memory the waveforms of the analog and digital probes, while in the list mode the firmware saves into memory the list of time stamp and energy values.

The Control Software then reads the board memory and it can plot and save the waveforms in the first case, and the time or energy histograms in the second case.

This chapter is intended to provide the encoding of how the software reads the board memory to get the proper information. Those who need to write their own acquisition software must take care of the following sections.

Event Data Format

Each channel has a fixed amount of RAM memory to save the event information. The memory is divided into a programmable number of buffers (also called “aggregates”), where each buffer contains a programmable number of events.

When the data readout is performed, the data format will appear as follows.

Channel Aggregate Data Format for 724 series

The Channel Aggregate is composed by the set of N_e events, where N_e is the programmable number of events contained in one aggregate. The structure of the Channel Aggregate of two events (EVENT 0 and EVENT 1) for 724 series is shown in Fig. 5.1, where:

“CHANNEL AGGREGATE” DATA FORMAT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	BIT
FI											AGGREGATE SIZE																		SIZE			
DT	ES	EE	ET					VP1	VP2	DP			NUM SAMPLES/2															FORMAT				
TT		TRIGGER TIME TAG																													EVENT 0	
T ₁	D ₁	S ₁										T ₀	D ₀	S ₀																		
T ₃	D ₃	S ₃										T ₂	D ₂	S ₂																		
T _{n-1}	D _{n-1}	S _{n-1}										T _{n-2}	D _{n-2}	S _{n-2}																		
											EXTRAS			PU	PEAK (ENERGY)															EVENT 1		
TT		TRIGGER TIME TAG																														
T ₁	D ₁	S ₁										T ₀	D ₀	S ₀																		
T ₃	D ₃	S ₃										T ₂	D ₂	S ₂																		
T _{n-1}	D _{n-1}	S _{n-1}										T _{n-2}	D _{n-2}	S _{n-2}																		
											EXTRAS			PU	PEAK (ENERGY)																	

Fig. 5.1: Channel Aggregate Data Format scheme.

FI: when 1, the second word is the Format Info

DT: Dual trace enabled flag (0 = disabled, 1 = enabled)

ES: Waveform (samples) enabled flag

EE: Energy enabled flag

ET: Time Tag enabled flag

VP1: Virtual Probe 1 Selection. VP1 can be selected among:

- 00 = "Input": the input signal from pre-amplified detectors
- 01 = "RC-CR": first step of the trigger and timing filter
- 10 = "RC-CR2": second step of the trigger and timing filter
- 11 = "Trapezoid": trapezoid resulting from the energy filter

VP2: Virtual Probe 2 Selection. VP2 can be selected among:

- 00 = "Input": the input signal from pre-amplified detectors
- 01 = "Threshold": the RC-CR2 threshold value
- 10 = "Trapezoid-BL": the trapezoid shape minus the baseline
- 11 = "Baseline": displays the input baseline

DP: Digital Virtual Probe Selection. DP can be selected among:

- 0000 = "TRG Window": shows the RT Discrimination Width
- 0001 = "Armed": digital input showing where the RC-CR2 crosses the Threshold
- 0010 = "Peak Run": starts with the trigger and last for the whole event (see **Fig. 4.3**)
- 0011 = "Peak Abort": shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event
- 0100 = "Peaking": shows where the energy is calculated
- 0101 = "Trg Validation Win": digital input showing the trigger validation acceptance window TVAW (refer to **Acquisition Modes** chapter and **[RD5]**)
- 0110 = "BSL Holdoff": shows the baseline hold-off parameter
- 0111 = "TRG Holdoff": shows the trigger hold-off parameter
- 1000 = "Trg Validation": ": shows the trigger validation signal TRG_VAL (refer to **Acquisition Modes** chapter and **[RD5]**)
- 1001 = "Acq Veto": this is 1 when either the input signal is saturated or the memory board is full

TT: Trigger Type (0=self trigger, 1=external trigger)

S_m ($m = 0, 2, 4... n-2$): Even Samples of VP1 at time $t = m$

$S_{m'}$ ($m' = 1, 3, 4... n-1$): if $DT=0$, then $S_{m'}$ correspond to the odd Samples of VP1 at time $t = m'$. Otherwise, if $DT=1$, they correspond to even Samples of VP2 at time $t = m' - 1$

T_n : bit identifying in which sample the Trigger occurred

D_n : Digital Virtual Probe for each sample. The Probe type can be read from the "DP" field in the header

PU: Pile Up. This bit is usually set to zero. The user can recognize a pile up event when also the Energy value is zero. The user can also choose to have this bit equal to 1 in case of pile-up event, by enabling bit 27 of the DPP_CTRL register (0x1n80 register address). In that case the energy value is what read from the algorithm

EXTRAS: bit[16] = DEAD_TIME. This is set to 1 when a dead time occurred before this event. The dead time can be due to either a signal saturation or a full memory status

bit[17] = ROLL_OVER. Identify a trigger time stamp roll-over

bit[18] = TT_RESET. Identify a trigger time stamp reset forced from external signals in S-IN (GPI for Desktop)

bit[19] = RESERVED

Notes:

- 1) DEAD_TIME in case of signal saturation (**Fig. 5.2**). If the input signal is over-range (exceeds the input dynamic range of 16k ADC channels) then the acquisition is inhibited. As soon as the input signal is out of saturation a fake event is saved. This fake will have the bit[16] is set to 1, and the energy value set to FFFF. The dead time is equal to the time difference between the last trigger occurred and the fake-event trigger after the saturation.
- 2) DEAD_TIME in case of FULL board memory (**Fig. 5.3**). When the memory of the board is full, no trigger is accepted. When the board is ready to read again the input, events start again to be triggered in the usual way (zero crossing of the RC-CR2 signal). The first event after the FULL will have the bit[16] set to 1, and the energy value as read from the algorithm. As before, the dead time is equal to the time difference between the last trigger occurred and the trigger after the FULL status.

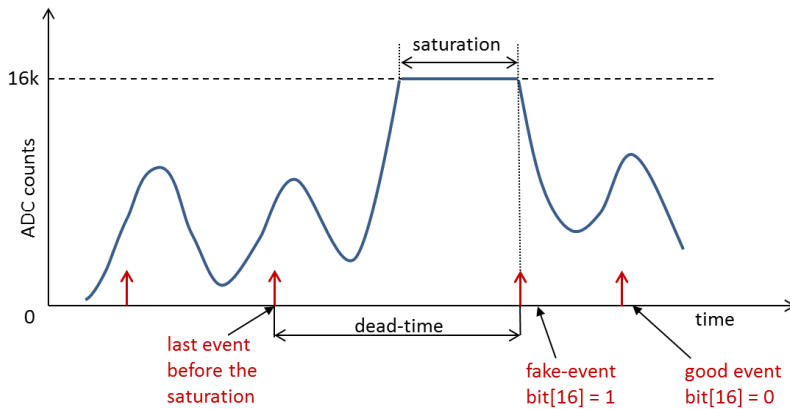


Fig. 5.2: Dead-time in case of signal saturation.

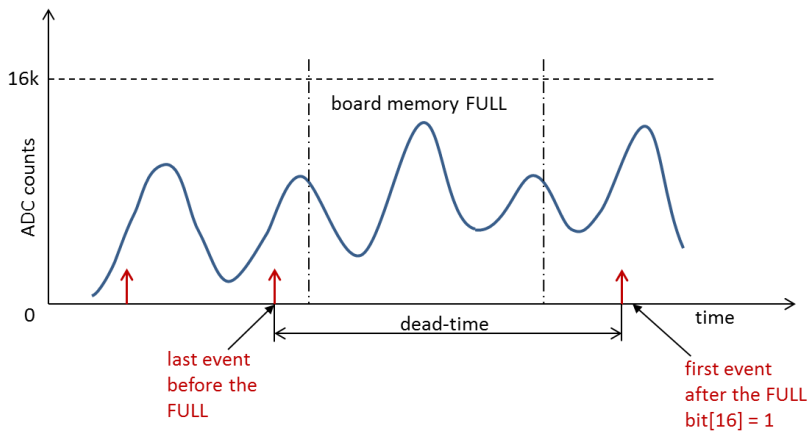


Fig. 5.3: Dead-time in case of FULL memory status.

Board Aggregate Data Format

For each readout request (occurring when at least one channel has available data to be read) the “interface FPGA (ROC)” reads one aggregate from each enabled channel memory. No more than one aggregate per channel is read each time. The set of Channel Aggregates is the Board Aggregate. If one channel has no data, that channel does not come into the Board Aggregate.

The data format when all 8 channels of a VME have available data is as shown in **Fig. 5.4**, where:

“BOARD AGGREGATE” DATA FORMAT

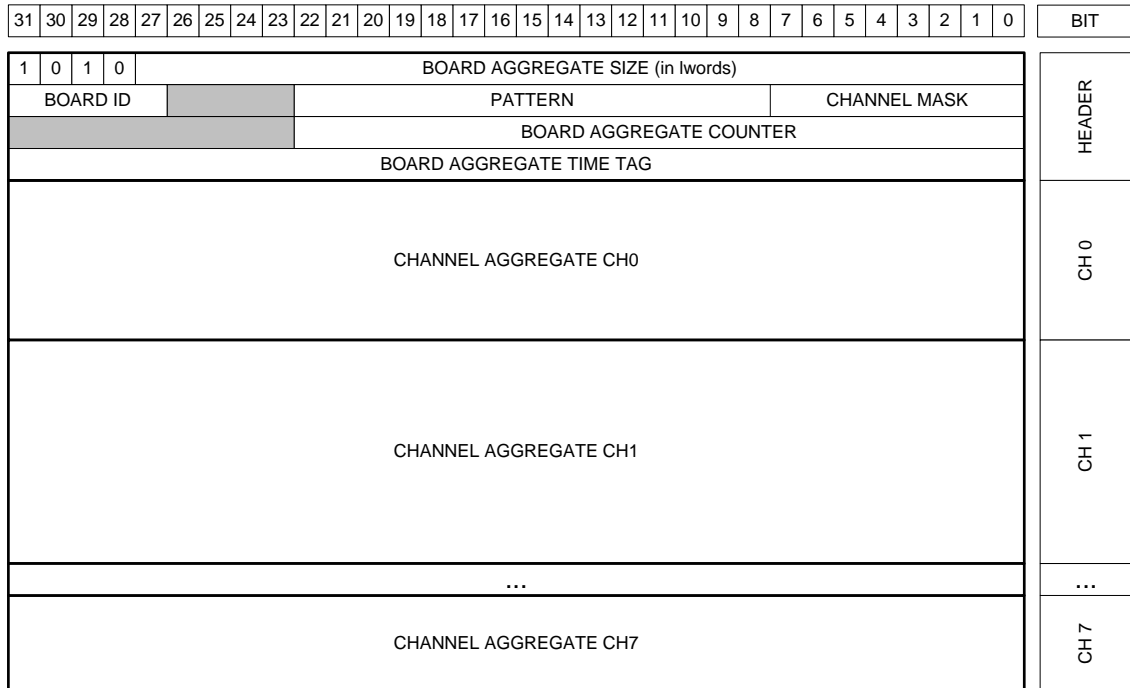


Fig. 5.4: Board Aggregate Data Format scheme

BOARD AGGREGATE SIZE: total size of the aggregate

PATTERN: is the value read from the LVDS I/O (VME only);

CHANNEL MASK: corresponds to those channels participating to the Board Aggregate;

BOARD AGGREGATE COUNTER: counts the board aggregate. It increase with the increase of board aggregates;

BOARD AGGREGATE TIME TAG: is the time of creation of the aggregate (this not corresponds to any physical quantity);

Data Block

The readout of the digitizer is done using the Block Transfer (BLT, refer to [RD4]); for each transfer, the board gives a certain number of Board Aggregates, consisting in the Data Block. The maximum number of aggregates that can be transferred in a BLT is defined by the READOUT_BTL_AGGREGATE_NUMBER. In the final readout each Board Aggregate comes successively. In case of n Board Aggregates, the Data Block is as in **Fig. 5.5**.

DATA BLOCK

BOARD AGGREGATE 0
BOARD AGGREGATE 1
...
BOARD AGGREGATE $n-1$

Fig. 5.5: Data Block scheme

6 Software Interface

Introduction

The DPP-PHA Control Software is an application that manages the communication and the acquisition in the digitizers which have the DPP-PHA firmware installed on it. The communication parameters can be properly set in order to communicate with the hardware, and the significant parameters of the algorithmic component (DPP-PHA) can be fixed for the acquisition. Waveforms and histograms can also be plotted in real time for one channel at a time (as described into the **GUI Description** paragraph).



Note: Limited to the DT5780 Digital MCA, the DPP-PHA Control Software manages also the programming of the variable input dynamics of the analog channels and features a special tab for the configuration of the HV channel settings.



Note: DPP-PHA Control Software is not provided with data analysis features and it is developed to work only with 724 Digitizer series and the DT5780.

Block Diagram

The DPP-PHA Control Software (**Fig. 6.1**) is made of different parts: there is a *GUI* whose purpose is to set all the parameters of the DPP-PHA algorithm and to manage the acquisition; the GUI directly handles the Acquisition Engine (*DPPRunner*) through run time commands and generates also a textual configuration file that contains all the selected parameters values. This file is read by *DPPRunner*, which is a C console application that programs the Digitizer according to the parameters, starts the acquisition and manages the data readout. The data, that can be waveforms, time stamps, energies or other quantities of interest, can be plotted using *gnuplot* as an external plotting tool, or saved to output files and used by third part data analysis tools spectrometry-oriented.

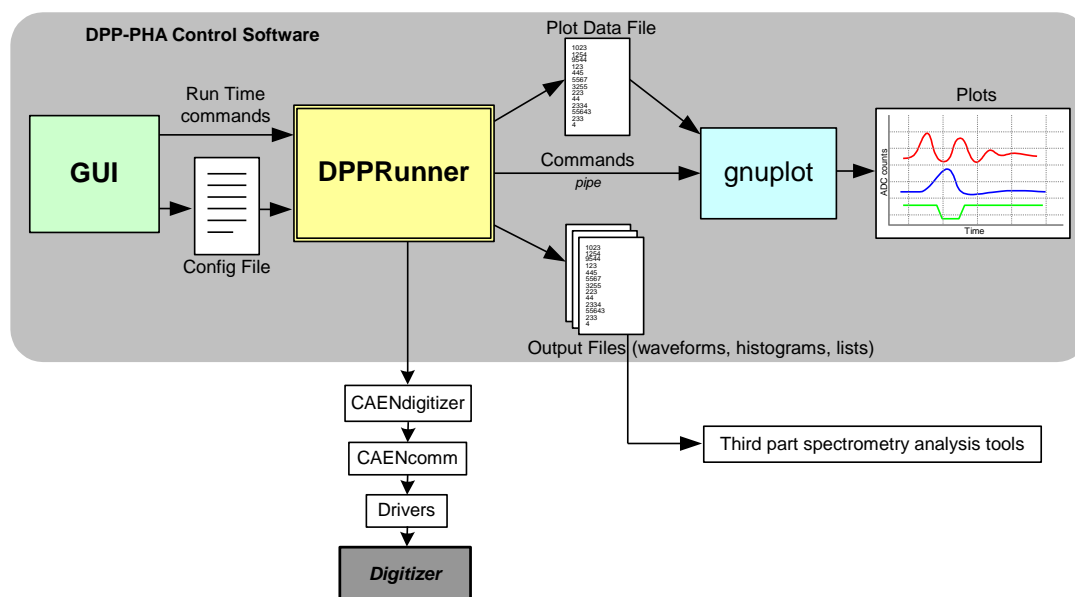


Fig. 6.1: The DPP-PHA Control Software block diagram

Libraries and Drivers

CAEN provides the drivers for all the different types of physical communication channels featured by the DPHA, and compliant with Windows and Linux OS:

- **USB 2.0.** The driver installation package is available on CAEN website in the ‘Software/Firmware’ area at the DT5724, N6724 or V1718 page.
- **CONET Optical Link**, managed by the A2818 PCI card or A3818 PCIe card. The driver installation package is available on CAEN website in the ‘Software/Firmware’ area at the A2818 or A3818 page.
- **VME bus**, accessed by the V1718 and V2718 bridge.



Note: For different Microsoft Windows versions, the USB drivers installation steps are detailed in **[RD1]**.

In addition, a set of C libraries is available:

- **CAENVMElib** is a set of ANSI C functions which permits an user program the use and the configuration of the CAEN Bridges V1718/VX1718 (VME-USB2.0 Bridge), V2718/VX2718 (VME-PCI Optical Link Bridge), A2818/A3818 (PCI CONET Controller).

The CAENVMElib installation package is available on CAEN website (www.caen.it) in the “Download” tab at:

Home / Products / Firmware/Software / Software Tools / Software Libraries / CAENVMElib Library

- **CAENComm** library manages the communication at low level (read and write access). The purpose of the CAENComm is to implement a common interface to the higher software layers, masking the details of the physical channel and its protocol, thus making the libraries and applications that rely on the CAENComm independent from the physical layer. Moreover, the CAENComm is based in turn on CAENVMElib and it requires the CAENVMElib library (access to the VME bus) even in the cases where the VME is not used. This is the reason why it is necessary that **the CAENVMElib is already installed on your PC before installing the CAENComm**.

The CAENComm installation package is available on CAEN website (www.caen.it) in the “Download” tab at:

Home / Products / Firmware/Software / Software Tools / Software Libraries / CAENComm Library

- **CAENDigitizer** is a library of functions designed specifically for the Digitizer family and it supports also the boards running the DPP firmware, as it happens in the DPHA. The CAENDigitizer library is based on the CAENComm which is based on CAENVMElib, as said above. For this reason, **the CAENVMElib and CAENComm libraries must be already installed on the host PC before installing the CAENDigitizer**.

The CAENDigitizer installation package is available on CAEN website (www.caen.it) in the “Download” tab at:

Home / Products / Firmware/Software / Software Tools / Software Libraries / CAENDigitizer Library

As far as the DPHA is concerned, the CAENComm (and so the CAENDigitizer) supports the following communication channels (see also **Fig. 6.2**):

PC → USB → Digitizer DT5724 or N6724 (Desktop and NIM models)

PC → USB → V1718 → VME → Digitizer V1724 (VME model)

PC → PCI (A2818) → CONET → Digitizer x724 (all models of the 724 series)

PC → PCI (A2818) → CONET → V2718 → VME → Digitizer V1724 (VME model)

PC → PCIe (A3818) → CONET → Digitizer x724 (all models of the 724 series)

PC → PCIe (A3818) → CONET → V2718 → VME → Digitizer V1724 (VME model)

CONET (Chainable Optical NETWORK) indicates the CAEN proprietary protocol for communication on Optical Link.

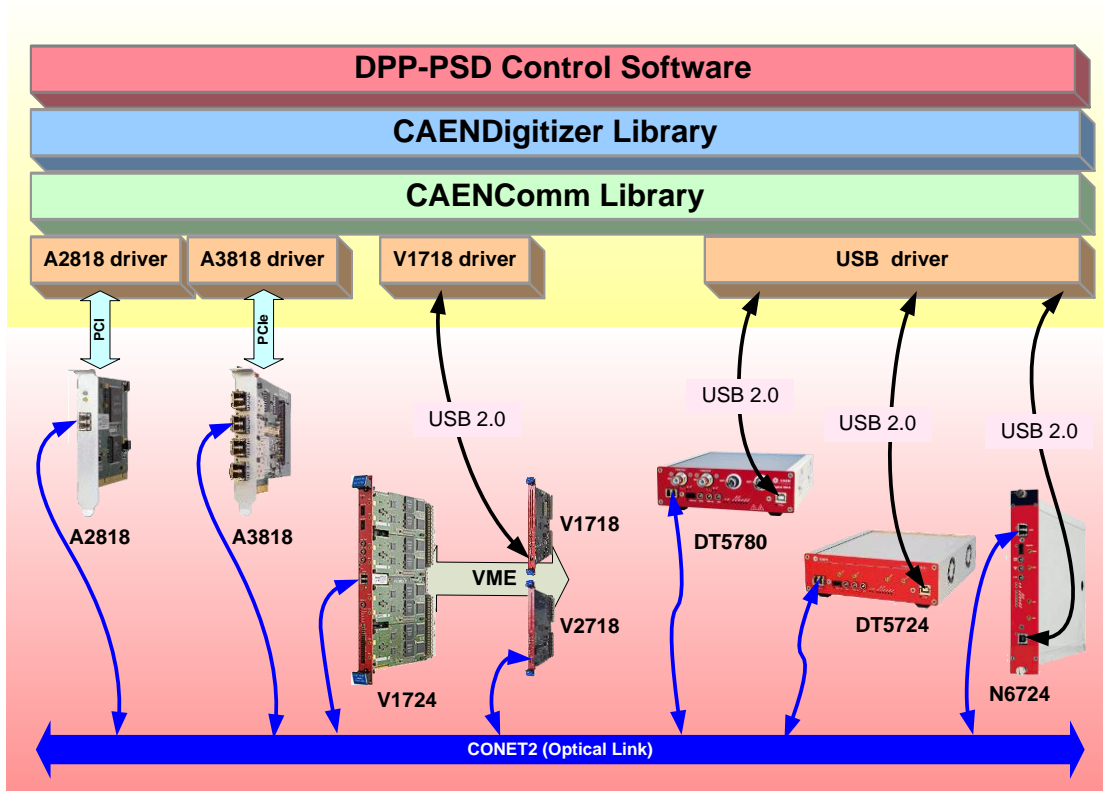


Fig. 6.2: Libraries and drivers required for the DPHA

Installation

In order to manage with DPHA system, the host station needs either Windows or Linux OS, and the third-party software **Java Runtime Environment** 6 or later (trademark of Oracle, Inc, downloadable from <http://www.java.com>). Linux users must also take care of proper installation of **gnuplot** graphical tool, as well as of **CAEN Libraries**. The latter can be downloaded from CAEN website (login required before to download).

- **Make sure** that your **hardware** (Digitizer and/or Bridge, or Controller) is **properly installed** (refer to the related User Manual for hardware installation instructions).
- **Make sure** you **have installed** the driver for your OS and the physical communication layer to be used. Driver installation packages are downloadable from CAEN website (**login required before to download**) as reported in the **Libraries and Drivers** paragraph (refer to the related User Manual for driver installation instructions).



Note: Hardware and USB drivers installation instructions for desktop digitizers and DT5780 are detailed in [RD1].

CAEN provides the full installation package for the **DPP-PHA Control Software** in a **standalone version** for **Windows OS**. This version installs all the binary files required to directly use the software. The installation package for **Linux OS** needs the presence of a set of required libraries to be installed apart.

- **Download the DPP-PHA Control Software installation package** compliant with your OS on CAEN website from the 'Download' area at the DPP-PHA Control Software page (**login required before to download**).
- **Extract files** to your host.

For Linux users:

- **Click on the red link** above the DPP-PHA Control Software package in order to download the required CAEN Libraries.
- **Install the libraries** in the following order:
 1. CAENVMLib
 2. CAENComm
 3. CAENDigitizer

The **installation instructions** can be found in the **README file** inside each library folder.

- **Install the DPP-PHA Control Software** according to the **installation instructions** of the **README file** inside the program folder.

For Windows users

- **Launch the DPP-PHA Control Software installer** and complete the Installation Wizard
- **Run the DPP-PHA Control Software GUI** by one of the following options:
 1. The **Desktop icon** for the program
 2. The **Quick Launch** icon for the program
 3. The **.bat file** in the main folder from the installation path on your host.

GUI Description

The Graphical User Interface (GUI) is composed of tabs, each one divided in one or more sections. In the different tabs there are all the commands needed to manage the connections, set the board and channel parameters and control the acquisition. An additional tab for HV management is featured by the GUI when interfacing to a DT5780 Digital MCA.




Here follows a table with the main parameters and their symbols (**Tab. 6.1**) used in the chapter, then a detailed explanation of the different tabs.

GUI Parameter	Symbol
Decimation	D
Decay Time	M
Rise Time	k
Flat Top	m
Baseline Mean	nsbl
Threshold	thr
Smoothing Factor	a
Delay	b
Peak Mean	nspk
Peak Holdoff	pkhoe
Baseline Holdoff	blhoe
Holdoff	trgho

Tab. 6.1: Table of relevant parameters and their symbols




A **Common Bar** lays at the bottom of the GUI (**Fig. 6.3**) and keeps visible from any tab active. The bar contains:

- **“Acquisition” button:** starts and stops the acquisition session.
- **“Acquisition Mode” menu:** sets the *“Oscilloscope”* or the *“Histogram”* acquisition mode.
- **“Transfer Rate” window:** displays the data transfer rate during the acquisition.
- **“Elapsing Time” window:** displays the time elapsing while an acquisition is on. Active in Histogram Mode. The acquisition will automatically stop if a *“non zero”* value is set for the Stop Time parameter.
- **“Connection” icon:** updates itself according to the connection status.

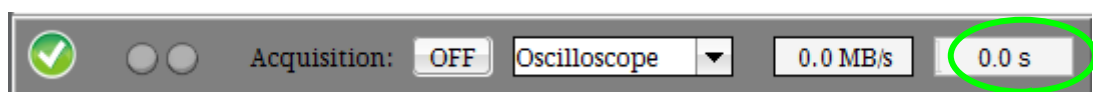
Icon	Status
	Disconnected
	Connection OK
	Connection Error

Tab. 6.2: Table of the Connection icon values

- **“HV Status LEDs” icons (AVAILABLE ONLY FOR DT7580):** visible only after the connection has been established, update themselves according to the related HV channel status.

Icon	Status
	Channel OFF
	POSITIVE channel ON
	NEGATIVE channel ON

Tab. 6.3: Table of the HV LEDs status values



Elapsing Time window

Fig. 6.3: Common Bar

The Tab “General”

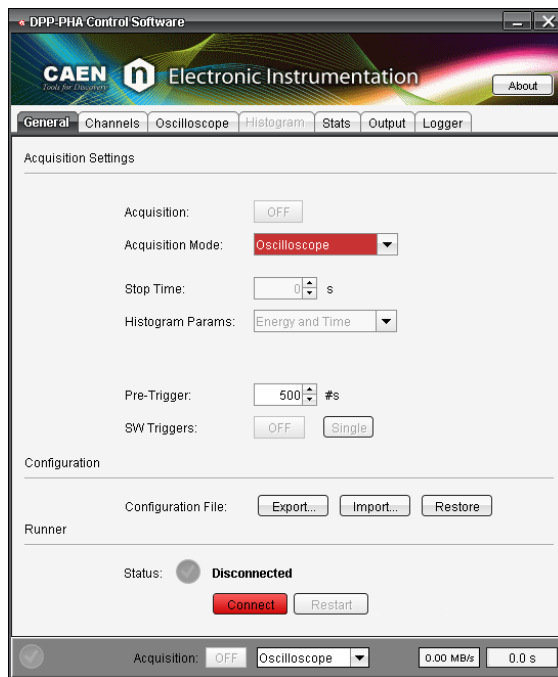


Fig. 6.4: Tab “General”

The **General Tab** is divided in three sections: **Acquisition Settings**, **Configuration**, **Runner**.

The **Acquisition Settings** section includes:

- **“Acquisition” button:** starts and stops the acquisition. It is duplicated in the Common Bar.
- **“Acquisition Mode” menu:** selects between the *“Oscilloscope”* mode, in which the raw waveform can be visualized and saved, or the *“Histogram”* mode, in which the spectra can be visualized and saved. This command is duplicated in the Common Bar.
- **“Stop Time” box:** sets the value (in seconds) for the acquisition Real Time in Histogram mode. At the end of the fixed time (visualized in the elapsing time window of the Common Bar) the acquisition will be automatically stopped. Set Stop Time to “0” for an indefinite acquisition time.
- **“Histogram Params” box:** selects the kind of data to be provided by the Digitizer in *“Histogram”* mode (Energy only or Energy and Time).
- **“Pre-Trigger” box:** selects the number of samples which the pre-trigger region will be composed of (available only in Oscilloscope mode). The allowed range is 0 up to 500 samples (i.e. 0 – 5 us)
- **“SW Triggers” buttons:** start and stop sending a software trigger from the computer to the board in a continuous or single-shot way.

The **Configuration** section includes:

- **“Configuration File” buttons:** store (*“Export”*) and recall (*“Import”*) the configuration of the software and the parameters for the acquisition. The user can so easily manage the different parameters during different acquisitions. *“Restore”* resets the parameters to their default values.

The **Runner** section shows the status of the connection between the board and the Control Software. It is made of:

- **“Connect” button:** opens the Connection window (Fig. 6.5).

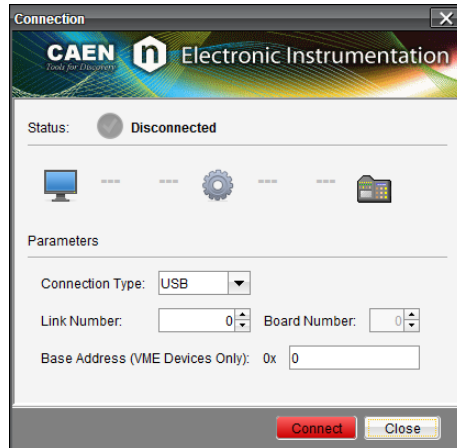


Fig. 6.5: Connection Window

In this window the connection parameters can be set (see [RD4] for detailed description):

- **“Connection Type” menu:** selects between “USB” or “PCI” according to the way the board is connected to the PC.
- **“Link Number” box:** sets the number of the port used in the connection and is valid for multiple boards connection.
- **“Board Number” box:** indicates the number of the desired board in a Daisy chain connection between different boards.
- **“Base Address” box** contains the VME base address in case of VME board use. Set “0” for direct connection.

In Tab. 6.4 some connection cases and the relative parameters setting are shown as useful examples.

Connection chain	Type	Link	Slave	Address
PC → USB → DT5724	USB	0	0	0
PC → USB → V1718 → VME → V1724	USB	0	0	32100000*
PC → PCI → A2818 → CONET → N6724	PCI	0	0	0
PC → PCI → A2818 → CONET → V1724	PCI	0	0	32100000*
PC → PCI → A2818 → CONET → V1724**	PCI	0	1	0
PC → USB → DT5724***	USB	1	0	0

Tab. 6.4: Examples of connection settings

* For the correct VME base address to be used, please refer to the Digitizer’s User Manual.

** The VME Digitizer is intended to be part of a Daisy chain (see the examples at the end of [RD2])

*** It is supposed that at least two USB ports are used by the PC to communicate with as many digitizers (see the examples at the end of [RD4]).

The connection is handled by:

- **“Connect” button:** establishes the connection. A green sign will confirm the correct connection.
- **“Close/Done” button:** closes the connection window.

When a connection is established, in the Runner section the **“Status”** field shows the *“Connected”* value.

- **“Restart” button:** restarts the software causing the board to reset and to reprogram with the actual parameters; the communication is unaffected. In case of DT5780, the Restart function has no effect on the HV channels.

1. The Tab “Channels”

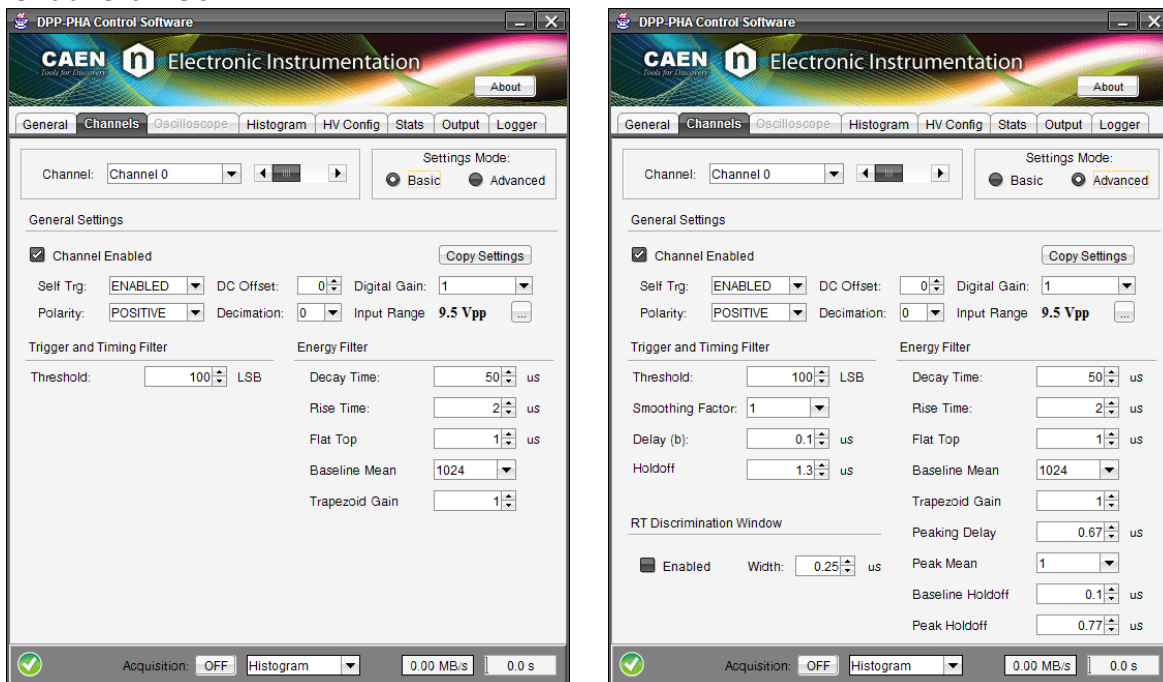


Fig. 6.6: Tab “Channels” in the Basic and Advanced configuration options

The **Channels Tab** is the core of the DPP-PHA Control Software, as in this tab it is possible to set all the parameters requested by the algorithm.

The tab sections are: **Channel**, **Setting Mode**, **General Settings**, **Trigger and Timing Filter**, **Energy Filter**, **RT Discrimination Window**. Trigger and Timing Filter, as well as Energy Filter, are different basing on the option enabled into the Setting Mode section; RT Discrimination Window is visible only in the Advanced configuration (see **Fig. 6.6**).

The **Channel** section includes:

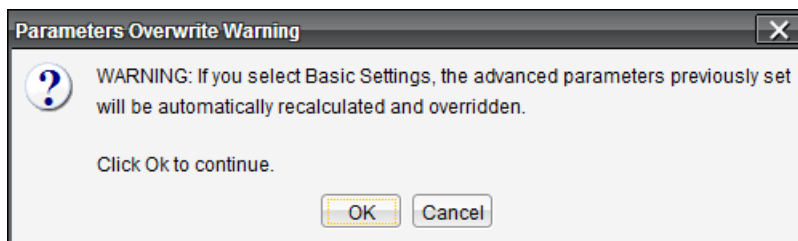
- **“Channel” menu:** selects the channel to which the parameters are referred. The channels are selectable either through the drop-down menu and the slider. Note that more than a channel can be selected: once all the parameter have been set for the current channel, a new parameters configuration tab will be available by selecting another channel.

The **Setting Mode** section enables two tab visualization options corresponding to two configuration options:

- **“Basic” option:** enables the basic configuration tab for the algorithm control.
- **“Advanced” option:** enables the advanced configuration tab where additional parameters for the fine tuning are disclosed.



Note: During the Basic operation some of the hidden parameters of the Advanced option (being linked to the basic parameters) are changed automatically by the software according to the basic parameters.



The **General Settings** section, common for Basic and Advanced mode, shows the following commands related to the channel selected in the Channel section:

- **“Channel Enabled” checkbox:** enables the selected channel to acquire data.
- **“DC Offset” box:** sets the value of the DC Offset applied to the channel, expressed as the percentage of the Full Scale Range. Allowed values are: -50% (Full negative) ÷ 50% (Full Positive).
- **“Pulse Polarity” menu:** selects the polarity of the input signal to be processed by the DPP-PHA algorithm. Since DPHA works only with positive input pulses, setting “NEGATIVE” will invert the input polarity.
- **“Input Digital Gain” menu:** multiplies the value of the samples coming out from the ADC channel by a constant value. If used in combination with the Decimation parameter, the Input Digital Gain provides a resolution improvement. The allowed values for the Input digital Gain parameter are: 1,2,4,8.
- **“Decimation” menu:** selects the value of parameter D (see **Tab. 6.1**) to be used, i.e. the number of samples to be averaged before the sampled signal is analysed by the algorithm. An important effect of Decimation is to extend the range of allowed values for the time parameters (ex. the trapezoid rise time). The allowed values are: 0, 2, 4, 8.
- **“Copy Settings” button:** copies the settings of the selected channel to other channels.
- **“Input Range Selection” menu (AVAILABLE ONLY FOR DT7580):** through the “...” button, it is possible to set the value of the input dynamics (Vpp) in the appearing Input Range Selection window.

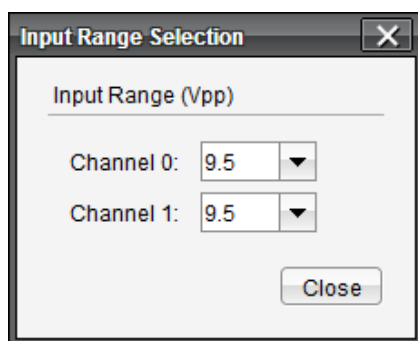


Fig. 6.7: Input Range Selection menu

The allowed values are:

“9.5”

“3.7”

“1.4”

“0.6”

In the **Trigger and Timing Filter** section the following parameters can be set:

- **“Threshold” box (basic):** sets the parameter thr which is the threshold for the board self-triggering. When the $RC-CR^2$ signal crosses the threshold the channel gets ready to fire the trigger. The trigger is issued as soon as the $RC-CR^2$ signal crosses the zero. Its value is expressed in LSB. The conversion between mV and LSB can be calculated according to the board input range (0.5, 2.25, 10V). For a board with 14-bit resolution and input range of 2.25 Volts, the LSB is:
$$LSB = 2.25 / 2^{14} = 0.137 \text{ mV}$$
- **“Smoothing Factor” menu (advanced):** sets the number of samples (parameter a of **Tab. 6.1**) to be used in the moving window of the low pass filter of the integrative component (RC) contained in the trigger-and-timing filter. This parameter helps in reducing the high frequency noise. Allowed values for the parameter a are 1, 2, 4, 8, 16 and 32.
- **“Delay” box (advanced):** sets the parameter b (**Tab. 6.1**) used in the derivative component of the trigger-and-timing filter (CR^2) in order to maximize its amplitude with respect to the input signal. The best way to find the optimum setting is to start from a value equal to the rise time of the input signal and then, looking at the $RC-CR^2$ signal on the plot, increase b until the signal reaches the maximum amplitude.
- **“Holdoff” box (advanced):** sets the minimum time interval that must exist between two consecutive triggers. Triggers that occur within the holdoff window ($trgho$) are rejected. The value of the $trgho$ parameter is expressed in μs . Maximum value is 5.040 μs .

In the **Energy Filter** section the parameters for the Trapezoidal Filter can be set:

- **“Decay Time” box (basic):** sets the exponential decay time constant M of the input pulses (**Tab. 6.1**). Setting M parameter is like to calibrate the pole-zero cancellation in a traditional Shaping Amplifier. The value of M is expressed in μs .

Fig. 6.8 (trace1 in green is the input and trace2 in red is the trapezoid) shows two cases of bad cancellation; on the left, the value of M is too high and gives overcompensation; on the right it is too low and gives under compensation. It is very important to set the right value for M otherwise the top of the trapezoid is not flat and the peak calculation becomes very inaccurate.

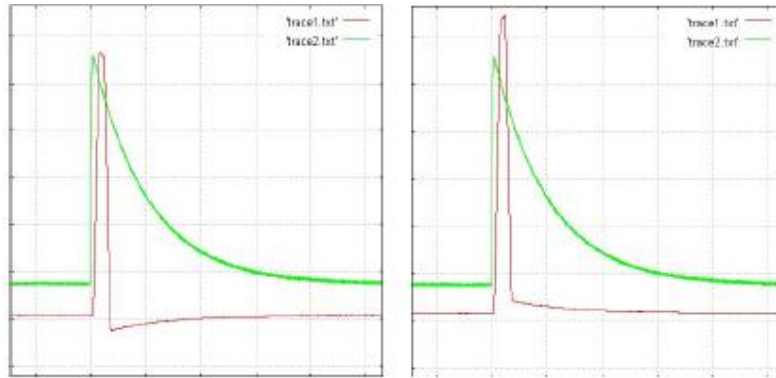


Fig. 6.8: Bad Decay Time setting effects on the Trapezoid signal

- **“Rise Time” box (basic):** sets the rise and the fall time of the trapezoid (k of **Tab. 6.1**), expressed in μs . Setting this parameter is like to change the shaping time constant of the traditional Shaping Amplifier. Higher values of k give a better signal to noise ratio, but increase the probability of pile-up. The user should find the best compromise between the overall resolution of the energy calculation and the dead time (ratio between the number of pulses converted and the total number of input pulses).
- **“Flat Top” box (basic):** sets the parameter m , i.e. the width of the trapezoid flat top, expressed in μs . As the rise time k , m has an influence on the signal to noise ratio and on the efficiency. Moreover, its value should be set long enough in order to reduce ballistic deficits.
- **“Baseline Mean” menu (basic):** sets the $nsbl$ parameter (see **Tab. 6.1**) which is the number of samples in the moving average filter window to calculate the baseline. The output signal of the trapezoidal filter has a baseline depending on the DC offset and on the trapezoid parameters. This baseline is also affected by low frequency fluctuation usually due to the ground loops (50 or 60 Hz noise), temperature variation and other slow components such as the microphone noise. In order to obtain a reliable baseline value as reference for the trapezoid peak calculation, a moving average filter is applied to the baseline signal. The $nsbl$ allowed values are 0, 16, 64, 256, 1024, 4096, 16384.
- **“Trapezoidal Gain” box (basic):** sets the parameter Dg , i.e. the *digital gain* of the trapezoid signal. The trapezoid is the output of a filter that contains accumulators, and, for this reason, the output signal is represented over a number of bits greater than the input.

In particular, the input is a 14 bit ADC sample and the output (trapezoid) is a 48 bits signed number whose amplitude with respect to the input is amplified by a *gain factor* $G = k * M$, where k and M are the rise and decay time, as defined above.

Unfortunately, it is very difficult to make a division inside an FPGA unless the divisor is a power of 2 (in this case it is just a right shift). In order to bring the representation of the trapezoid signal (and the peak) on a reasonable number of bit, the FPGA divides the output to the closest power of two smaller than G (called G_{pow2}), and keeps the 15 lower significant bits. The number that comes out is amplified with respect to the input by a factor $G_f = G / G_{pow2}$, where $1 \leq G_f < 2$.

Note that the energy histogram is first calculated using the 15 bit peak values (32768 channels); since the x-axis scale of the energy histogram depends on G_f , i.e. on the parameters k and M , a re-binning is made to recalculate the bin heights for a 16384 channel histogram (14 bit) applying the scaling factor G_f and restoring the correct scale for the pulse amplitude expressed in ADC counts.

In this way the digital gain is simply a way to artificially amplify the trapezoidal signal, as we just make:

$$G = k * M / Dg$$

The default value for the digital gain is “1”.

- **“Peaking Delay” box (advanced):** defines the point on the flat top (referred to the starting of the flat top) where to make the peak calculation and it is expressed in μs . Due to the ballistic deficit typical of particle detectors, the trapezoid flat top doesn’t start exactly after its Rise Time, according to the theory, but shows a round shaped knee. Therefore, it is necessary to delay the peaking window and bring it into the flat part of the top.
- **“Peak Mean” menu (advanced):** sets the parameter N_{spk} (Tab. 6.1) which is the number of samples to be averaged for the calculation of the trapezoidal height. Allowed values are 1, 4, 16, 64.
- **“Baseline Holdoff” box (advanced):** sets the baseline holdoff extension parameter ($blhoe$). The baseline calculation is inhibited from the start to the end of the trapezoid. The user can add a fixed amount of time after the end of the trapezoid to further inhibit the baseline calculation. The value is expressed in μs and the maximum value is 2.550 μs .
- **“Peak Holdoff” box (advanced):** sets the peak holdoff extension parameter ($pkhoe$), i.e. the time interval between two trapezoids for a correct peak measurement. Theoretically the minimum distance in time is Rise Time + Flat Top (with $pkhoe = 0$), but the user can modify this parameter according to his/her needs. Two consecutive peaks within this time interval will cause the second to be rejected. Maximum value for $pkhoe$ is 20.40 μs .

The **RT Discrimination Windows** section manages the rise time discriminator which implements an enhanced Pile-Up Rejection technique (see also section **Normal (Individual) Trigger Mode**) through two relevant features:

- **“Enabled” checkbox (advanced):** enables/disables the Rise Time Discriminator function.
- **“Width” box (advanced):** sets a fixed time window (expressed in μs) for the RT Discrimination. The algorithm fires a valid trigger when the time interval between the $RC-CR^2$ threshold and zero crossing is less than the “Width” value. In case of pile-up the zero crossing is shifted to higher values, so that if no zero crossing would happen inside the “Width” window, a second trigger is issued at the end of the “Width” window. The fine tuning of this parameter allows the user to reject the pulses which overlap on the rise time. Maximum value allowed is 1.023 μs .

2. The Tab “Oscilloscope”

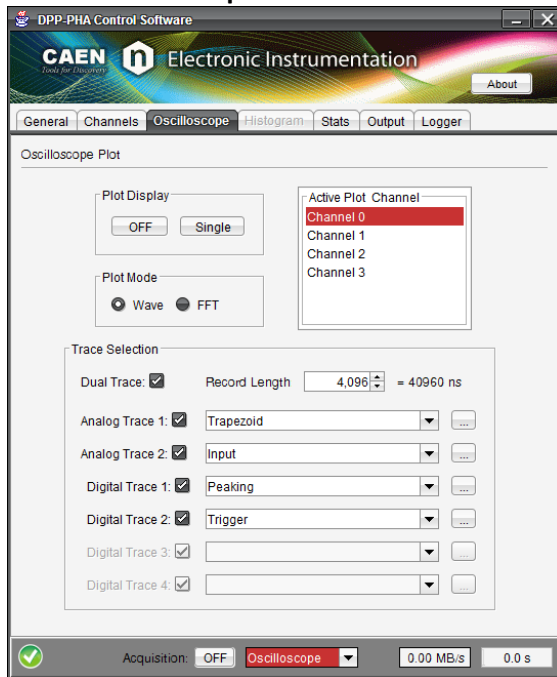


Fig. 6.9: Tab “Oscilloscope”

The **Oscilloscope Tab** consists only of the **Oscilloscope Plot** section in which all the parameters for the signals visualization are set. A maximum of four (4) traces can be simultaneously displayed.

The **Oscilloscope Plot** section includes:

- **“Plot Display” buttons:** enable/disable the plot visualization and let the user to visualize the waveform continuously (“ON/OFF”) or by single shots (“Single”).
- **“Active Plot Channel” menu:** selects the channel whose signals are visualized. Only one channel a time can be plotted. The selected channel has to be checked in the Tab Channels
- **“Trace Selection” menu** with the following functions:
 - **“Plot Mode” checkcells:** select to visualize the Waveform (“Wave”) or the Fast Fourier Transform (“FFT”). The FFT option can be used only with the signals in Analog Trace 1.
 - **“Dual Trace” checkbox:** enables/disables two analog traces (the ones selectable in the Trace 1 and Trace 2 dropdown menu) to be visualized in the same plot. Useful in the setting of the parameters, in this modality the two traces are visualized each with halved number of samples.
 - **“Analog Trace 1” menu:** selects the first analog trace to be visualized in the plot:
 - “Input”: the input signal from pre-amplified detectors
 - “RC-CR”: first step of the trigger and timing filter (see section **CAEN Digital Approach**)
 - “RC-CR2”: second step of the trigger and timing filter (see section **CAEN Digital Approach**)
 - “Trapezoid”: trapezoid resulting from the energy filter (see section **CAEN Digital Approach**)
 - **“Analog Trace 2” menu:** selects the second analog trace to be visualized in the plot:
 - “Input”: the input signal from pre-amplified detectors
 - “Threshold”: the RC-CR2 threshold value (see section **The Tab “Channels”**)
 - “Trapezoid-BL”: displays the trapezoid shape minus the baseline. When the baseline calculation is correctly made, the trapezoid base is at zero
 - “Baseline”: displays the input baseline

Trace 2 is not active if Dual Trace is unchecked.

- **“Digital Trace 1” menu:** selects the first digital trace to visualize:
 - “TRG Window”: shows the RT Discrimination Width
 - “Armed”: digital input showing where the RC-CR2 crosses the Threshold
 - “Peak Run”: starts with the trigger and last for the whole event (see **Fig. 4.3**)
 - “Peak Abort”: shows when there is a pile-up event and corresponds to the time interval when the energy calculation is disabled due to the pile-up event
 - “Peaking”: shows where the energy is calculated
 - “Trg Validation Win”: digital input showing the trigger validation acceptance window TVAW (refer to **Acquisition Modes** chapter and **[RD5]**)
 - “BSL Holdoff”: shows the baseline holdoff parameter (see section **The Tab “Channels”**)
 - “TRG Holdoff”: shows the trigger holdoff parameter (see section **The Tab “Channels”**)
 - “Trg Validation”: shows the trigger validation signal TRG_VAL (refer to **Acquisition Modes** chapter and **[RD5]**)
 - “Acq Veto”: this is 1 when either the input signal is saturated or the memory board is full.
- **“Digital Trace 2” menu:** selects the second digital trace to be visualized:
 - “Trigger”: shows where the trigger is fired
- **“Digital Trace3” menu:** *not available for DPP-PHA.*
- **“Digital Trace 4” menu:** *not available for DPP-PHA.*
- **“...” button:** opens the Trace Setting window (**Fig. 6.10**) where to set the DC offset and the gain of the signal.

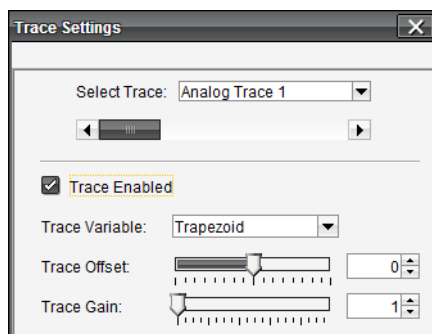


Fig. 6.10: The Trace Settings window

- **“Record Length” box:** selects the length of the acquisition window expressed in number of steps (1 step = 10ns × Decimation).

3. The Tab “Histogram”

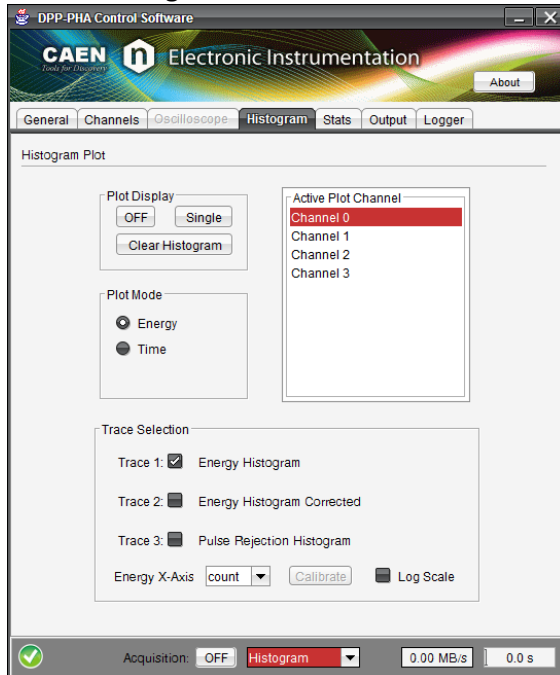


Fig. 6.11: Tab “Histogram”

The **Histogram Tab** contains in the **Histogram Plot** section all the functions for the plotting of an Energy or Time Histogram.

The **Histogram Plot** section includes the following settings:

- **“Plot Display” buttons:** The “ON/OFF” button enables/disables the continuous plotting of the histogram. In the OFF position is possible to update manually the plot by pushing the “Single” button. The “Clear Histogram” button clears the histogram (i.e. resets the plotting to zero).
- **“Active Plot Channel” menu:** selects the channel whose signals are visualized. Only one channel at a time can be plotted. The selected channel has to be checked in the Tab Channels.
- **“Trace Selection” menu** including:
 - **“Plot Mode” checkcells:** selects if a “Energy” or “Time” Histogram is visualized.
 - **“Trace 1” menu:** enables/disables the visualization of the Energy/Time Histogram. As Time Histogram is to be intended the histogram of the time intervals between subsequent triggers.
 - **“Trace 2” menu:** enables/disables the visualization of the Energy Histogram Corrected. It is the energy histogram corrected by applying the live correction method.
 - **“Trace 3” menu:** enables/disables the visualization of the Rejected Pulses Histogram. It is the redistribution of the lost counts (due to the pileup), within fixed acquisition time windows, with respect to the energy distribution in the same windows. It takes part in the live correction method.
 - **“Energy X-Axis” menu:** selects the unit of measurement of the Energy x-axis in the histogram between “ADC Counts” and “keV”. In order to define a keV scale, the “Calibrate” button opens the Energy Calibration window (**Fig. 6.12**) where it is possible to calibrate the spectrum by a dedicated menu: a customized Calibration line can be built here. Different calibration lines are available for the different channels.

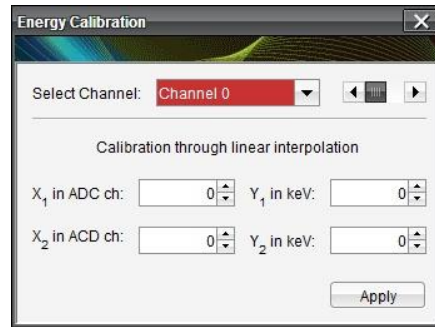


Fig. 6.12: Energy Calibration window

- **“Log Scale” checkbox:** enables/disables the logarithmic scale for the plotted histogram.

4. The Tab “Stats”

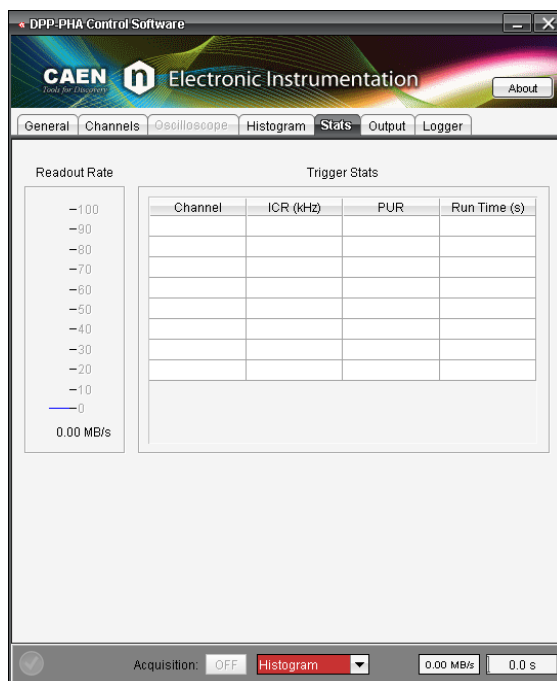


Fig. 6.13: Tab “Stats”

In the **Stats Tab** are resumed some of the most important statistics and values of every acquired channel. Two sections compose the tab: **Readout Rate** and **Trigger Stats**

The **Readout Rate** section hosts:

- **“Readout Rate” display:** shows the data throughput from the board to the computer in MB/s (the same value is visible in the Common Bar).

The **Trigger Stats** section is made by:

- **“Trigger Stats” table:** reports in real time the Incoming Counting Rate (“ICR” expressed in kHz), the Pile Up Rejection (“PUR” expressed in percentage), the Run Time (in seconds) and the related channel (“Channel”).

6. The Tab “Output”

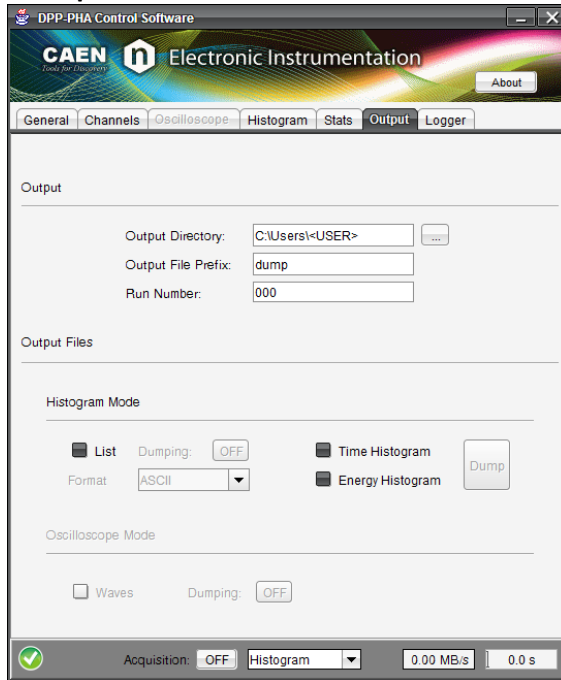


Fig. 6.14: Tab “Output”

In the **Output tab** there are all the commands to save output files containing spectra, waveforms and lists on a disk drive.

Note: From the input pulse energy (i.e. the height) E_{in} , that is represented as a 14-bit value, the digitizer provides out the trapezoid height E_{out} , that is a 15-bit integer, according to the following formula:

$$E_{out} = G_f * E_{in}$$

where G_f ($1 \leq G_f < 2$) is a residual gain factor due to internal mathematical approximation; G_f depends on the rise time of the trapezoid (parameter k) and the decay time of the input pulse (parameter M):

$$G_f = G_f(k, M)$$

The DPP-PHA Control Software first uses the 15-bit E_{out} data to calculate internally the energy histogram (32768 channels). As the X-axis scale of such a histogram depends on G_f (so on k and M), in order to keep the scale constant when these parameters change, the software applies a rebinning function that recalculates the bin width for a 16384-channel histogram (14 bit) by applying the scaling factor G_f and restoring the correct scale for the pulse amplitude expressed in ADC counts. This rebinned histogram over 16384 channels is the Energy Histogram plotted by the Control Software and saved into the "Energy Histogram" output file.

The sections in this tab are **Output** and **Output Files**.

The **Output** section includes the following settings:

- **“Output Directory” menu:** selects the destination directory of the saved files by writing or browsing in the relative box (a default destination path is set, according to the Operating System version, if not action is performed by the user).
- **“Output File Prefix” box:** contains the prefix for the output file name written by the user (a default prefix is set if no action is performed by the user).
- **“Run Number” box:** contains a numeric identifier of the actual run acquisition section. It is incremented every time a new acquisition is started by the Acquisition button.

The complete file name will be *Prefix_ABC_XY_N.dat* where:

ABC is the run number; *XY* is “eh” in case of Energy Histogram, “th” in case of Time Histogram, “ls” in case of List and wf in case of Waveform; *N* is the channel number.

Data saving is activated by selecting the options in the **Output Files** section:

- **“Energy Histogram” checkbox (active only in Histogram Mode):** saves the Energy Histogram data (ASCII format) in a n-column file, where the first column is made by the bin numbers (ADC counts) and every other column (as many as the energy traces selected in the Histogram Plot section of the Histogram Tab) consists of the energy histogram values. This is the histogram of energy Eout rebinned over 14 bit (16384 channels). Data saving is enabled by the **DUMP** button.
- **“Time Histogram” checkbox (active only in Histogram Mode):** saves the Time Histogram data (ASCII format) in a 2-column file (bin numbers on the first and histogram values on the second). The bins represent the time interval ΔT (in units of clock period = 10 ns) between two consecutive time stamps. Data saving is enabled by the **DUMP** button.
- **“List” checkbox (active only in Histogram Mode):** saves the whole event data (which are raw, non-histogram data) in a ASCII or BINARY format, according to the list Format menu

ASCII list format: is a 2-column file, where the first column consists in the time stamps in units of clock period and the second column is made by the energy values as 15-bit integer (i.e Eout).

BINARY list format: the file contains the sequence of the recorded events in the format as below:

EVENT = |Event|Event|Event|.....|Event|;

Event = (unsigned 64 bit int)TimeTag|(unsigned 16 bit)Energy.

Data saving starts/stops by the **DUMPING “ON/OFF”** button



Note: Users who intend to use the list output data for the energy histogram calculation over 32768 channels must take into account that they need to rebin the histogram every time they change k and/or M parameters.

- **“Waves” checkbox (active only in Oscilloscope Mode):** saves the samples of the digitised waveforms (ASCII format). Data saving starts/stops by the **DUMPING “ON/OFF”** button.

7. The Tab “Logger”

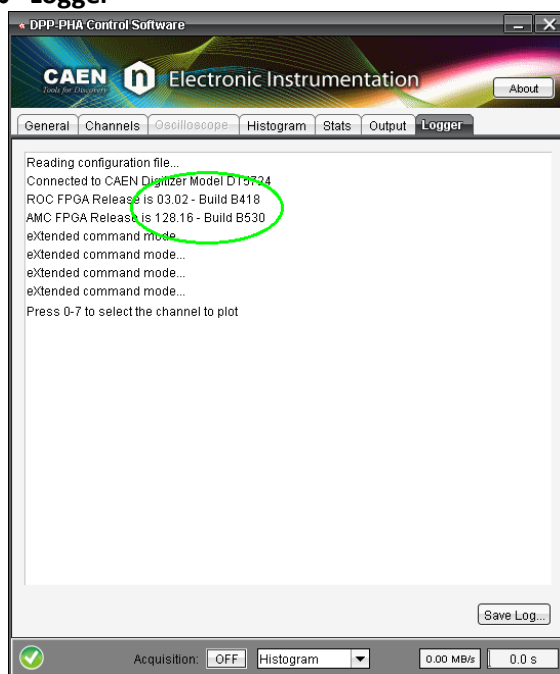


Fig. 6.15: Tab “Logger”

In the **Logger Tab** the user can read board and firmware information (Fig. 6.15) and have a direct view of the parameters values and the mode options being set during the current program session. The session log can be saved on disk by using the “Save Log” button.

8. The Tab “HV Config”

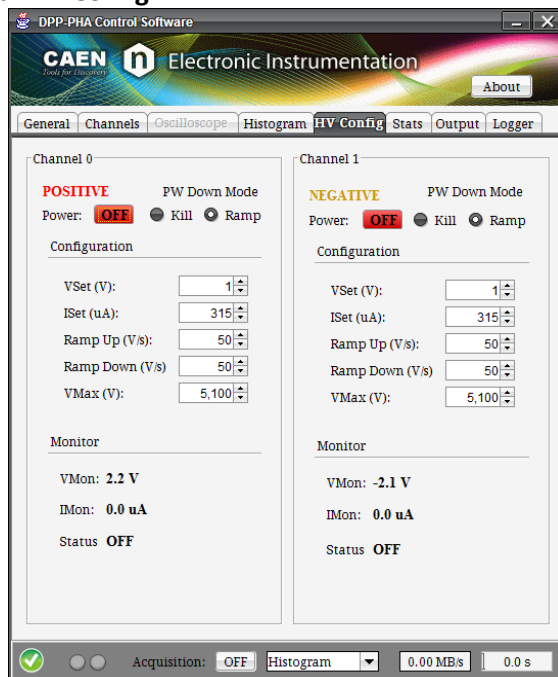


Fig. 6.16: Tab “HV Config”

Available only for DT5780 Digital MCA, the **HV Config** tab controls the settings of the two HV channels in the sections **Channel 0** and **Channel 1** by means of:

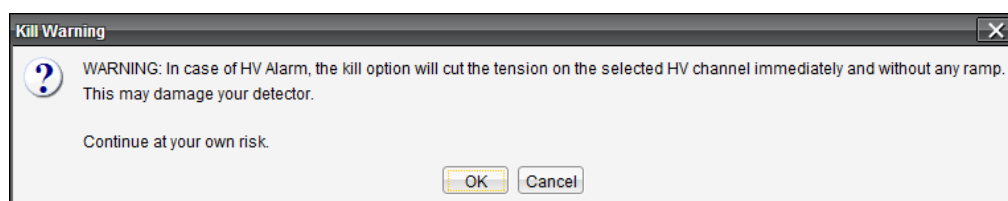
- **“Power” button:** enables/disables the HV channel power supply according to the Configuration settings.
- **“PW Down Mode” checkcells:** selects the power down mode of the HV channel in case of an overcurrent or an inhibit event occurs. The selectable options are:

“Kill”, that performs an immediate shutdown;

“Ramp”, that performs a stepwise shutdown.



WARNING: Use with caution the **Kill** setting, because the abrupt stop of the HV channels may cause damage to the attached detector.



The **Configuration** section contains:

- **“VSet (V)” box:** sets the value of the channel bias voltage in Volt [range 0:5100 in steps of 0.1 V].
- **“ISet (uA)” box:** sets the value of the channel bias current in micro Ampere [range 0:315 in steps of 0.01 V].
- **“Ramp UP (V/s)” box:** sets the step width of the bias voltage ramp up in Volt per second [range 0:500 in steps of 1 V/s].
- **“Ramp Down (V/s)” box:** sets the step width of the bias voltage ramp down in Volt per second [range 0:500 in steps of 1 V/s].
- **VMax (V)” box:** sets the maximum value of the channel bias voltage [range 0: 5100 in steps of 10 V].

In the **Monitor** section, the following parameters are monitored in real time:

- **“VMon”**: monitors the actual value of the channel bias voltage.
- **“IMon”**: monitors the actual value of the channel bias current.
- **“Status”**: monitors the channel status. Possible options are:
 - **“OFF”**: the HV channel is powered off.
 - **“ON”**: the HV channel is powered on.
 - **“Disabled”**: the HV channel is in inhibit.
 - **“Ramp Up”**: the bias voltage of the HV channel is ramping up.
 - **“Ramp Down”**: the bias voltage of the HV channel is ramping down.
 - **“Over Voltage”**: the monitored bias voltage of the HV channel is over the VSet value.
 - **“Under Voltage”**: the monitored bias voltage of the HV channel is under the VSet value.
 - **“Over Current”**: the monitored bias current of the HV channel is over the ISet value.
 - **“MaxV Protection”**: the monitored bias voltage of the HV channel is over the VMax value.
 - **“MaxI Protection”**: the monitored bias current of the HV channel is over the maximum value allowed.
 - **“Over Temperature”**: the temperature of the HV channel is over the safety limit.
 - **“Temperature Warning”**: the temperature of the HV channel is close to the overtemperature condition.

Config File Syntax

The Graphical User Interface (GUI) interacts with the board through a Configuration File which is modified by the GUI itself. Moreover, in the configuration file there are some advanced controls that are not present in the GUI. Acting in the different sections of the Configuration File makes possible to enable/disable/modify these advanced features. In this section there is a brief description of the Configuration File and of the Syntax used in it.

The Configuration File is a text file called **DPPRunnerConfig.txt** generated by the program in a different destination path according to the user.

Here follows some examples of paths in typical Operative Systems:

Windows: %HomePath%\AppData\Local\DPP-PHA_ControlSoftware\DppRunnerConfig.txt

Where in

- Windows XP: %HomePath% is C:\Documents and Settings\<USER>
- Windows 7: %HomePath% is C:\Users\<USER>

Linux: /home/<USER>/DPP-PHA_ControlSoftware/DppRunnerConfig.txt



Note: this is the Configuration file that has to be used for enabling/disabling/modifying the GUI controls.

The safer procedure to modify the Configuration File is:

1. Disconnect the board via GUI
2. Modify the Configuration File
3. Save the Configuration File
4. Connect the board via GUI
5. Start acquisition

The Configuration File is divided in two (2) sections: COMMON and INDIVIDUAL.

Common Settings are listed in the file after the [COMMON] keyword and are the ones common to all the channels of the Digitizer.

Individual Settings are the ones related to a single channel of the Digitizer. Each list of individual parameters set for the same channel is to be reported after a [i] keyword, where "i" is the number of the channel section:

[0]

ENABLE_INPUT	YES	# setting 1 of channel "0" section
DC_OFFSET	40	# setting 2 of channel "0" section

[1]

ENABLE_INPUT	NO	# setting 1 of channel "1" section
DC_OFFSET	40	# setting 1 of channel "1" section

Every parameter not present in the Individual Settings section is intended to assume the value defined in the Common Settings section.

Each command has a description in which are shown the different options to modify it. The commands are textual so it is very easy to modify the different parameters.

Example 1: Enabling the External Trigger with no propagation

Go in the # **EXTERNAL_TRIGGER** section and modify the EXTERNAL_TRIGGER line from:

```
EXTERNAL_TRIGGER    DISABLED
```

to

```
EXTERNAL_TRIGGER    ACQUISITION_ONLY
```

In this way the board will be ready to accept an external trigger.

Other commands must be modified with numerical values and, in this case, the units are expressed in the description.

Example 2: Setting the Pre-Trigger value

PRE_TRIGGER: pre trigger size in number of samples

options: **1 to 511**

The relative command line will therefore be:

```
PRE_TRIGGER 500
```

In the Configuration File is even possible to manually modify the registers of the board within the Write Register section. For more information about the registers please look through the x724 User's Manual.

A copy of the Configuration File can be found in the "Data" folder of the program and it is called **DPPRunnerConfigDefault.txt**. This file contains the default values for all the parameters and it is read by the GUI when the **Restore** button is pushed.

At the same destination path of the *DPPRunnerConfig.txt*, another file is generated by the program, that is the **GuiConfig.txt**: it contains the structure definition of the GUI (not to be modified by the user) and a section with the trace parameters shown in **Fig. 6.10** (Trace Offset and Trace Gain).

Notes on Firmware and Licensing

The DPHA supports the DPP-PHA Firmware common to the 724 series of CAEN digitizers and the DT5780 Digital MCA. When running the DPP-PHA Control Software, the program checks for the firmware loaded in the target board and pops up a warning message if no licensed version is found (**Fig. 6.17**).

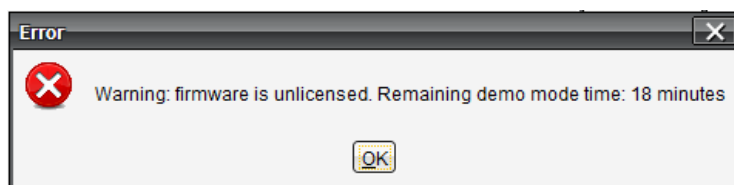


Fig. 6.17: Firmware unlicensed warning message

Note that when running the DPP-PHA Control Software, the program checks for the firmware loaded in the target Digitizer. If no license is found, a pop-up warning message shows up and reports the time left before the acquisition is stopped (trial version). In order to unlock the DPP firmware and use it without any time limitation, you need to purchase a license from CAEN. Refer to **[RD2]** for detailed instructions on how to use CAENUpgrader and on the licensing procedure.



Note: The DT5780 is an exception, since it is delivered already running a licensed version (i.e. not time limited) of the DPP-PHA Firmware. This means that no license needs to be bought by the user when purchasing a DT5780

7 Specifications

The following tables contain the relevant specifications about the hardware (x724 digitizer or DT5780), the firmware and the software components of a DPHA. For more details, please refer to the User Manual of the specific board.

x724 Specifications

PACKAGE	
DT5724/DT5724A	Desktop module: 154 x 50 x 164 mm ³ (WxHxD). Weight: 680 gr
N6724/N6724A	1 Unit NIM module
V1724/VX1724	1 Unit wide VME 6U module
Nr. OF INPUT CHANNELS	
DT5724/N6724	4 channels
DT5724A/N6724A	2 channels
V1724/VX1724	8 channels
ANALOG INPUT	
Dynamic Range	DT5724/DT5724A/N6724/N6724A/V1724/VX1724: 2.25 / 0.5 / 10 Vpp single ended, optionable (see ordering options) V1724/VX1724: 2.25 Vpp differential, optionable (see ordering option)
Connector Type	DT5724/DT5724A/N6724/N6724A/V1724/VX1724: MCX, Zin=50 Ω (2.25 / 0.5 Vpp), Zin=1 kΩ (10 Vpp) V1724/VX1724: AMP MODU II, differential, Zin=100 Ω
DC Offset	DT5724/DT5724A/ N6724/N6724A/V1724/VX1724: adjustable in the single ended ranges ±1.125/0.25/5 Vpp
DIGITAL CONVERSION	
Resolution	14 bit
Sampling Rate	100 MS/s simultaneously on each channels
Bandwidth	40 MHz
ENOB	11.98
I/O PORTS	
TRG-IN	External trigger input: NIM/TTL, Zin=50 Ω. LEMO connector
GPI/S-IN	Programmable input: NIM/TTL, Zin=50 Ω. LEMO connector
GPO/TRG-OUT	Programmable output: NIM/TTL across 50 Ω. LEMO connector
CK-IN	AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML. AMP MODU II connector, Zdiff=110 Ω
CLK-OUT	Clock output: DC coupled (LVDS), Zdiff = 110 Ω. AMP MODU II connector.
Digital I/Os	N.16 programmable differential LVDS I/O signals, Zdiff_in = 110 Ohm. Four Independent signal group 0÷3, 4÷7, 8÷11, 12÷15, In / Out direction control. 34-pin Header Connector
COMMUNICATION INTERFACES	
VME	VME64X compliant; D32 – BLT32 – MBLT64 – CBLT32/64 – 2eVME – 2eSST data modes; Multi Cast Cycles
USB	USB2.0 and USB1.1 compliant; up to 30 MB/s transfer rate
Optical Link	CONET protocol: CAEN proprietary optical link controlled by A2818 PCI or A3818 PCIe cards with a transfer rate up to 100 MB/s. Optical Daisy chain let 8 boards (A2818) up to 32 (A3818) to be managed by a single Controller
TRIGGER	
Trigger Source	Auto: each channel can detect the input pulse according to a programmable threshold and generates a trigger on it Global: a trigger common to all the channels Individual: a trigger related to a specific channel Software: a trigger generated by software (acts as global)
Trigger Propagation	Trigger can be propagated out through GPO (in Desktop and NIM modules) or TRG-OUT and LVDS I/Os (in VME modules) to other boards, and it can be feed in through TRG-IN (in all modules) or LVDS I/Os (VME only)
POWER REQUIREMENTS	
DT5724/DT5724A	Power input: +12 ± 10% Vdc
N6724/N6724A	Power consumptions: 3.9 A @ +6 Vdc, 90 mA @ -6 Vdc
V1724/VX1724	Power consumptions: 4.5 A @ +5 Vdc, 0.2 A @ +12 V, 0.2 A @ -12 V

Tab. 7.1: x724 Specifications Table

DT5780 (MCA) Specifications

PACKAGE	
Desktop module: 140 x 44 x 163 mm ³ (W x H x L). Weight: 950 g.	
ANALOG INPUT	
Channels	2 analog input channels on BNC connectors ($Z_{in} = 1\text{ k}\Omega$)
Dynamic Range	0.6 / 1.4 / 3.7 / 9.5 Vpp; single ended; software selectable
DC Offset	Adjustable in the full range
DIGITAL CONVERSION	
Resolution	14 bit
Sampling Rate	100 MS/s simultaneously on each channel
Bandwidth	40 MHz
I/O PORTS	
TRG-IN	External trigger input: NIM/TTL on LEMO connector ($Z_{in}=50\text{ }\Omega$)
GPI	Programmable input: NIM/TT On LEMO connector ($Z_{in}=50\text{ }\Omega$)
GPO	Programmable output: NIM/TTL on LEMO connector (requires $50\text{ }\Omega$ termination)
CLK-IN	AC coupled differential input clock: LVDS, ECL, PECL, LVPECL, CML on AMP MODU II connector
COMMUNICATION INTERFACE	
USB	USB2.0 and USB1.1 compliant; up to 30 MB/s transfer rate
Optical Link	CONET protocol: CAEN proprietary optical link controlled by A2818 PCI or A3818 PCIe cards with a transfer rate up to 80 MB/s. Optical Daisy-chain let 8 boards (A2818) up to 32 (A3818) to be managed by a single Controller
TRIGGER	
Trigger Source	Auto: each channel can detect the input pulse according to a programmable threshold and generates a trigger on it (individual independent trigger) External (special use): trigger on TRG_IN connector coming from an external generator (global trigger) Software: a trigger generated by software (global trigger)
Trigger Propagation	Trigger can be propagated out through GPO to other boards and it can be feed in through TRG-IN connector
HV	
Channels	2 HV channels on SHV connectors; on/off ramp programmable by software: 1 to 500 V/s in steps of 1 V/s
Polarity	Negative, Positive and Mixed, selectable by ordering options
Voltage (Vset)	5 kV
Current (Iset)	300 μ A
Vset / Vmon resolution	100 mV
Iset / Imon resolution	5 nA
Voltage ripple	< 5 mVpp
PREAMP	
Channels	2 LV channels on DB9 female connectors
Power	$\pm 24\text{ V}$ @50 mA and $\pm 12\text{ V}$ @100 mA with an output voltage tolerance of $\pm 2\%$
Voltage ripple	< 5 mVpp
HV Inhibit	Active High or Low, selectable through dedicated external switch; inhibit signal on DB9 connector duplicated on dedicated BNC connector
POWER REQUIREMENTS	
Power input	+12 VDC, 45 W (by the power supply included in the kit)
POWER CONSUMPTIONS	
3.3 A @ 12 VDC (max.)	

Tab. 7.2: DT5780 (MCA) Specifications Table

Firmware Specifications

DIGITAL PROCESSING	
Firmware	Digital Pulse Processing for Pulse Height Analysis (DPP-PHA)
Algorithms	Trapezoidal Filter for pulse energy calculation Trigger-and-timing Filter for the detection of the input pluses and the calculation of the relevant time stamp
Digital controls	Decimation: 1 / 2 / 4 / 8 selectable values
	Input Signal Gain: 1 / 2 / 4 / 8 selectable values
	Decay Time: 200 ns up to 5 ms accepted range for time constant of exponentially decaying pulses
	Shaping Time: 50 ns up to 80 μ s selectable trapezoid rise times (equivalent to 22 ns – 36 μ s shaping)
	Flat Top: finely tuneable to compensate the ballistic deficit
	Baseline mean: 0 / 16 / 64 / 256 / 1024 / 4096 / 16384 selectable values
	Trigger threshold: selectable in LSB for self-triggering
Additional parameters for advanced setting	
Pile-up	Optional Rise Time Discriminator (RTD) technique for advanced pile-up rejection management
	Programmable hold-off windows for trigger and pile-up rejection in high counting rate acquisitions
Dead Time	No dead time due to conversion. Spectrum live correction with respect to the piled-up events, very important in case unsteady radiation sources are used, e.g. short living isotopes or activity transients.
ICR	Up to 1 Mcps

Tab. 7.3: Firmware Specifications Table

Software Specifications

SOFTWARE	
Control Interface	DPP-PHA Control Software for configuration, acquisition, plotting, HV management (only DT5780)
Histograms	Two histograms built by the software: <ul style="list-style-type: none"> Energy histogram: histogram of the energy distribution Time histogram: histogram of the pulse timing distribution (Δt between pulses)
Operating Modes	Oscilloscope Mode: monitoring of input waveforms and internal filters digital output signals Histogram Mode: histogram representation of energy and pulse timing distributions
Setting Modes	Basic: a limited selection of configurable filter parameters for typical applications Advanced: extended selection of configurable filter parameters; RTD and hold-off window options
Plotting	Up to 4 traces simultaneously selectable per input channel in Oscilloscope Mode: 2 analogs (using Dual Trace option) and 2 digitals. Energy and Time histogram options selectable per input channel in Histogram Mode. Note: only one channel at a time can be plotted both in Oscilloscope and in Histogram Mode
Saving Options (FORMAT)	Energy histograms (ASCII) Lists of energy & time stamp events (ASCII – BINARY) Waveforms (ASCII) Time histograms (ASCII))
HV control (only DT5780)	Channel Powering: ON/OFF ramp controlled Bias Monitoring HV Status Monitoring Power Down Mode Setting: Kill/Ramp programmable
Libraries	To users who wants to develop their own software, CAEN provides a high-level library to configure the hardware, handle the acquisition and retrieve the acquired data (in form of energy histograms)

Tab. 7.4: Software Specifications Table

8 Technical support

CAEN makes available the technical support of its specialists at the e-mail addresses below:

- support.nuclear@caen.it
(for questions about the hardware)
- support.computing@caen.it
(for questions about software and libraries)



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