ICCAD 2019 CAD

Contest

Problem B: System-level FPGA Routing with Timing Division Multiplexing Technique

Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao
Synopsys Taiwan Co., Ltd.,
1F., No. 25, Gongye E. 4th Rd., Hsinchu Science Park, Hsinchu, Taiwan

Contents

0. Announcement

October

- 2018-10--

August

- 2018-08--
- 2018-08--
- 2018-08--

July

- 2018-07--
- 2018-07--
- 2018-07--
- 2018-07--
- 2018-07--

June

- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--
- 2018-06--

May

- 2018-05--
- 2018-05--
- 2018-05--

April

-

March

- 2019-03-19- ProblemB updated.

Fabruary

- 2019-02-19- ProblemB updated.
- 2019-02-13- ProblemB description updated.
- 2019-02-11- ProblemB description updated.
- 2019-02-01- ProblemB announced.

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Yu-Hsuan Su, Emplus Huang, Hung-Hao Lai, and Yi-Cheng Zhao
Synopsys Taiwan Co., Ltd.,
1F., No. 25, Gongye E. 4th Rd., Hsinchu Science Park, Hsinchu, Taiwan

I. Introduction

As IC process geometry shrinks rapidly, the size of VLSI circuits as well as fabrication costs are also increased. Logic verification is one of the most important methodologies in advanced sub-nanometer technology and beyond, according to ITRS roadmap.

One of the strategies for logic verification is software logic simulation. It provides visibility and debugging capabilities. However, it consumes huge runtime and significant cost since it have to emulate each logic gate one by one and the circuit size is extremely large. Another way to perform logic verification is the hardware emulation. It greatly reduces runtime but the implementation cost is very high. The other approach for logic verification is using FPGA prototyping system. The FPGA prototyping verifies the circuit by a configurable FPGA system. Due to the capacity limitation of one FPGA, a multi-FPGA prototyping system is developed to verify a large circuit design. It is faster and cheaper. Thus, the FPGA prototyping system is widely used in industry.

To adapt a design to the FPGA prototyping system, a large VLSI circuit must be partitioned into sub-circuits and each of them fits a single FPGA. Since the number of I/O pins in an FPGA is fixed and limited, the routing signals can usually exceed the number of I/O pins. A time-multiplexing division [Babb, et al.] is required to transfer multiple I/O signals by time division technique.

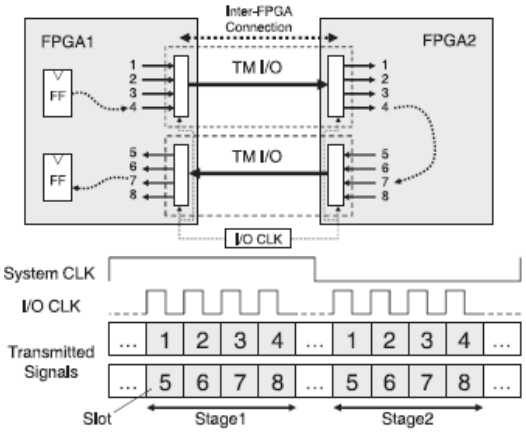


Fig. 1. The time multiplexing division (TDM) technique. Total eight routing signals can be transmitted in one system clock period. The technique increases the signal capability in one FPGA and the high routability for the prototyping system. However, this technique also slows down the inter-FPGA signal delay. [Babb, et al., "Virtual wires: Overcoming pin limitations in FPGA-based logic emulators", IEEE FCCM 1993]

Here introduce the time multiplexing division technique (TDM) as shown in Fig. 1. Without this technique, only two routing signals can be transmitted through one FPGA in one system clock period. With the time multiplexing technique, eight routing signals can be transmitted in one system clock period. The technique dramatically increases routing capability in the FPGA prototyping system. However, this technique also slows down the inter-FPGA signal delay which is increased by the time multiplexing rate. For example, the time multiplexing rate in Fig. 1 is eight.

The challenges for system-level FPGA routing lies in the side-effect of TDM. For example, with TDM, routing can always complete. But the inter-FPGA signal delay is increased by time-multiplexing of I/O pins [M. Inagi, et al., 2010].

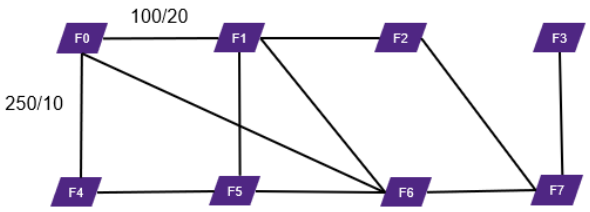


Fig. 2. We can model this system-level FPGA routing problem to a graph. Each FPGA connection can be modeled as one graph edge and each signal belongs to one or multiple net groups. Please kindly notice that TDM ratio is defined as an even number due to multiplexing hardware implementation. For example, TDM ratio = 26 for 250/10 but not 25 for the F0 and F4 connection. 250 is the number of total wires in the inter-FPGA connection and 10 is the total number of I/O pins.

Intuitively we can model this system-level FPGA routing problem to a routing graph as shown in Fig. 2. Each FPGA connection can be modeled as one graph edge and each signal belongs to one or multiple net groups. We can also define the capacity of each edge as the number of pins, and demand of each edge as the number of signals. Please kindly notice that TDM ratio is defined as an even number due to multiplexing hardware implementation. Each signal in an edge should have its TDM ratio and the TDM ratio is defined as an even number. For example, TDM ratio = 26 for 250/10 but not 25 for the connection between F0 and F4 in Fig. 2. Suppose there are total 250 wires

routing through the inter-FPGA connection F0 and F4, and there are total 10 I/O pins available in this inter-FPGA connection.

In addition, we will define a net group including several nets in one group due to design purpose. For example, nets belongs to similar attributes or same power consumption would be in the same net group.

There are mainly two approaches for the system-level FPGA routing system. One is to model as an optimization problem and solved by ILP [M. Inagi, et al.] and the other is a heuristic method by modelling as a routing graph [M. Turki, et al.].

II. Problem Formulation

Given a netlist (with two-pin and/or multi-pin nets), a multi-FPGA system with timing division multiplexing (TDM) channels between each FPGA connection pair, and net groups, route the nets and assign TDM ratio for each channel, with minimized maximum total TDM ratio for each net group and minimized run time. Each net could belong to several net groups. The output is the routing path of each net and the TDM ratio along this routing path. The objective is to minimize the maximum total TDM ratio of each net group and runtime simultaneously.

Each routing signal should have its TDM ratio. The TDM ratio is an even number and at least two. That is, the smallest TDM ratio is two. In addition, the TDM ratios of all routing signals on a routing edge (on an inter-FPGA connection) should satisfy $1 >= (1/2) * r_2 + (1/4) * r_4 + (1/6) * r_6 ... + (1/k) * r_k$, where r_i is #signal using TDM ratio i, $i=1\sim k$. That is, there could be TDM ratio = r_2, r_4, r_6,…, or r_k in one inter-FPGA connection. For example, $r_2 = 2$ and $r_4 = 4$.

Formally, we have below definition of TDM constraint for one FPGA connection:

The TDM ratio on one FPGA connection (a graph edge) is $1 >= (1/2) * r_2 + (1/4) * r_4 + (1/6) * r_6 + ... + (1/k) * r_k$, where r_i is #signal using TDM ratio i, $i=1\sim k$ and $r_i \% 2 = 0$ (Equation 1).

III. Input Format

There are mainly four parts in the input format.

The first part describes total number of FPGAs, total number of FPGA connections, total number of nets, and total number of nets including two-pin nets and multi-pin nets, and total number of net groups.
Format: **<Total number of FPGA> <Total number of FPGA connections> <Total number of nets> <Total number of net groups>**

The second part is FPGA connections. The number of lines in the second part is the number of FPGA connection.
Format: **<FPGA id> <FPGA id>**

The third part is the net description. The first label is the source and the remaining labels describing the targets. The number of lines for the third part is equal to the total number of nets.
Format: **<FPGA source> <FPGA target 1> <FPGA target 2>…**

The final part is the net groups describing net ids in one net group. The number of lines for the fourth part is equal to the total number of net groups.
Format: **<Net id> <Net id>…**

More precisely, the first line of input file contains four positive integers N_f *(1≤* N_f *≤500),* N_e *(1≤*N_e *≤*N_f*(*N_f*−1)/2),* N_w*(1≤* N_w *≤1000000),* and N_g *(1≤*N_g*≤1000000)* separated by space. N_f is the total number of FPGA, N_e is the total number of FPGA connections or graph edges, N_w is the total number of nets, N_g is the total number of net groups.

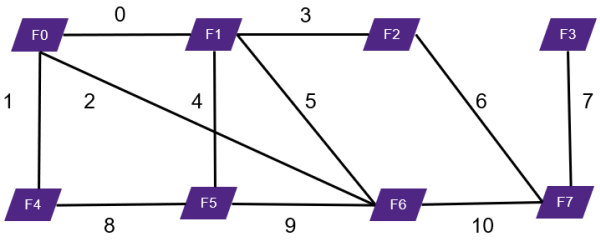
Next we have N_e lines represent N_e graph edges. The line number indicates edge id starting from zero to N_e*-1*. The *i*-th line contains two positive integers *j* and *k (0 ≤ j<k < *N_f*)* separated by space represents the edge id *i (0≤i<*N_e*)* connects FPGA F_j and F_k. We guarantee that FPGA graph is a connected graph.

And then we have N_s lines represent N_s routing nets. The line number indicates net id starting from zero to N_s*-1*. The *m*-th line includes positive integers s and t_k *(0≤*t_k*<*N_f*)* separated by spaces represents the source of the net id *m (0≤m<*N_s*)* is *s* and the target is t_k.

Finally we have N_g lines represent N_g net groups. The line number indicates net group id starting from zero to N_g*-1*. The *n*-th line includes integers g_m *(0≤*g_m*<*N_e*)* separated by spaces represents that there are $|g_m|$ nets for net group id *n*. We guarantee that all nets will be in one group.

Sample input of the inter-FPGA connections in Fig. 2 is below:

```
8 11 5 3
0 1
0 4
0 6
1 2
1 5
1 6
2 7
3 7
4 5
5 6
6 7
0 1
1 5
5 6
0 4 5 6
5 7
0 1 2
3
4
```



Net id	Source FPGA id	Target FPGA id
0	0	1
1	1	5
2	5	6
3	0	4, 5, 6
4	5	7

Fig. 3. The five nets and the corresponding FPGA source and target ids for the five nets from sample input. The number labelled on the edge is the edge id.

IV. Output Format

Output the data in the order of the net id referred to the input format.

For each net, the first line prints out the total number of edges for the net. Then print out n_e lines for total n_e edges of this net. There are two numbers for each line. One is the net id and the other is the TDM ratio for this net on this routing path.

For example, below is the format of a routing path using two routing edges:

<total number of routing edge>

<edge id> <TDM ratio>

<edge id> <TDM ratio>

A feasible solution for the sample input:

1
0 2
1
4 2
1
9 2
3
1 2
8 2
9 4
2
9 4
10 2

There could be several TDM ratios on a graph edge if it satisfies 1 >= (1/2) * r2 + (1/4) * r4 + (1/6) * r6…+ (1/k) * rk. For example, the TDM ratio of edge id 9 is 4 because it satisfies 1>= 1/4 * 3. In addition, there are three wires route through edge id 9 which are net ids 2, 3, and 4. Because there is only one routing wire routes through edge id 10, TDM ratio of net 4 on edge id 10 is two.

V. Evaluation Methodology

To emphasize on the runtime impact for large designs, runtime is considered in the evaluation score.

Evaluation score = alpha * runtime + beta * maximum total TDM ratio of all net groups, where alpha = beta = 0.5.

VI. References

1. M. Inagi, Y. Takashima, and Y. Nakamura, “Globally optimal time-multiplexing of inter-FPGA connections for multi-FPGA prototyping systems.” TSLM, pp. 388-397, 2010
2. M. Inagi, Y, Takashima, Y. Nakamura, and A. Takahashi, “ILP-based

optimization of time-multiplxed I/O assignment for multi-FPGA system.” IEEE 2008

3. M. Turki, Z. Marrakachi, H.Mehrez, and M. Abid, “Signal multiplexing approach to improve inter-FPGA bandwidth of prototyping platform.” DATS, 2015

VII. FAQ

Q1. The descriptions under the picture Fig.1 and Fig.2 in page2 is almost the same.

A1. There should be two corresponding descriptions for Fig. 1 and Fig. 2

Q2. How to set the TDM ratio in the output file? Is each group of nets set from 2 if not used?

Because there seems to be no mention how to set the TDM ration in the whole document, only mention the TDM ratio=26, 250/10. What is 250 and 10 ? and there is no similar number in the Input file.

A2. Please refer to the problem formulation: The TDM ratio is an even number and at least two.

I have updated in the introduction: Suppose there are total 250 wires routing through the inter-FPGA connection F0 and F4, and there are total 10 I/O pins available in this inter-FPGA connection.

Q3. The TDM ratios of all " routing signals "on a routing edge should satisfy 1 >= (1/2) * r2 + (1/4) * r4 + (1/6) * r6…+ (1/k) * rk, where ri is #signal using TDM ratio i, i=1~k.

Does "routing signal" mean a net group?

Because the TDM ratio of edge 9 has two values in the output file given by the example, I think the above description means each net groups can only have own TDM ratio.

A3. Routing signals mean the routing wires.

There could be several TDM ratios on a graph edge if it satisfies 1 >= (1/2) * r2 + (1/4) * r4 + (1/6) * r6…+ (1/k) * rk. But there is a typo in the value so I have updated the sample output. The TDM ratio of edge id 9 is 4 because it satisfies 1>= 1/4 * 3. In addition, there are three wires route through edge id 9 which are net ids 2, 3, and 4.

Q4. Last paragraph in the example output file

1

9 4

Is there a wrong answer here?

Because this net is routing from FPGA id = 5 to 7, but edge 9 is only connected from 5 to 6, so we need to route extra edge 10 to connect from 5 to 7.

A4. The sample output has been modified as

2

9 4
10 2
Because there is only one routing wire routes through edge id 10. So TDM ratio of net 4 on edge id 10 is two.

Q5. Follow problem 4, how to set TDM ratio = 4 of edge 9? Because the previous net group 1 (0 1 2) has used edge 9 (TDM ratio = 2), so the TDM ratio = 4 here ?
A5. There could be several TDM ratios on a graph edge if it satisfies 1 >= (1/2) * r2 + (1/4) * r4 + (1/6) * r6…+ (1/k) * rk. The TDM ratio of edge id 9 is 4 because there are three wires route through edge id 9 which are net ids 2, 3, and 4. In addition, it satisfies 1>= 1/4 * 3.

Q6. Is the FPGA I/O pin is fixed to 1 in this problem?
A6. To simply the problem, we abstract the multiple FPGA I/O pin hardware architecture as just one graph edge between two FPGAs and define the #pin as the edge capacity. For example, there are 100 FPGA pins for an FPGA interconnection. Then the capacity of this graph edge is 100.

Q7. What is the function of the net group? Is used to calculate the Evaluation score? How to determine the maximum total TDM ratio of all net groups? Could you give some example?
A7. Yes, it is used to calculate the evaluation score. For example, the total TDM ratio of net group 1, 2, and 3 are 100, 24, and 50. Then the maximum total TDM ratio of the design is 100.

Q8. Does each net can't have multiple source? Like the 4th net group, I want to output '6 2' rather than '9 2'. And this output seems better than previous one.
A8. Thanks for your question. Yes, each net is single source.

Q9. How is the ouput '8 2' generated? Does that mean the signal has been transfered to F4 and now it can directly be tranfered from F4 to F5?
A9. The source of net id 3 is F0 and targets are F4, F5, and F6. So it could route through edge 1, 8, 9 and route through F4, F5, and F6.

Q10. Why the TDM ratio = 4 of edge 9 at the end of the output while it is 2 for the 3rd net? I think the ratio of edge 9 should all be 9. Is there something wrong here?

A10. Thanks for your observation. We have updated “9 2” to “9 4” to satisfy the TDM constraint equation (Equation 1 in problem formulation).

Q11. How to set TDM ratio =2 of edge 9? The net id 2, 3, and 4 are all through the edge which edge id is 9, but why their TDM ratio is not the same.
A11. There could be many TDM ratio values in one edge (one FPGA connection). But the ratio should satisfy TDM constraint equation (Equation 1 in problem formulation). So there is one net with TDM ratio = 2 and two nets with TDM ratio = 4 to satisfy 1 >= (1/2) * 1 + (1/4) * 2. We have updated the example output.

Q12. In the example output file
3
1 2
8 2
9 2
Is there a wrong answer here?
The signal goes from FPGA 0 to FPGA 5 through the edge 1 and the edge 8, why this net's TDM ratio is not 4.
A12. Yes, there is a wrong output in the current version. We have updated “9 2” to “9 4” for net 3 to satisfy 1 >= (1/2) * 1 + (1/4) * 2.

Q13. I have some further question about Q3 in Problem B, FAQ.
It said that"The TDM ratio of edge id 9 is 4 because it satisfies 1>= 1/4 * 3. In addition, there are three wires route through edge id 9 which are net ids 2, 3, and 4."
However, in part IV, the sample output had the egde id 9 with 3 TDM ratio 2, 2, 4, respectively.
Therefore, in my point of view, r2=2 and r4=1 refering to this inequality "1 >= (1/2) * r2+ (1/4)* r4+ (1/6) * r6...+ (1/k) * rk".
Here comes my quetion. Why is the inequalit shown in Q3 said the TDM ration in sample output satisfied 1>= 1/4 * 3, not 1/2*2 + 1/4*1(which violate the inequality)?
Then, when we calculating total TDM ratio, whether we should use 2 or 4 for edge id 9 in netgroup 1 and 2? That is, total TDM ration for netgroup (0, 1, 2) is either (2+2+2, 2+2+2, 4+2) or (2+2+4, 2+2+4, 4+2)?
Besides, can you please give some other examples which can help us understand this problem more?
A13. Thanks for your question. Please refer to the answer to A12.

Q14. I think there is a misleading inequality specified in the problem description, for edge number 9 in the given example, this equation: 1 >= (1/2) * 2 + (1/4) * 1 actually does not hold? Is there any mistake made in the official FAQs?

A14. Thanks for your question. Please refer to the answer to Q12.