

ESS: Exercise Set 4

Timers

Question 1:

Calculate the parameters to setup a periodic timer with the following properties:

- System Clock of 64 MHz
- Prescaler of 1,2,8,16,32 (PRESCALE)
- 16 bit period compare register (PERIOD)

For each one, calculate the actual frequency you obtain and the percentage error. Also compute whether the desired period could be attained with an 8 bit period compare register and what the percentage error would be.

- (a) A period of 1 μ S
- (b) A frequency of 50 kHz
- (c) A frequency of 128 Hz
- (d) A frequency of 57.6 kHz (common baudrate)
- (e) A frequency of 1 Hz

Solution:

Using a clock of 64 MHz, and a prescaler ranging from (1,2,8,16,32), we can achieve effective clock rates of (64,32,8,4,2) MHz. We can now compute what effective periods/frequencies we can achieve with these clock rates.

	Desired Frequency (Hz)				
Clock Freq (MHz)	1000000.00	50000.00	128.00	57600.00	1.00
64	64.00	1280.00	500000.00	1111.11	64000000.00
32	32.00	640.00	250000.00	555.56	32000000.00
8	8.00	160.00	62500.00	138.89	8000000.00
4	4.00	80.00	31250.00	69.44	4000000.00
2	2.00	40.00	15625.00	34.72	2000000.00

The table above shows the divisors (period) that need to be used to achieve each of the desired frequencies, depending on the prescaler input. Cells which are shaded in red are not achievable with a 16 bit width.

From this, we can see that achieving very low frequencies (e.g. 128 Hz or 1 Hz) can be impossible for certain divisors and clock speeds.

All the “nice” like 1MHz, 50kHz, 128kHz can be achieved exactly i.e. no rounding errors.

For strange frequencies like 57600 Hz, you can see that the divisor is a non-integer. Obviously, in reality, it has to be an integer, and this leads to rounding errors.

For example, if we use a prescaler of 2 (effective 32 MHz clock rate), then the period register needs to be set to 555. Thus, the actual clock rate is $32 \text{ MHz} / 555 = 57657 \text{ Hz}$, which is a 57 Hz error (0.1%).

If we use an 8 bit period register, many clock configurations are not possible:

	Desired Frequency (Hz)				
Clock Freq	1000000.00	50000.00	128.00	57600.00	1.00
64	64.00	1280.00	500000.00	1111.11	64000000.00
32	32.00	640.00	250000.00	555.56	32000000.00
8	8.00	160.00	62500.00	138.89	8000000.00
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Interrupts

Question 2:

What must be done as a minimum to enable interrupts?

Solution:

- Set up the Vector Table (in Keil, references are defined to the ISR vectors like `void TIM4_IRQHandler(void)`)
- Set the priority level in the interrupt itself

- Enable the interrupt
- Enable global interrupts