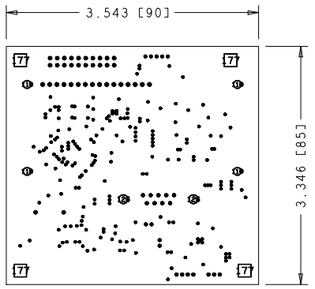
DRILL CHART: TOP to BOTTOM ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	10.0	+0.0/-10.0	PLATED	10
•	13.0	+0.0/-13.0	PLATED	191
•	35.0	+3.0/-3.0	PLATED	5
•	37.0	+3.0/-3.0	PLATED	4
•	40.0	+3.0/-3.0	PLATED	16
•	42.0	+3.0/-3.0	PLATED	2
•	43.0	+3.0/-3.0	PLATED	20
•	48.0	+3.0/-3.0	PLATED	16
⓫	110.0	+3.0/-3.0	PLATED	4
⓬	126.0	+3.0/-3.0	PLATED	2
⑦⑦	177.0	+3.0/-3.0	NON-PLATED	4



NOTES (UNLESS OTHERWISE SPECIFIED):

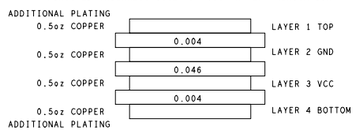
1. GENERAL
   - 1.0 PWB MUST BE ROHS/WEEE COMPLIANT.
   - 1.1 STANDARDS-ALL RAW CARDS MUST CONFORM TO IPC-6012 CLASS 2 USING THE MOST CURRENT REVISION LEVEL.
   - 1.2 FOR INSPECTION, BOARDS MUST MEET THE REQUIREMENTS OF THE ACCEPTABLE LEVEL OF IPC-600 USING THE MOST CURRENT REVISION LEVEL.
2. MATERIAL
   - 2.0 NEMA GRADE FR-4
   - 2.1 TD>=340 DEGREES C, TG>=170 DEGREES C, Z-AXIS EXPANSION =< 3.5%
   - 2.2 REFER TO DETAIL "B" FOR LAYER STACKUP AND THICKNESS.
   - 2.3 FLAMMABILITY RATING 94V-0.
3. ETCH
   - 3.0 ETCH TOLERANCE ON ALL FOIL FEATURES INCLUDING FINISHED TRACE WIDTH AND SPACING TOLERANCE IS +/-20% OF THE ORIGINAL ARTWORK/GERBER DESIGN.
4. FINISH
   - 4.0 PLATE THRU WITH COPPER.
   - 4.1 ELECTROLESS NICKEL IMMERSION GOLD IN ACCORDANCE WITH IPC-4552.
5. IMPEDANCE CONTROL
   - 5.0 REFER TO DETAIL "A" FOR IMPEDANCE CONTROL TARGETS.
6. SOLDERMASK
   - 6.0 VENDOR MUST USE THE ARTWORK SUPPLIED, THIS ARTWORK MAY CONTAIN VIAS THAT ARE PARTIALLY COVERED (ENCROACHED) WITH SOLDERMASK. ON NON-VIA HOLES AND SURFACE MOUNT PADS THERE SHOULD BE NO SOLDERMASK ON PADS AND A MAXIMUM OF .004 CLEARANCE AFTER FABRICATION WITHOUT EXPOSING ANY TRACES.
   - 6.1 FOR VIAS WITH SOLDERMASK DEFINITION ON BOTH SIDES, FOLLOW GERBER TO BUILD. FOR VIAS WITHOUT SOLDERMASK DEFINITION, USE SOLDERMASK TO FILL VIAS AT LEAST 80%. FOR VIAS WITH SOLDERMASK DEFINITION ON SINGLE SIDE, PLUG VIAS FROM THE SIDE WHERE THERE IS NO SOLDERMASK DEFINITION.
   - 6.2 SOLDERMASK TO BE LPI GREEN.
   - 6.3 SOLDERMASK TO BE IN ACCORDANCE WITH IPC-SM-840 CLASS H.
7. DRILLING
   - 7.0 ALL HOLE DIAMETERS IN HOLE CHART ARE FINISHED SIZES.
   - 7.1 SSH(SPECIAL SHAPE HOLE) TO BE ROUTED AND PLATED IN ACCORDANCE WITH OUTLINE AROUND IF THERE IS SSH FIGURE IN THE DRILL CHART.
8. MARKING
   - 8.0 MARKING TO BE WHITE.
   - 8.1 MARKING NOT TO ENCROACH ON SURFACE MOUNT LANDS.
9. VENDOR OPTIONS/REQUIREMENTS
   - 9.0 REMOVAL OF NON-FUNCTIONAL PADS NEED WRITTEN APPROVAL FROM JABIL.
   - 9.1 ANY THIEVING ON INTERNAL OR EXTERNAL LAYERS NEED WRITTEN APPROVAL FROM JABIL. IF THIEVING IS ALLOWED,THE MINIMUM SPACING TO CONDUCTIVE FEATURES IS .100".
   - 9.2 REPLACE THE TEXT IN THIS AREA WITH VENDOR COMPANY LOGO, UL LOGO, DATE CODE, AND UL FLAMMABILITY RATING.
   - 9.3 X-OUT IS NOT ALLOWED WITHOUT WRITTEN APPROVAL FROM JABIL.
   - 9.4 ANY OTHER CHANGES NEED WRITTEN APPROVAL FROM JABIL.
10. NETLIST
    - 10.0 NETLIST SUPPLIED IN IPC-D-356 FORMAT.
11. BACKDRILL
    - 11.0 IF THE BOARD REQUIRES BACKDRILL, ALL BACKDRILL HOLES ARE NON-PLATED.
    - 11.1 REMOVE THE PADS AT STARTING LAYER FOR BACKDRILL HOLES IF NECESSARY.
12. ELECTRICAL TEST
    - 12.0 PWB MUST BE TESTED PER IPC-9252 USING SUPPLIED IPC-D-356 NETLIST.
    - 12.1 ELECTRICAL TEST CERTIFICATION MARK "ET" IS STAMPED USING PERMANENT, NON-CONDUCTIVE ROHS COMPLIANT INK.
    - 12.2 THE STAMP SHALL BE PLACED IN A LOCATION FREE OF PADS, TEST POINTS, FIDUCIALS, OR OTHER MARKINGS.
    - 12.3 EACH INDIVIDUAL BOARD IN ARRAY FORM SHALL BE STAMPED.

LAYER NAME	IMPEDANCE TOLERANCE +/-10%	
	LINE WIDTH/OHMS SINGLE ENDED	LINE WIDTH/SPACE/OHMS DIFFERENTIAL PAIRS
LAYER 1 TOP	N/A	N/A
LAYER 2 GND PLANE	N/A	N/A
LAYER 3 VCC PLANE	N/A	N/A
LAYER 4 BOTTOM	N/A	N/A

DETAIL A
SCALE: NONE

4 LAYER STACKUP

FINISHED THICKNESS .062 +/- .004 AFTER FABRICATION



DETAIL B
SCALE: NONE

CHANGES

A United Technologies Company

SPB

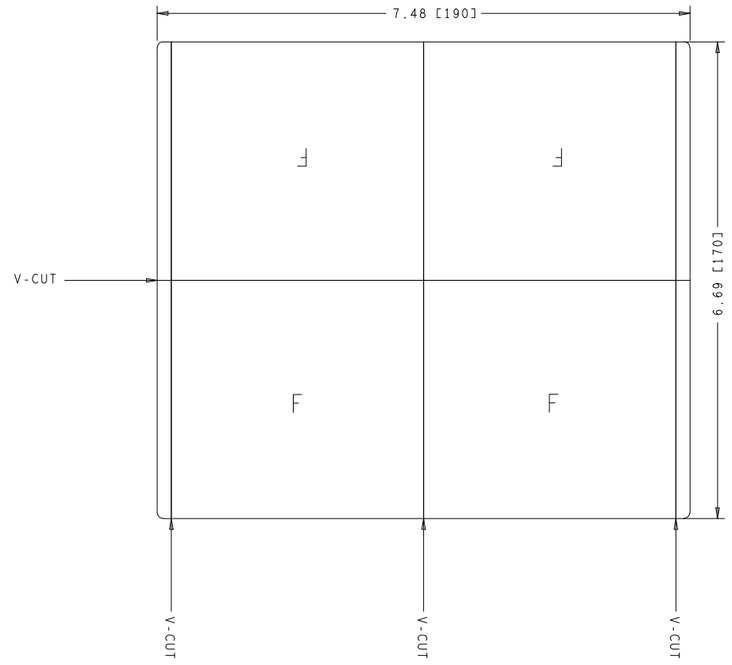
DWG DAA610EC1

OTIS ENGINEERING CENTER
SHANGHAI

MATERIAL:	DRAWN	APPLE GUO	ORIGINAL DATE 2016-04-08
	CHK	VINCENT TIAN	
SPEC:	APPD	VINCENT TIAN	14 SHEETS
FINISH:	AUTH	CN831799	SHEET 1

ALL DIMENSIONS METRIC

DRAFTED IN ACCORDANCE WITH OTIS DOCUMENT 52847



CHANGES

A United Technologies Company

SPB

MATERIAL:

SPEC:

FINISH:

DWG DAA610EC1

OTIS ENGINEERING CENTER
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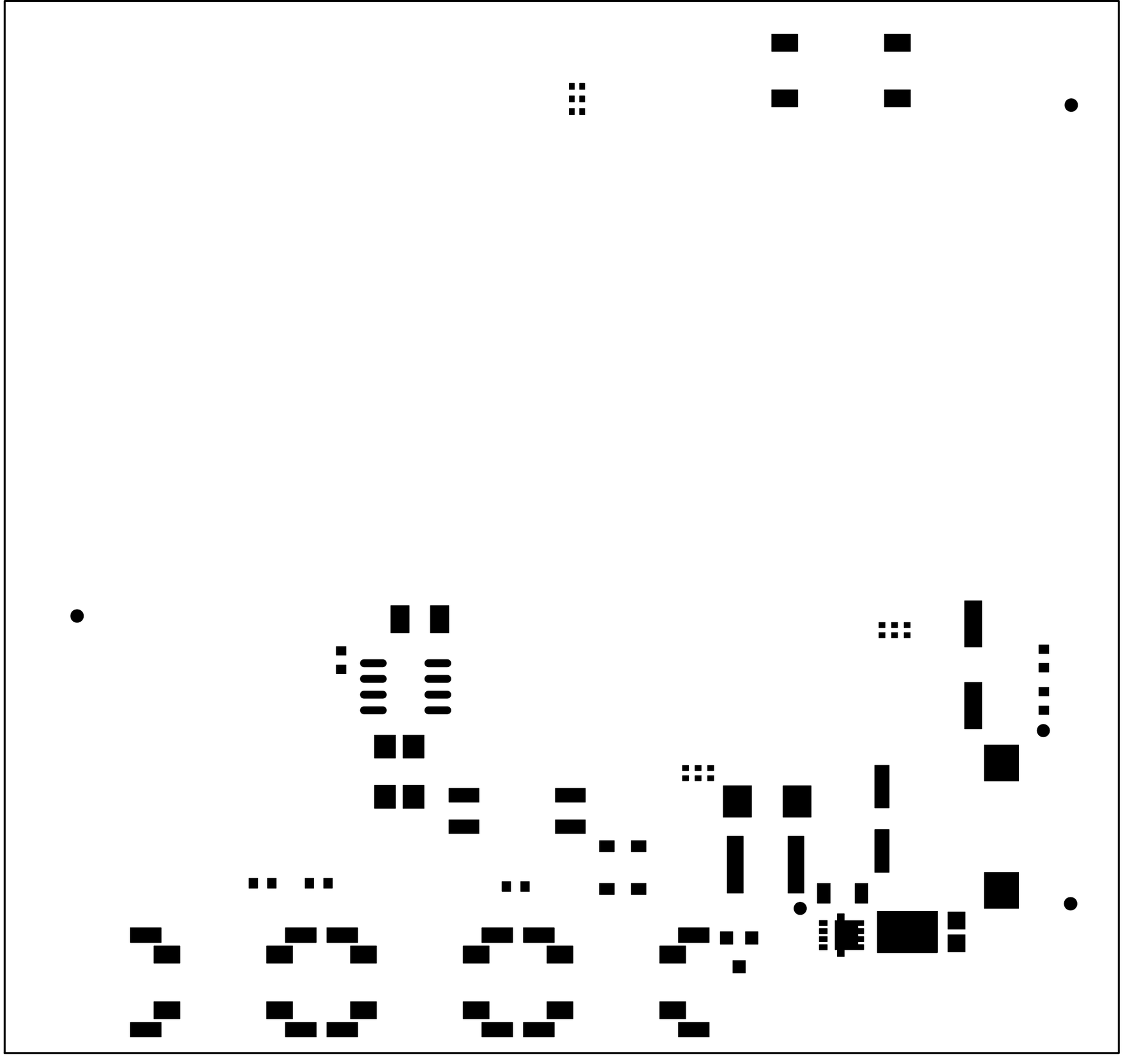
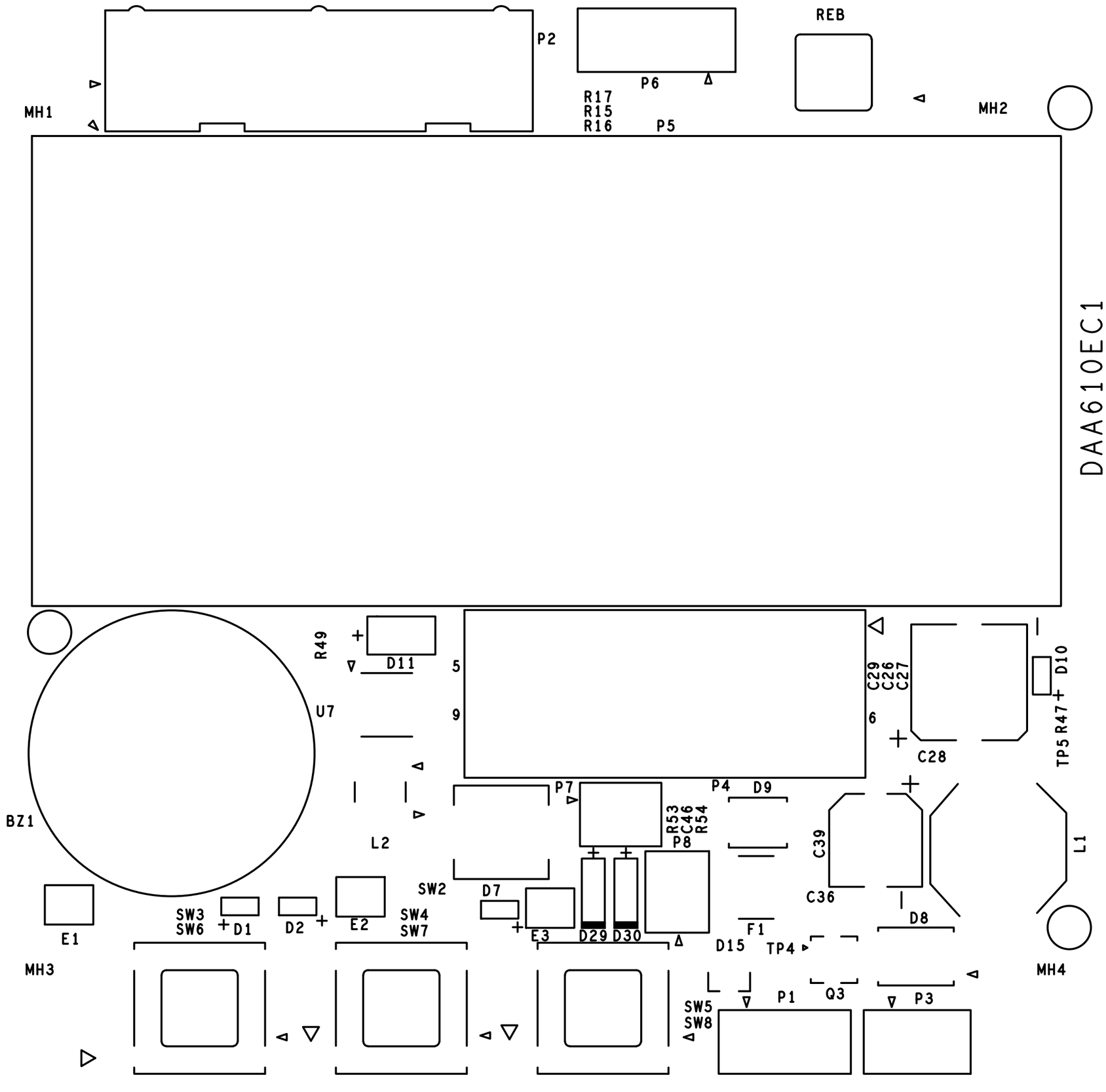
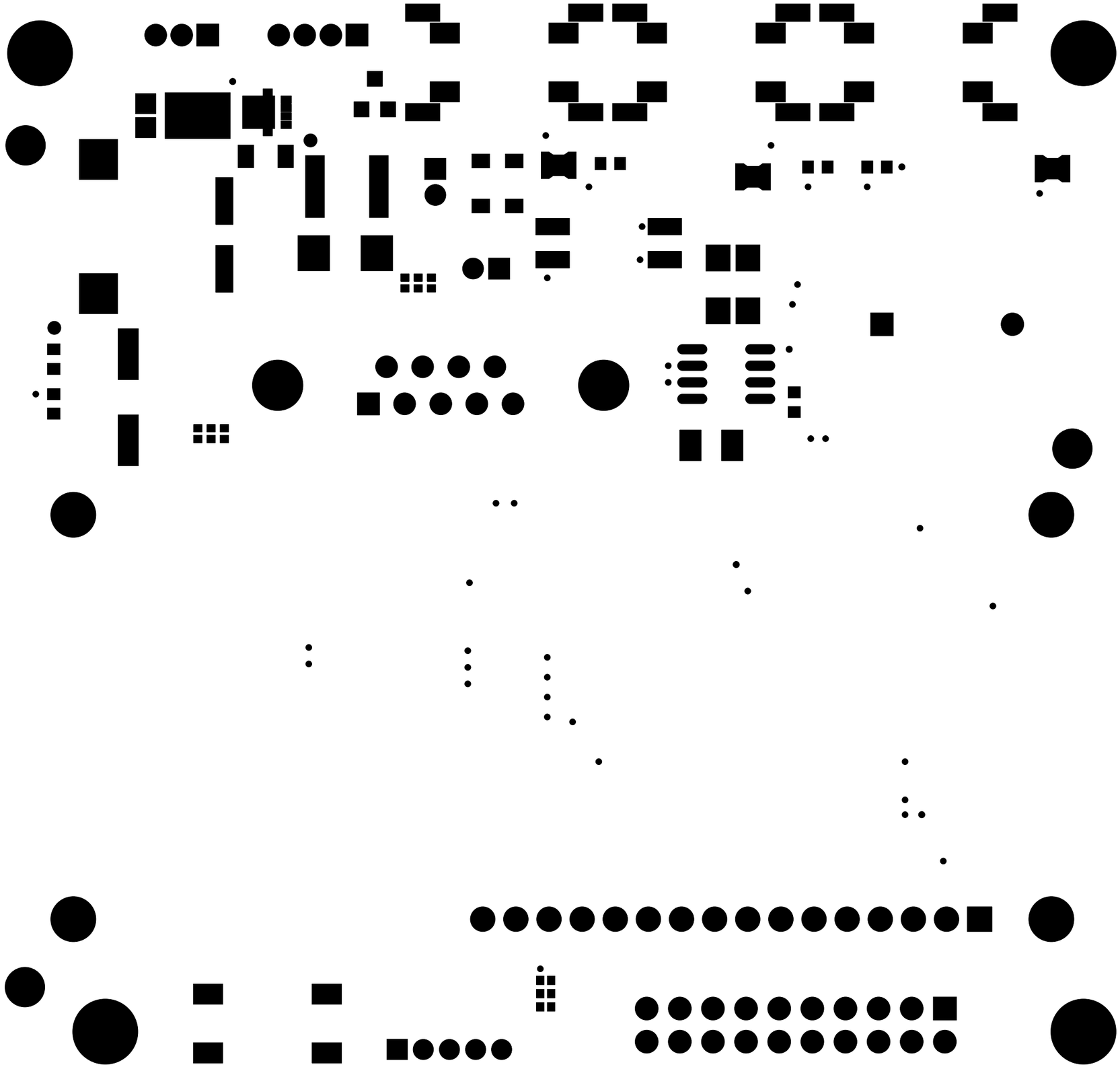
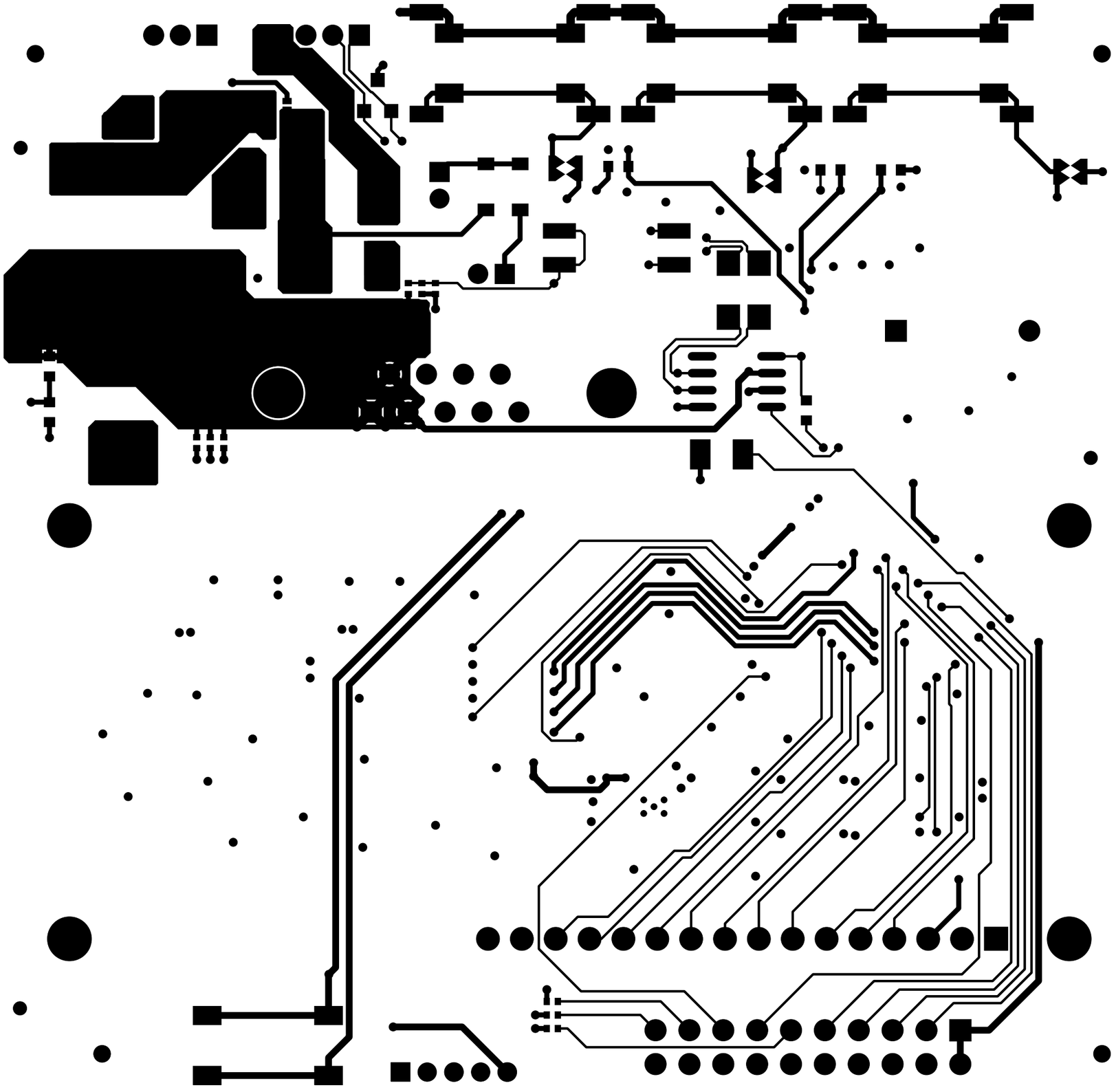
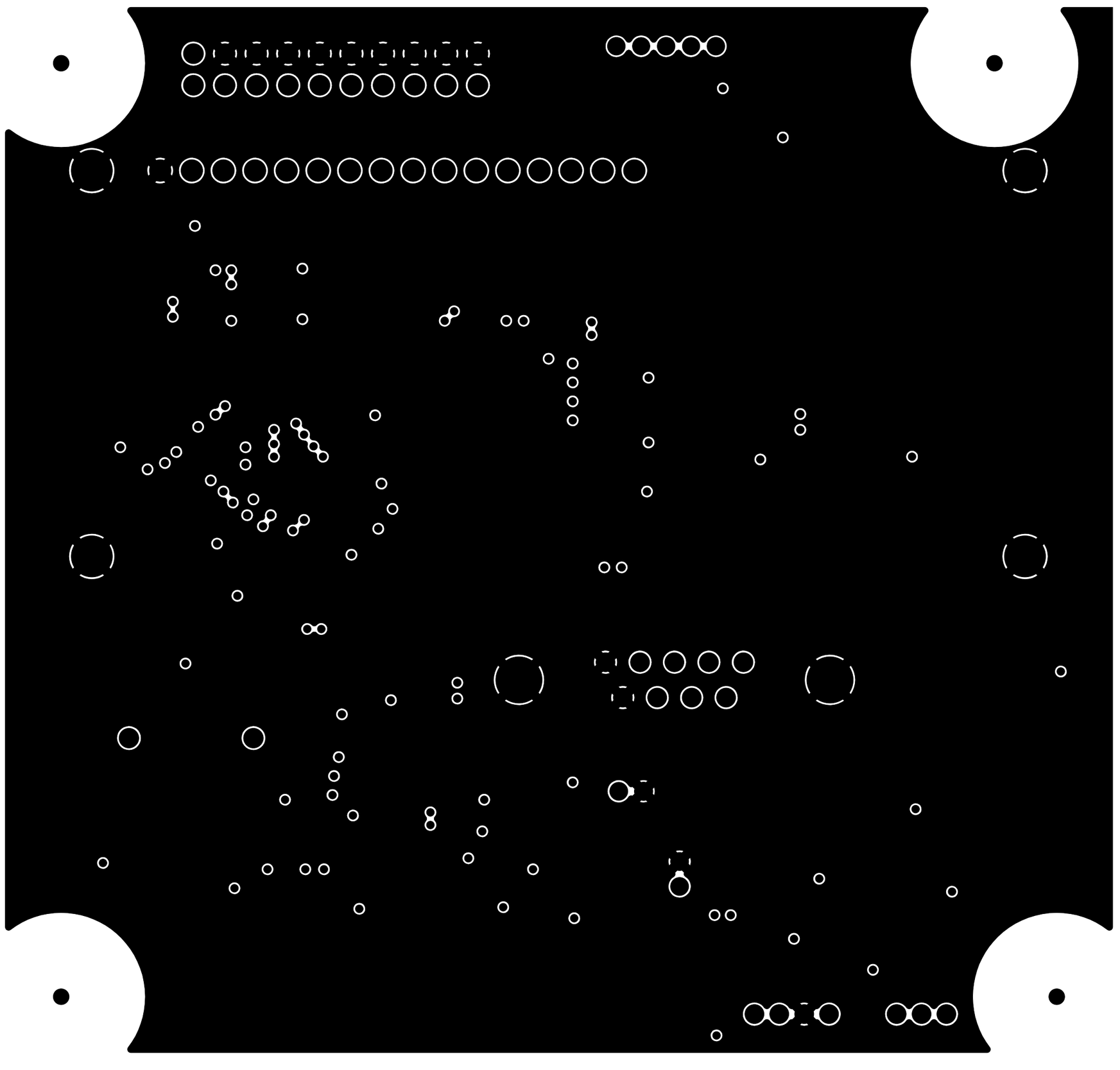
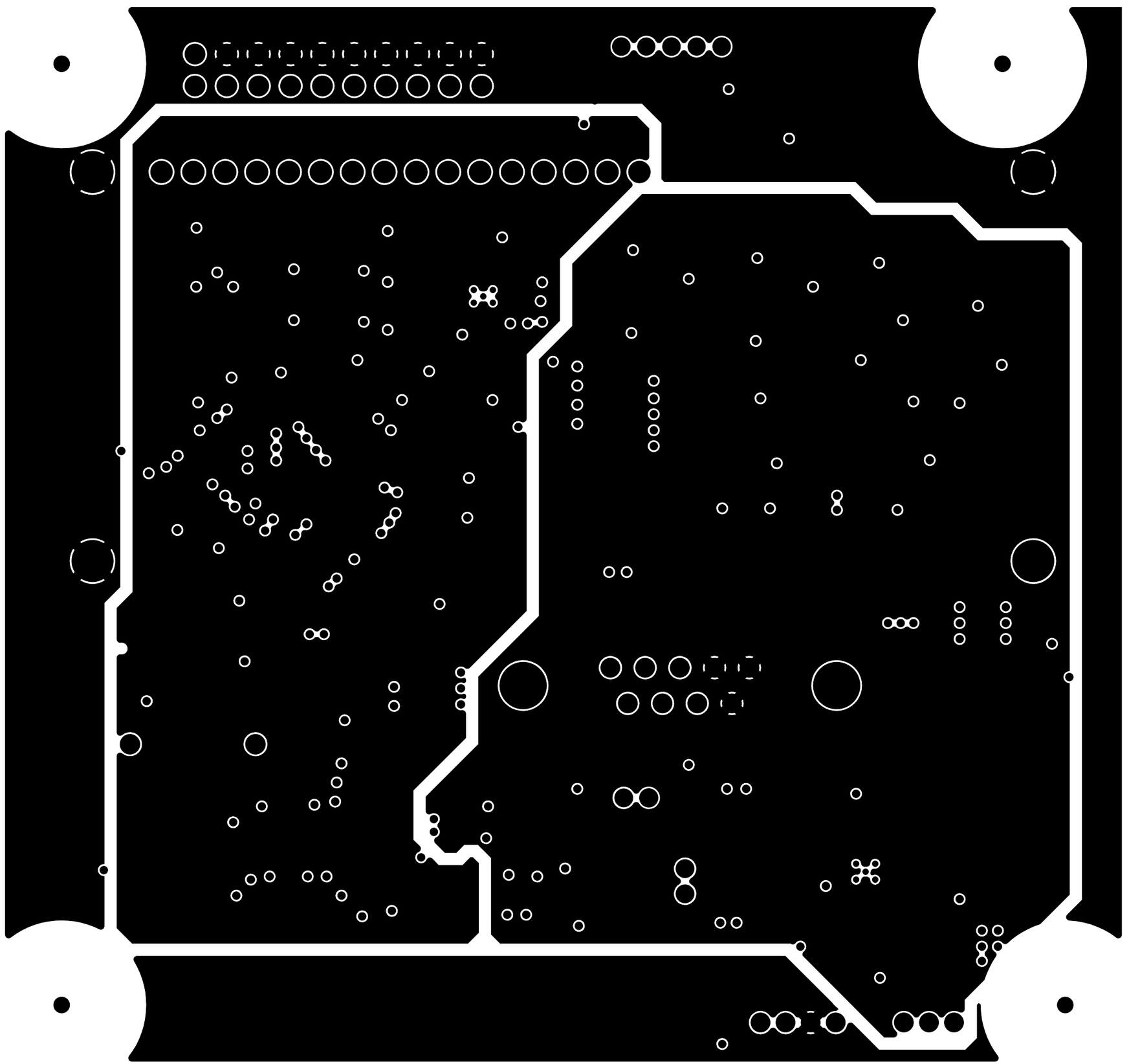



P2
P6
REB
MH1
R17
R15
R16
P5
MH2
DAA610EC1
R49
D11
U7
5
9
6
C29
C26
C27
D10
TP5
R47
C28
BZ1
P7
P4
D9
R53
C46
R54
P8
L2
C39
L1
SW2
D7
C36
SW3
SW6
D1
D2
E2
SW4
SW7
D8
E1
E3
D29
D30
F1
D15
TP4
MH3
MH4
SW5
SW8
P1
Q3
P3









DAA610EC1
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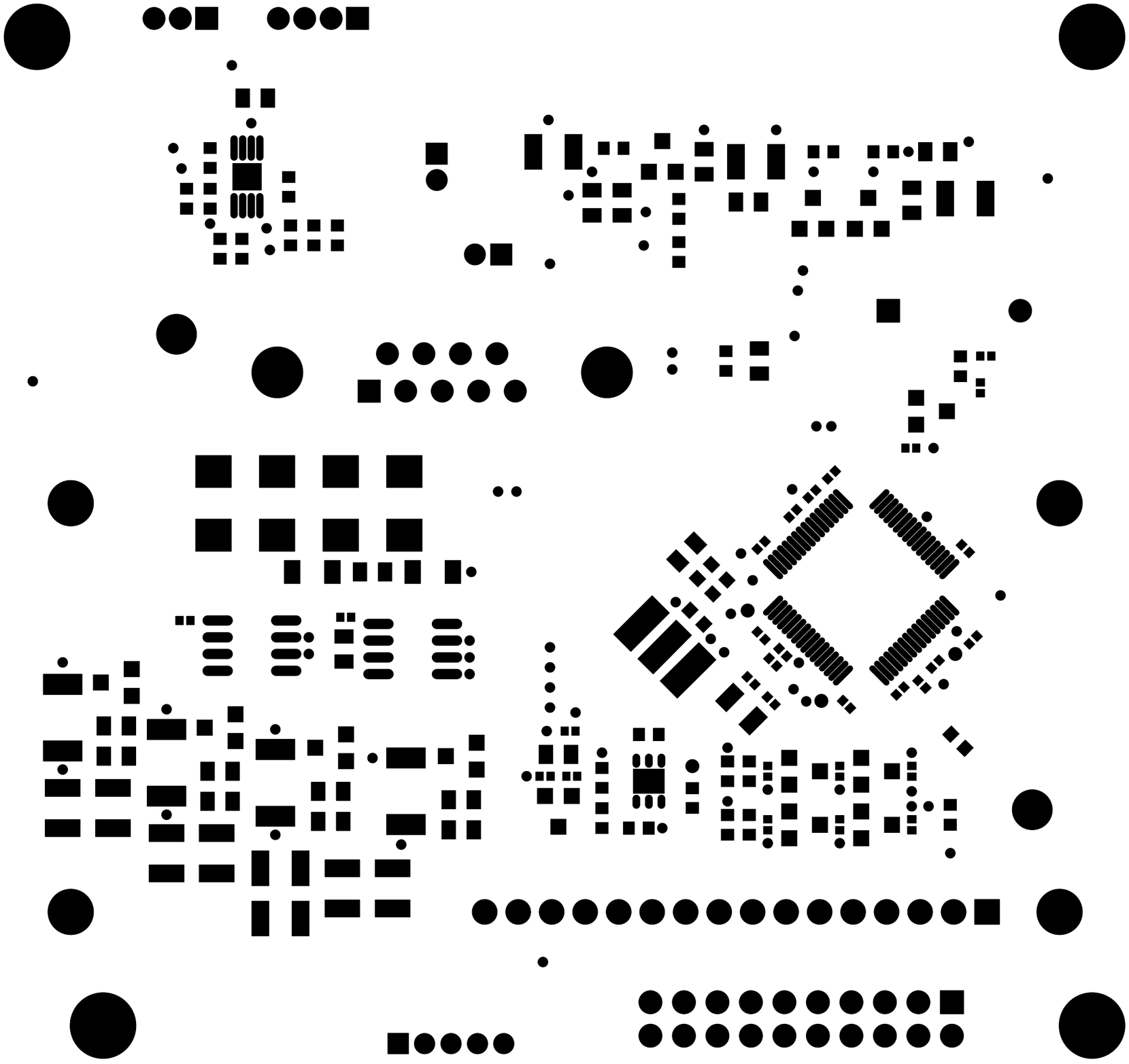
2015-11-20



LABEL Y22A

BOARD LABEL