FUJITSU MICROELECTRONICS
DATA SHEET

Jan 19 2010

Memory FRAM

CMOS

64 K (8 K x 8) Bit I2C

MB85RC64

■ DESCRIPTION

The MB85RC64 is a FRAM (Ferroelectric Random Access Memory) Stand-Alone chip in a configuration of 8,192 words x 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
The MB85RC64 adopts the two-wire serial interface (compatible with the world standard I2C bus).
Unlike SRAM, the MB85RC64 is able to retain data without using a data backup battery.
The read/write endurance of the non-volatile memory cells used for the MB85RC64 has improved to be at least 10^{10} cycles, significantly outperforming Flash memory and EEPROM in the number.
The MB85RC64 does not need a polling sequence after writing to the memory such as the case of Flash memory nor EEPROM.

■ FEATURES

- Bit configuration : 8,192 words x 8 bits
- Operating power supply voltage : 2.7 V to 3.6 V
- Operating frequency : 400kHz (Max.)
- Two-wire serial interface : I2C-bus specification ver. 2.1 compliant, supports Standard-mode/Fast-mode. Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating temperature range : -40 °C to +85 °C
- Data retention : 10 years (<+55 °C)
- Read/write endurance : 10^{10} times (Min.)
- Package : Plastic / SOP, 8 pin (FPT-8P-M02)
- Low power consumption : Operating current 400μA (Max.: @400kHz), Standby current 10μA (Typ.)

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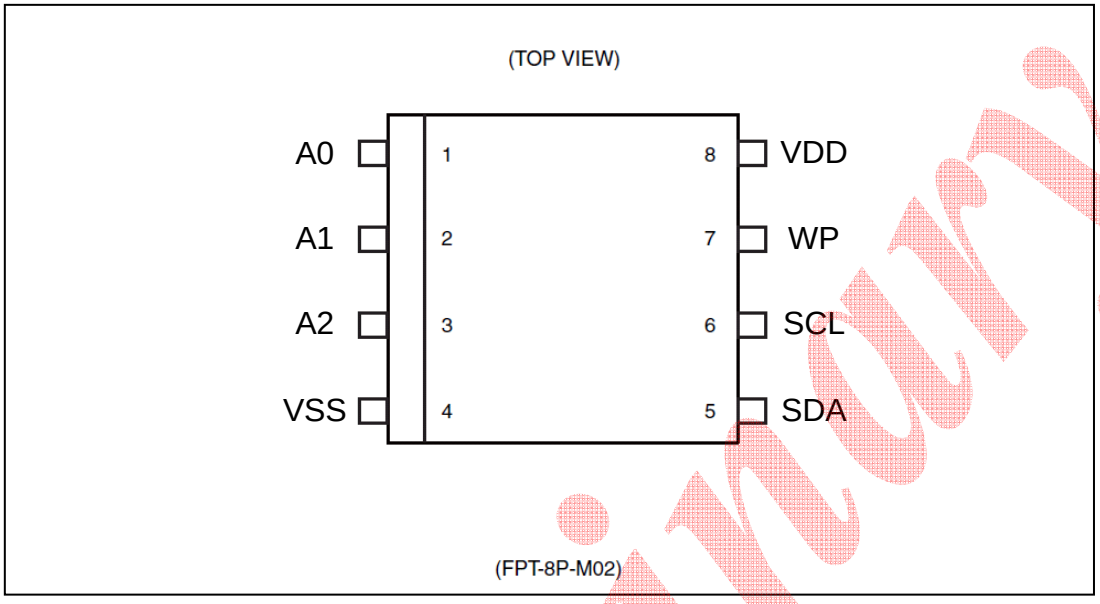
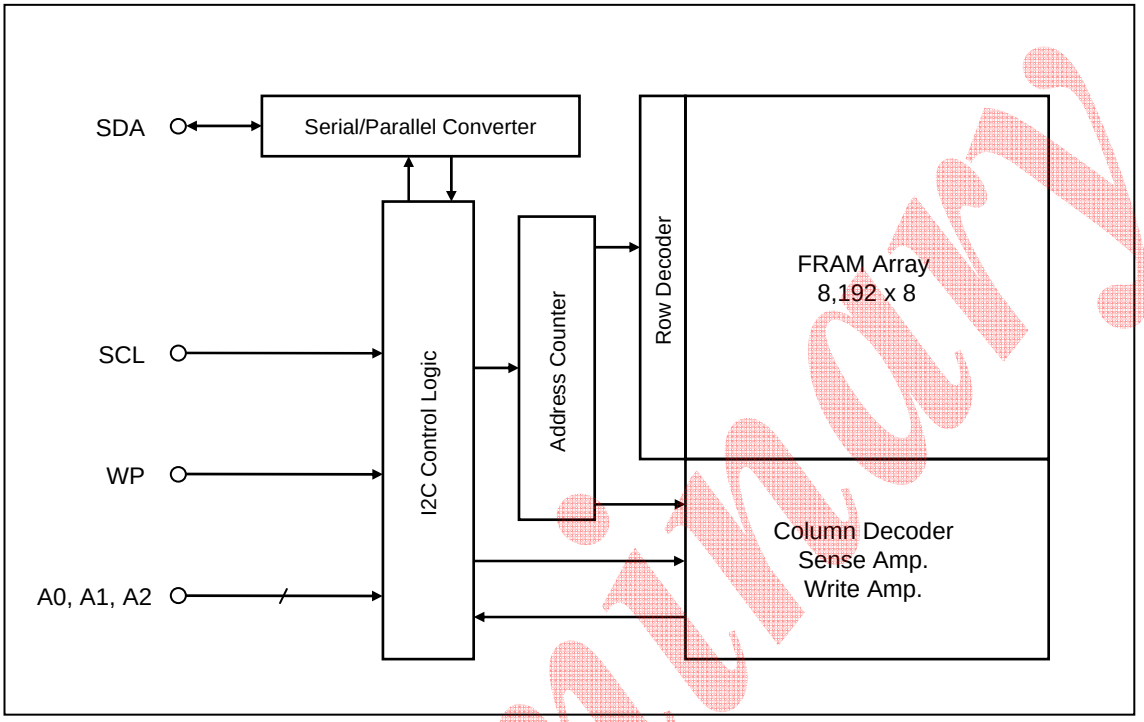
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

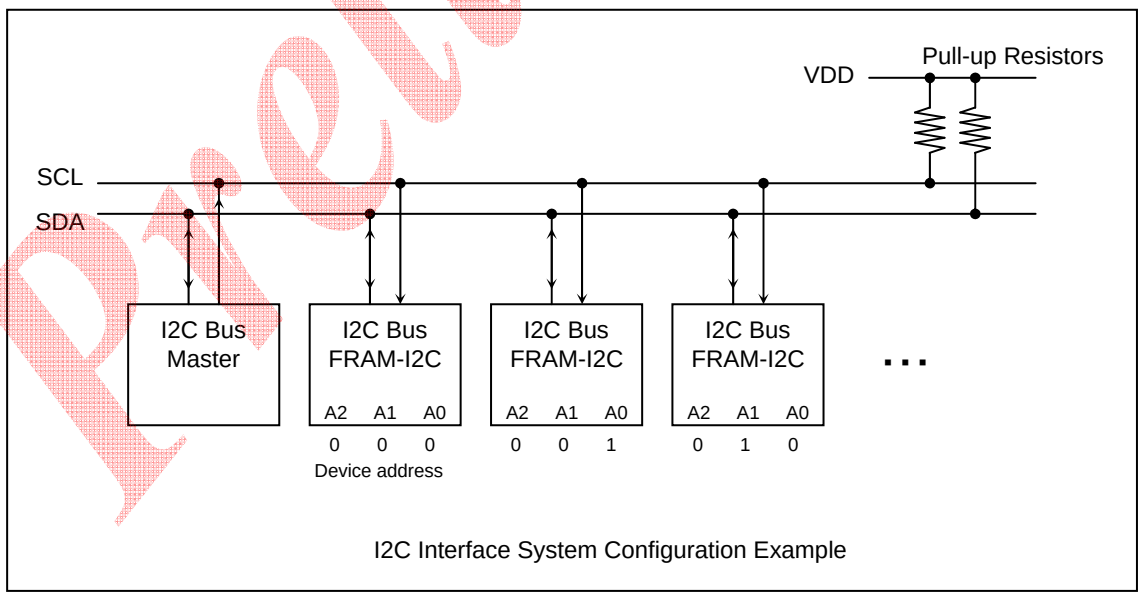
Pin Number	Pin Name	Functional Description
5	SDA	Serial Data I/O This is an I/O pin of serial data for performing bidirectional communication of address and writing or reading data of FRAM memory cell array. It is an open drain output that may be wired OR with other open drain or open collector signals on the bus, so a pull-up resistance is required to be connected to the external circuit.
6	SCL	Serial Clock This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect When WP is "H", writing operation is disabled. When WP is "L", the entire memory region can be overwritten. Reading operation is always enabled regardless of the WP input level. If WP is not forced as "H" or "L", WP is internally pull-downed.
1 to 3	A0 to A2	Device Address Device addresses are used in order to identify each of the devices. The MB85RC64 can be connected to the same I2C bus up to 8 devices. The MB85RC64 only operates when the A0, A1, and A2 combination of "H" and "L" matches the device address code input from the SDA pin. In the open pin state, A0, A1, and A2 are internally pulled-down and recognized as "L".
8	VDD	Supply Voltage
4	VSS	Ground

■ BLOCK DIAGRAM



■ I2C (Inter-Integrated Circuit)

The MB85RC64 has a two-wire serial interface, supports the I2C™ bus*, and operates as a slave device. (*: I2C is a registered trademark of Philips.) The I2C bus defines communication roles of "master" and "slave" devices, with the master side holding the authority to initiate control. Furthermore, a I2C bus connection is possible where a single master device is connected to multiple slave devices. In this case, it is necessary to assign a unique device address to the slave device.



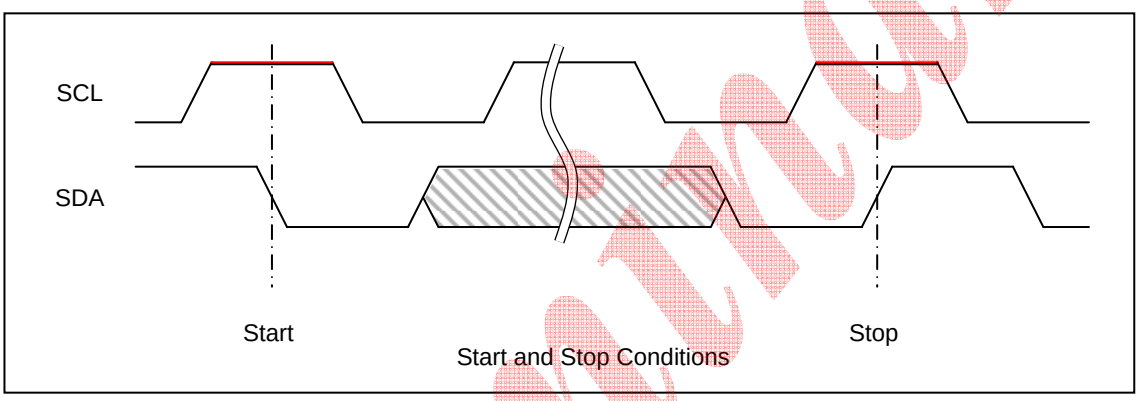
I2C Interface System Configuration Example

■ DEVICE CONITION

The I2C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The SDA signal should change while SCL is Low. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is High.

• Start Condition
Start is identified by a falling edge of SDA while SCL is stable in the High state.

• Stop Condition
Stop is identified by a rising edge of SDA while SCL is stable High. Stop condition terminates communication between the device and the bus master. The MB85RC64 need not spend time to any polling sequence for internal writing memory such as EEPROM, so a Stop condition at the end of a write command force the device into the pure stand-by mode.



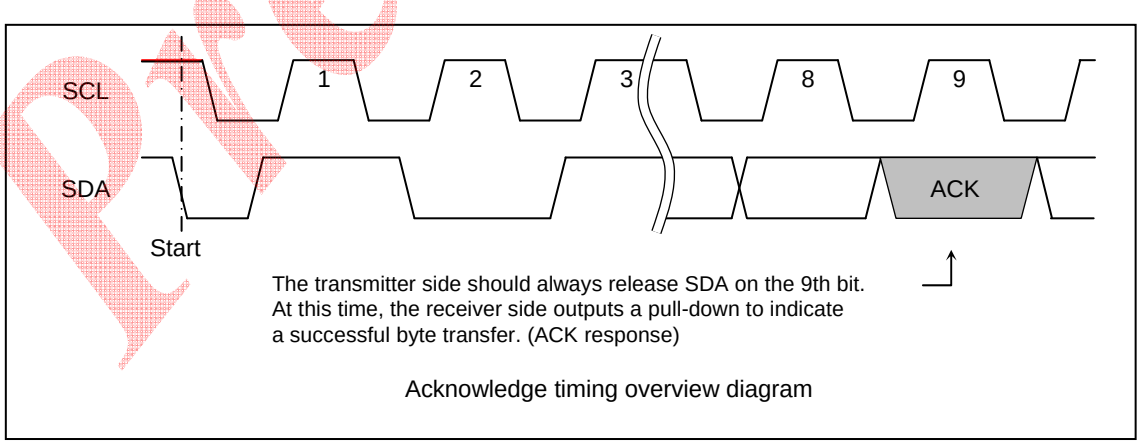
Start and Stop Conditions

Note: The FRAM device does not need the programming time (tWC) after issuing the Stop Condition.

■ Acknowledge (ACK)

In the I2C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every each 8 bits of the data is successfully sent and received. The information receiver side usually outputs "L" every time on the 9th SCL clock after each 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released to HiZ every time on this 9th clock to allow the acknowledge signal to be received and checked. During this HiZ-released period, the receiver side pulls the SDA line down to indicate "L" that the previous 8bits communication is successfully received.

If the information receiver side detects Stop condition before driving the acknowledge "L", the read operation ends and the I2C bus enters the standby state. If Stop condition is not sent, nor does the transmitter detect the acknowledge "L", the bus remains in the released state "H" without doing anything.



Acknowledge timing overview diagram

■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the bus master sends the 8bits device address word (Slave address) to start I2C communication. The device address word (8bits) consists of a device Type code (4bits), device address code (3bits), and a read/write code (1bit).

• Device Type Code (4bits)
The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at "1010" for the MB85RC64.

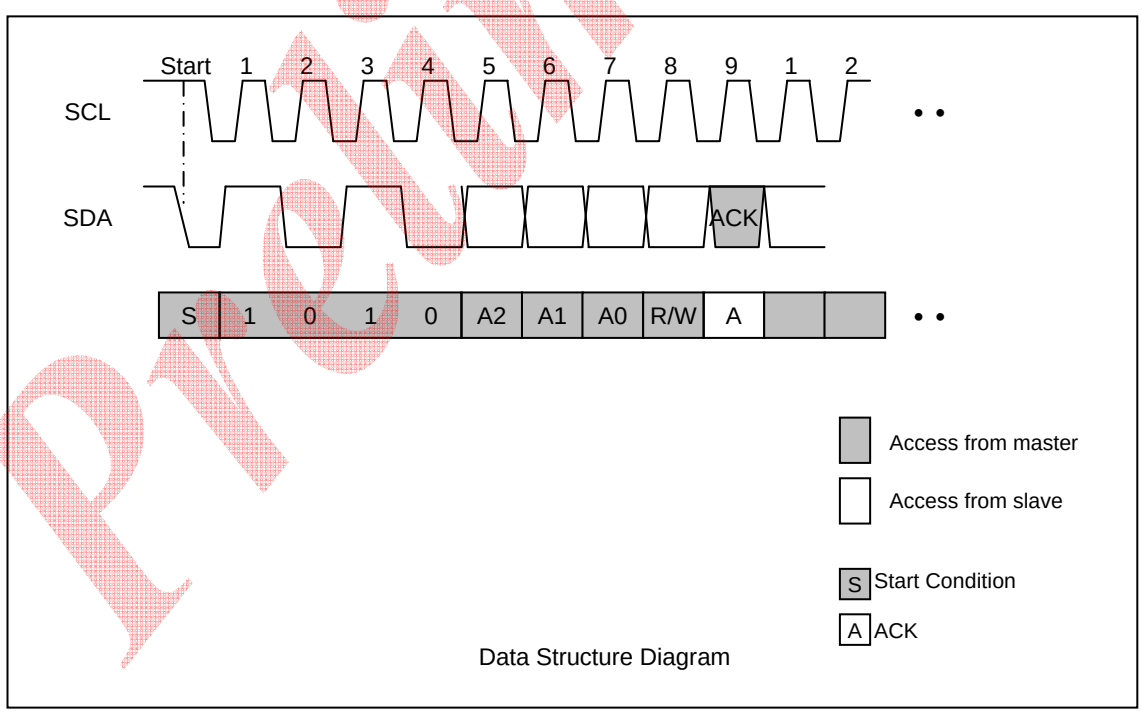
• Device Address Code (3bits)
Following the device type code, the 3 bits of the device address code are input in order of A2, A1, and A0. Each MB85RC64 is given a unique 3bits code on the device address pin (external hardware pin A2, A1, and A0). When the device address code is received by the slave device, the slave only responds if the hardware device address of which is equal to its unique 3bits code.

• Read/Write Code (1bit)
The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is "L", a write operation is enabled, and the R/W code is "H", a read operation is enabled for the MB85RC64.

■ DATA STRUCTURE

In the I2C bus, the acknowledge "L" is output on the 9th bit after the 8 bits of the device and address word following the start condition. After confirming the acknowledge response at the slave, the I2C master outputs 8bits x2 memory address to the I2C slave. When the memory address input ends, the slave again outputs the acknowledge "L". After this operation, the I/O data follows in units of 8 bits, with the acknowledge "L" output after every 8bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. For a write operation the slave will accept 8bits from the master then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8bits. For a read operation the slave will place 8bits on the I2C bus, then wait for an acknowledge from the master.



Data Structure Diagram

■ FRAM Acknowledge -- Polling Not Required

The MB85RC64 performs write operations at the same speed as read operations, so any waiting time for an ACK polling* does not occur. The write cycle takes no additional time.

*: As to EEPROM, the Acknowledge Polling is performed as a progress check in the write programming step. It places NAK condition on the bus as of "not acknowledged" during the writing programming period. The busy status for the write programming is given from 9th ACK bit. That "done" condition is placed onto I2C bus by EEPROM I2C device and your program had to poll the bus in order to sense that condition.

■ Write Protect (WP)

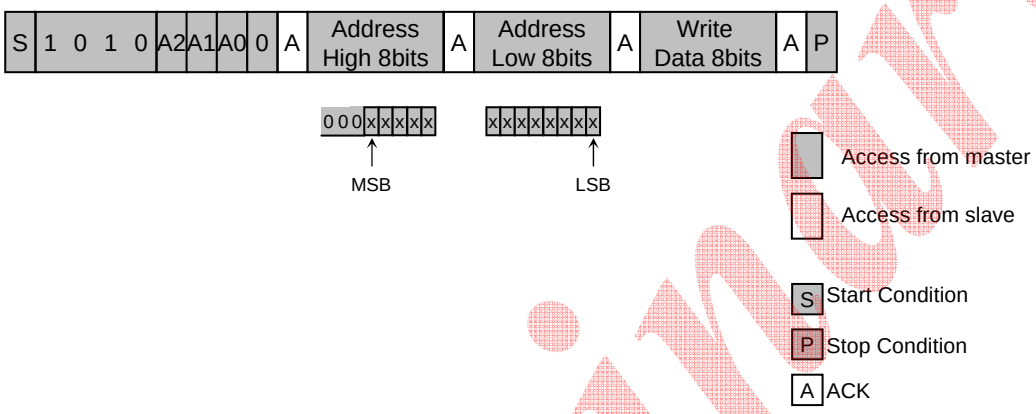
The memory array can be write protected using the WP pin. When the WP is set to ”H”, the entire memory map will be write protected. When the write protect pin is ”L”, all addresses may be overwritten. The WP pin is pulled down internally to VSS, therefore if the WP pin is open, the pin status is detected as Low (write enabled).

■ COMMAND

• Byte Write

If the 8th bit of the device address word (R/W)="L" is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by master, generating a stop condition at the end.

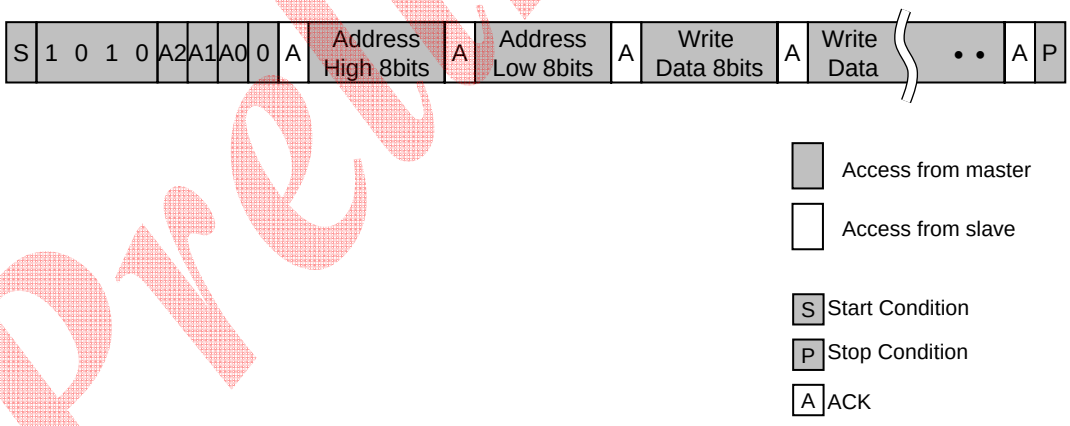
Note: In the MB85RC64, input 000 as the upper 3 bits of the High 8 bits.



• Page Write

If additional 8bits are sent after the same command as Byte Write, a page write is performed. If more bytes are sent than will fit up to the end of the address, the address rolls over to 0000h. Therefore, if more than 8KBytes are sent, the data is overwritten in order starting from the start of the FRAM memory address that was written first. Because FRAM performs write operations at bus speed, the data will be written to FRAM after the ACK response finishes immediately*.

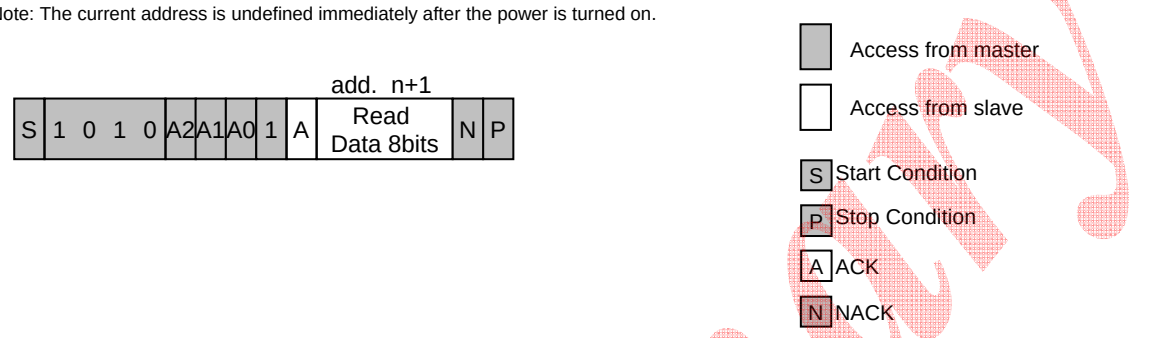
*: It is not necessary to take a period for internal write programming cycles from the buffer to the memory after the stop condition is generated.



• Current Address Read

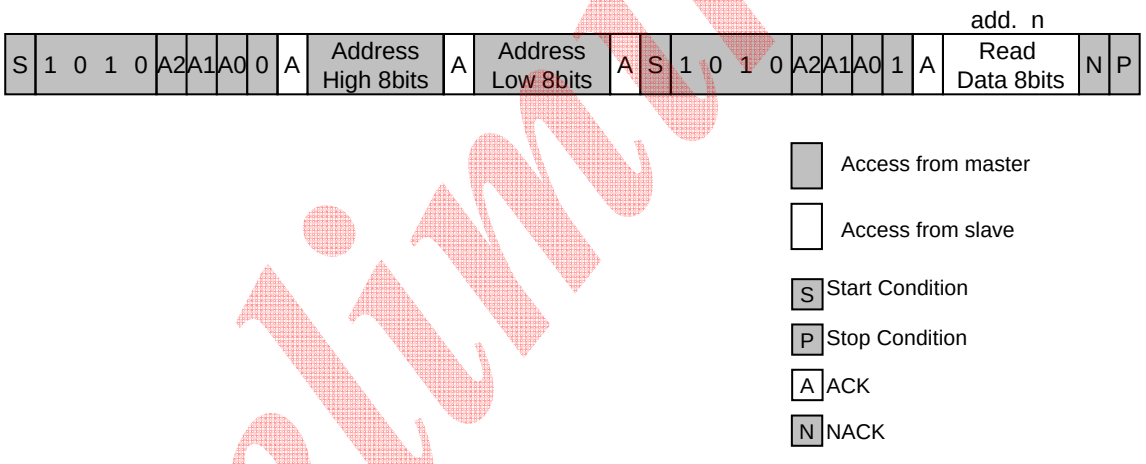
When the previous write or read operation finishes successfully up to the stop command and if the last accessed address is taken to be ‘n’, then the address at ‘n+1’ is read by sending the following command unless turning the power off. If the end of the address range is reached internally, the address counter will roll over to 0000h.

Note: The current address is undefined immediately after the power is turned on.



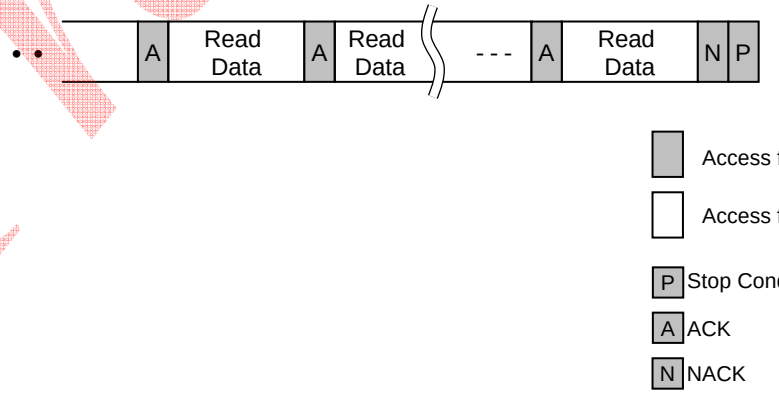
• Random Read

The one byte of data at the address as saved in the buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Control Byte (R/W)=1. The final NACK is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



• Sequential Read

Data can be received continuously following the control byte after specifying the address the same as for Random Read. If the read exceeds the maximum 8KBytes of the MB85RC64, the internal read address automatically rolls over to 0000h.



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage	V_{DD}	-0.5	+4.0	V
Input voltage	V_{IN}	-0.5	VDD + 0.5 (≤ 4.0)	V
Output voltage	V_{OUT}	-0.5	VDD + 0.5 (≤ 4.0)	V
Ambient temperature	T_A	-40	+85	°C
Storage temperature	Tstg	-40	+125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage	V_{DD}	2.7	3.3	3.6	V
”H” level input voltage	V_{IH}	0.8 ×VDD	-	V_{DD} + 0.5 (≤ 4.0)	V
”L” level input voltage	V_{IL}	-0.5	-	+0.6	V
Ambient temperature	T_A	-40	-	+85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	$\|I_{LI}\|$	V_{IN} = 0V to V_{DD}	-	-	1*	µA
Output leakage current	$\|I_{LO}\|$	V_{OUT} = 0V to V_{DD}	-	-	1	µA
Operating power supply current	I_{CC}	SCL = 400kHz	-	0.4	1	mA
Standby current	I_{SB}	SCL,SDA = V_{DD} A0,A1,A2 = V_{DD} or V_{SS}	-	10	50	µA
"L" level output voltage	V_{OL}	I_{OL}= 2mA	-	-	0.4	V

*: Pull-down pins WP, A0, A1, and A2 have a maximum input leakage of 50 µA

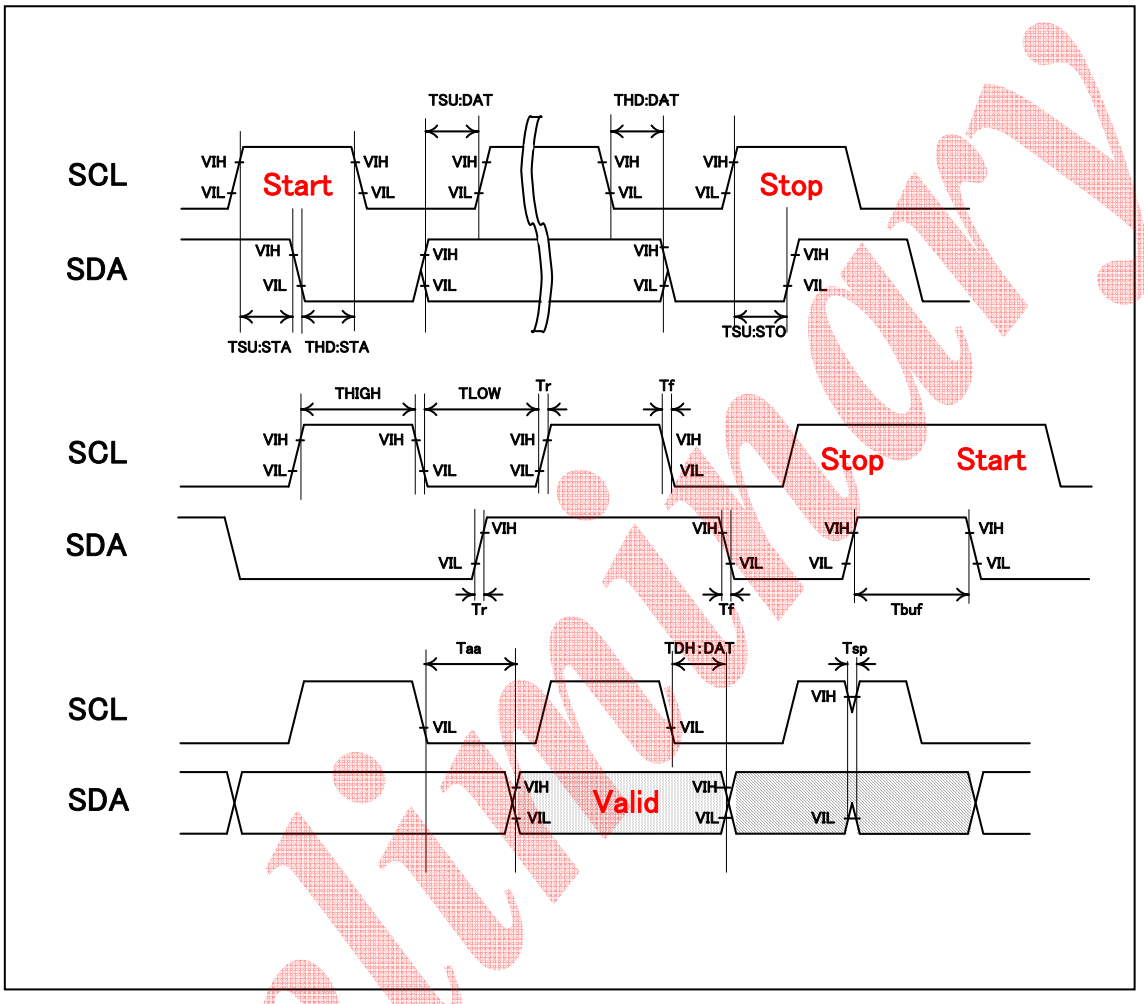
2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCL clock frequency	FSCL	0	400	kHz
Clock high time	T_{HIGH}	600	-	ns
Clock low time	T_{LOW}	1300	-	ns
SCL/SDA rise time	T_r	-	300	ns
SCL/SDA fall time	T_f	-	300	ns
Start condition hold	$T_{HD:STA}$	600	-	ns
Start condition setup	$T_{SU:STA}$	600	-	ns
SDA input hold	$T_{HD:DAT}$	0	-	ns
SDA input setup	$T_{SU:DAT}$	100	-	ns
SDA output hold	$T_{DH:DAT}$	0	-	ns
Stop condition setup	$T_{SU:STO}$	600	-	ns
SDA output access after SCL fall	T_{aa}	-	900	ns
Pre-charge time	T_{buf}	1300	-	ns
Pulse width ignored (Input Filter on SCL and SDA)	T_{SP}	-	50	ns

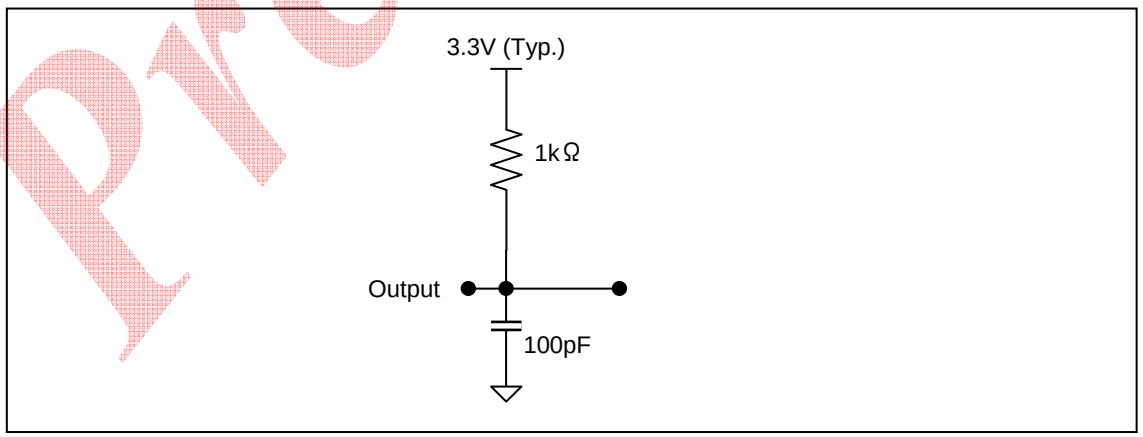
AC characteristics were measured under the following measurement conditions.

Power supply voltage : 2.7 V to 3.6 V
Operating temperature : -40°C to +85°C
Input voltage magnitude : 0.3 V to 2.7 V
Input rise time : 5 ns
Input fall time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

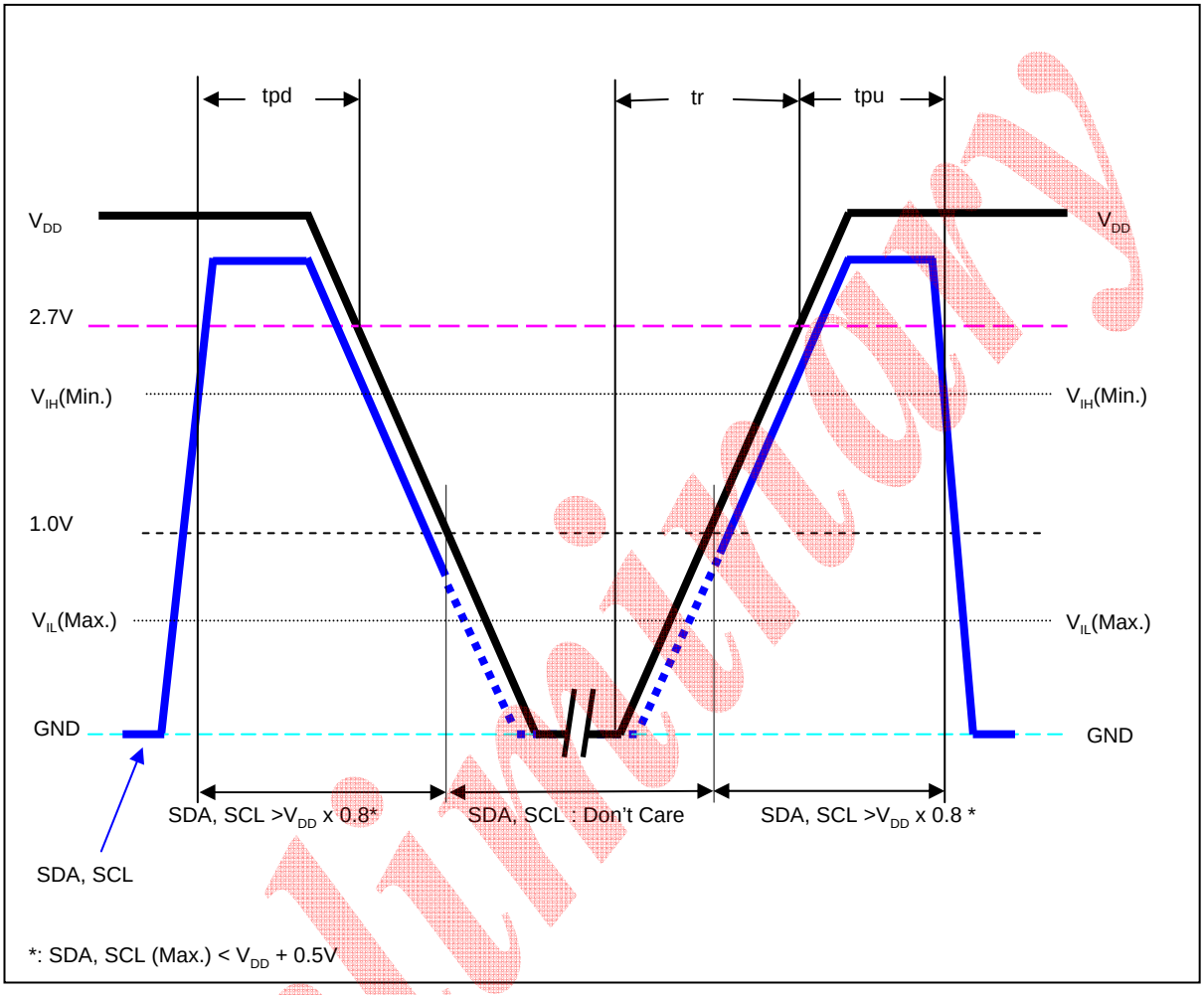
3. AC Timing Definitions



4. AC Test Load Circuit



■ POWER ON/OFF SEQUENCE

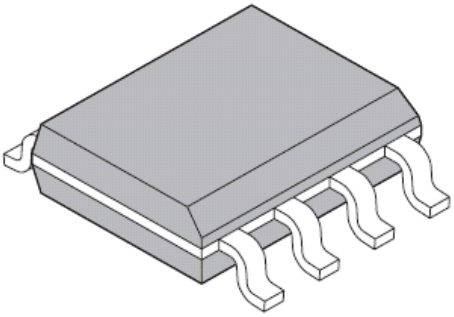


Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	-	ns
SDA, SCL level hold time during power up	tpu	85	-	ns
Power supply rise time	tr	10	-	µs

■ NOTES ON USE

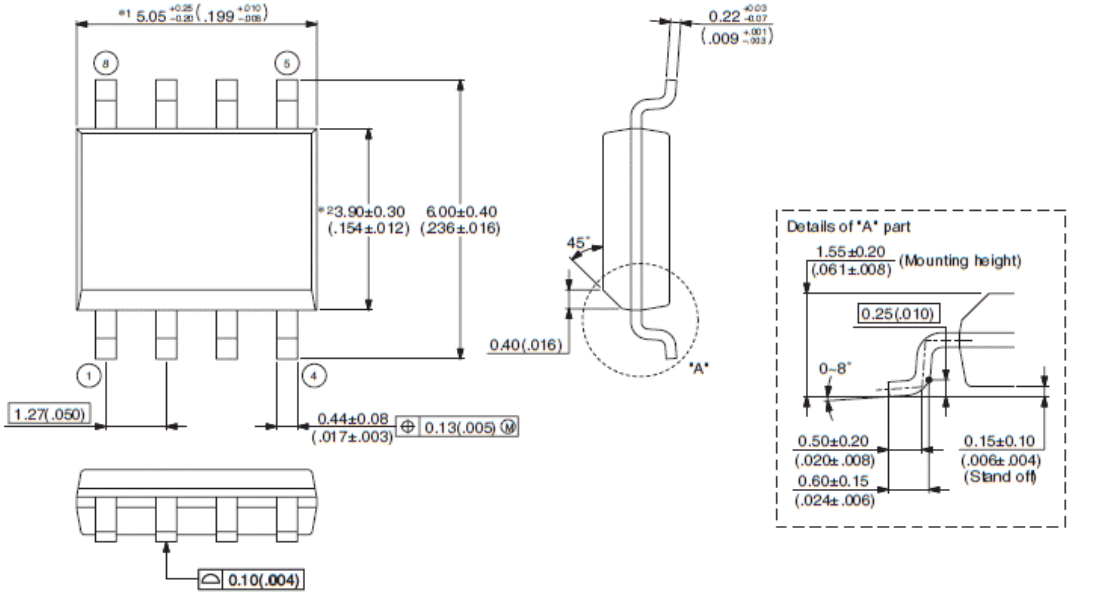
Data written before performing IR reflow is not guaranteed.
VDD is required to be rising from 0V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.
During the access period from the start condition to the stop condition, keep the level of WP, A0, A1, and A2 pins to "H" or "L".

■ PACKAGE DIMENSION

8-pin plastic SOP		
 (FPT-8P-M02)	Lead pitch	1.27 mm
	Package width × package length	3.9 × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP
(FPT-8P-M02)

Note 1) *1 : These dimensions include resin protrusion.
Note 2) *2 : These dimensions do not include resin protrusion.
Note 3) Pins width and pins thickness include plating thickness.
Note 4) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

MEMO

MEMO

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