


# CAN TRANSCEIVER

## FEATURES

- **Drop-In Improved Replacement for the PCA82C250 and PCA82C251**
- **Bus-Fault Protection of ±36 V**
- **Meets or Exceeds ISO 11898**
- **Signaling Rates(1) up to 1 Mbps**
- **High Input Impedance Allows up to 120 SN65HVD251 Nodes on a Bus**
- **Bus Pin ESD Protection Exceeds 14 kV HBM**
- **Unpowered Node Does Not Disturb the Bus**
- **Low Current Standby Mode . . . 200 µA Typical**
- **Thermal Shutdown Protection**
- **Glitch-Free Power-Up and Power-Down Bus Protection For Hot-Plugging**
- **DeviceNet Vendor ID # 806**

## APPLICATIONS

- **CAN Data Buses**
- **Industrial Automation**
  - **DeviceNet™ Data Buses**
  - **Smart Distributed Systems (SDS™)**
- **SAE J1939 Standard Data Bus Interface**
- **NMEA 2000 Standard Data Bus Interface**
- **ISO 11783 Standard Data Bus Interface**

## DESCRIPTION

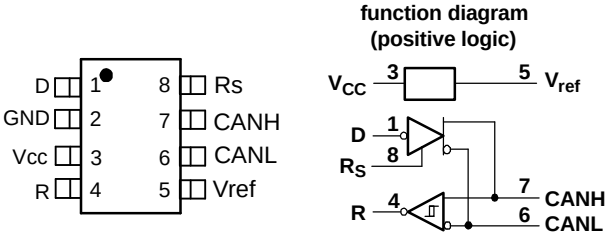
The SN65HVD251 is intended for use in applications employing the Controller Area Network (CAN) serial communication physical layer in accordance with the ISO 11898 Standard. The SN65HVD251 provides differential transmit capability to the bus and differential receive capability to a CAN controller at speeds up to 1 megabits per second (Mbps).

Designed for operation in harsh environments, the device features cross-wire, over-voltage and loss of ground protection to ±36 V. Also featured are over-temperature protection as well as -7 V to 12 V common-mode range, and tolerance to transients of ± 200 V. The transceiver interfaces the single-ended CAN controller with the differential CAN bus found in industrial, building automation, and automotive applications.

Rs, pin 8, provides for three different modes of operation: high-speed, slope control, or low-power mode. The high-speed mode of operation is selected by connecting pin 8 to ground, allowing the transmitter output transistors to switch as fast as possible with no limitation on the rise and fall slope. The rise and fall slope can be adjusted by connecting a resistor to ground at pin 8; the slope is proportional to the pin's output current. Slope control with an external resistor value of 10 kΩ gives ~ 15 V/us slew rate; 100 kΩ gives ~ 2 V/us slew rate.

If a high logic level is applied to the Rs pin 8, the device enters a low-current standby mode during which the driver is switched off and the receiver remains active . The local protocol controller reverses this low-current standby mode when it needs to transmit to the bus.

The SN65HVD251 may be used in CAN, DeviceNet™ or SDS™ applications with the Texas Instruments' TMS320F241 and TMS320F243 DSPs with CAN 2.0B controllers.




## (1)ORDERING INFORMATION

| PART NUMBER | PACKAGE | MARKED AS |
|---|---|---|
| SN65HVD251D | 8-pin SOIC (Tube) | VP251 |
| SN65HVD251DR | 8-pin SOIC (Tape & Reel) | VP251 |
| SN65HVD251P | 8-pin DIP | 65HVD251 |

(1) (1)The signaling rate of a line is the number of voltage transitions that are made per second expressed in the units bps (bits per second).

## ABSOLUTE MAXIMUM RATINGS(1),(2)

| | | | SN65HVD251 |
|---|---|---|---|
| Supply voltage range, $V_{CC}$ | | | -0.3 V to 7V |
| Voltage range at any bus terminal (CANH or CANL) | | | -36 V to 36 V |
| Transient voltage per ISO 7637, pulse 1, 2, 3a, 3b | | CANH, CANL | ±200 V |
| Input voltage range, $V_I$ (D, Rs, or R) | | | -0.3 V to $V_{CC}$ + 0.5 |
| Electrostatic discharge | Human Body Model (3) | CANH, CANL and GND | 14 kV |
| | | All pins | 6 kV |
| | Charged-Device Model (4) | All pins | 1 kV |
| Continuous total power dissipation | | | (see Dissipation Rating Table) |
| Storage temperature range, $T_{stg}$ | | | -65C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | | 260°C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

## ABSOLUTE MAXIMUM POWER DISSIPATION RATINGS

| PACKAGE | CIRCUIT BOARD MODEL | $T_A$ = 25°C POWER RATING | DERATING FACTOR (1) ABOVE $T_A$ = 25°C | $T_A$ = 85°C POWER RATING | $T_A$ = 125°C POWER RATING |
|---|---|---|---|---|---|
| SOIC (D) | Low-K(2) | 600 mW | 4.4 mW/°C | 312 mW | 120 mW |
| | High-K(3) | 963 mW | 7.7 mW/°C | 501 mW | 193 mW |
| PDIP (P) | Low-K(2) | 984 mW | 7.8 mW/°C | 512 mW | 197 mW |
| | High-K(3) | 1344 mW | 10.8 mW/°C | 699 mW | 269 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-3.
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-7.

## THERMAL CHARACTERISTICS

| PARAMETER | | TEST CONDITIONS | | VALUE MIN | VALUE TYP | VALUE MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $\Theta_{JB}$ | Junction-to-board thermal resistance | | D | | 78.7 | | °C/W |
| | | | P | | 56.5 | | |

## THERMAL CHARACTERISTICS (continued)

| PARAMETER | | TEST CONDITIONS | | VALUE | | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | |
| $\Theta_{JC}$ | Junction-to-board thermal resistance | | D | | 44.6 | | °C/W |
| | | | P | | 54.5 | | |
| $P_D$ | Device power dissipation | $V_{CC}$ = 5 V, Tj = 27 °C, RL = 60Ω, $R_S$ at 0 V, Input to D a 500-kHz 50% duty cycle square wave | | | | 97.7 | mW |
| | | $V_{CC}$ = 5.5 V, Tj = 130°C, RL = 60Ω, $R_S$ at 0 V, Input to D a 500-kHz 50% duty cycle square wave | | | | 142 | mW |
| $T_{SD}$ | Thermal shutdown junction temperature | | | | 165 | | °C |

## RECOMMENDED OPERATING CONDITIONS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.5 | | 5.5 | V |
| Voltage at any bus terminal (separately or common mode) $V_I$ or $V_{IC}$ | | -7(1) | | 12 | V |
| High-level input voltage, $V_{IH}$ | D input | 0.7 $V_{CC}$ | | | V |
| Low-level input voltage, $V_{IL}$ | D input | | | 0.3 $V_{CC}$ | V |
| Differential input voltage, $V_{ID}$ | | -6 | | 6 | V |
| Input voltage to Rs, $V_{I(Rs)}$ | | 0 | | $V_{CC}$ | V |
| Input voltage at Rs for standby, $V_{I(Rs)}$ | | 0.75 $V_{CC}$ | | $V_{CC}$ | V |
| Rs wave-shaping resistance | | 0 | | 100 | kΩ |
| High-level output current, $I_{OH}$ | Driver | -50 | | | mA |
| | Receiver | -4 | | | |
| Low-level output current, $I_{OL}$ | Driver | | | 50 | mA |
| | Receiver | | | 4 | |
| Operating free-air temperature, $T_A$ | | -40 | | 125 | °C |
| Junction temperature, $T_j$ | PDIP Package | | | 145 | °C |
| | SOIC Package | | | 150 | |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

## DRIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{O(D)}$ | Bus output voltage (Dominant) | CANH | Figure 1 & Figure 2 , D at 0 V Rs at 0 V | 2.75 | 3.5 | 4.5 | V |
| | | CANL | | 0.5 | | 2 | |
| $V_{O(R)}$ | Bus output voltage (Recessive) | CANH | Figure 1 & Figure 2 , D at 0.7$V_{CC}$ , Rs at 0 V | 2 | 2.5 | 3 | |
| | | CANL | | 2 | 2.5 | 3 | |
| $V_{OD(D)}$ | Differential output voltage (Dominant) | | Figure 1 , D at 0 V, Rs at 0 V | 1.5 | 2 | 3 | V |
| $V_{OD(D)}$ | Differential output voltage (Dominant) | | Figure 2 & Figure 3 , D at 0 V, Rs at 0 V | 1.2 | 2 | 3.1 | V |
| $V_{OD(R)}$ | Differential output voltage (Recessive) | | Figure 1 & Figure 2 , D at 0.7 $V_{CC}$ | -120 | | 12 | mV |
| $V_{OD(R)}$ | Differential output voltage (Recessive) | | D at 0.7 $V_{CC}$, no load | -0.5 | | 0.05 | V |
| $V_{OC(pp)}$ | Peak-to-peak common-mode output voltage | | Figure 9, Rs at 0 V | | 600 | | mV |
| $I_{IH}$ | High-level input current, D Input | | D at 0.7 $V_{CC}$ | -40 | | 0 | µA |
| $I_{IL}$ | Low-level input current, D Input | | D at 0.3 $V_{CC}$ | -60 | | 0 | µA |

(1) All typical values are at 25°C and with a 5-V supply.

## DRIVER ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{OS(SS)}$ | Short-circuit steady-state output current | | Figure 11, $V_{CANH}$ at -7 V, CANL Open | -200 | | | mA |
| | | | Figure 11, $V_{CANH}$ at 12 V, CANL Open | | | 2.5 | |
| | | | Figure 11, $V_{CANL}$ at -7 V, CANH Open | -2 | | | |
| | | | Figure 11, $V_{CANL}$ at 12 V, CANH Open | | | 200 | |
| $C_O$ | Output capacitance | | See receiver input capacitance | | | | |
| $I_{OZ}$ | High-impedance output current | | See receiver input current | | | | |
| $I_{IRs(s)}$ | Rs input current for standby | | Rs at 0.75 $V_{CC}$ | -10 | | | µA |
| $I_{IRs(f)}$ | Rs input current for full speed operation | | Rs at 0 V | -550 | | 0 | µA |
| $I_{CC}$ | Supply current | Standby | Rs at $V_{CC}$, D at $V_{CC}$ | | | 275 | µA |
| | | Dominant | D at 0 V, 60Ω load, Rs at 0 V | | | 65 | mA |
| | | Recessive | D at $V_{CC}$, no load, Rs at 0 V | | | 14 | |

## DRIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pLH}$ | Propagation delay time, low-to-high-level output | Figure 4, Rs at 0 V | | 40 | 70 | ns |
| | | Figure 4, Rs with 10 kΩ to ground | | 90 | 125 | |
| | | Figure 4, Rs with 100 kΩ to ground | | 500 | 800 | |
| $t_{pHL}$ | Propagation delay time, high-to-low-level output | Figure 4, Rs at 0 V | | 85 | 125 | |
| | | Figure 4, Rs with 10 kΩ to ground | | 200 | 260 | |
| | | Figure 4, Rs with 100 kΩ to ground | | 1150 | 1450 | |
| $t_{sk(p)}$ | Pulse skew ($\lvert t_{pHL} - t_{pLH} \rvert$) | Figure 4, Rs at 0 V | | 45 | 85 | |
| | | Figure 4, Rs with 10 kΩ to ground | | 110 | 180 | |
| | | Figure 4, Rs with 100 kΩ to ground | | 650 | 900 | |
| $t_r$ | Differential output signal rise time | Figure 4, Rs at 0 V | 35 | | 100 | |
| $t_f$ | Differential output signal fall time | | 35 | | 100 | |
| $t_r$ | Differential output signal rise time | Figure 4, Rs with 10 kΩ to ground | 100 | | 250 | |
| $t_f$ | Differential output signal fall time | | 100 | | 250 | |
| $t_r$ | Differential output signal rise time | Figure 4, Rs with 100 kΩ to ground | 600 | | 1550 | |
| $t_f$ | Differential output signal fall time | | 600 | | 1550 | |
| $t_{en}$ | Enable time from standby to dominant | Figure 8 | | | 0.5 | µs |

## RECEIVER ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going input threshold voltage | Rs at 0 V, (See Table 1) | | 750 | 900 | mV |
| $V_{IT-}$ | Negative-going input threshold voltage | | 500 | 650 | | |
| $V_{hys}$ | Hysteresis voltage ($V_{IT+}$ - $V_{IT-}$) | | | 100 | | |
| $V_{OH}$ | High-level output voltage | Figure 6, $I_O$ = -4mA | 0.8 Vcc | | | V |
| $V_{OL}$ | Low-level output voltage | Figure 6, $I_O$ = 4mA | | | 0.2 Vcc | V |

## RECEIVER ELECTRICAL CHARACTERISTICS (continued)

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_I$ | Bus input current | | CANH or CANL at 12 V | Other bus pin at 0 V, Rs at 0 V, D at 0.7 $V_{CC}$ | | | 600 | µA |
| | | | CANH or CANL at 12 V, $V_{CC}$ at 0 V | | | | 715 | |
| | | | CANH or CANL at -7 V | | -460 | | | |
| | | | CANH or CANL at -7 V, $V_{CC}$ at 0 V | | -340 | | | |
| $C_I$ | Input capacitance, (CANH or CANL) | | Pin-to-ground, $V_I$ = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 $V_{CC}$ | | | 20 | | pF |
| $C_{ID}$ | Differential input capacitance | | Pin-to-pin, $V_I$ = 0.4 sin (4E6πt) + 0.5 V, D at 0.7 $V_{CC}$ | | | 10 | | pF |
| $R_{ID}$ | Differential input resistance | | D at 0.7 $V_{CC}$, Rs at 0 V | | 40 | | 100 | kΩ |
| $R_{IN}$ | Input resistance, (CANH or CANL) | | D at 0.7 $V_{CC}$, Rs at 0 V | | 20 | | 50 | kΩ |
| $I_{CC}$ | Supply current | Standby | Rs at $V_{CC}$, D at $V_{CC}$ | | | | 275 | µA |
| | | Dominant | D at 0 V, 60Ω Load, Rs at 0 V | | | | 65 | mA |
| | | Recessive | D at $V_{CC}$, No Load, Rs at 0 V | | | | 14 | |

## RECEIVER SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{pLH}$ | Propagation delay time, low-to-high-level output | Figure 6 | | 35 | 50 | ns |
| $t_{pHL}$ | Propagation delay time, high-to-low-level output | | | 35 | 50 | |
| $t_{sk(p)}$ | Pulse skew ($\|t_{pHL} - t_{pLH}\|$) | | | | 20 | |
| $t_r$ | Output signal rise time | | | 2 | 4 | |
| $t_f$ | Output signal fall time | | | 2 | 4 | |
| $t_{p(sb)}$ | Propagation delay time in standby | Figure 12, Rs at $V_{CC}$ | | | 500 | |

## VREF-PIN CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_O$ | Reference output voltage | -5 µA < $I_O$ < 5 µA | 0.45 $V_{CC}$ | | 0.55 $V_{CC}$ | V |
| | | -50 µA < $I_O$ < 50 µA | 0.4 $V_{CC}$ | | 0.6 $V_{CC}$ | |

## DEVICE SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{loop1}$ | Total loop delay, driver input to receiver output, recessive to dominant | Figure 10, Rs at 0 V | | 60 | 100 | ns |
| | | Figure 10, Rs with 10 kΩ to ground | | 100 | 150 | |
| | | Figure 10, Rs with 100 kΩ to ground | | 440 | 800 | |
| $t_{loop2}$ | Total loop delay, driver input to receiver output, dominant to recessive | Figure 10, Rs at 0 V | | 115 | 150 | ns |
| | | Figure 10, Rs with 10 kΩ to ground | | 235 | 290 | |
| | | Figure 10, Rs with 100 kΩ to ground | | 1070 | 1450 | |
| $t_{loop2}$ | Total loop delay, driver input to receiver output, dominant to recessive | Figure 10, Rs at 0 V, $V_{CC}$ from 4.5 V to 5.1 V, | | 105 | 145 | ns |

## PARAMETER MEASUREMENT INFORMATION

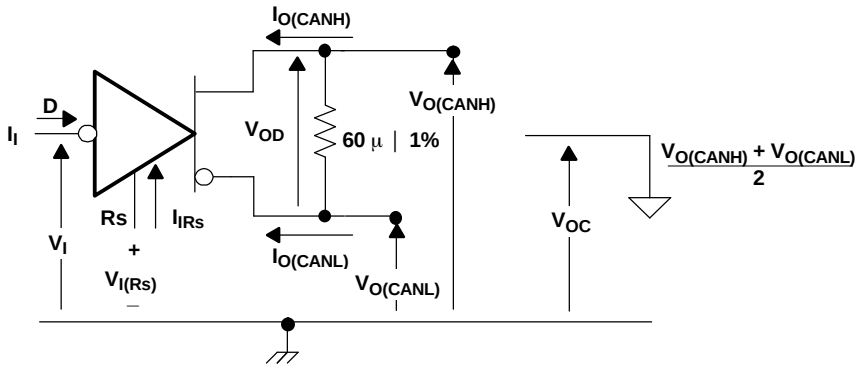



**Figure 1. Driver Voltage, Current, and Test Definition**

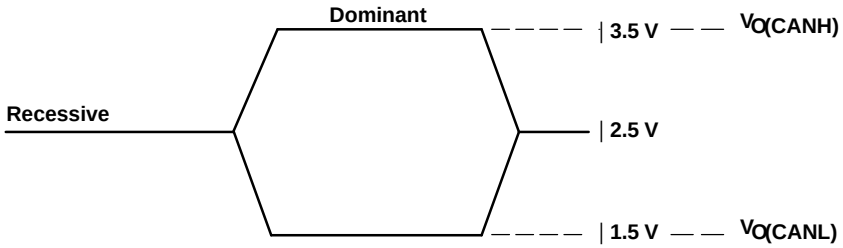



**Figure 2. Bus Logic State Voltage Definitions**

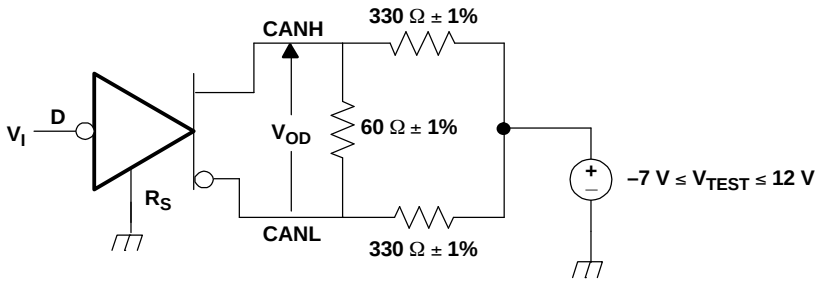



**Figure 3. Driver $V_{OD}$**

## PARAMETER MEASUREMENT INFORMATION (continued)

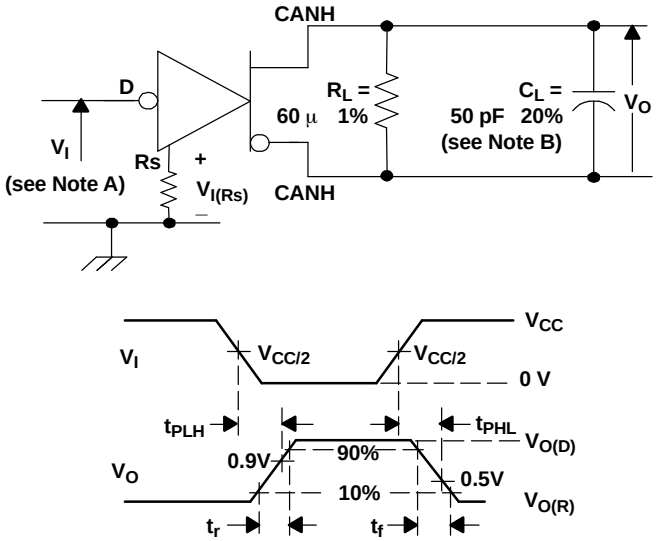



**Figure 4. Driver Test Circuit and Voltage Waveforms**

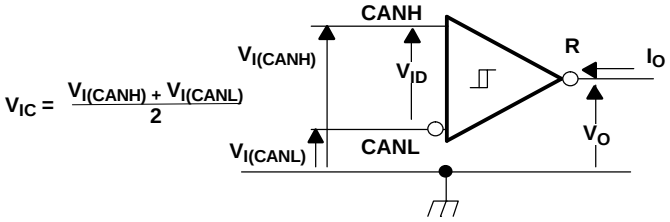
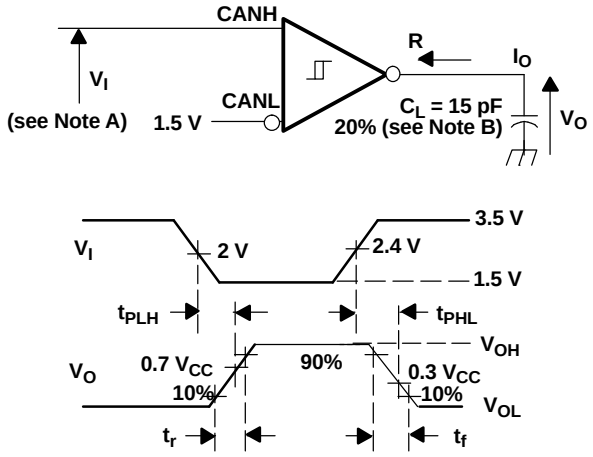



**Figure 5. Receiver Voltage and Current Definitions**

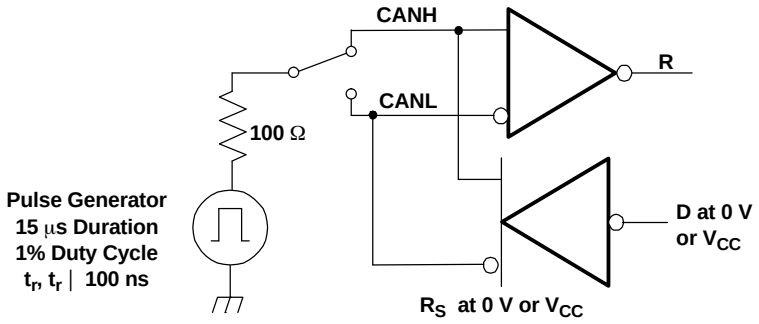



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r$≤ 6ns, $t_f$≤ 6ns, $Z_O$ = 50Ω.

B. $C_L$ includes instrumentation and fixture capacitance within ±20%.

**Figure 6. Receiver Test Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION (continued)




A. This test is conducted to test survivability only. Data stability at the R output is not specified.

**Figure 7. Test Circuit, Transient Over-Voltage Test**

**Table 1. Receiver Characteristics Over Common Mode Voltage**

| INPUT | | MEASURED | OUTPUT | |
|---|---|---|---|---|
| $V_{CANH}$ | $V_{CANL}$ | $\lvert V_{ID}\rvert$ | R | |
| 12 V | 11.1 V | 900 mV | L | $V_{OL}$ |
| -6.1 V | -7 V | 900 mV | L | |
| -1 V | -7 V | 6 V | L | |
| 12 V | 6 V | 6 V | L | |
| -6.5 V | -7 V | 500 mV | H | $V_{OH}$ |
| 12 V | 11.5 V | 500 mV | H | |
| -7 V | -1 V | 6 V | H | |
| 6 V | 12 V | 6 V | H | |
| open | open | X | H | |

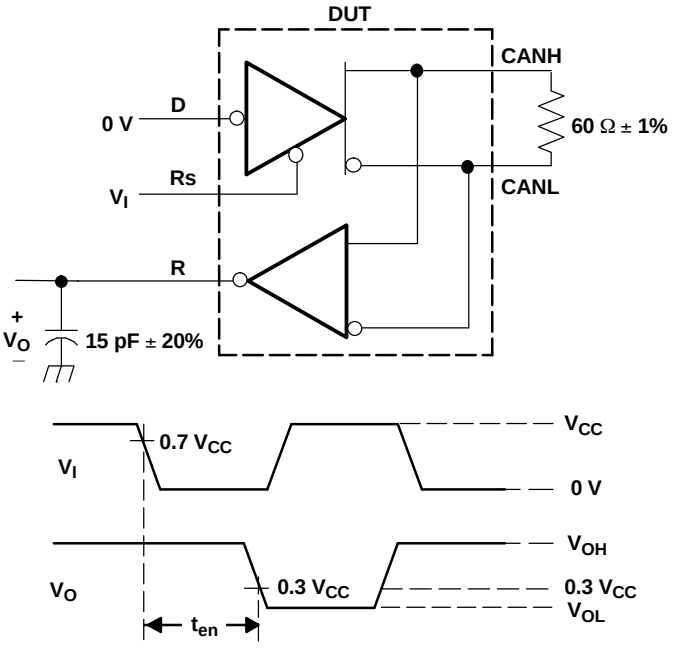
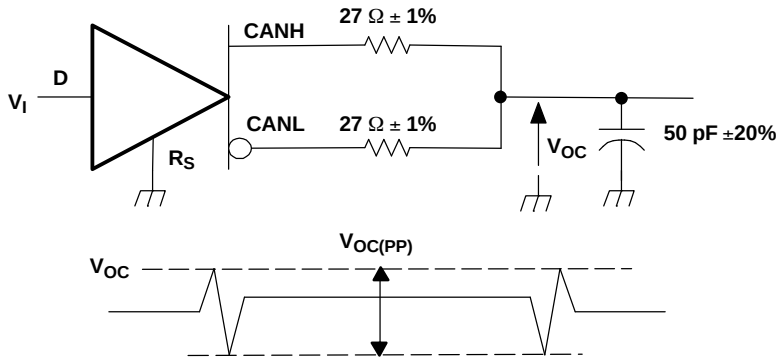



**Figure 8. $t_{en}$ Test Circuit and Voltage Waveforms**




A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r$≤ 6ns, $t_f$≤ 6ns, $Z_O$ = 50Ω.

**Figure 9. Peak-to-Peak Common Mode Output Voltage**

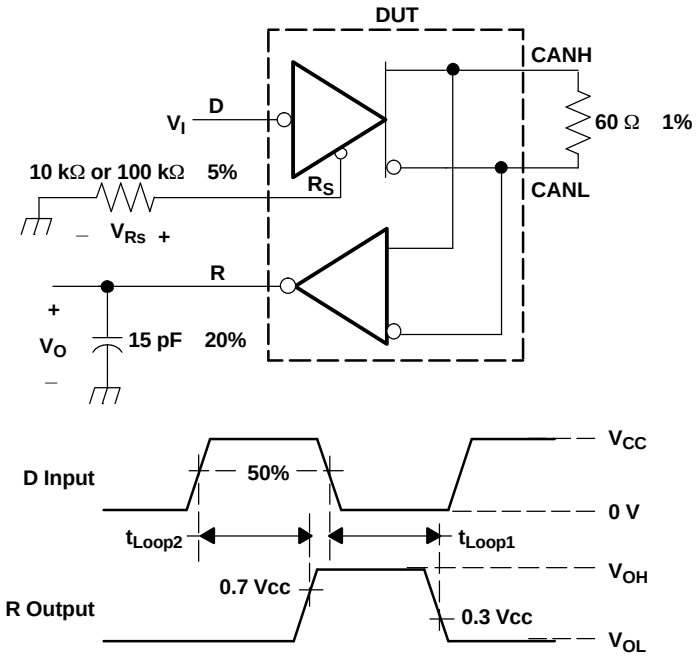



**Figure 10. $t_{LOOP}$ Test Circuit and Voltage Waveforms**

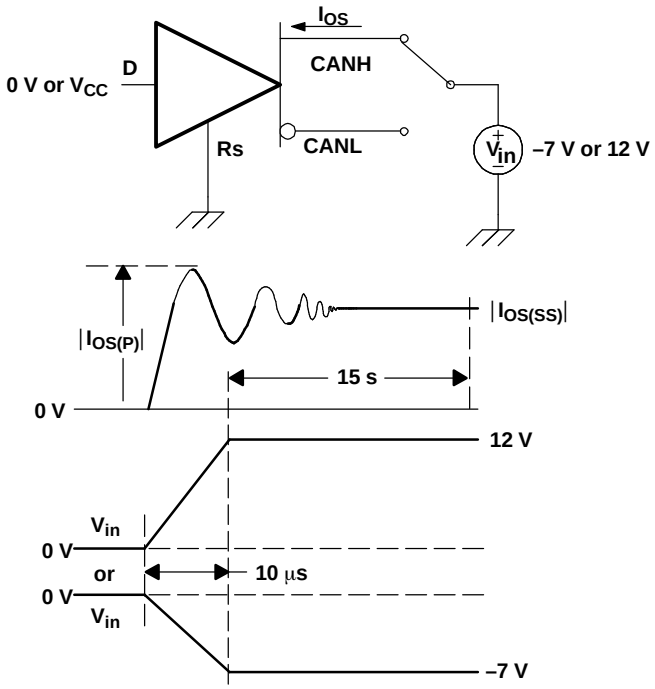
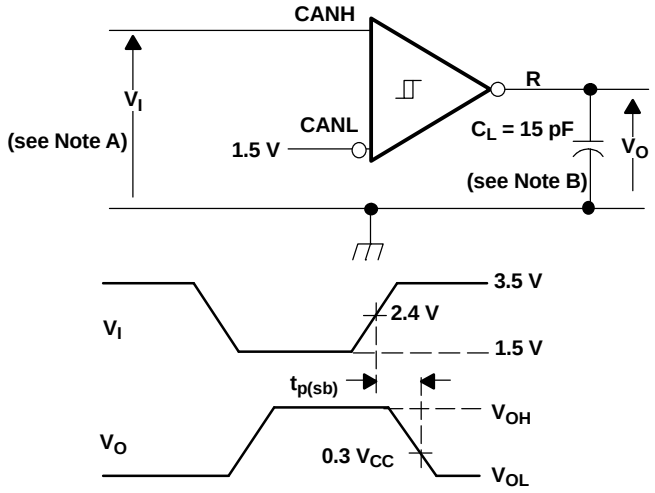



**Figure 11. Driver Short-Circuit Test**

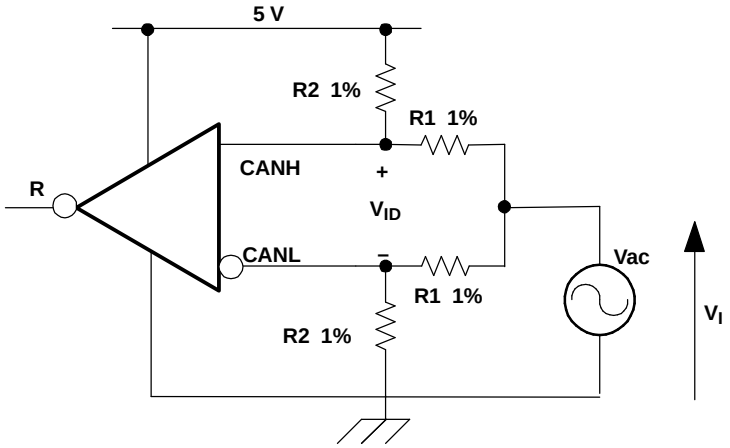



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 125 kHz, 50% duty cycle, $t_r$≤ 6ns, $t_f$≤ 6ns, $Z_O$ = 50Ω.

B. CL includes instrumentation and fixture capacitance within ±20%.

**Figure 12. Receiver Propagation Delay in Standby Test Circuit and Waveform**

## DEVICE INFORMATION




| $V_{ID}$ | R1 | R2 |
|---|---|---|
| 500 mV | 50 Ω | 450 Ω |
| 900 mV | 50 Ω | 227 Ω |


A. All input pulses are supplied by a generator having the following characteristics: f < 1.5 MHz, $T_A$ = 25°C, $V_{CC}$ = 5.0 V.

**Figure 13. Common-Mode Input Voltage Rejection Test**

## FUNCTION TABLES

**Table 2. DRIVER**

| INPUTS | Voltage at $R_S$, $V_{Rs}$ | OUTPUTS | | BUS STATE |
|---|---|---|---|---|
| D | | CANH | CANL | |
| L | $V_{Rs}$ < 1.2 V | H | L | Dominant |
| H | $V_{Rs}$ < 1.2 V | Z | Z | Recessive |
| Open | X | Z | Z | Recessive |
| X | $V_{Rs}$ > 0.75 $V_{CC}$ | Z | Z | Recessive |

**Table 3. RECEIVER**

| DIFFERENTIAL INPUTS [$V_{ID}$ = V(CANH) - V(CANL)] | OUTPUT R(1) |
|---|---|
| $V_{ID}$≥ 0.9 V | L |
| 0.5V < $V_{ID}$ < 0.9 V | ? |
| $V_{ID}$ ≤ 0.5 V | H |
| Open | H |

(1) H = high level; L = low level; X = irrelevant; ? = indeterminate; Z = high impedance

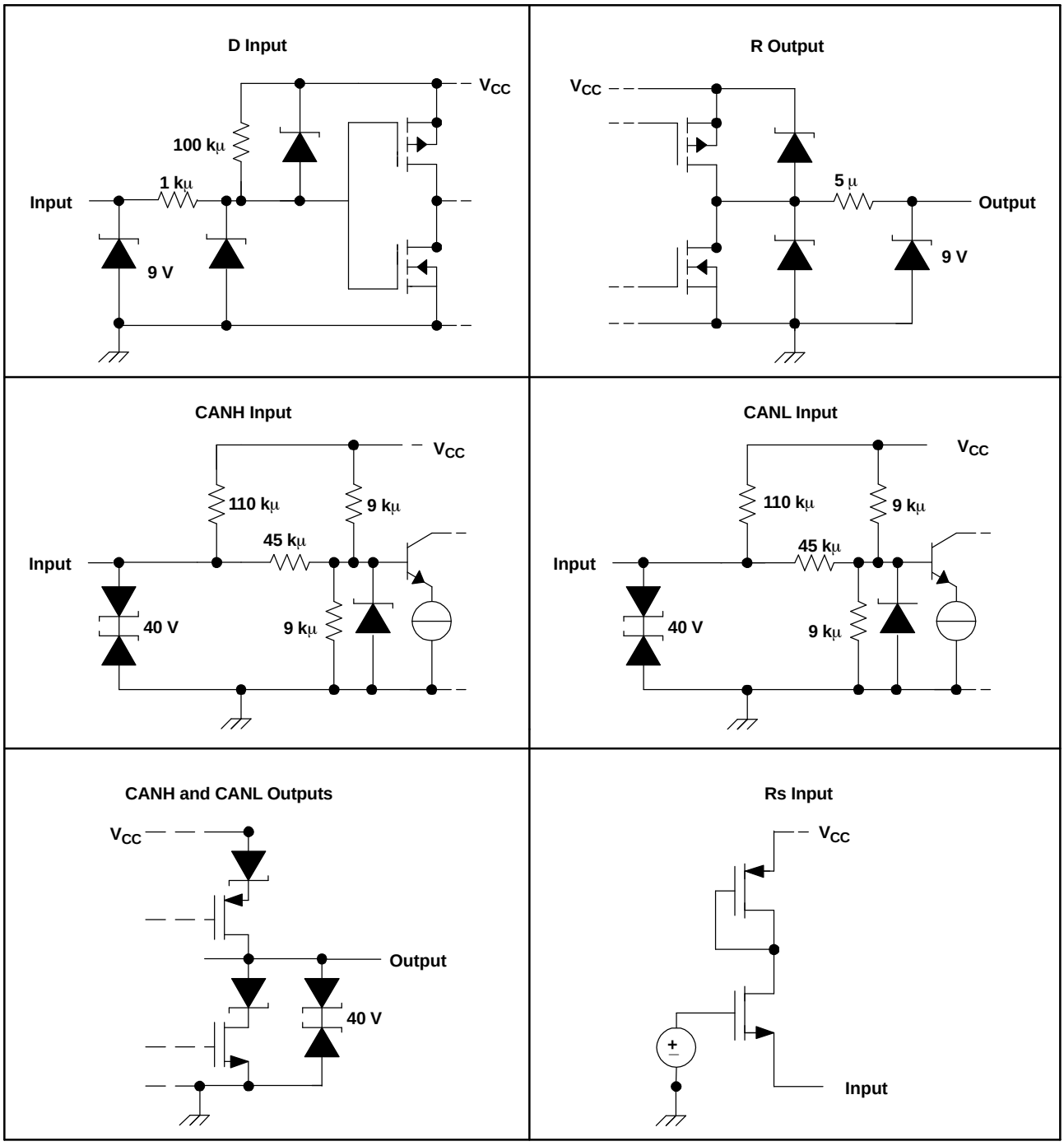



**Figure 14. Equivalent Input and Output Schematic Diagrams**

## TYPICAL CHARACTERISTICS

**tLOOP1-LOOP TIME vs FREE-AIR TEMPERATURE**

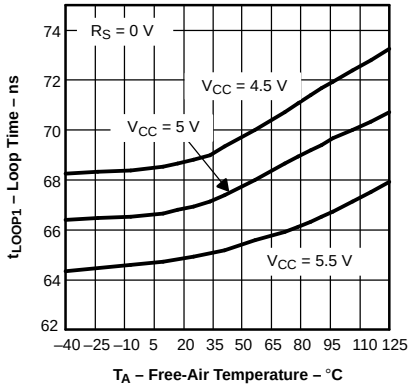



**Figure 15.**

**tLOOP2-LOOP TIME vs FREE-AIR TEMPERATURE**

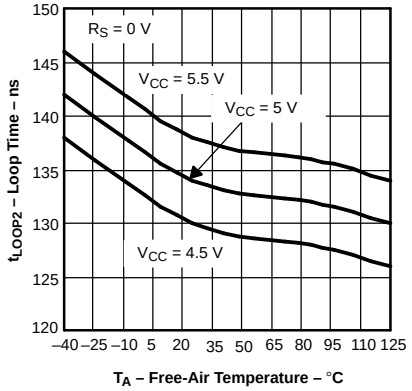



**Figure 16.**

**SUPPLY CURRENT (RMS) vs SIGNALING RATE**

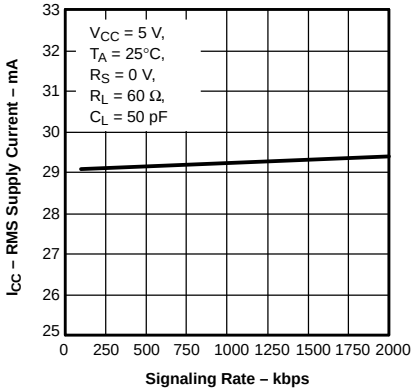



**Figure 17.**

**DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE**

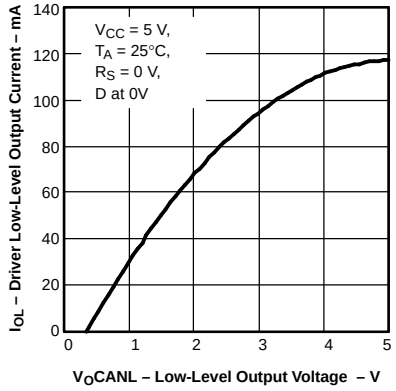



**Figure 18.**

**DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE**

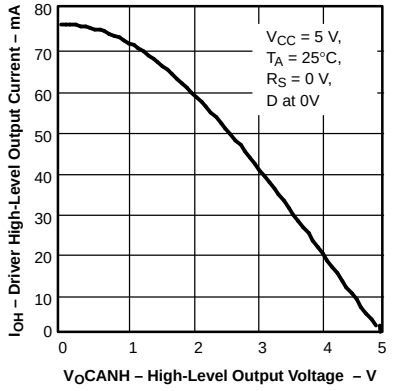



**Figure 19.**

**DOMINANT DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

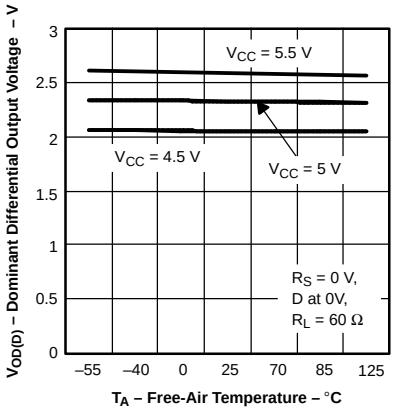



**Figure 20.**

**DRIVER OUTPUT CURRENT vs SUPPLY VOLTAGE**

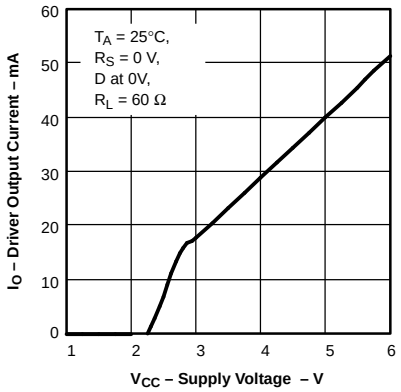



**Figure 21.**

**DIFFERENTIAL OUTPUT FALL TIME vs SLOPE RESISTANCE (Rs)**

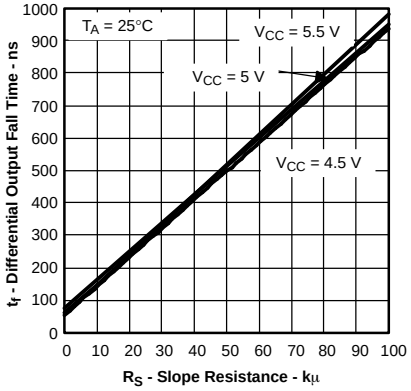



**Figure 22.**

**INPUT RESISTANCE MATCHING vs FREE-AIR TEMPERATURE**

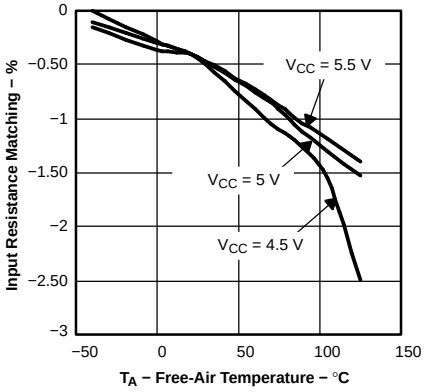



**Figure 23.**

## APPLICATION INFORMATION

The basics of arbitration require that the receiver at the sending node designate the first bit as dominant or recessive after the initial wave of the first bit of a message travels to the most remote node on a network and back again. Typically, this *sample* is made at 75% of the bit width, and within this limitation, the maximum allowable signal distortion in a CAN network is determined by network electrical parameters.

Factors to be considered in network design include the ≈ 5 ns/m propagation delay of typical twisted-pair bus cable; signal amplitude loss due to the loss mechanisms of the cable; and the number, length, and spacing of drop-lines (stubs) on a network. Under strict analysis, variations among the different oscillators in a system also need to be accounted for with adjustments in signaling rate and stub & bus length. Table 2 lists the maximum signaling rates achieved with the SN65HVD251 in high-speed mode with several bus lengths of category 5, shielded twisted pair (CAT 5 STP) cable.

**Table 4. Maximum Signaling Rates for Various Cable Lengths**

| BUS LENGTH (m) | SIGNALING RATE (kbps) |
|---|---|
| 30 | 1000 |
| 100 | 500 |
| 250 | 250 |
| 500 | 125 |
| 1000 | 62.5 |

The ISO 11898 Standard specifies a maximum bus length of 40 m and maximum stub length of 0.3 m with a maximum of 30 nodes. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes on a bus. (Note: Non-standard application may come with a trade-off in signaling rate.) A large number of nodes requires a transceiver with high input impedance such as the HVD251.

The Standard specifies the interconnect to be a single twisted-pair cable (shielded or unshielded) with 120Ω characteristic impedance (Zo). Resistors equal to the characteristic impedance of the line terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines connect nodes to the bus and should be kept as short as possible to minimize signal reflections.

Connectors, while not specified by the Standard should have as little effect as possible on standard operating parameters such as capacitive loading. Although unshielded cable is used in many applications, data transmission circuits employing CAN transceivers are usually used in applications requiring a rugged interconnection with a wide common-mode voltage range. Therefore, shielded cable is recommended in these electronically harsh environments, and when coupled with the Standard's –2-V to 7-V common-mode range of tolerable ground noise, helps to ensure data integrity. The HVD251 enhances the Standard's insurance of data integrity with an extended –7-V to 12-V range of common-mode operation.

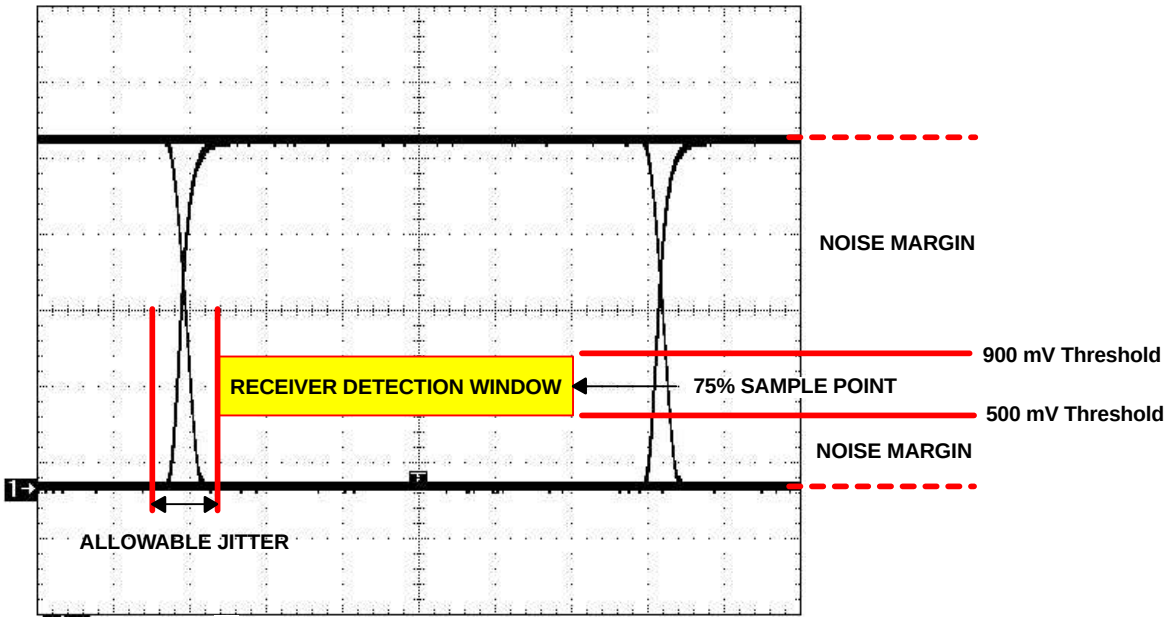



**Figure 24. Typical CAN Differential Signal Eye-Pattern**

An eye pattern is a useful tool for measuring overall signal quality. As displayed in Figure 24, the differential signal changes logic states in two places on the display, producing an *eye*. Instead of viewing only one logic crossing on the scope, an entire *bit* of data is brought into view. The resulting eye pattern includes all of the effects of systemic and random distortion, and displays the time during which a signal may be considered valid.

The height of the eye above or below the receiver threshold voltage level at the sampling point is the noise margin of the system. Jitter is typically measured at the differential voltage zero-crossing during the logic state transition of a signal. Note that jitter present at the receiver threshold voltage level is considered by some to be a more effective representation of the jitter at the input of a receiver.

As the sum of skew and noise increases, the eye closes and data is corrupted. Closing the width decreases the time available for accurate sampling, and lowering the height enters the 900 mV or 500 mV threshold of a receiver.

Different sources induce noise onto a signal. The more obvious noise sources are the components of a transmission circuit themselves; the signal transmitter, traces & cables, connectors, and the receiver. Beyond that, there is a termination dependency, cross-talk from clock traces and other proximity effects, VCC & ground bounce, and electromagnetic interference from near-by electrical equipment.

The balanced receiver inputs of the HVD251 mitigate most all sources of signal corruption, and when used with a quality shielded twisted-pair cable, help insure data integrity.

## Typical Application

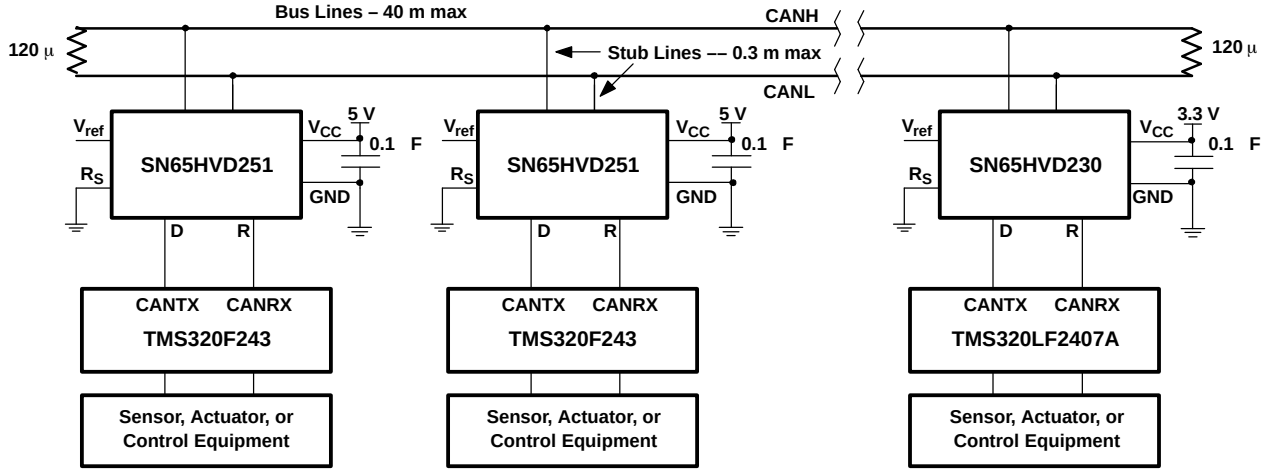
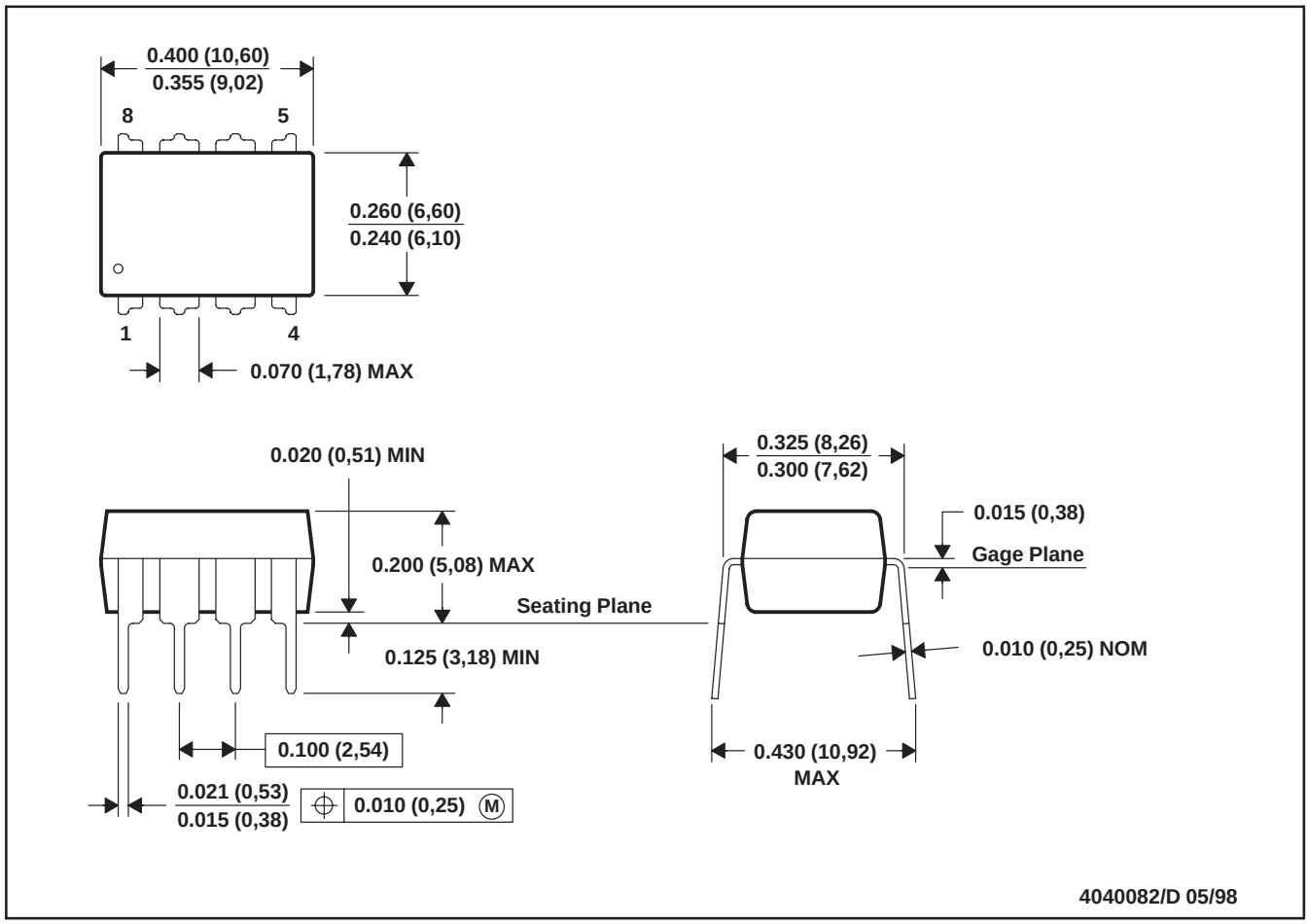



**Figure 25. Typical HVD251 Application**

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

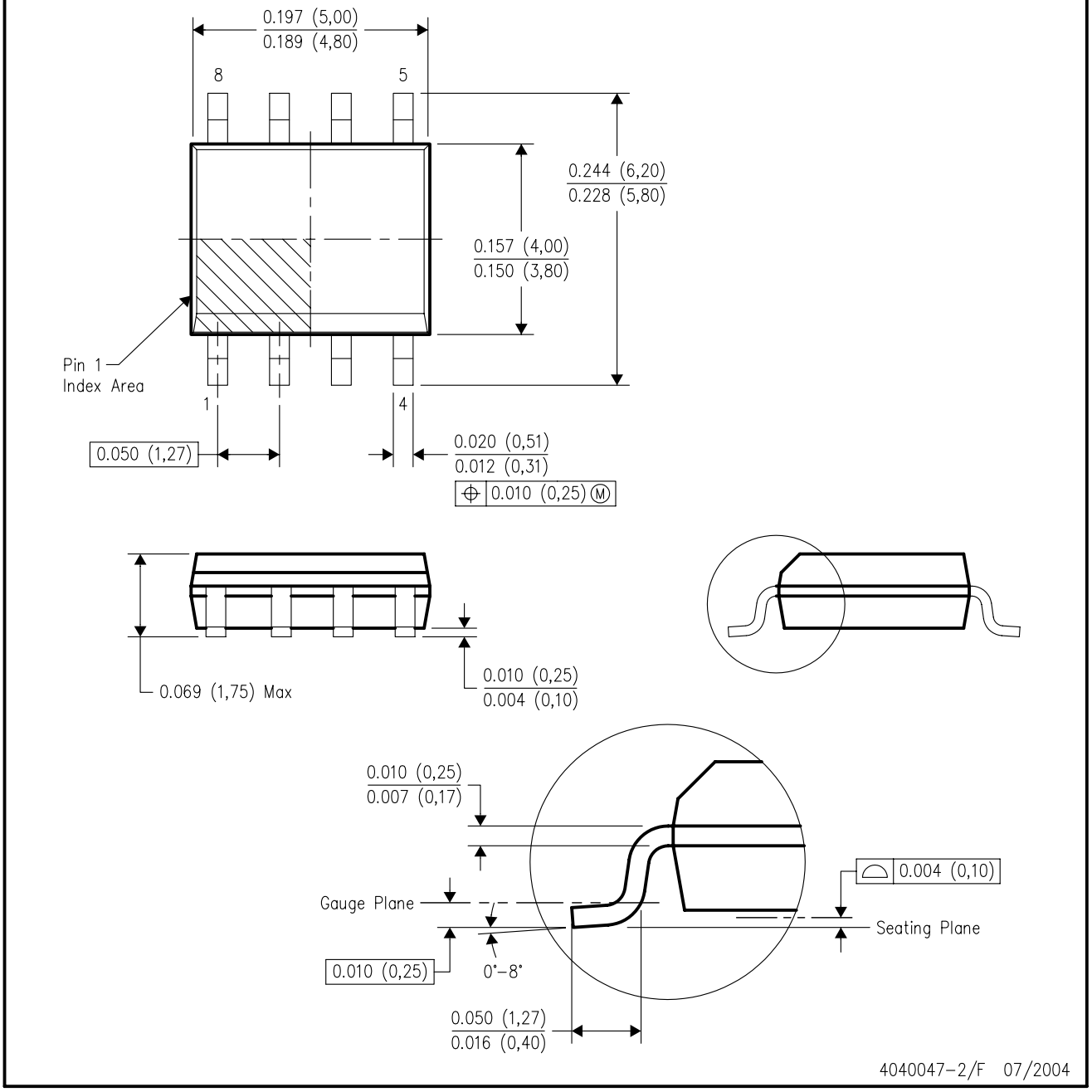
**P (R-PDIP-T8)** **PLASTIC DUAL-IN-LINE**




NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

## D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AA.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265