Weizhe Chen

UNDERGRADUATE STUDENT

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Education

Shanghai Jiao Tong University   *Shanghai, China*
HONORS BACHELOR OF COMPUTER SCIENCE   *Sep 2017 - PRESENT*
- Member of ACM class in SJTU, which is an elite CS program for 5 % talented student.
- First year GPA: 87.5/100, rank:11/48
- Second year GPA: 88.6/100, rank:10/48

Research Experience

Apex Lab@SJTU   *Shanghai, China*
UNDERGRADUATE RESEARCHER   *July 2019 - PRESENT*
- Supervised by Prof. Yong Yu and Prof. Weinan Zhang.
- My current research interest is machine learning, reinforcement learning, multi-agent reinforcement learning, game theory, application machine learning, and AI for social good.

Publications

Bi-level Actor-Critic for Multi-agent Coordination

HAIFENG ZHANG, **WEIZHE CHEN**, ZEREN HUANG, MINNE LI, YAODONG YANG, WEINAN ZHANG, JUN WANG
- Proposed an algorithm called Bi-AC which add asymmetric to multi-agent studies.
- Did a converge analysis of our Bi-AC algorithm that showed our algorithm can converge in very specific time.
- Experiment conducted in matrix game and a modified version of highway-env to show that the algorithm will result in an asymmetric result which can be a potential better result for all agents.
- Paper accepted by AAAI 2020 as oral presentation paper.

Learning to Combat Poaching: Lessons Learned from Field Deployment
- Give a prediction of find poaching activity in heatmap form and give a possible route planning result method with only satellite image and elevation data as input.
- Showed that neural networks are applicable in anti-poaching area.
- Did some study to help building human-AI trust.
- Paper submitted to KDD-2020 applied data science track.

When to Follow the Tip: Security Games with Strategic Informants

WEIRAN SHEN, **WEIZHE CHEN**, TAOAN HUANG, ROHIT SINGH, FEI FANG
- Conducted all the experiments.
- Paper accepted by IJCAI-PRICAI 2020.

Course Projects

M_compiler
- `https://github.com/laonahongchen/M_compiler`
- This project is a compiler for Mx* language, a C-and-Java like language. The compiler also include some basic optimizations like graph coloring.

RISC-V CPU
- `https://github.com/laonahongchen/RISC-V`
- This is a RISC-V 5-stage cpu implemented in Verilog.

Honors and Awards

Rong Chang Innovation Scholarship
A REWARD FOR TOP 0.5% STUDENT IN SJTU   *2019*

Team Member of Programming Contest Team Quasar
- 15th place in 'The 2018 CCPC final'.
- 2nd place in 'The 2018 ICPC Asia Nakhon Pathom Regional Contest'.
- 12th place in '2018 ICPC China Qingdao Provincial Programming Contest'.
- 4th place in '2018 CCPC Guilin Provincial Programming Contest'.

Team Member of Programming Contest Team Obsidian
- 3rd place in 'The 2018 ICPC China JiangSu Provincial Programming Contest'.

Team Member of Programming Contest Team Blazar
- 6th place in '2017 CCPC QinHuangDao Regional Contest'.
- 5th place in '2017 ACM ICPC Asia-Manila Regional Contest'.

Zhiyaun Honors Scholarship

A REWARD FOR TOP 5% STUDENT IN SJTU   *2017, 2018, 2019*

Shanghai Jiao Tong University Scholarship   *Type B*

A REWARD FOR TOP 5% STUDENT IN SJTU   *2018, 2019*

Teaching Experience

Programming Contest Team of Shanghai Jiao Tong University   *Shanghai, China*

STUDENT CO-COACH   *Spring, Fall 2019*

Machine Learning course (CS420) in Shanghai Jiao Tong University   *Shanghai, China*

TEACHING ASSISTANT   *Spring 2020*