

1.
(a) DADDI R4, R0, 0xFFFF
DSRL R5, R4, 16
LW R8, 1000(R10)
AND R9, R8, R5
SW R9, 1000(R10)
LW R6, 2000(R10)
SW R6, 1004(R10)
OR R7, R6, R5

(b) 2 stalls are still necessary

1.
LW R8, 1000(R10) ①
AND R9, R8, R5 ②

① F D X M W

② F D S X M W

R8 in ② needs to wait till the end of MEM phase in ①

2. LW R6, 2000(R10) ③
SW R6, 1004(R10) ④

F D X M W

F D S X M W

for same reason, R6, in ④ needs to wait till the end of MEM phase. So a stall is needed.

2. DSLL R2, R2, #2 (A) R2 = 400
 DADD R3, R1, R2 (B) R3 = R1 + 400
 L1: LW R4, 0(R1) (1)
 DSUB R4, R0, R4 (2)
 SW R4, 0(R1) (3)
 DADDI R1, R1, #4 (4)
 SLT R5, R1, R3 (5)
 BNE R5, R0, L1 (6)
 DSUB R2, R0, R0 (7)

iteration times : 100

1 2 3 4 5 6 7 8 9 10 11 12 13

ca) ① F D X M W

② F D S X M W

③ F S D X M W

④ F D X M W

⑤ F D X M W

⑥ F S D X M W

incorrect

F S S S S ; or ⑦ F D X M W

F D X M W

in first 99 loops: 9 cycles each

last loop: 13 cycles

① F D X M W

② F D X M W

③ F D X M W

before loop: 2 cycles

Total : $2 + (9 \times 99) + 13 = 906$ cycles

(b) 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

(A) F D X M W

(B) F D X M W

(1) F D X M W

(2) F D X M W

(3) F S D X M W

(4) F D X M W

(5) F D X M W

(6) F S D X M W

(7) F D X M W

or (7)

F D X M W

$$99 \times 8 + 15$$

$$= 807 \text{ cycles}$$

3.

(a) $-0.625 = (-0.101)_2 = -1.01 \times 2^{-1}$

$S = 1, e = 1, f = 01$

$127 + 1 = 128 = 1000\ 0000$

single precision :

1 1000 0000 010 0000 0000 0000 0000 0000

(b) (i) 1.0101010000

rounding up 1.0101100000

rounding down 1.0101000000

nearest even 1.0101000000

(ii) 1.0011100001

up 1.0011110000

down 1.0011100000

nearest even 1.0011100000

(iii) 1.0100110000

up 1.0101000000

down 1.0100100000

nearest even 1.0101000000

(iv) 1.0011010001

up 1.0011100000

down 1.0011000000

nearest even 1.0011000000

4.

(a) 2 way set
set

0	M0	M4	M8	M12	M16	8x				
0	M0	M4	✓	✓	✓					
1	M1	M5	M9	M13	M17					
1	M1	M5	✓	✓	✓					
2	M2	M6	M10	M14	M18					
2	M2	M6	✓	✓	✓					
3	M3	M7	M11	M15	M19	11x	3x	15x	15✓	11x
3	M3	M7	✓	✓	✓	7x	11x	19x	3x	

1 hit in 10 times

miss rate ~~80%~~ 90%

(b) addr set h/m compulsory capacity conflict

11	3	miss	✓		
7	3	miss	✓		
3	3	miss		✓	
11	3	miss			✓
15	3	miss		✓	
19	3	miss		✓	
15	3	hit			
3	3	miss			✓
8	0	miss	✓		
11	3	miss			✓

5.

(12)

(a) write back

~~bandwidth of read hit~~

~~read miss~~

$$\text{read hit} : 0.9 \times 0.8 \times 4 \times 10^8$$

$$= 2.88 \times 10^8$$

$$\text{read miss} : \cancel{0.9} \times 0.1 \times 0.8 \times 4 \times 10^8 = \cancel{0.32} \times 3.2 \times 10^7$$

$$\text{write hit} : = 0$$

$$\text{write miss} = 0.1 \times 0.2 \times (4 \times 0.3 + 4) \times 10^8$$

$$= 1.04 \times 10^7$$

$$\text{total} : 2.88 \times 10^8 + 3.2 \times 10^7 + 1.04 \times 10^7$$

$$= 3.304 \times 10^8$$

(b) write through