ECEN 651 HW3 Zhenlei Song

3.1

	instruction	cycles
Loop:	LD F2, 0(Rx)	4+1 = 5
I0:	DIVD F8, F2, F0	12+1 = 13
I1:	MULTD F2, F6, F2	5+1 = 6
I2:	LD F4, 0(Ry)	4+1 = 5
I3:	ADDD F4, F0, F4	1+1 = 2
I4:	ADDD F10, F8, F2	1+1 = 2
I5:	ADDI Rx, Rx, #8	1
I6:	ADDI Ry, Ry, #8	1
I7:	SD F4, 0(Ry)	1+1 = 2
I8:	SUB R20, R4, Rx	1
I9:	BNZ R20, Loop	1+1 = 2

total 40 clock cycles

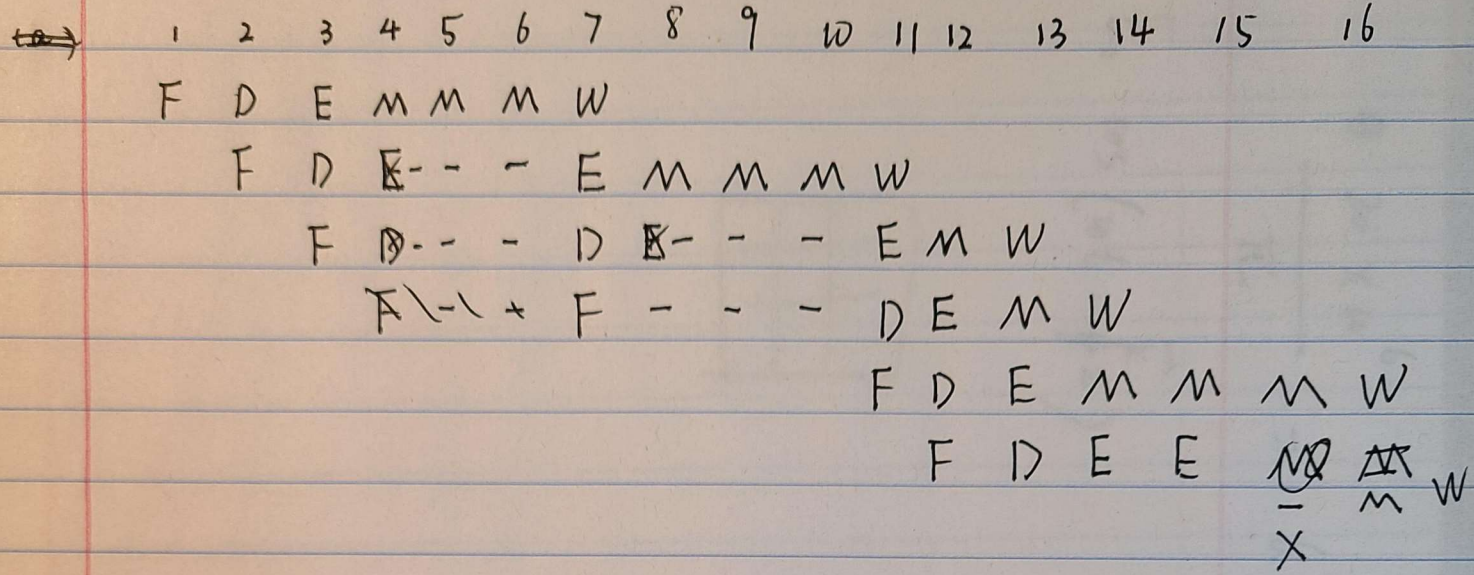
3.2

```
LD     F2, 0(Rx)
stall  x 4
DIVD   F8, F2, F0
MULTD  F2, F6, F0
LD     F4, 0(Ry)
stall x4
ADDD   F4, F0, F4
stall x1
stall x3
ADDD   F10, F8, F2
ADDI   Rx, Rx, #8
ADDI   Ry, Ry, #8
SD     ...
SUB    ...
BNZ    ...
stall x1
```

12 cycles

25 cycles in total

3.11



(a) new loop will start on cycle 16

(b) using a static predictor, new loop will start on cycle 14. 2 cycles wasted

(c) using dynamic predictor, new loop will start on cycle 13. 1 cycle wasted

3.14

(b) 5 times unrolled

```
foo:  LD     F2,  0(R1)
      LD     F8,  8(R1)
      LD     F14, 16(R1)
      LD     F20, 24(R1)
      LD     F26, 32(R1)
      MUL.D  F4,  F2, F0
      MUL.D  F10, F8, F0
      MUL.D  F16, F14, F0
      MUL.D  F22, F20, F0
      MUL.D  F28, F26, F0
      LD     F6,  0(R2)
      LD     F12, 8(R2)
      LD     F18, 16(R2)
      LD     F24, 24(R2)
      LD     F30, 32(R2)
      ADD.D  F6,  F4, F6
      ADD.D  F12, F10, F12
      ADD.D  F18, F16, F18
      ADD.D  F24, F22, F24
      ADD.D  F30, F28, F30
      SD     F6   0(R2)
      SD     F12  8(R2)
      SD     F18  16(R2)
      SD     F24  24(R2)
      SD     F30  32(R2)
      DADDIU R1, R1, #40
      DADDIU R2, R2, #40
      DSLTU  R3, R1, R4
      BNEZ   R3, foo
```

29 cycles