Lab Report3

1. Register File

1.1 Design

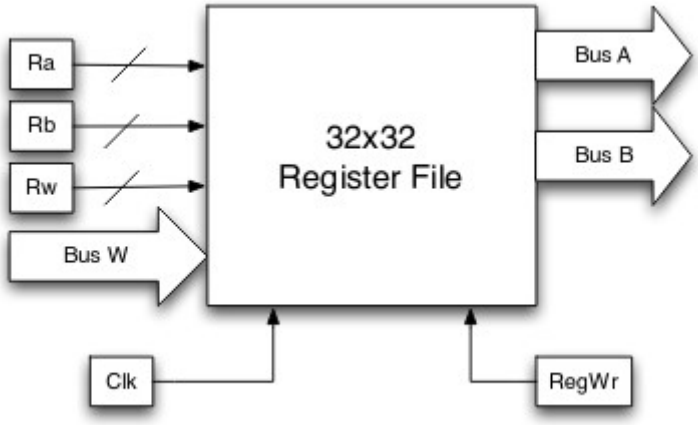

Fig 1.1 Register File Schematic

This register file has 32*32 registers, 31 of them is writable, register 0 is always 0 to simulate r0 in actual processor. Output Bus A and Bus B are respectively allocated as output of Ra and Rb.

1.2 Result

Report Check Netlist:

	Item	Errors	Warnings	Status	Description
1	multi_driven_nets	0	0	Passed	Multi driven nets

Fig 1.2 Synthesis Report

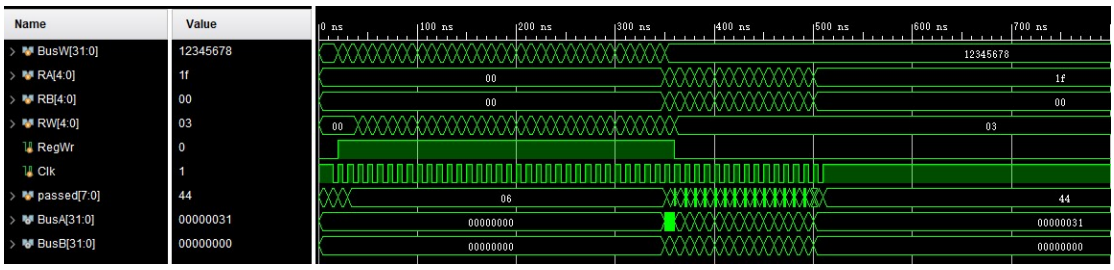

Fig 1.3 Register File Waveform

```
              Value Stayed Same 10 passed
            Initial Value Check 21 passed
            Initial Value Check 22 passed
              Value Not Updated 11 passed
              Value Stayed Same 11 passed
            Initial Value Check 23 passed
            Initial Value Check 24 passed
              Value Not Updated 12 passed
              Value Stayed Same 12 passed
            Initial Value Check 25 passed
            Initial Value Check 26 passed
              Value Not Updated 13 passed
              Value Stayed Same 13 passed
            Initial Value Check 27 passed
            Initial Value Check 28 passed
              Value Not Updated 14 passed
              Value Stayed Same 14 passed
            Initial Value Check 29 passed
            Initial Value Check 30 passed
              Value Not Updated 15 passed
              Value Stayed Same 15 passed
            Initial Value Check 31 passed
              Value Not Updated 16 passed
All tests passed
```

Fig 1.4 Register File output

2. Data Memory

2.1 Design

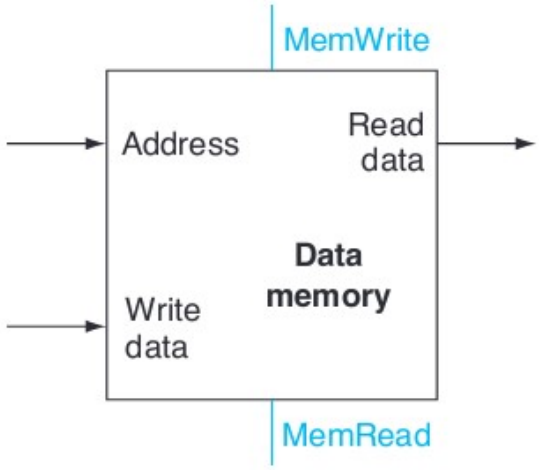

Fig 2.1 Data Memory Schematic

There is no input pin for write enable or read enable because writing and reading are impulsed by negedge and posedge.

2.2 Result

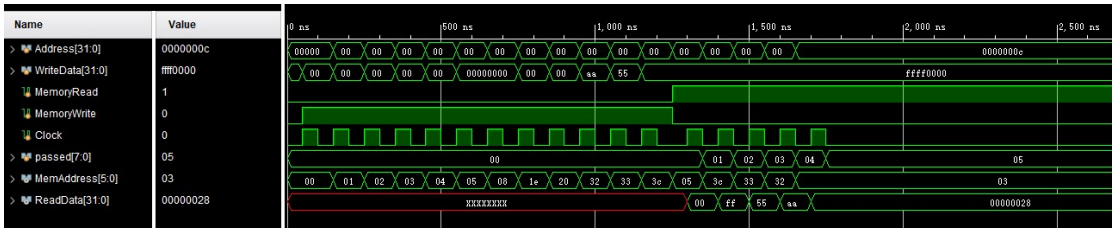

Fig 2.2 Wave form

```
# run 1000ns
Init Memory with some useful data
INFO: [USF-XSim-96] XSim completed. Design snapshot 'DataMemoryTest_v_behav' loaded.
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
run 2 us
                Read address 0x14 passed
                Read address 0xf0 passed
                Read address 0xcc passed
                Read address 0xc8 passed
                 Read address 0xc passed
All tests passed
```

Fig 2.3 Logs

Report Check Netlist:

	Item	Errors	Warnings	Status	Description
1	multi_driven_nets	0	0	Passed	Multi driven nets

Fig 2.4 Report

3. Questions

1. Yes. It could be done. By using dual-ported module, the size will be doubled as well. Considering the price of RAM and the speed of RAM and CPU, RAM is waiting for CPU orders, instead of the opposite way. Because memory is waiting for CPU commands for most of the time. Adding a not frequently used module is a waste. It's not a good design.

2. MemRead is used when CPU needs to read data from memory. Yes it's necessary. Because if there is no MemRead port, then the data will be continuously read from memory which cannot be accessed by CPU at once. On the other hand, the size of register file is much smaller than

memory. Plus each unit has their own address, thus they can be accessed at once thus there is no need to set a switch(like MemRead) to control.

3. Synthesizable means the Verilog program can be corresponded into actual hardware connections. For example, ‘always @ xxx‘ is not synthesizable. Because it’s impossible to implement this phrase in hardware.