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ESNUG 522 Item 4) ---------- [04/18/13]

From: [Jim Hogan of Vista Ventures LLC]
Subject: Hogan compares Palladium, Veloce, EVE ZeBu, Aldec, Bluespec, Dini

Hi, John,

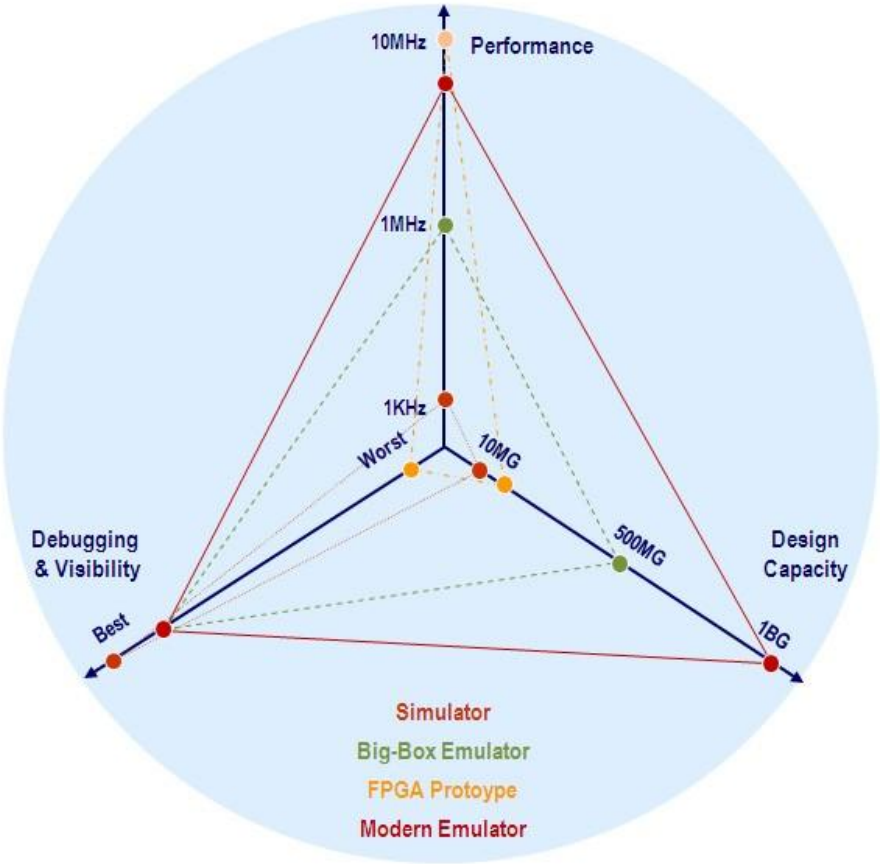
Below I have mapped top-level information for each vendor, according to the emulation metrics I mentioned earlier. I derived the information for the snapshot below from each vendor's website plus my general accumulated knowledge to date.

- **Category 1**. Emulators are based on application-specific processors. Cadence Palladium's processor is implemented in an ASIC-structured custom fabric. Mentor Veloce's processor is implemented in a custom FPGA fabric.

- **Category 2**. Emulation with a standard FPGA product at its core. Synopsys-EVE is currently the player in this sector.

- **Category 3**. Other emulators with HW based on a standard FPGA product. The primary differentiator between category 2 and 3 is capacity; however, there are other differences as shown below. Aldec, Bluespec, Cadence RPP, Dini Group, S2C, and HyperSilicon are primary vendors in this segment.

The emulator best suited to the designer problem is defined by what problem they are trying to solve.



Source: EVE, Embedded Computing, 2010

The optimal choice lies in the intersection of a number of factors, with one example outlined above.

Emulation Vendors	**Cadence Palladium, Mentor Veloce**	**Synopsys EVE Zebu**	Other: **Aldec, Bluespec, Cadence RPP, HyperSilicon**
Emulator Architecture	custom silicon, custom board, custom box (32 M to 2 B)	off-the-shelf FPGA, custom board, custom box (25 M - 200 M)	off-the-shelf FPGA, off-the-shelf board, off the shelf box (2 M - 50 M)
Price/gate	2-5 cents	0.5 - 2 cents	0.25 -1 cent
Dedicated Support	yes	mixed	no
Design Capacity	Claims up to 2 billion. Typical usage 100 M to 1 B gates.	Claims up to 1 billion. Typical usage 25 M to 200 M gates.	Claims up to 50+ million. Typical usage 2 M to 25 M gates.
Primary Target Designs	SoCs 100 M to 1 B gates. Large CPUs, GPUs, multi-chip systems, application processors.	SoCs from 25 M to 200 M gates	IP blocks, sub-system, and SoCs from 2 M to 25 M
Speed range (cycles/sec)	100 K to 2 M	500 K to 5 M	500 K to 20 M
Compile time	10-30 M gates/hour. Single workstation (Palladium). PC farm (Veloce). Includes automated partitioning time. Parallelizable: Yes	25 M - 100 M gates/hr for PC farm. Proprietary software for fast FPGA partitioning, synthesis and P&R. Parallelizable: Yes	1 M - 15 M gates/hr for PC farm. Constrained by FPGA vendor synthesis and P&R times. Doesn't include partitioning time. Parallelizable: Yes
Partitioning	automated	automated	semi-automated. Partitioning depends on # of FPGAs. Time range 30 min to 4 hours.
Visibility	full visibility. at-speed probe capture.	static, dynamic probes. at-speed probe capture.	static, dynamic probes (vendor dependent). at-speed probe capture (vendor dependent).
Debug	Breakpoints, assertions, simulation hot-swap, SW debug.	Breakpoints, assertions, simulation hot-swap, SW debug.	Breakpoints, assertions, simulation hot-swap, SW debug.
Virtual platform API	Yes	Yes	varies by vendor
Transactor Availability	Standard/off-the-shelf: Good. Custom: developed ad hoc	Standard/off-the-shelf: Good. Custom: developed ad hoc	Standard/off-the-shelf: Mixed. Custom: developed ad hoc

Verification Language - Native support	C++, SystemC, Specman e, SystemVerilog, OVM, SVA, PSL, OVL	Synthesizable Verilog, VHDL, System Verilog	Synthesizable Verilog, VHDL, System Verilog
Memory	up to 1 TB	up to 200 GB	up to 32 GB
Users	1 to 512 users	1 to 49	1 user

Here is my quick summary of the different emulation vendors for 2013.

Category 1:

- **Cadence Palladium**. Hats off to Cadence for being pioneers in emulation and sustaining innovation to maintain a very competitive product year-over-year.

- **Mentor Veloce**. Their revenue numbers show emulation is a growing segment for them. (See ESNUG 510 #7.) Clearly Wally and Greg have been investing heavily in emulation.

Category 2:

- **Synopsys EVE Zebu**. This has been the choice for companies and design groups doing mid-size SoCs or blocks for emulation. It is no secret that Intel was an EVE customer. (See ESNUG 508 #6.) My expectation is that with the Synopsys acquisition, EVE will now move upstream to challenge Cadence and Mentor at the high end.

Category 3:

- **Aldec HES-DVM**. The company initially grew out of providing system emulation/simulation using FPGAs for eventual implementation in FPGAs. FPGAs will continue to be a choice for system designers with low volumes, including the mil-aero world. Will they try to move into the SoC market?

- **Bluespec Semu**. Bluespec expanded their emulation footprint in March with a new FPGA-based desktop form factor verification and hybrid emulator. They emphasize low cost, ease of use, fast deployment using third-party FPGA boards, dynamic hardware debug (no re-instrument and re-synthesis) and a C API to integrate SystemC/C/C++ models and test benches. Bluespec claims to need only 1 day set up.

- **Cadence RPP**. The Cadence FPGA-based Rapid Prototyping Platform is an FPGA-based prototyper for early software development and high-performance system validation. While not positioned as an emulator (See ESNUG 517 #6) it uses the core technology of FPGA-based emulators and confirms the need for boxes with higher performance and lower cost than processor-based emulators for pre-silicon software development.

- **The Dini Group**. An established leader in FPGA boards for prototyping and emulation. The Dini Group consistently delivers high quality, high capacity boards with the shortest time-to-market for leading edge FPGAs.

- **S2C**. Offers FPGA boards and software and IP for system-level design verification and acceleration. Their new boards based on 14 M gate Xilinx FPGAs.

- **HyperSilicon**. Company to watch from mainland China, focusing on

FPGA prototyping boards. Offers boards similar to S2C.

My conclusion is that emulation has indeed gone mainstream. Its growth extends from the rise of the SoC as the cornerstone of system hardware, with its associated multiple SW functions. What's also helped emulation grow is its better debug, increased FPGA sizes, and its newer ability to handle complex designs.

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The reason for my report was to analyze the segment and try to put some order to the market place. I'm not the only source of info on this. I'd like to invite the DeepChip readers to feel free to add their perspective and to update the charts and data I have gathered.

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