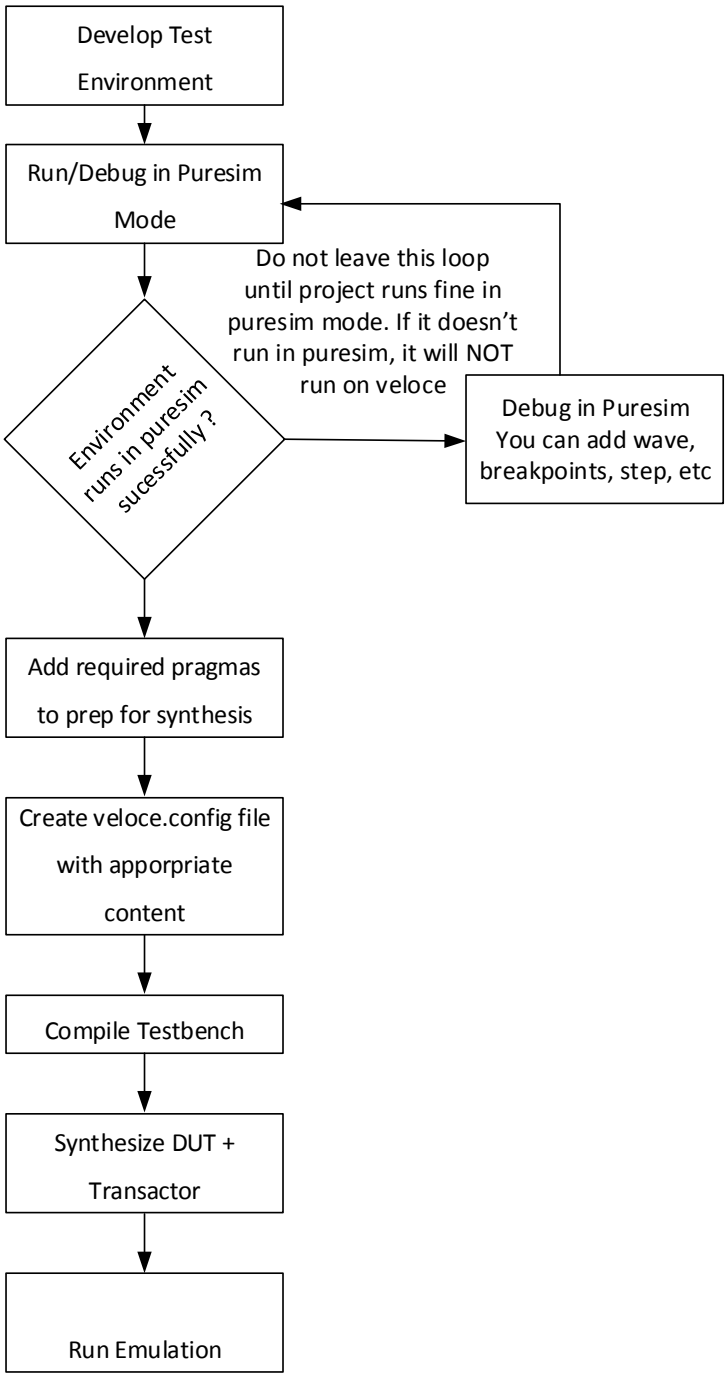
Veloce Emulation TBX Mode Flow
(with Examples)
Updated for VeloceOS3 by- Sameer Ghewari, May 2014

Generic Project Flow for TBX Mode



## What is Puresim Mode ?

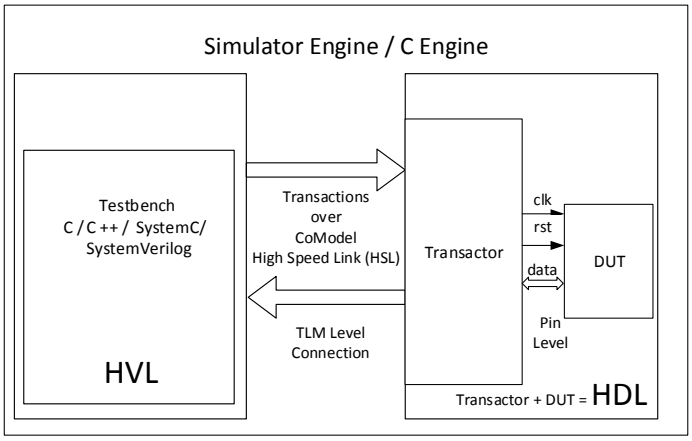



Fig. Puresim mode. Everything runs on the workstation.

- Puresim mode is when you run everything on workstation (Questa/C engine) despite of the fact that your test environment is TLM based
- It is **very essential** to debug in puresim mode, unless environment works here it will not work on emulator
- Since everything runs in a simulator, you have 100% visibility into the environment and DUT
- For debug purposes you can – Add breakpoints, View any signal in wave, temporarily add $display in your Transactor/DUT, etc
- Note that in Veloce mode you do not have direct visibility into transactor/DUT and debug becomes difficult. The purpose of Puresim mode is to make debug easy.

## What is Veloce Mode ?

- Once your environment runs fine in puresim, it is ready to be ported for veloce mode
- We now add required pragmas (//tbx clkgen, etc) and follow flow for veloce compile
- Design is partitioned and HVL runs on workstation, HDL runs on emulator

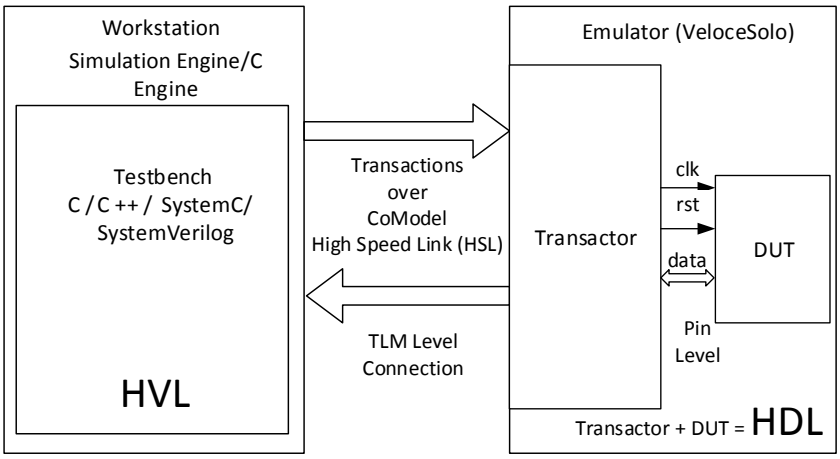
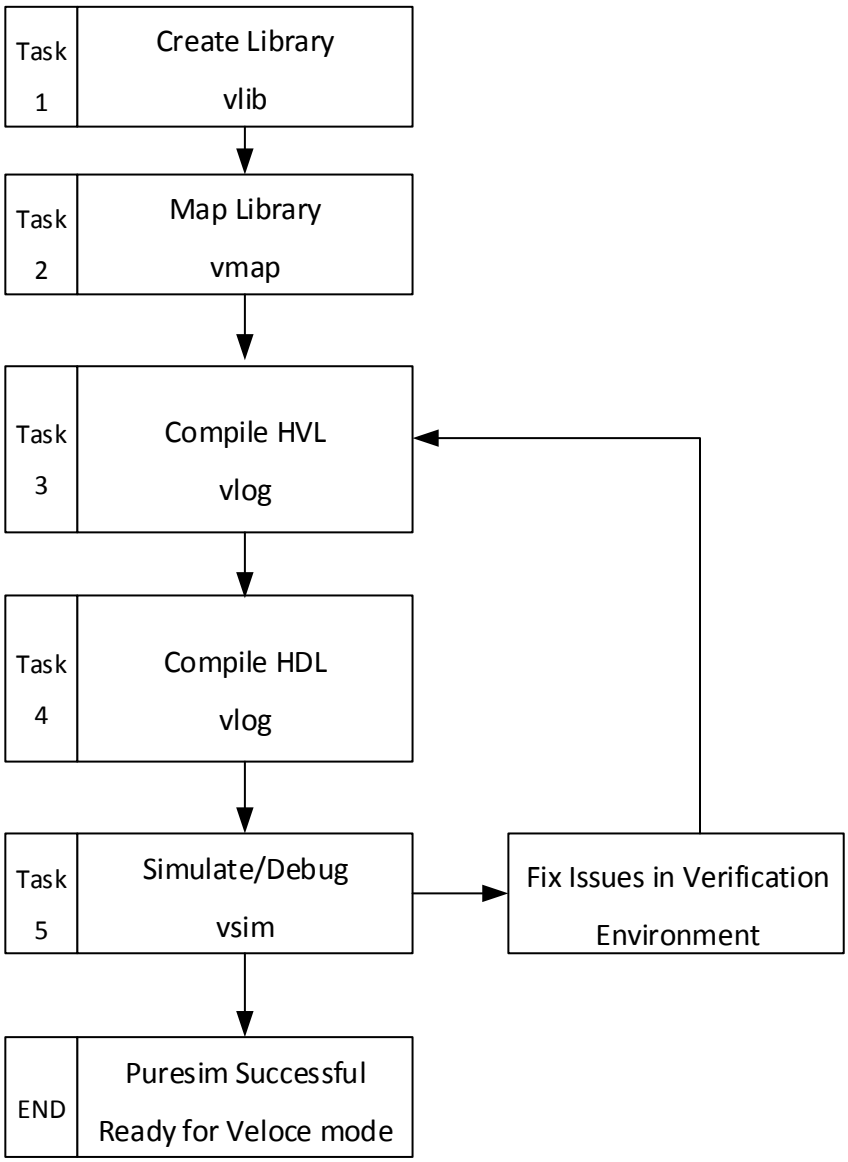



Fig. Veloce Mode – HVL on workstation, HDL on emulator

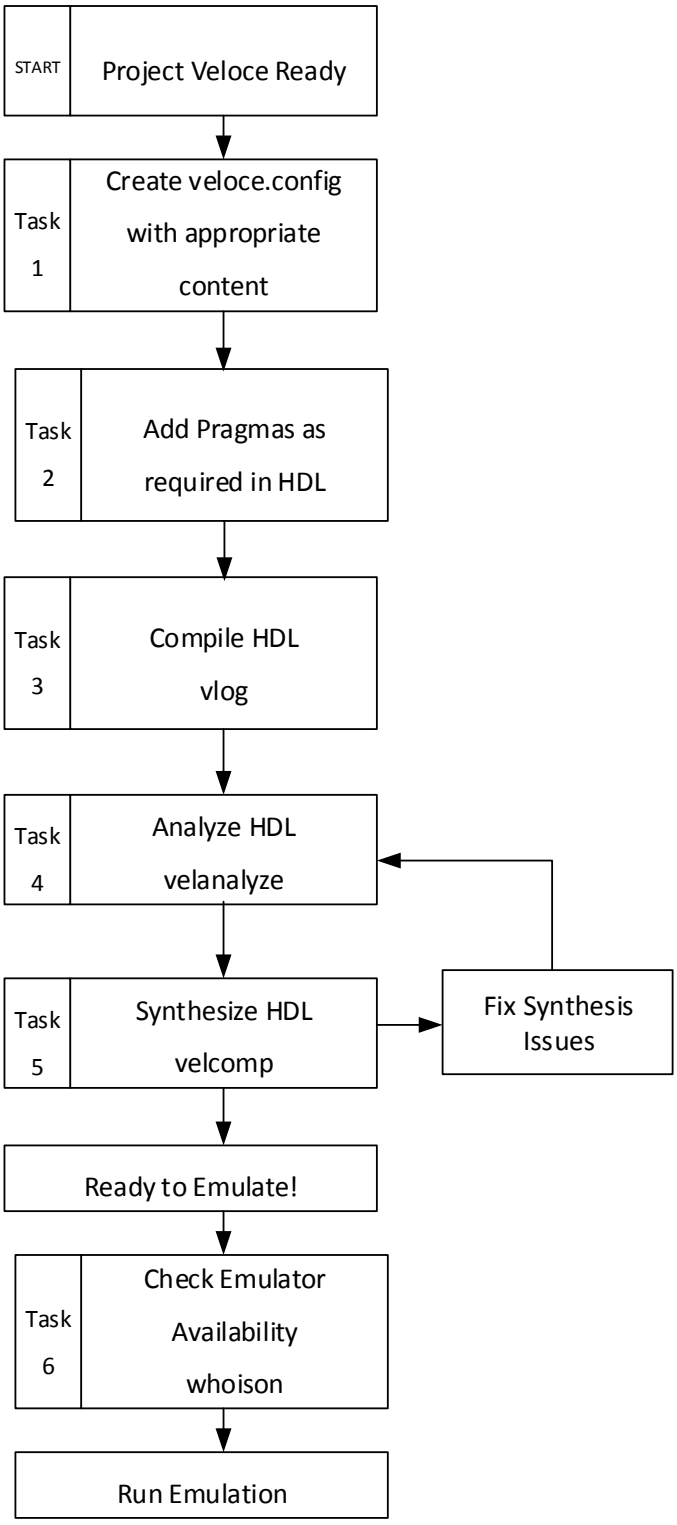
## Puresim Flow

As explained above, we compile everything and run on workstation. No synthesis involved in this mode.




Once project works in puresim mode, it is ready for veloce mode. Follow the next flow to prepare project for Veloce mode.

## Veloce Mode Flow




Please look at example veloce.config files, they come with comments and should help you to create your own config file.

## Examples

Each example directory contains its own document. Please read it before executing.

DPI-C CoModel Example
$PSU_EXAMPLES/examples/TBX/Booth_DPI.tar.gz

SCEMI Pipe Example
$PSU_EXAMPLES/examples/TBX/Booth_TBX.tar.gz

BFM Example
$PSU_EXAMPLES/examples/TBX/Booth_BFM.tar.gz

BFM Virtual Interface Example
$PSU_EXAMPLES/examples/TBX/Booth_BFM_vi.tar.gz

## More Features and Examples

The new VeloceOS3 releases supports functional coverage, assertions and power analysis in emulation.
Examples on these can be found at $VMW_HOME/examples
Also refer to documents at $VMW_HOME/doc/pdfdocs