

# Verification Academy



## Navigating the Perfect Storm

*Trends in Functional Verification*

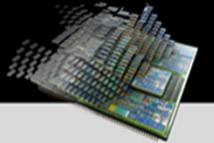
*Harry Foster*

*Chief Verification Scientist*

*info@verificationacademy.com* | *www.verificationacademy.com*

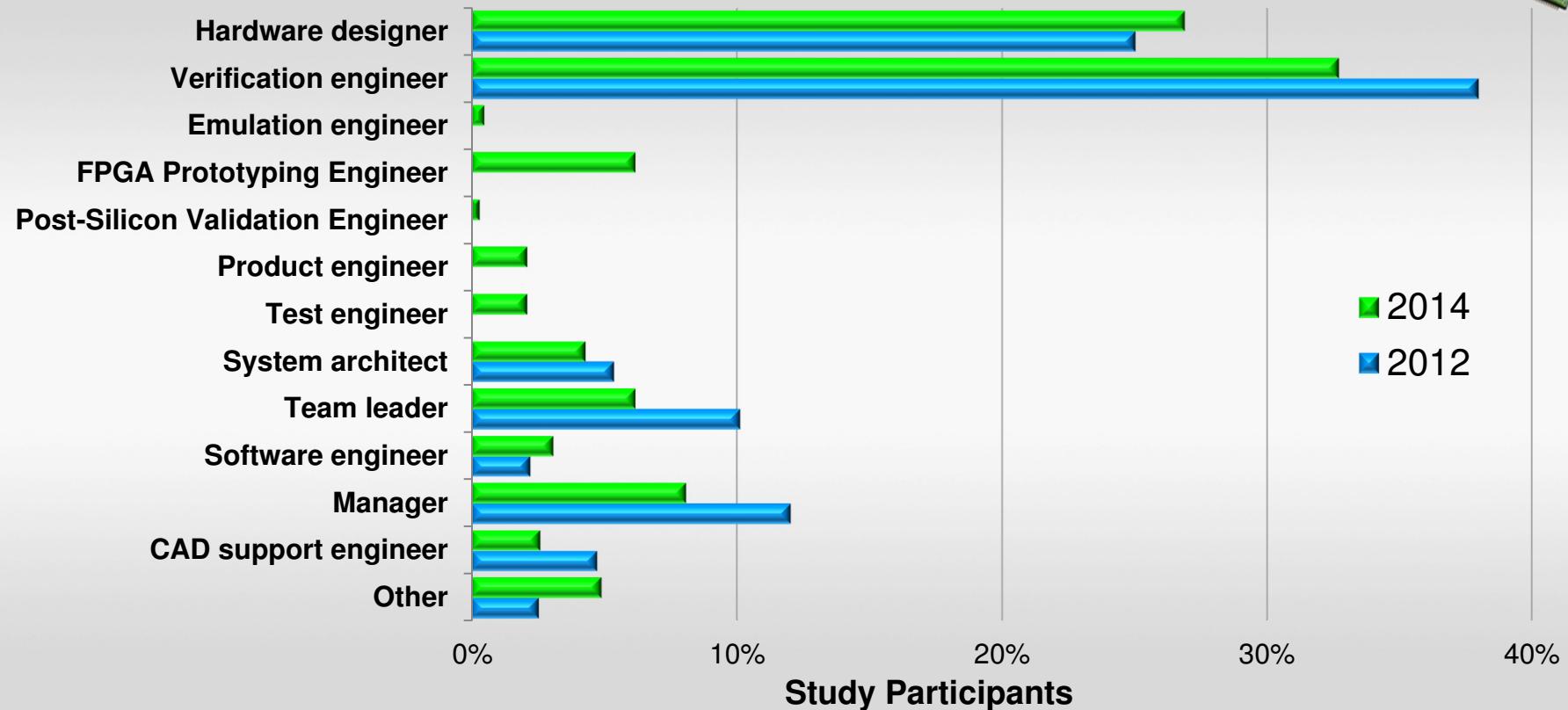
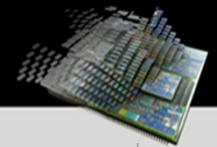
**Mentor**  
**Graphics**<sup>®</sup>

# 2014 Wilson Research Group Study



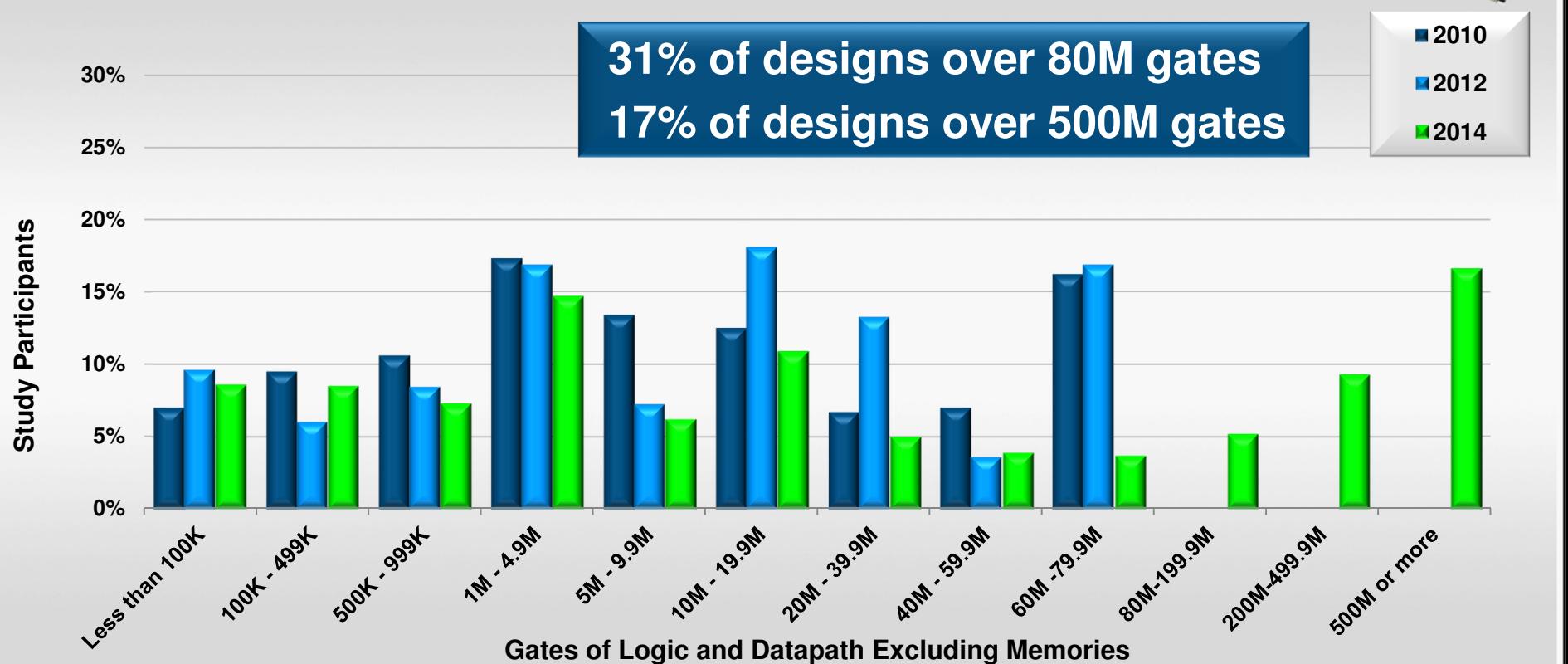
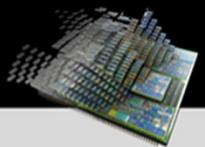
- **2014 Double blind functional verification study**
- **Worldwide study conducted in four phases**
  - North America, Europe, Japan, Rest of World
- **Sample frame consisted of 1886 participants**
  - 3.3x larger than our 2012 study
  - 9.4x larger than the 2004 Collett study
- **Confidence interval 95%**
  - $\pm 2.19\%$  Margin of Error

# Study Makeup by Participant Job Title



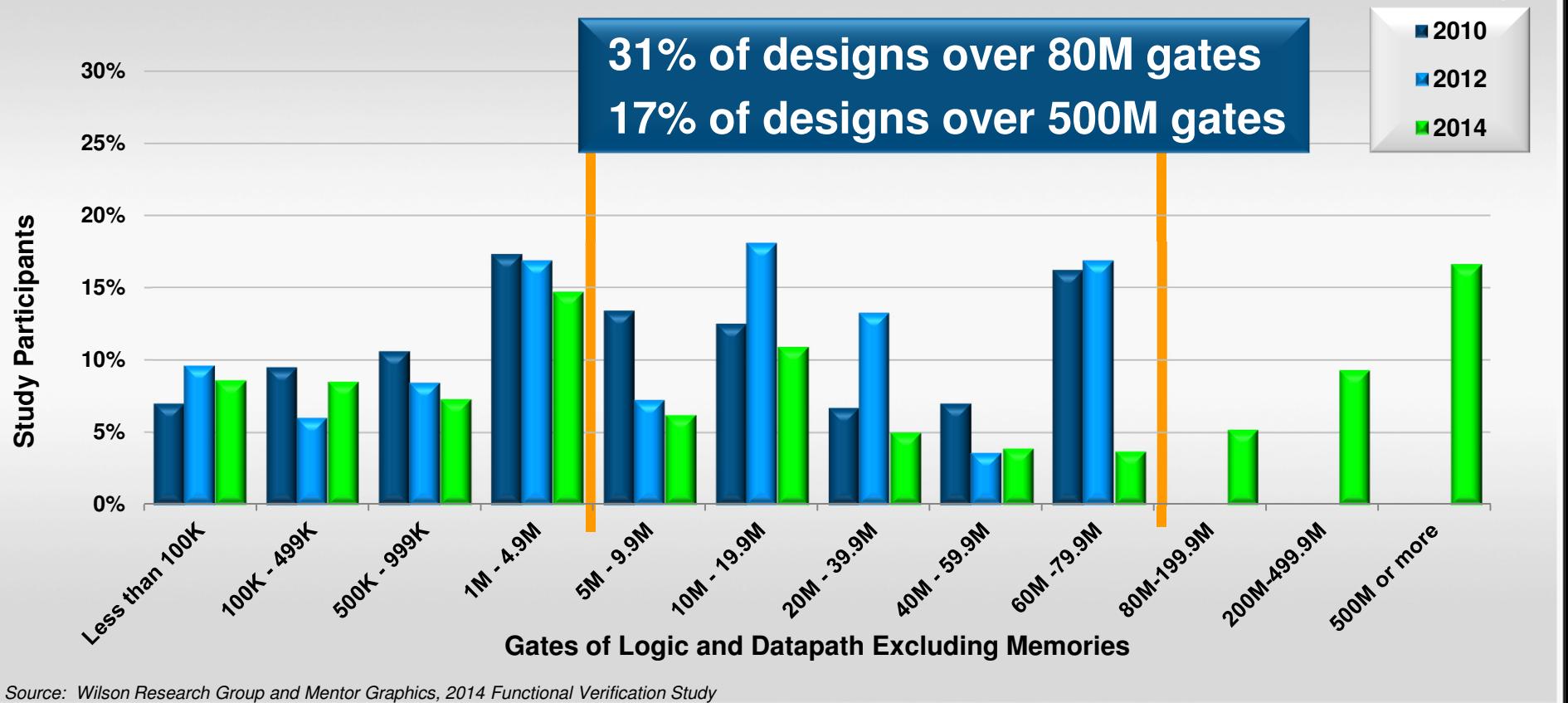
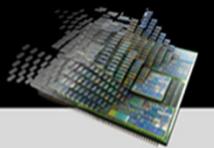
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Larger and Larger Designs



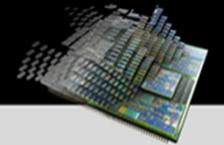
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# Larger and Larger Designs



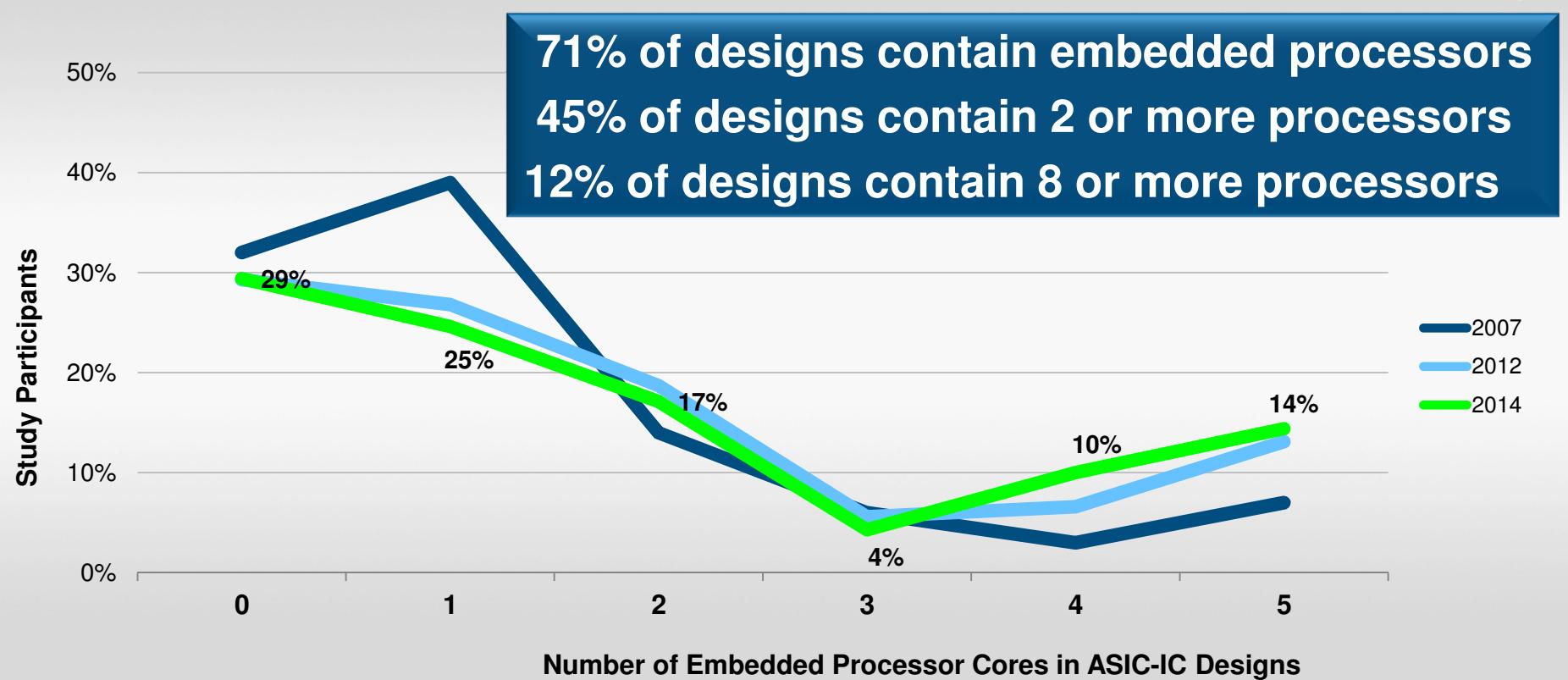
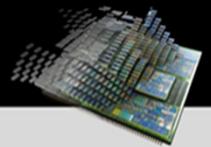
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# The perfect storm is brewing



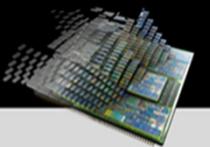
Perfect storm—an expression that describes an event where a combination of circumstances will aggravate a situation drastically.

# What's changed in design?

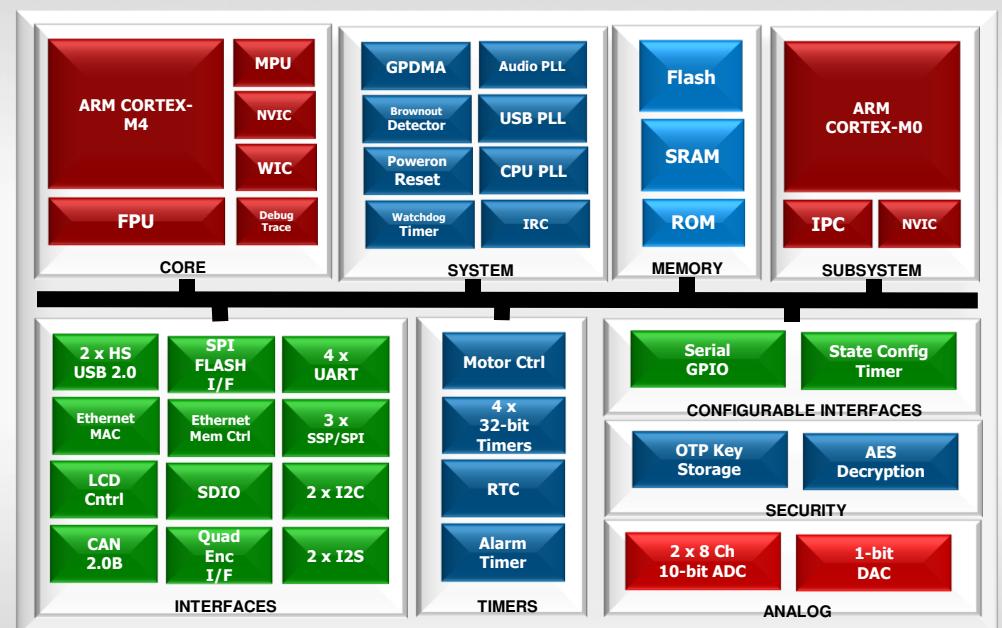


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

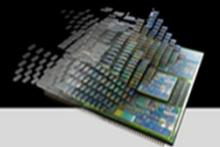
# SoC Changed Everything!



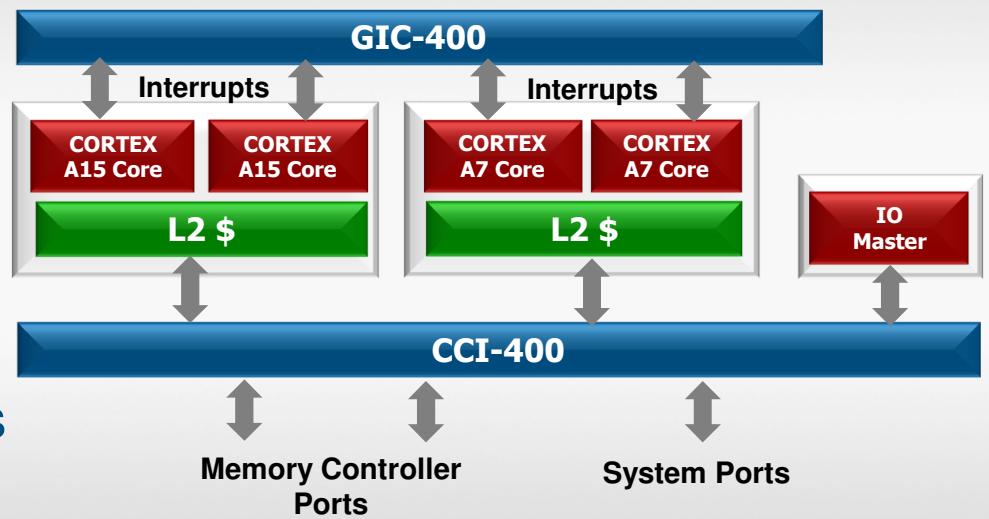
- **Target Market**
  - Embedded Processing
- **Design Trends**
  - Multiple Embedded Cores
  - Re-use of IP Blocks
  - Distributed design teams



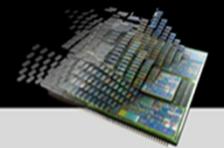
# System Architectures to Reduce Power



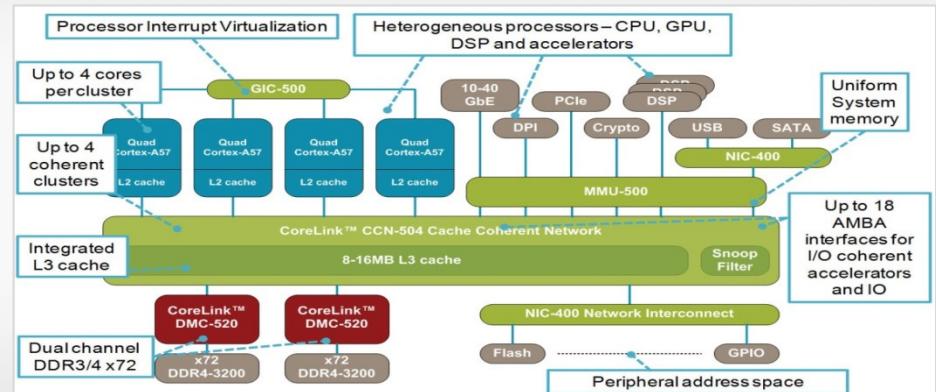
- **Target Market**
  - Mobile Applications
- **Design Trends**
  - Multiple Embedded Cores
  - Re-use of IP Blocks
  - Distributed design teams
  - Heterogeneous Processors
  - Complex Interconnect



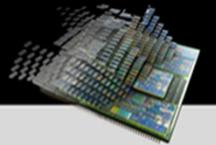
# Cache-Coherent Architectures for Performance



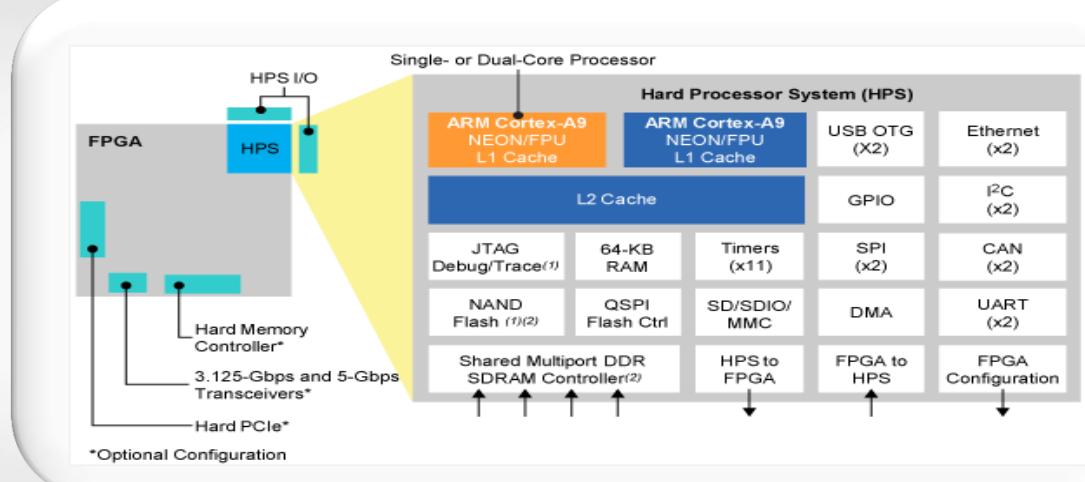
- **Target Market**
  - Enterprise Computing
- **Design Trends**
  - Multiple Embedded Cores
  - Re-use of IP Blocks
  - Distributed design teams
  - Heterogeneous Processors
  - Complex Interconnect
  - Network on Chip
  - Multi-level Caching



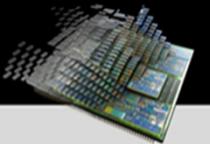
# Today's FPGAs are SoC



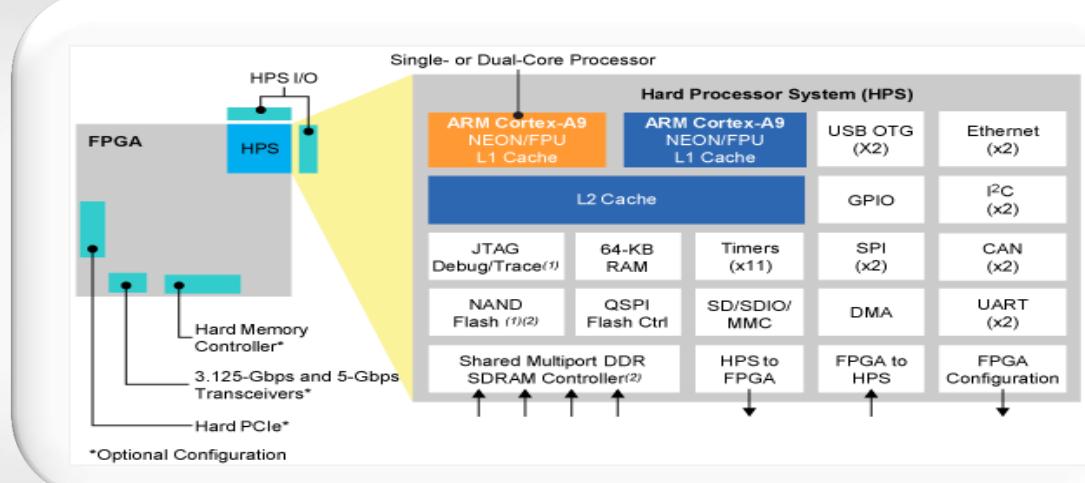
- **Target Market**
  - FPGA Applications
- **Design Trends**
  - Same as SoC...



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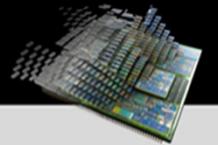


- **Target Market**
  - FPGA Applications
- **Design Trends**
  - Same as SoC...



Yet, increased functionality is only part of the verification challenge!

# The Emergence of New Layers of Verification



**Software**

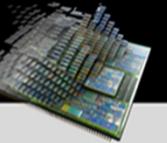
**Security Domains**

**Power Domains**

**Clock Domains**

**Functional**

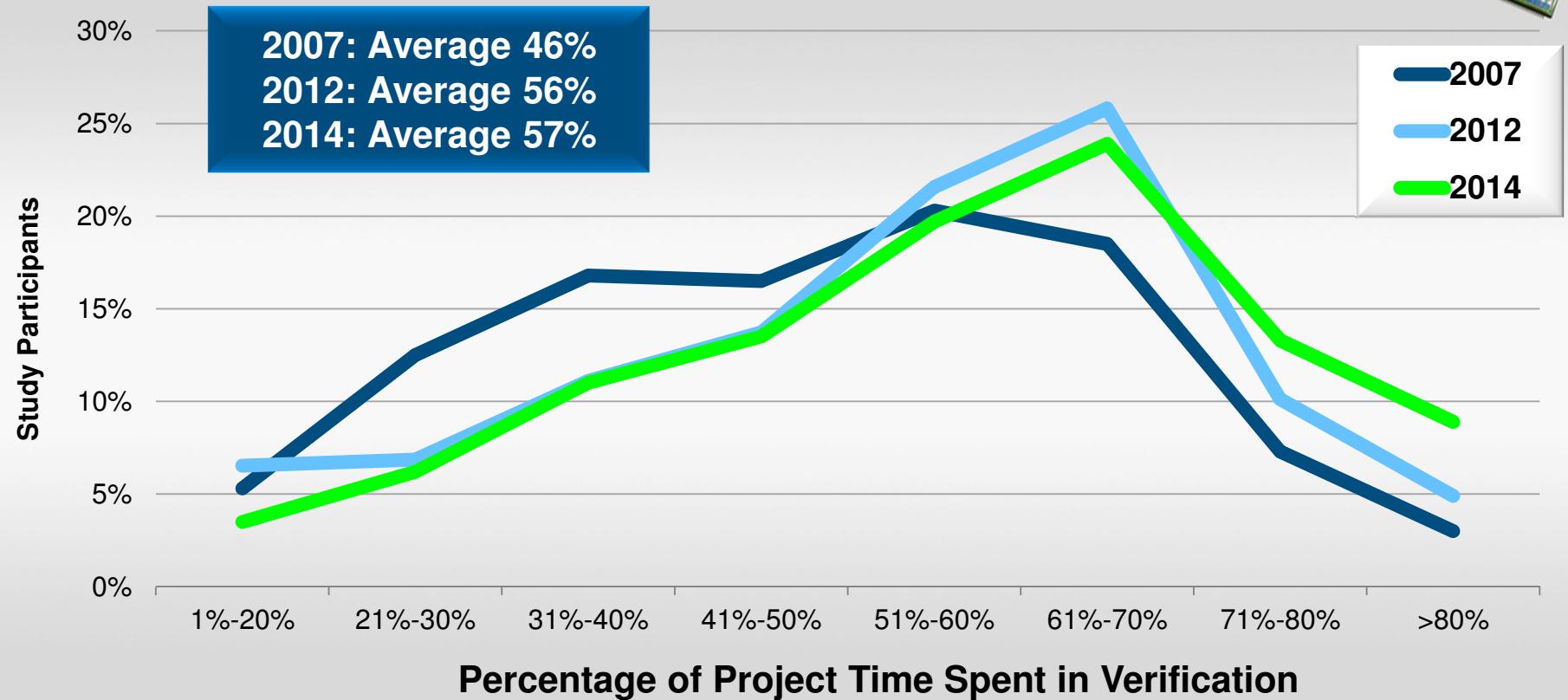
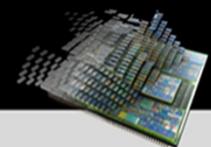
# What's the Impact with today's Rising Complexity?



*All these verification layers are converging to form the perfect storm.*

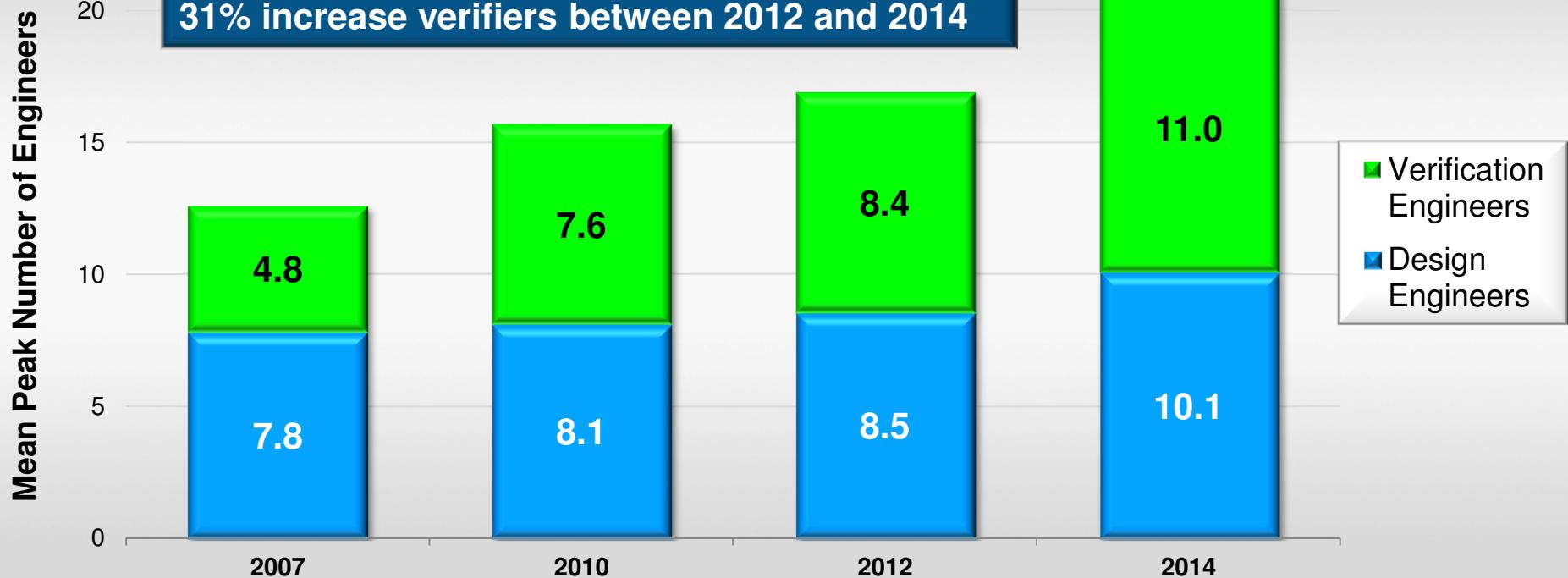
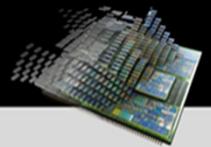


# Verification Consumes Majority of Project Time



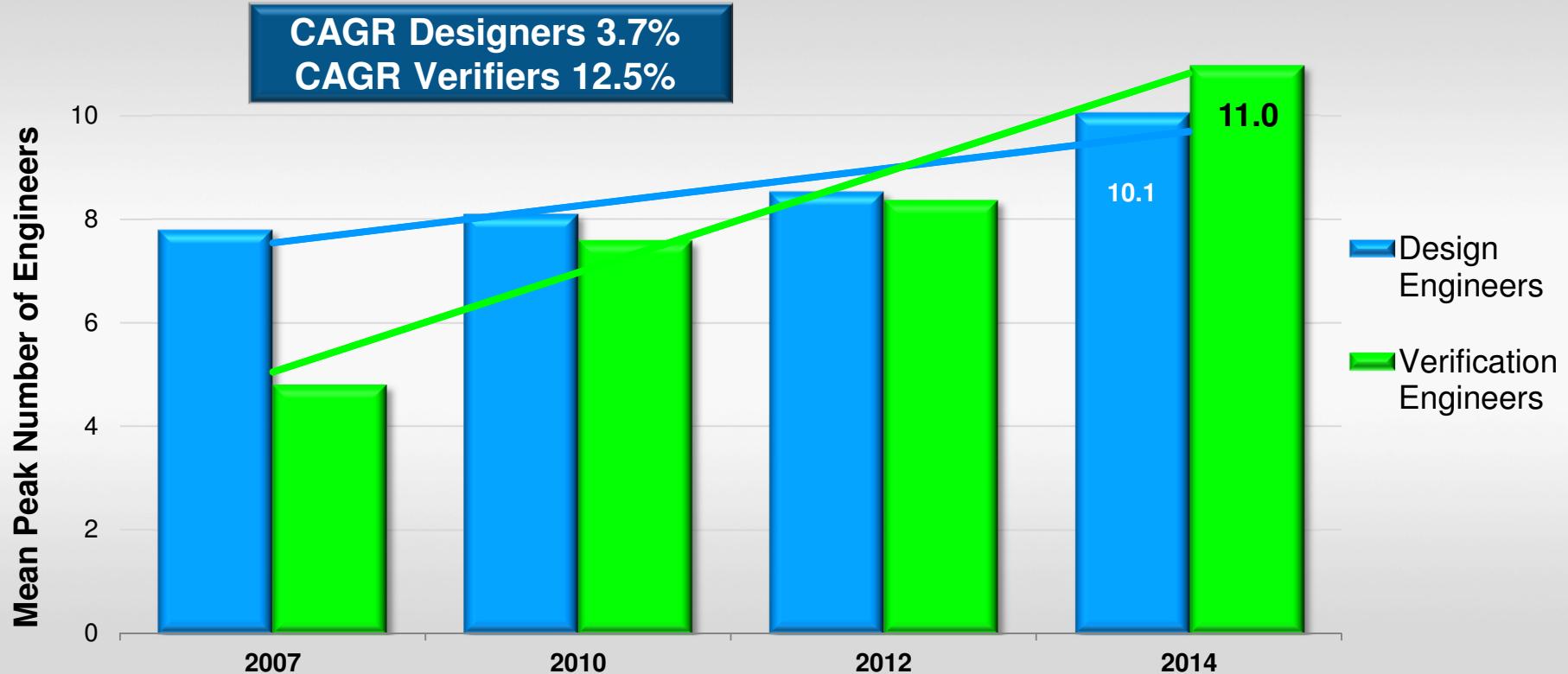
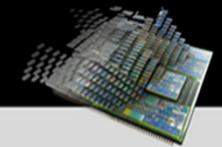
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Mean Peak Number Engineers Increasing



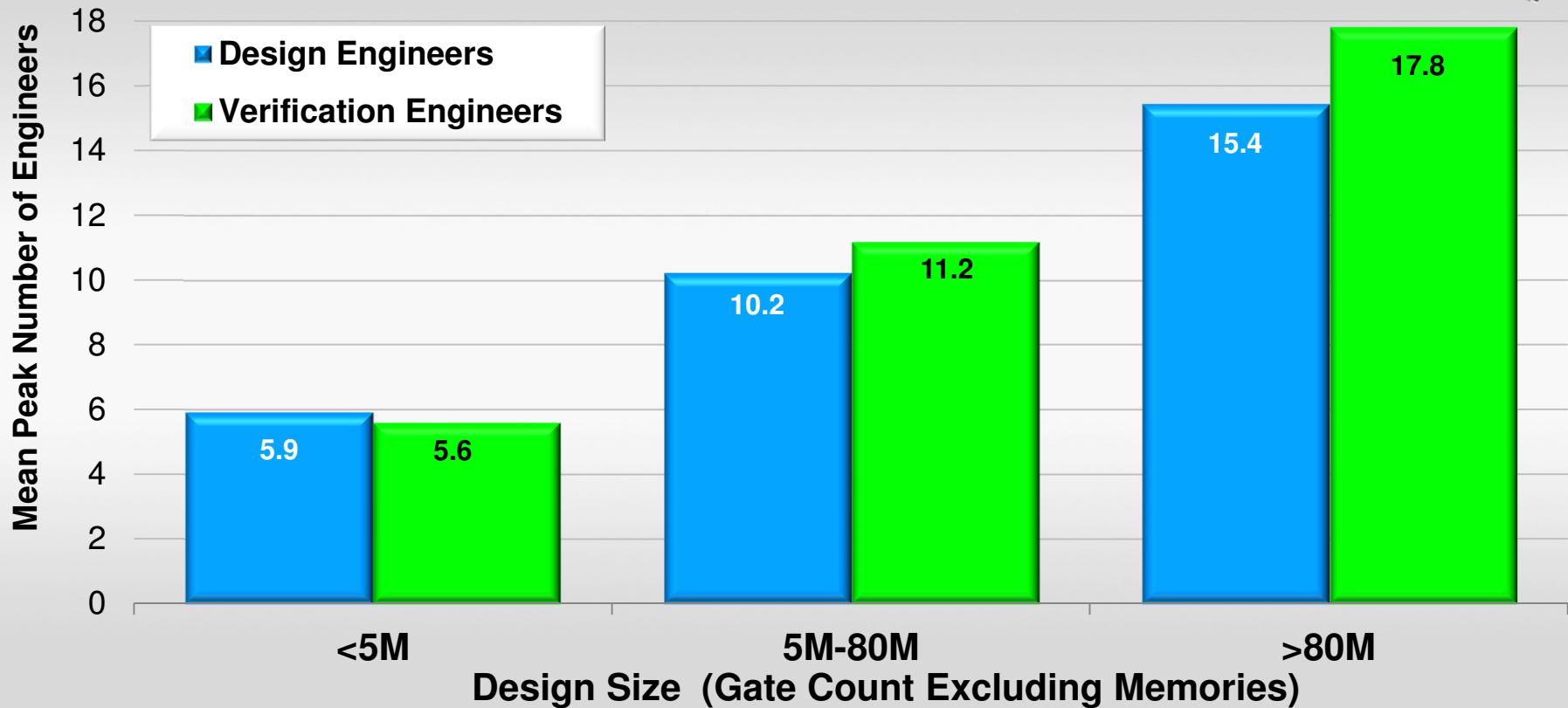
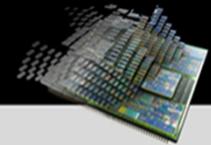
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# More Verification Engineers vs Design Engineers



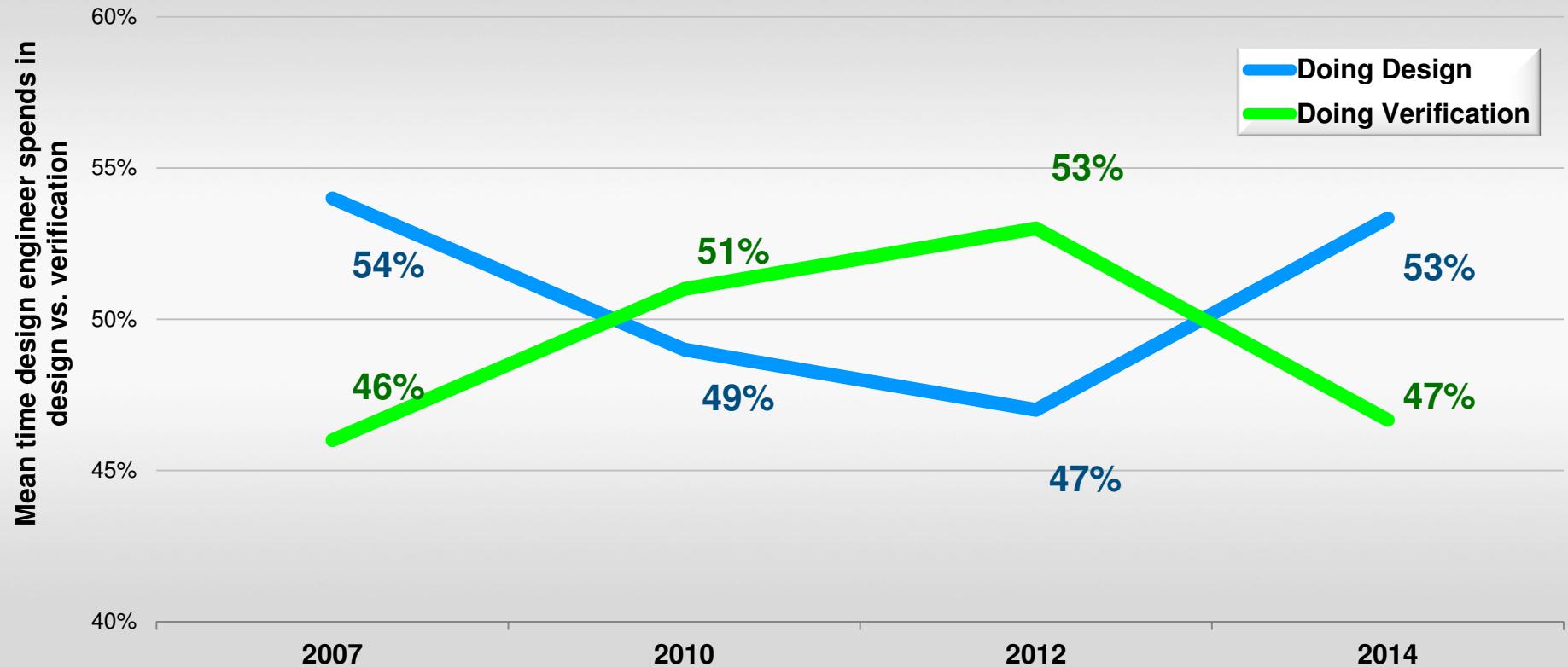
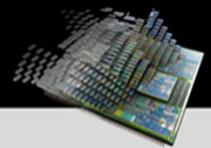
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# 2014 Mean Peak Engineers by Design Size



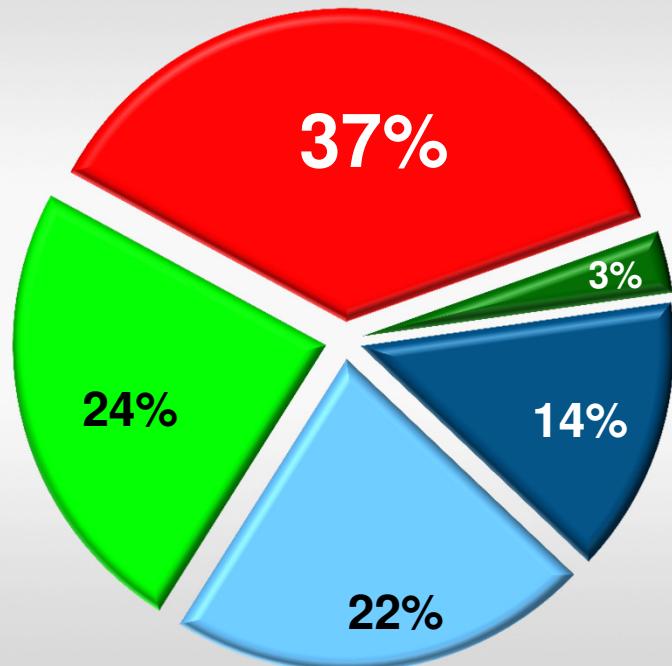
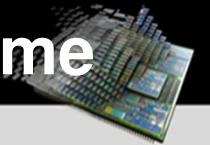
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Where Designers Spend Their Time



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

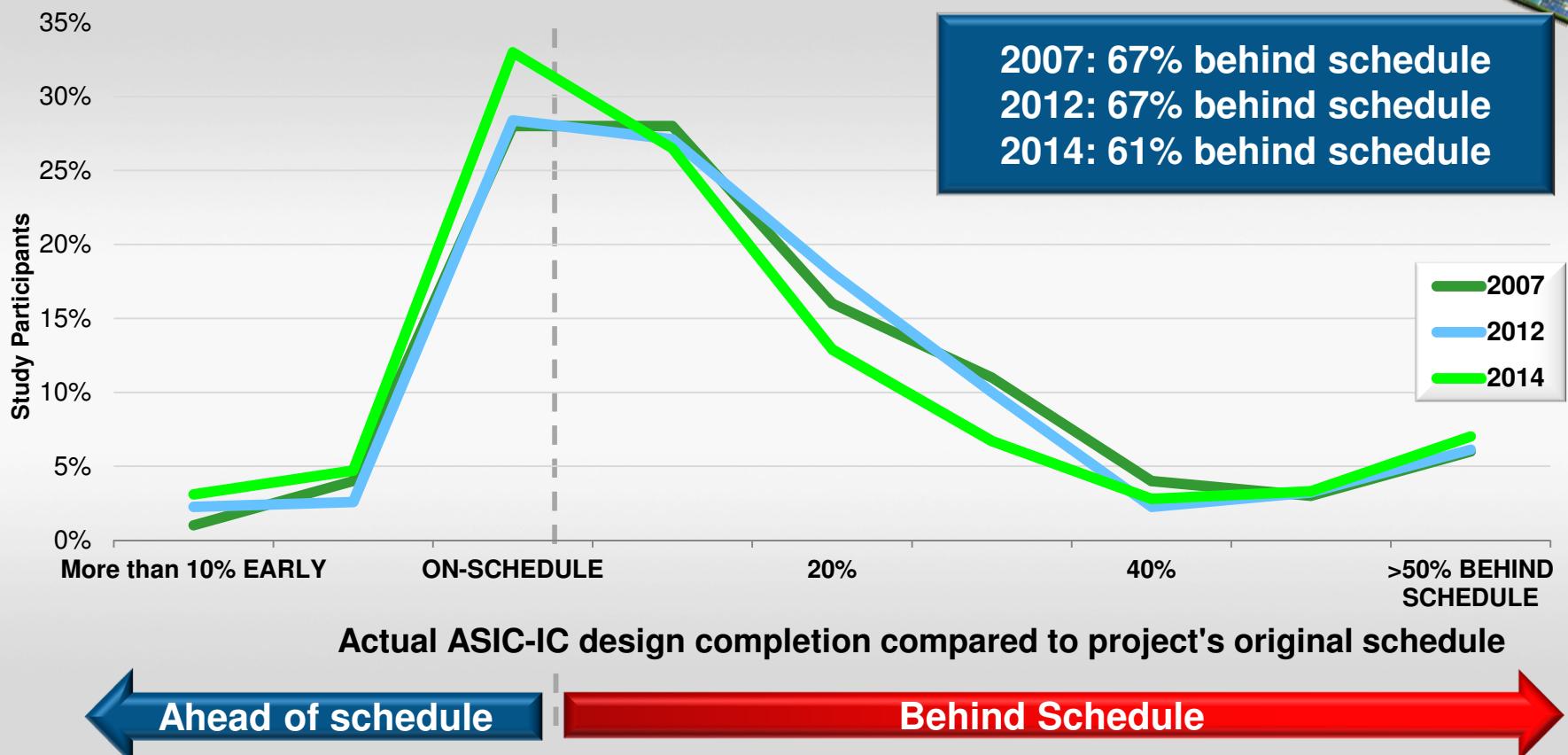
# 2014 Where Verification Engineers Spend Their Time



- Test Planning
- Testbench Development
- Creating Test and Running Simulation
- Debug
- Other

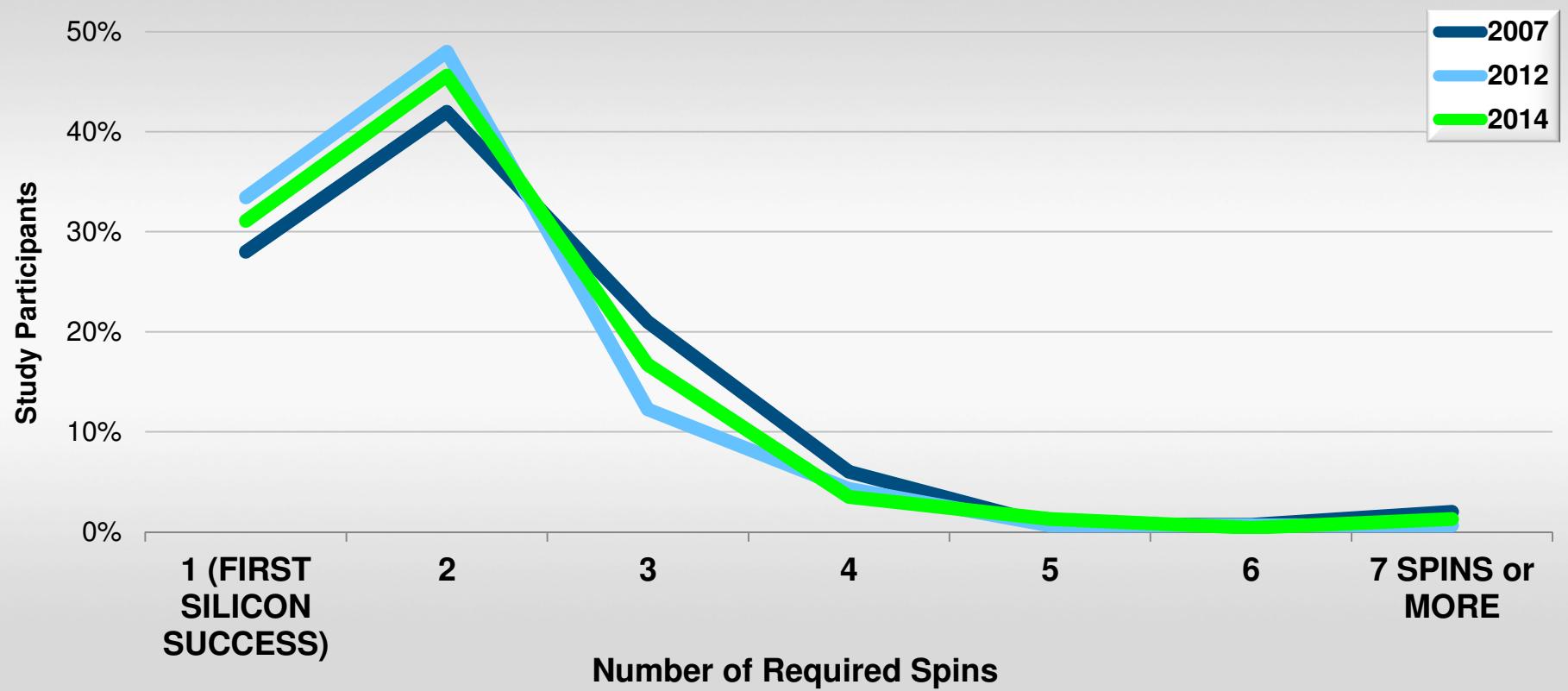
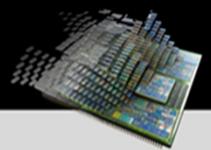
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Many Projects Miss Schedule



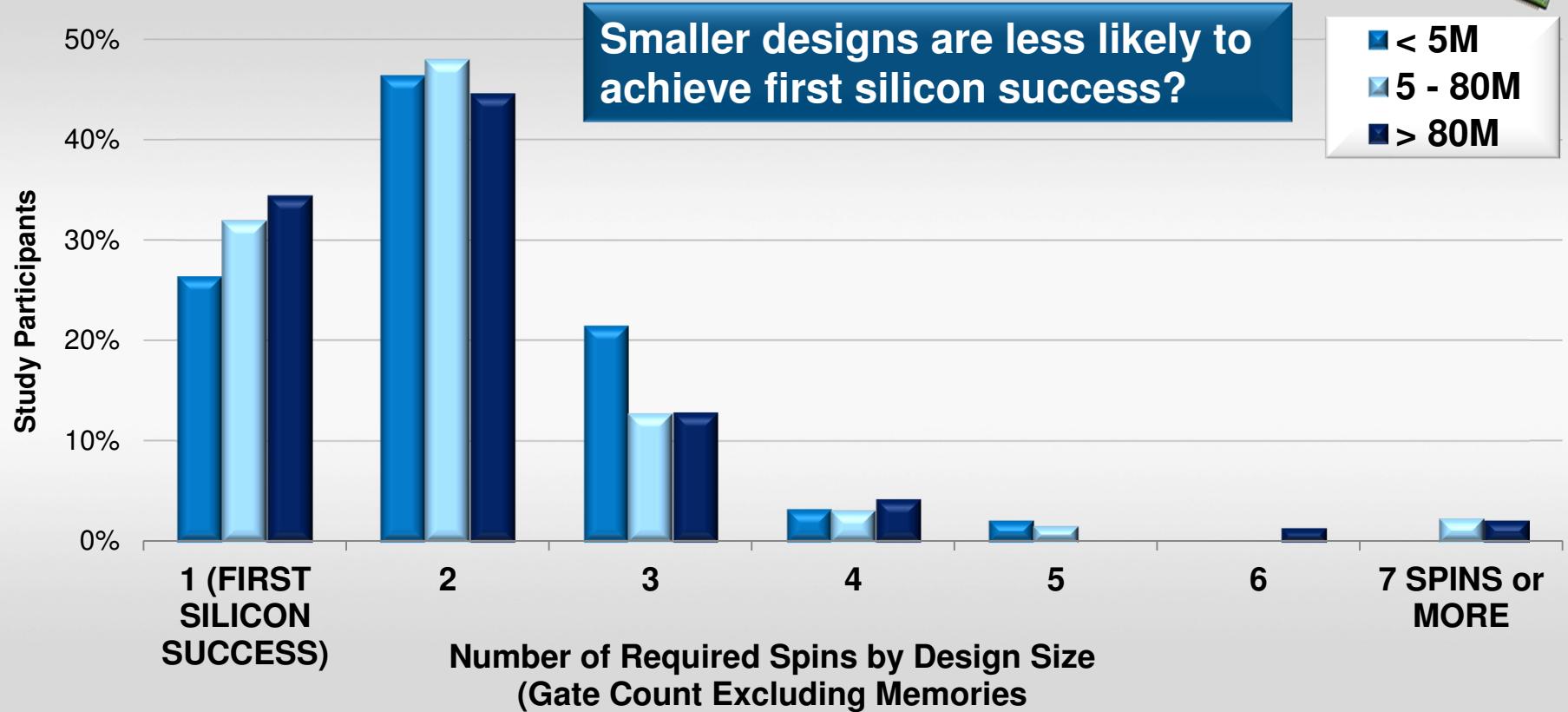
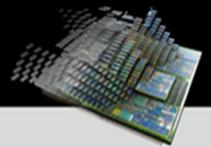
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Few Designs Achieve First Silicon Success



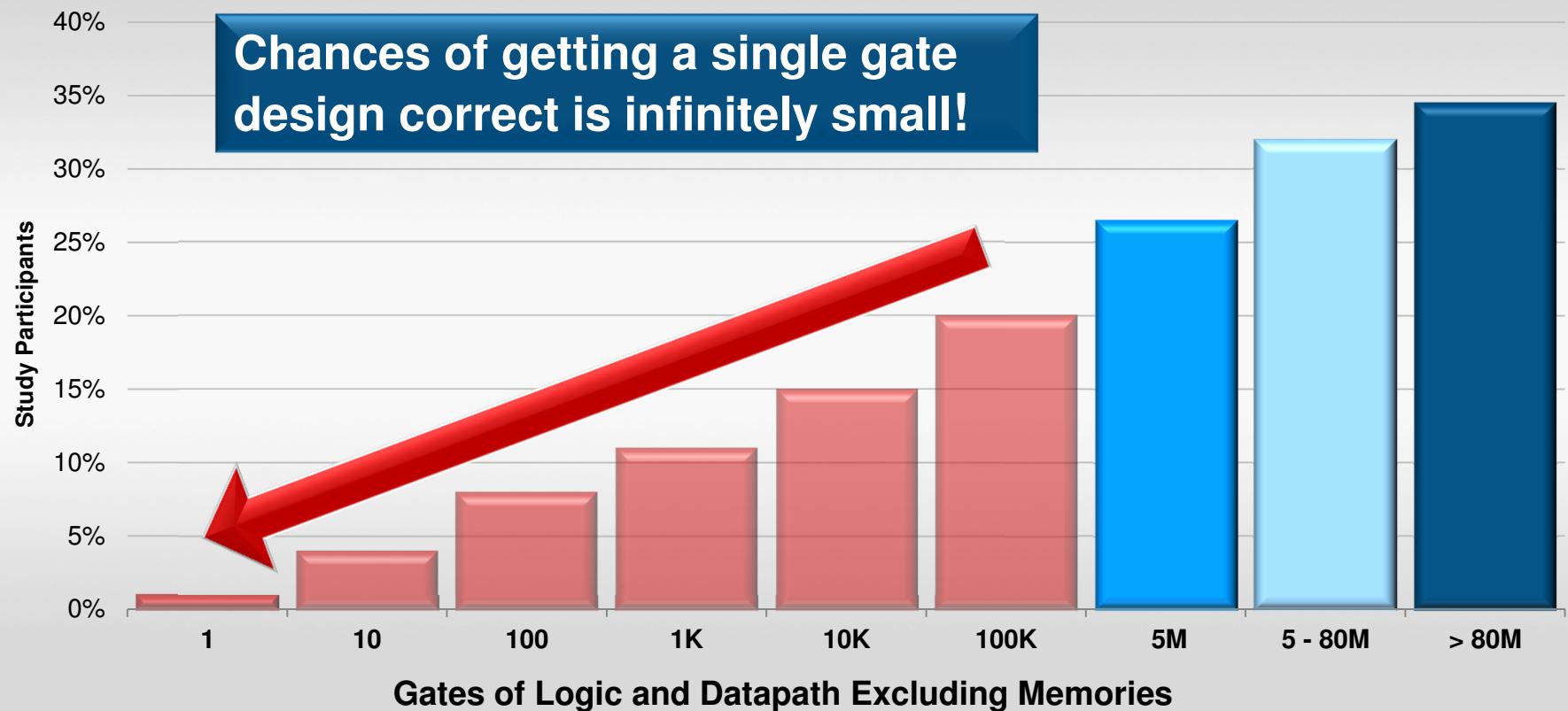
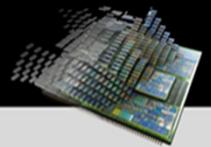
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# 2014 Number of Spins by Design Size

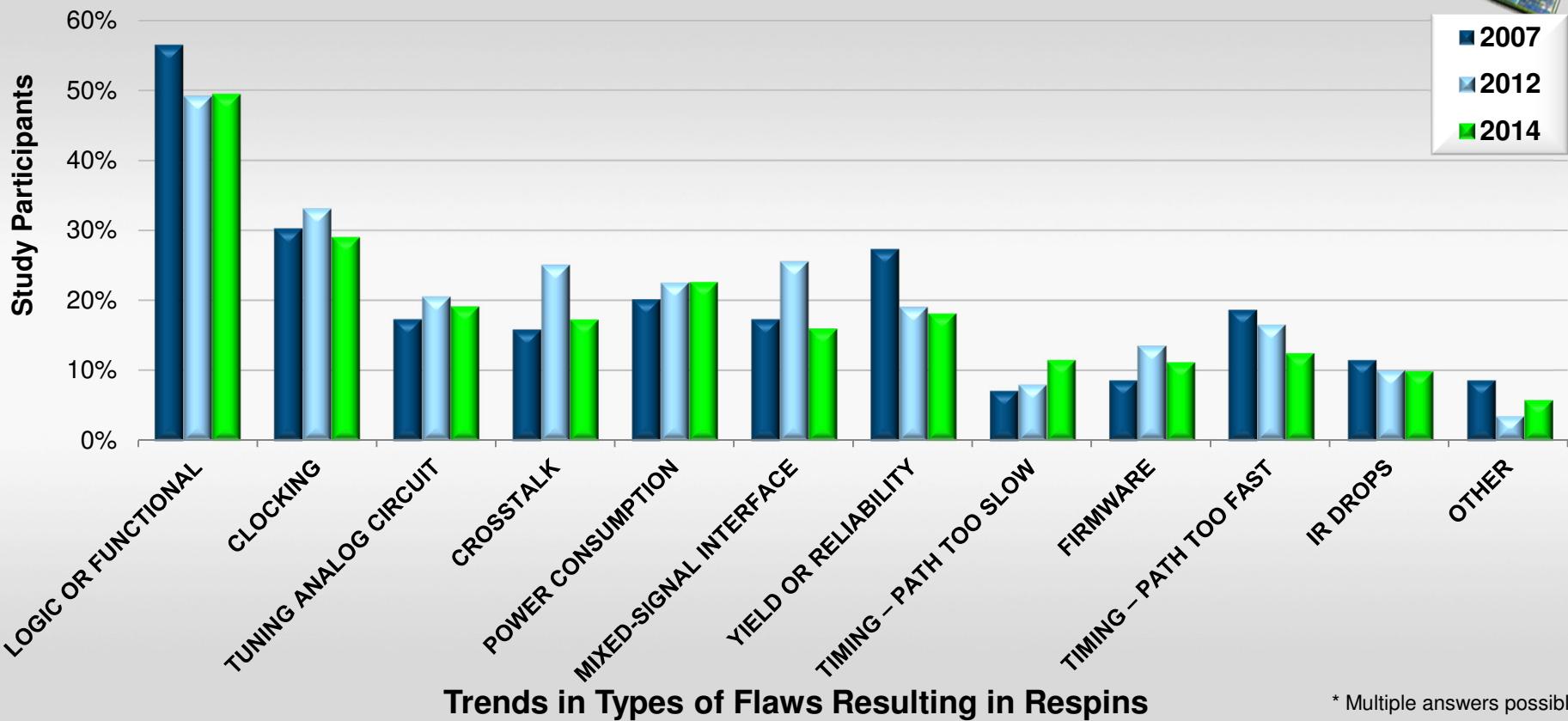
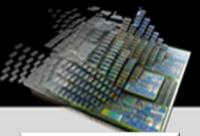


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# 2014 First Silicon Success by Design Size



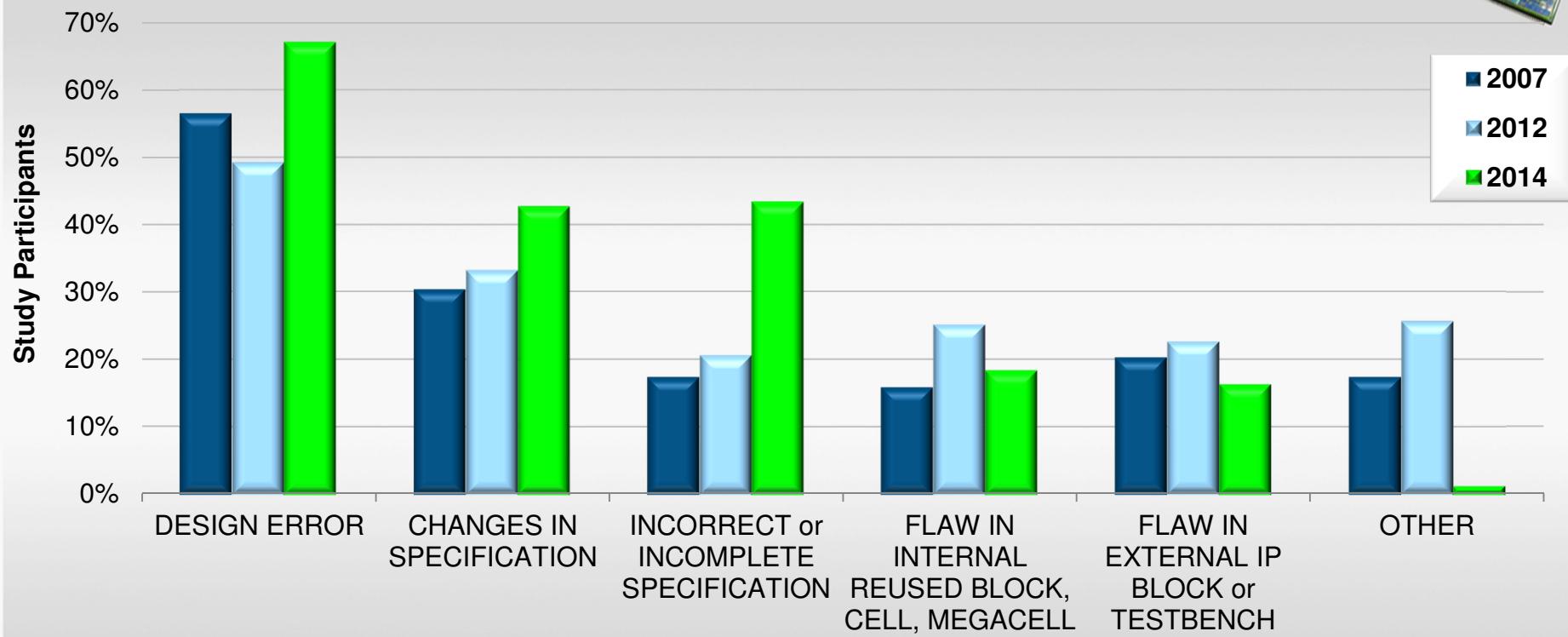
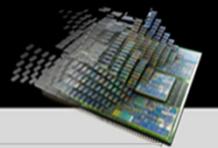
# Flaws Contributing to Respins



\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Root Cause of Functional Flaws

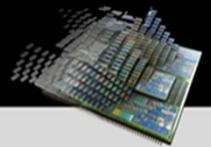


## Root Cause of Functional Flaws

\* Multiple answers possible

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# Verification Layer Trends



**Software**

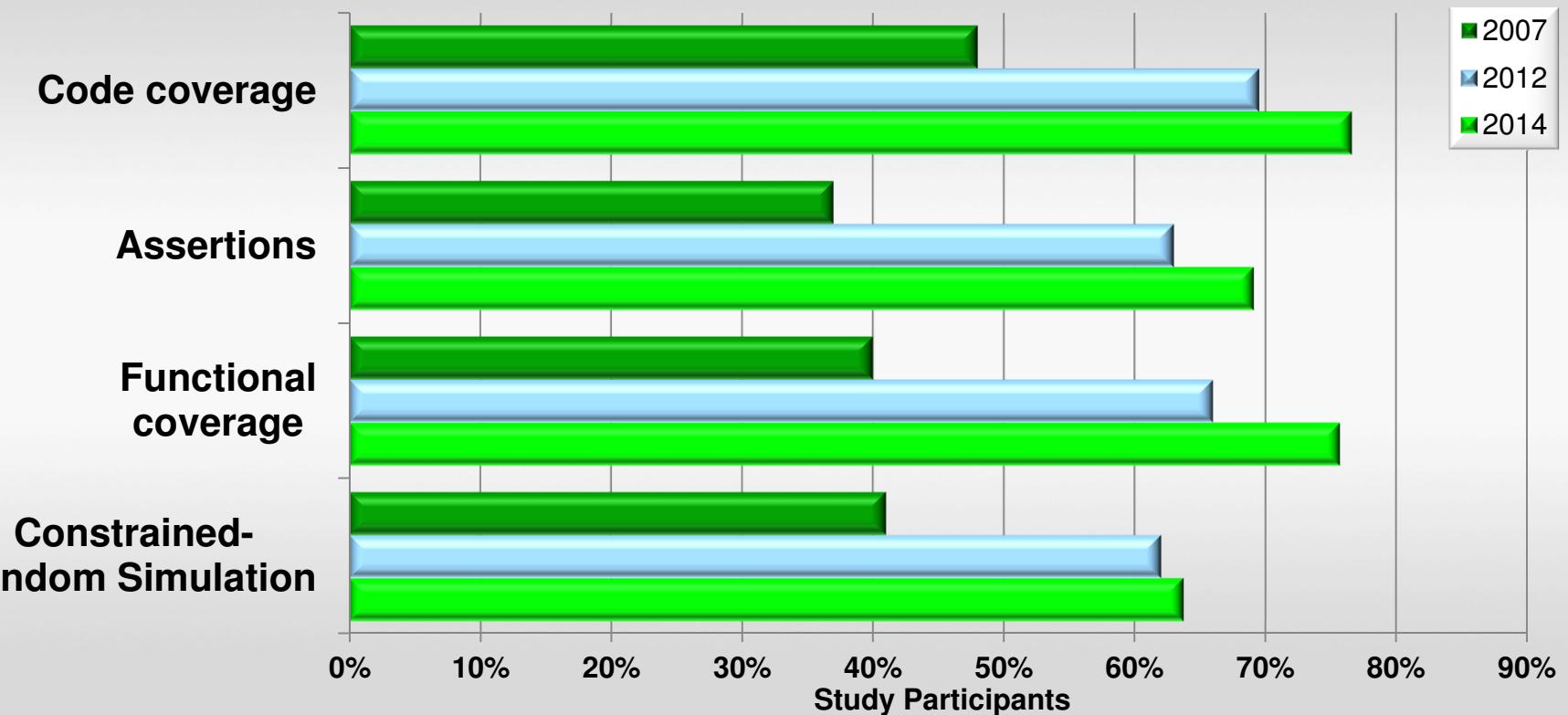
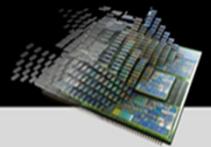
**Security Domains**

**Power Domains**

**Clock Domains**

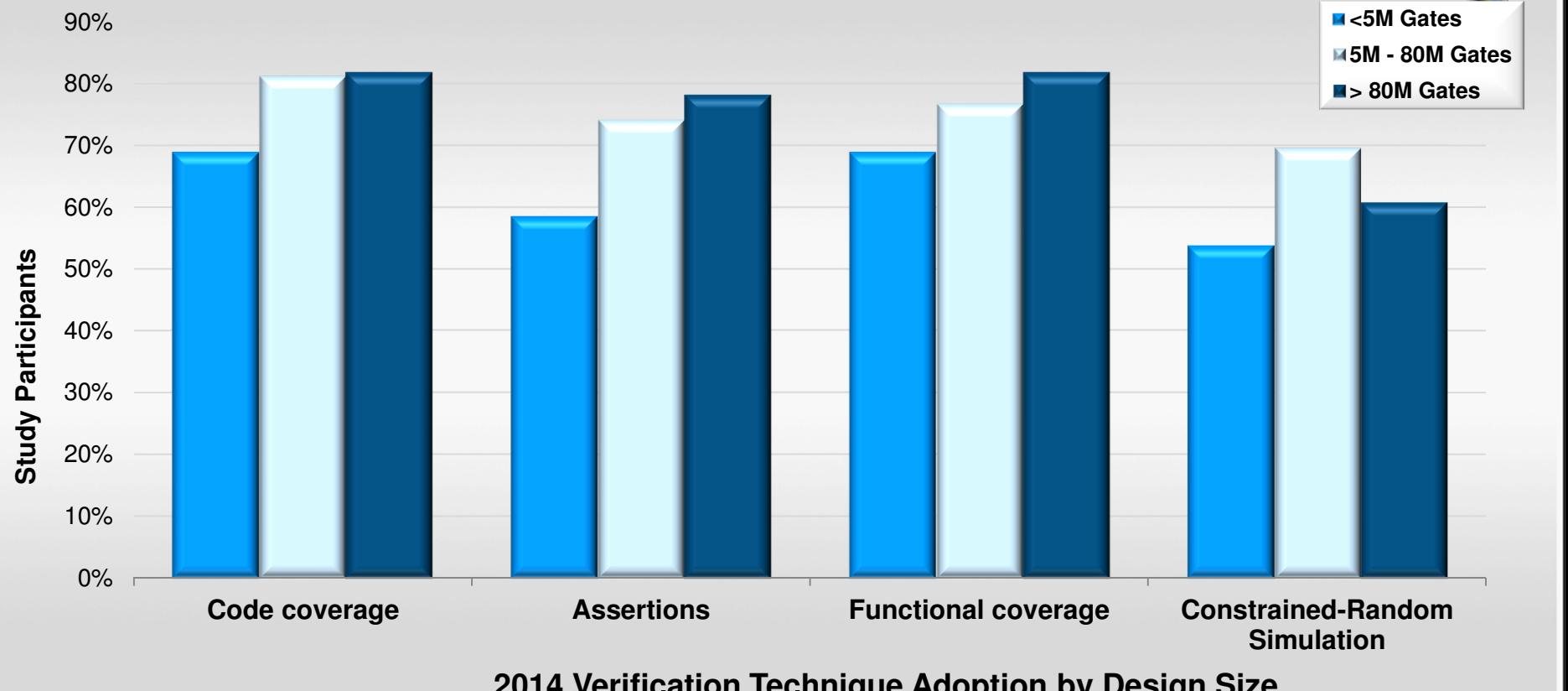
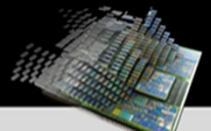
**Functional**

# Trends in Verification Techniques



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

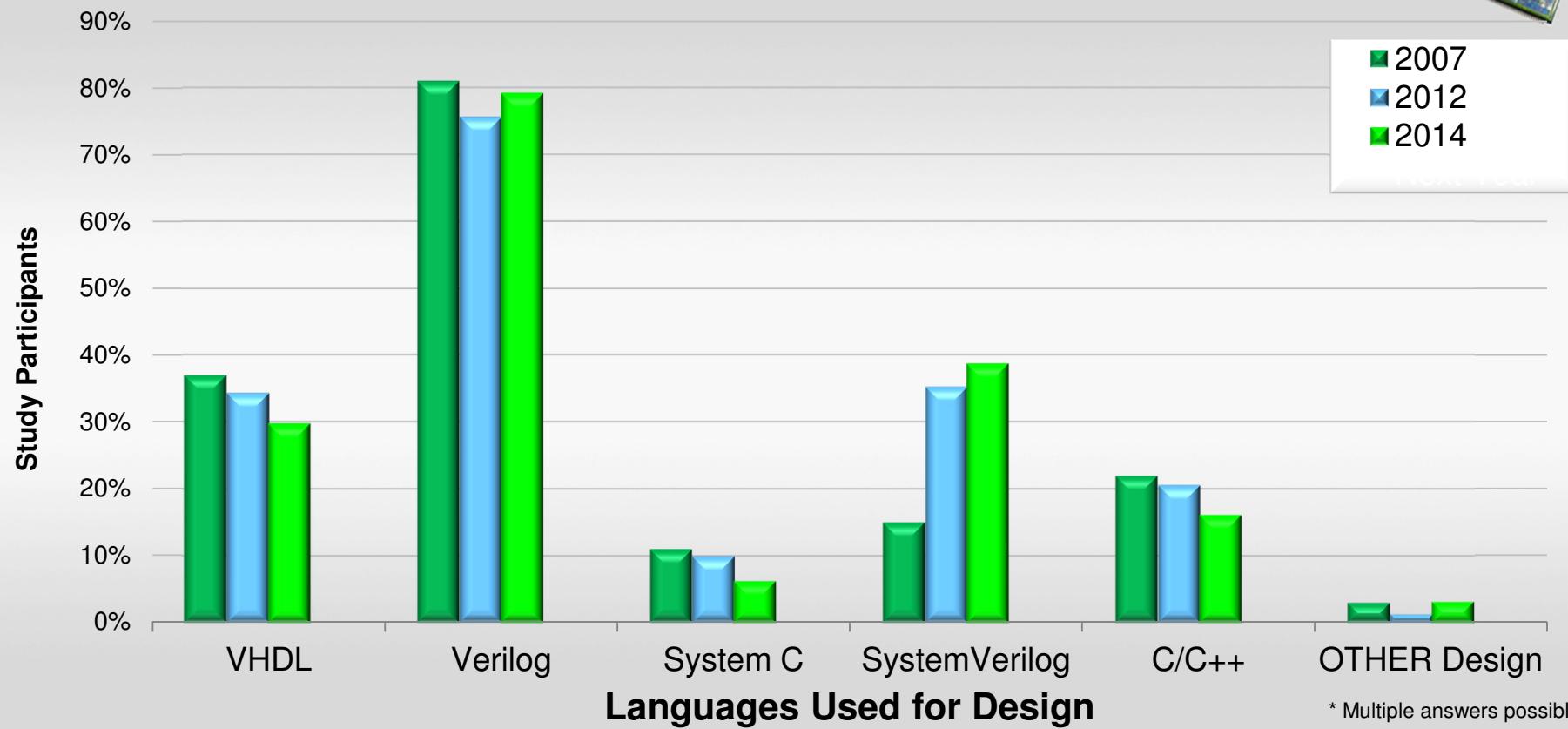
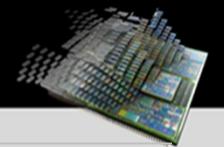
# Verification Technique Adoption by Design Size



2014 Verification Technique Adoption by Design Size

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

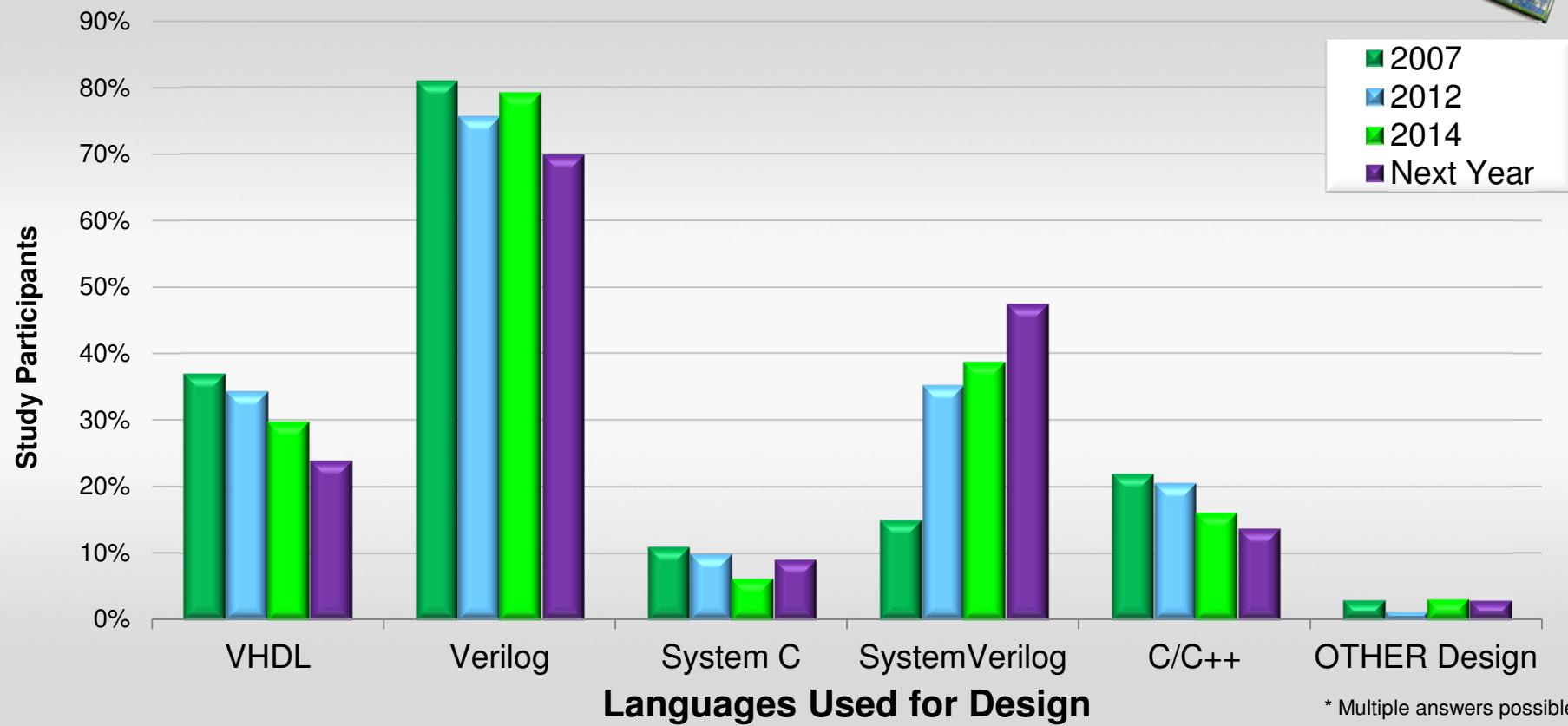
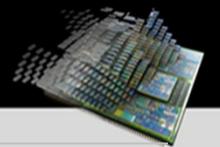
# Design Language Adoption Trends



\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

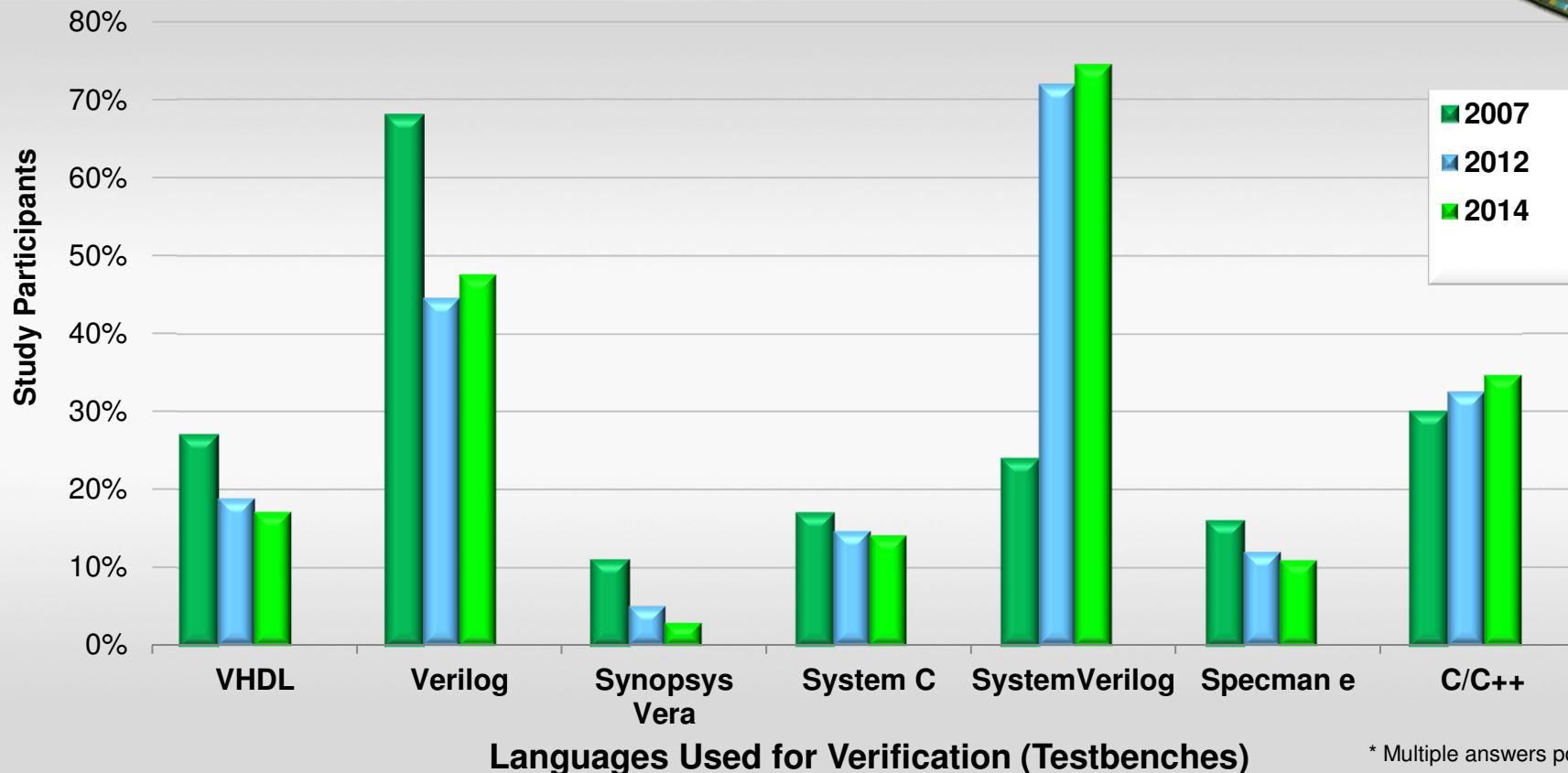
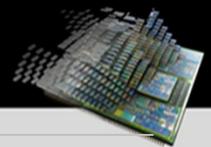
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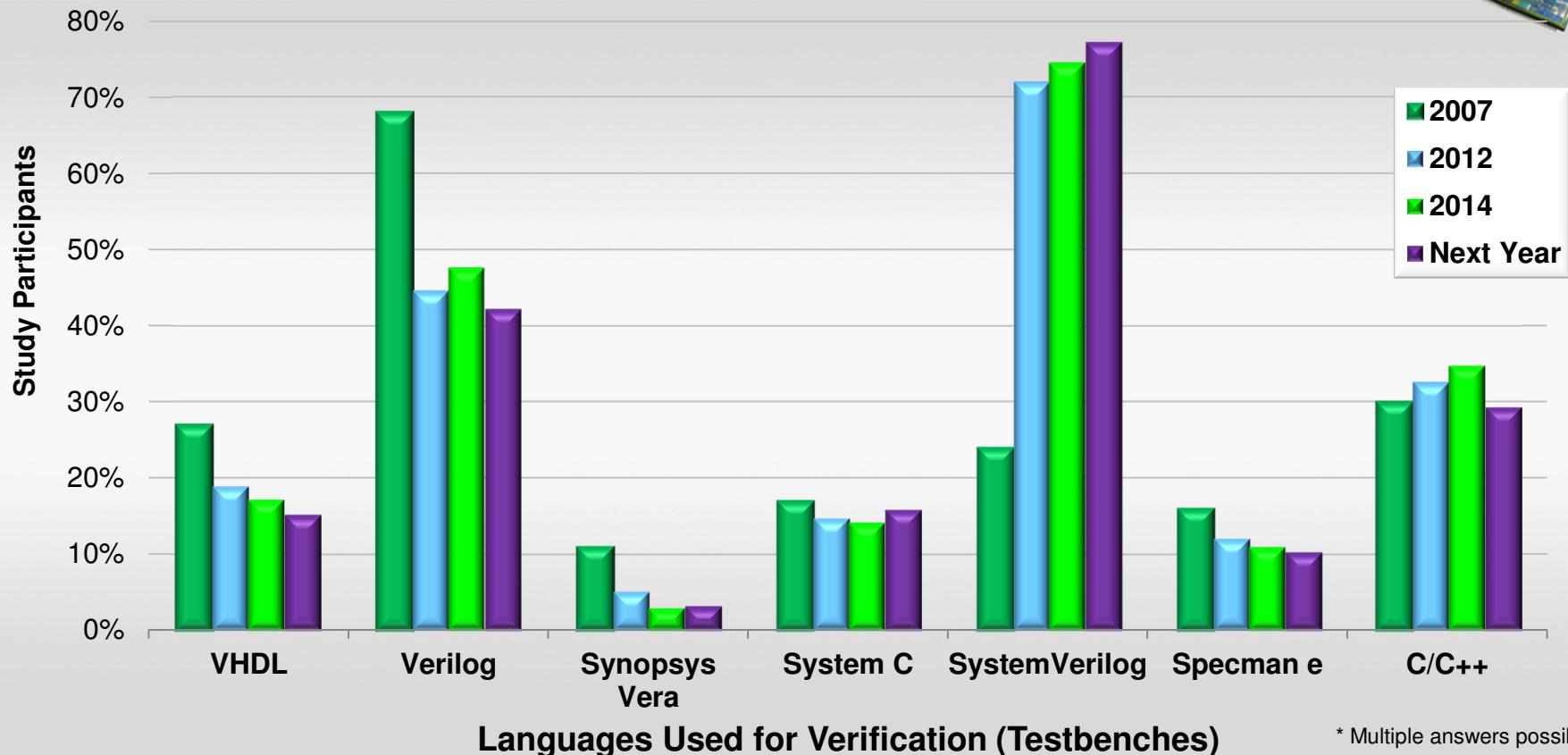
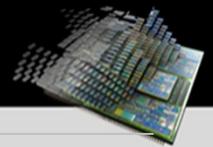
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Verification Language Adoption Trends



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

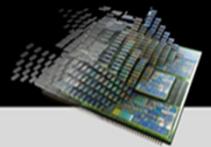
# Verification Language Adoption Trends



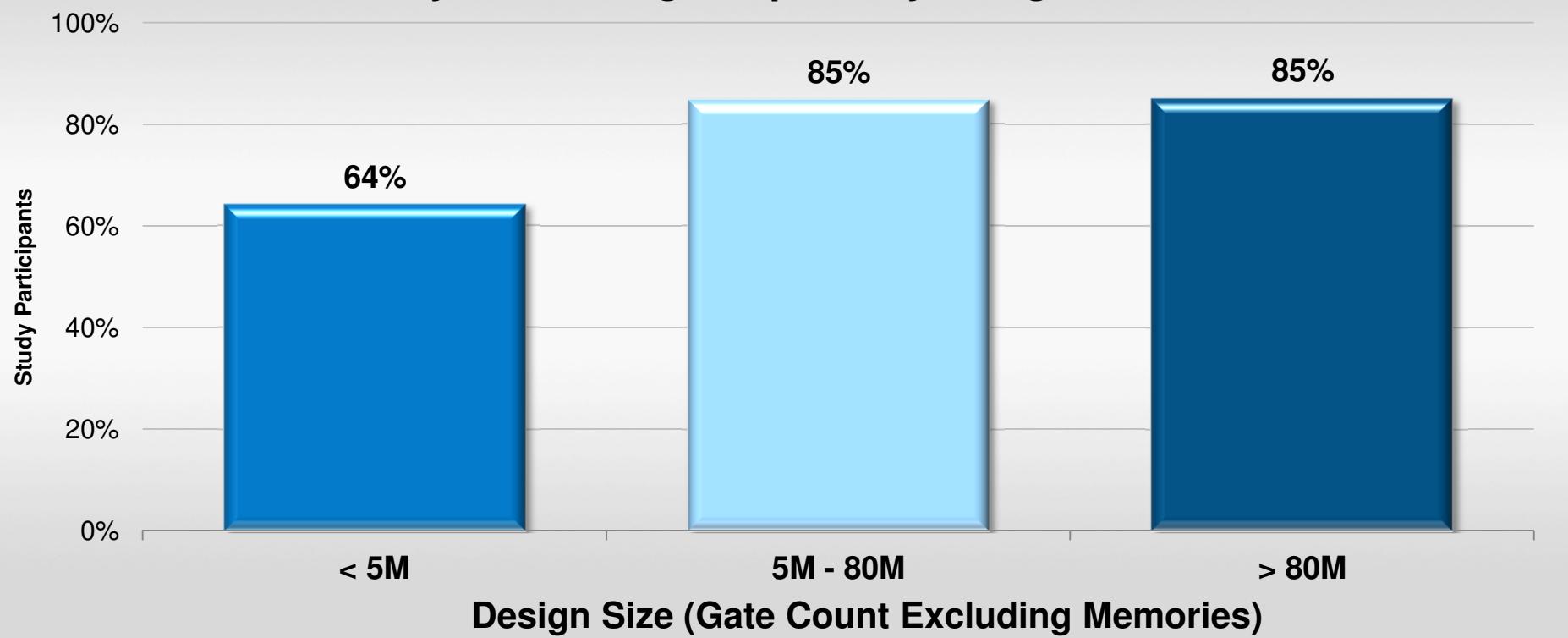
\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# SystemVerilog is Mainstream

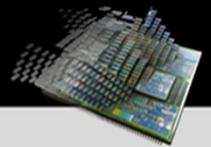


SystemVerilog Adoption by Design Size

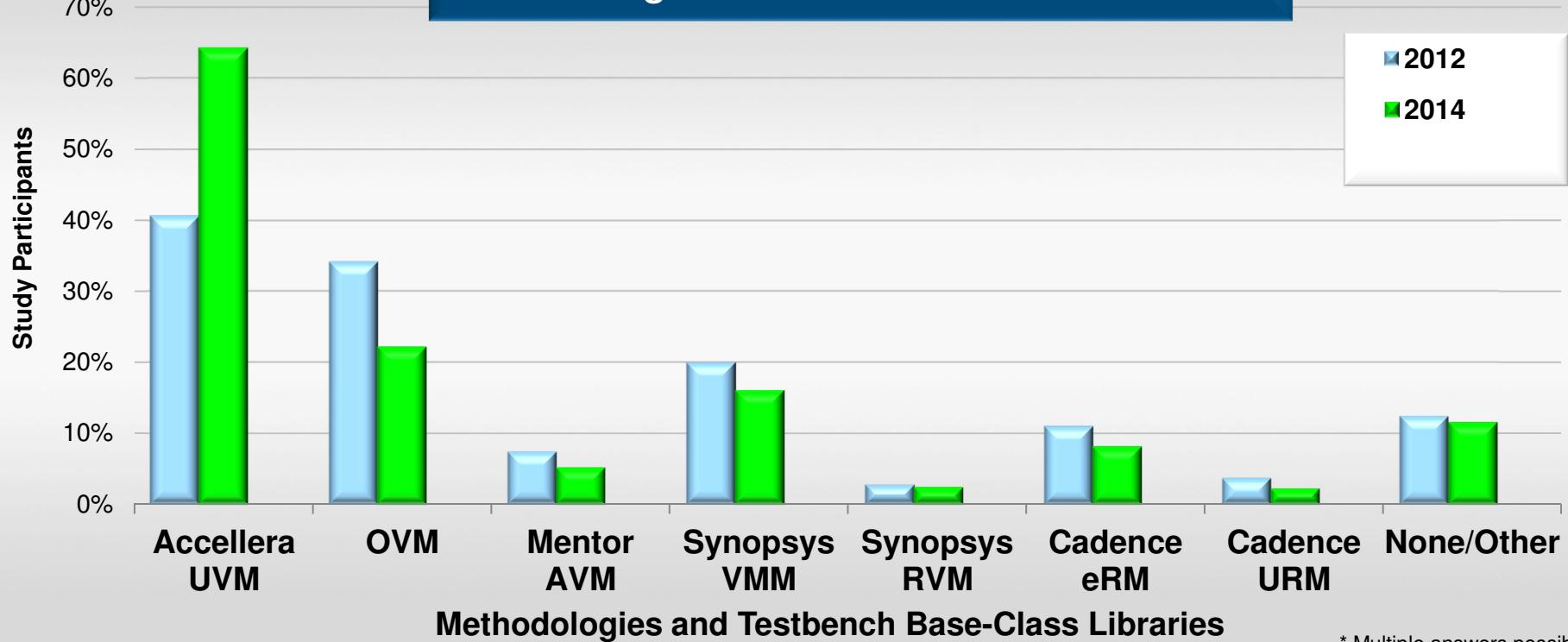


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Testbench Methodology Adoption Trends



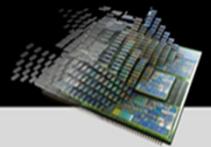
56% UVM growth between 2012 and 2014



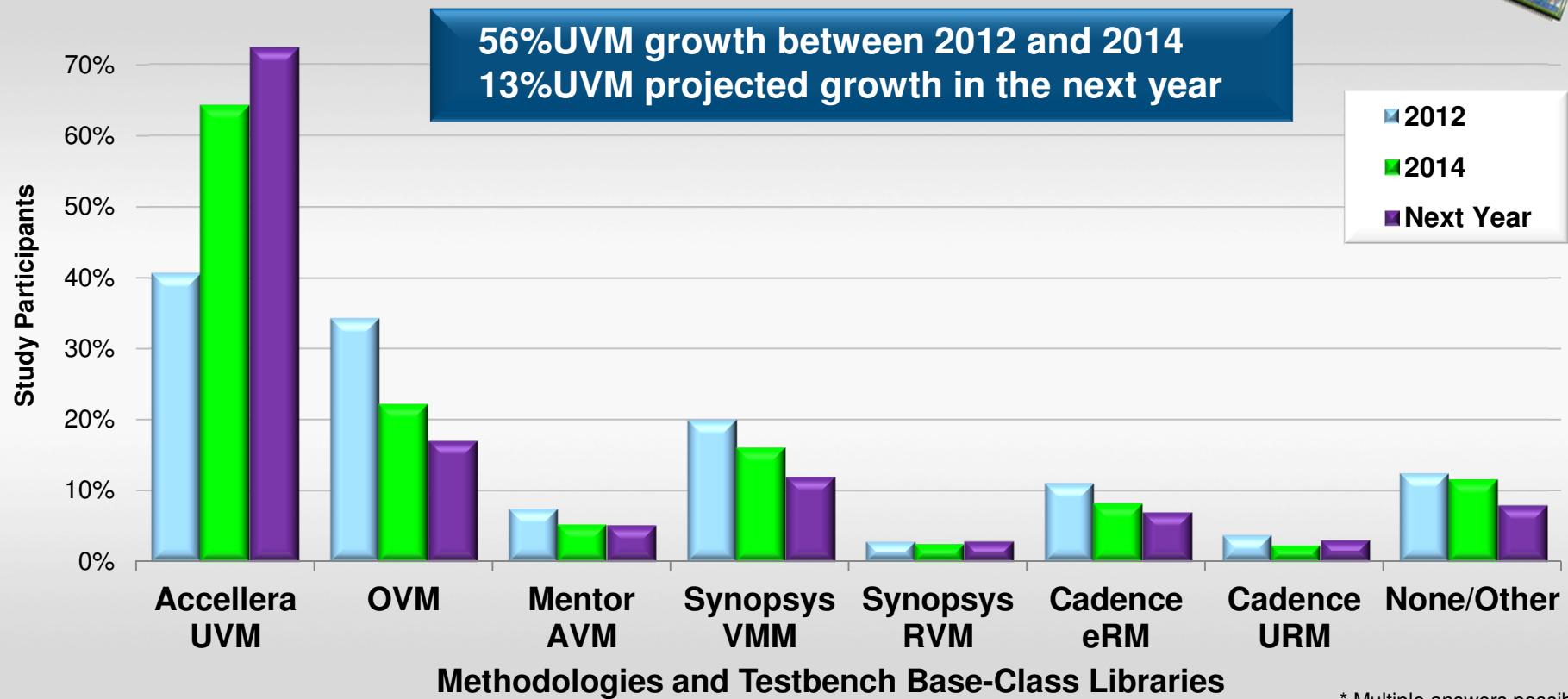
\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Testbench Methodology Adoption Trends



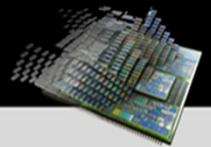
56%UVM growth between 2012 and 2014  
13%UVM projected growth in the next year



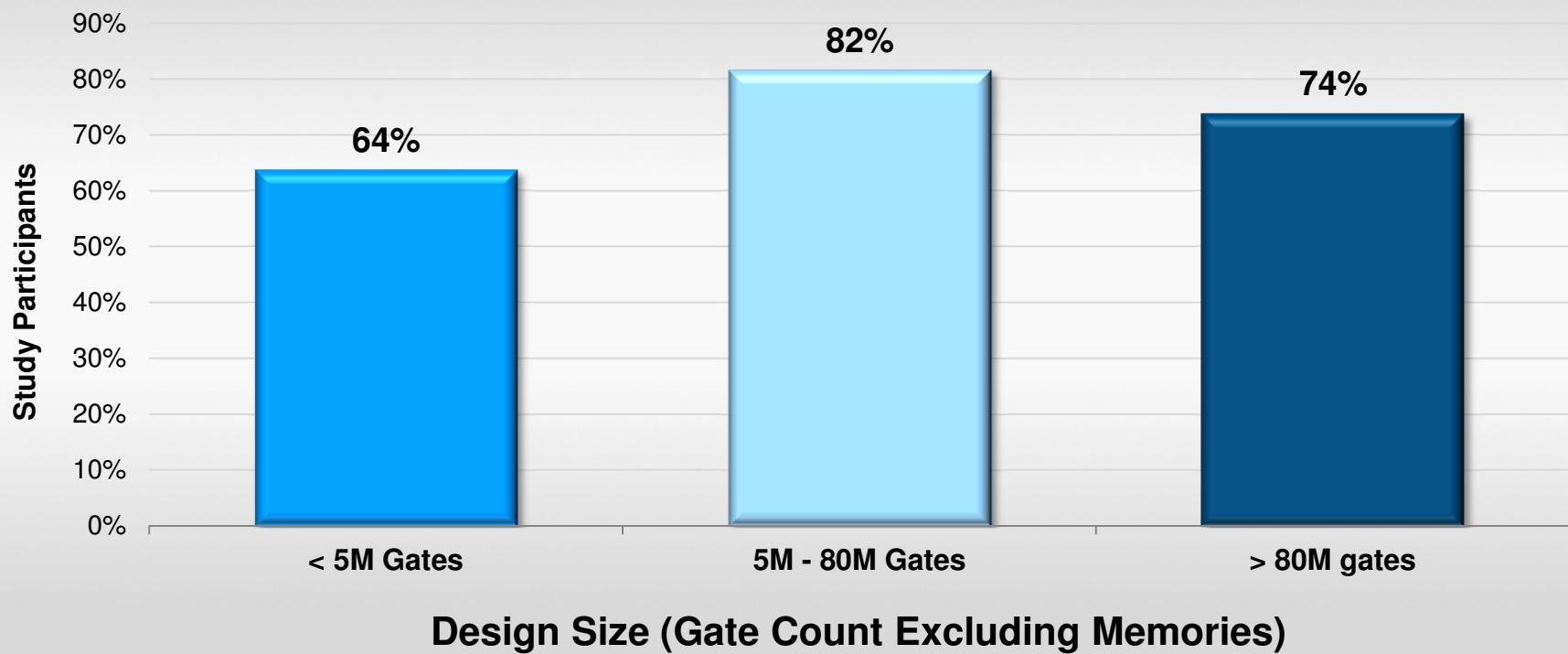
\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# UVM is Mainstream

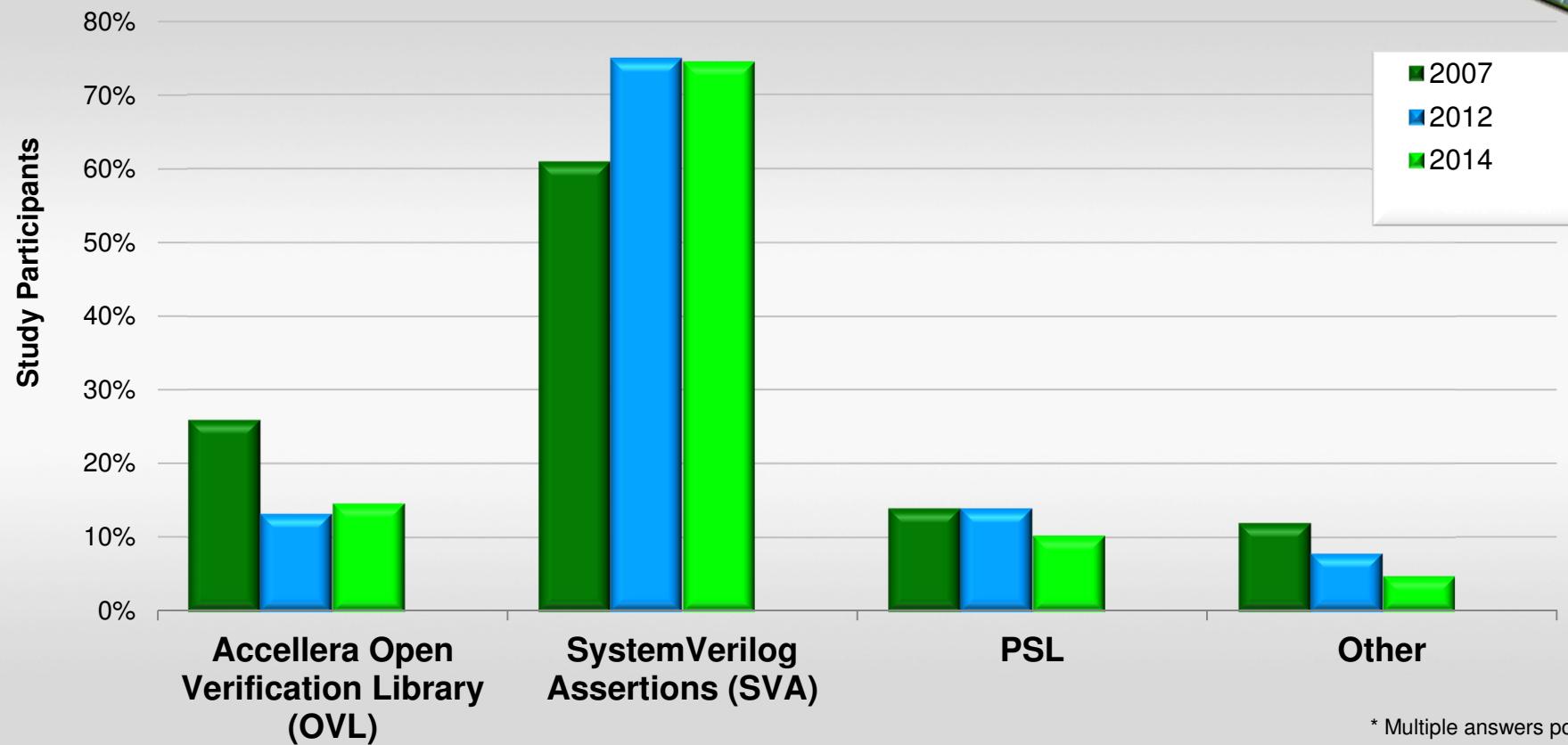
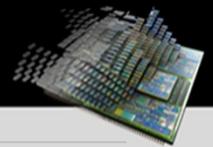


## UVM Adoption by Design Size



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

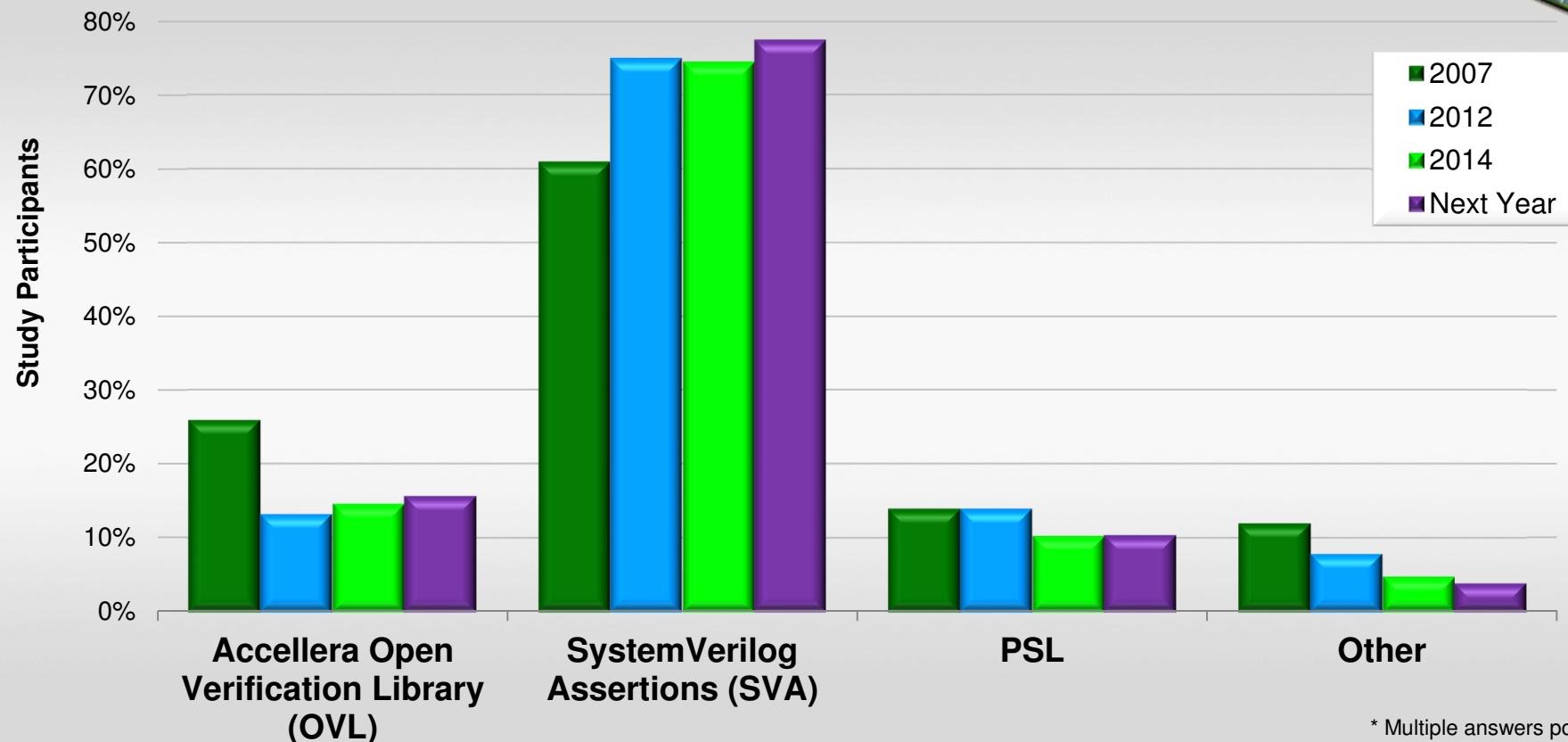
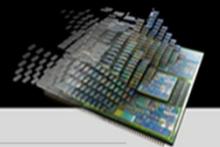
# Assertion Language Adoption



\* Multiple answers possible

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

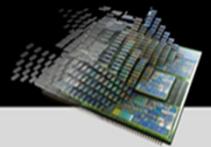
# Assertion Language Adoption



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# Verification Layer Trends



**Software**

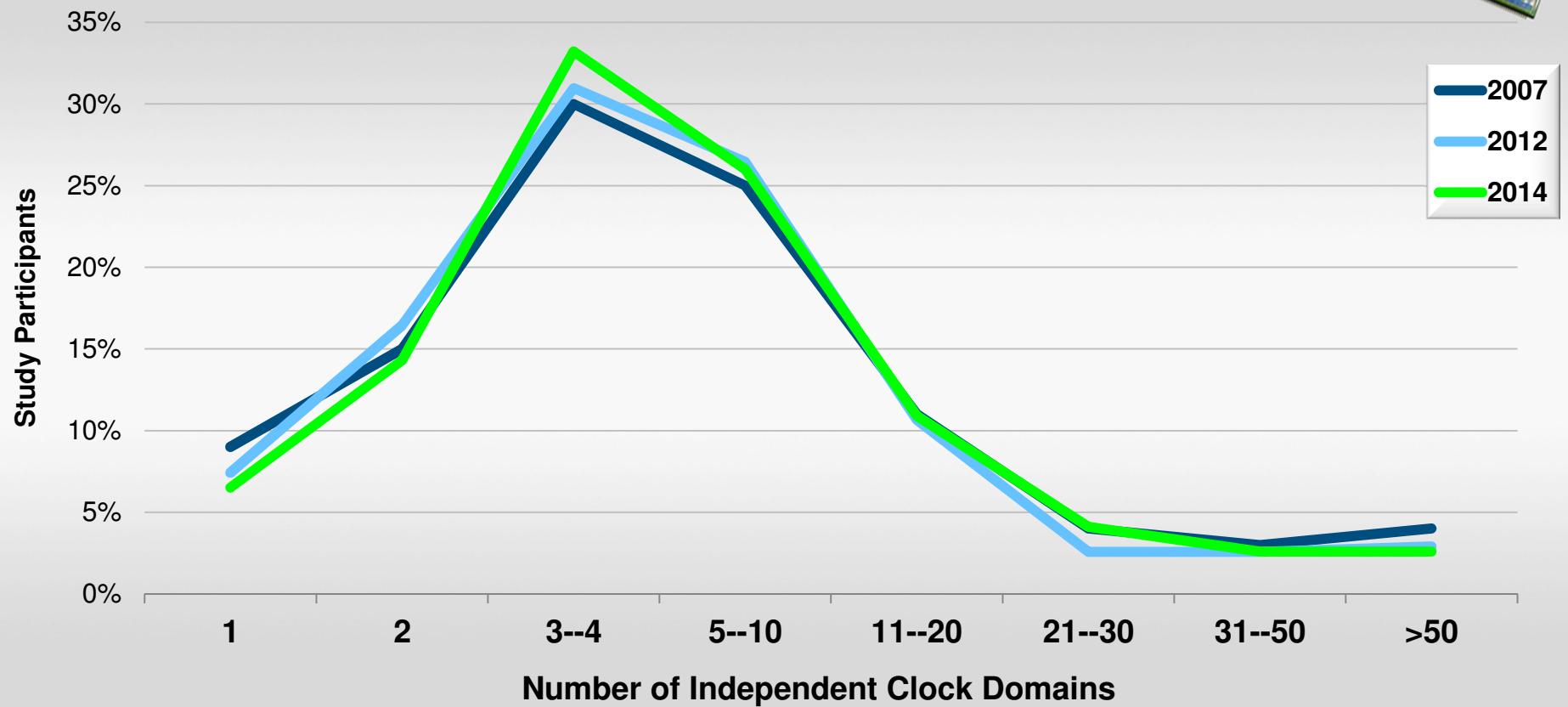
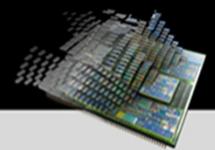
**Security Domains**

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**Clock Domains**

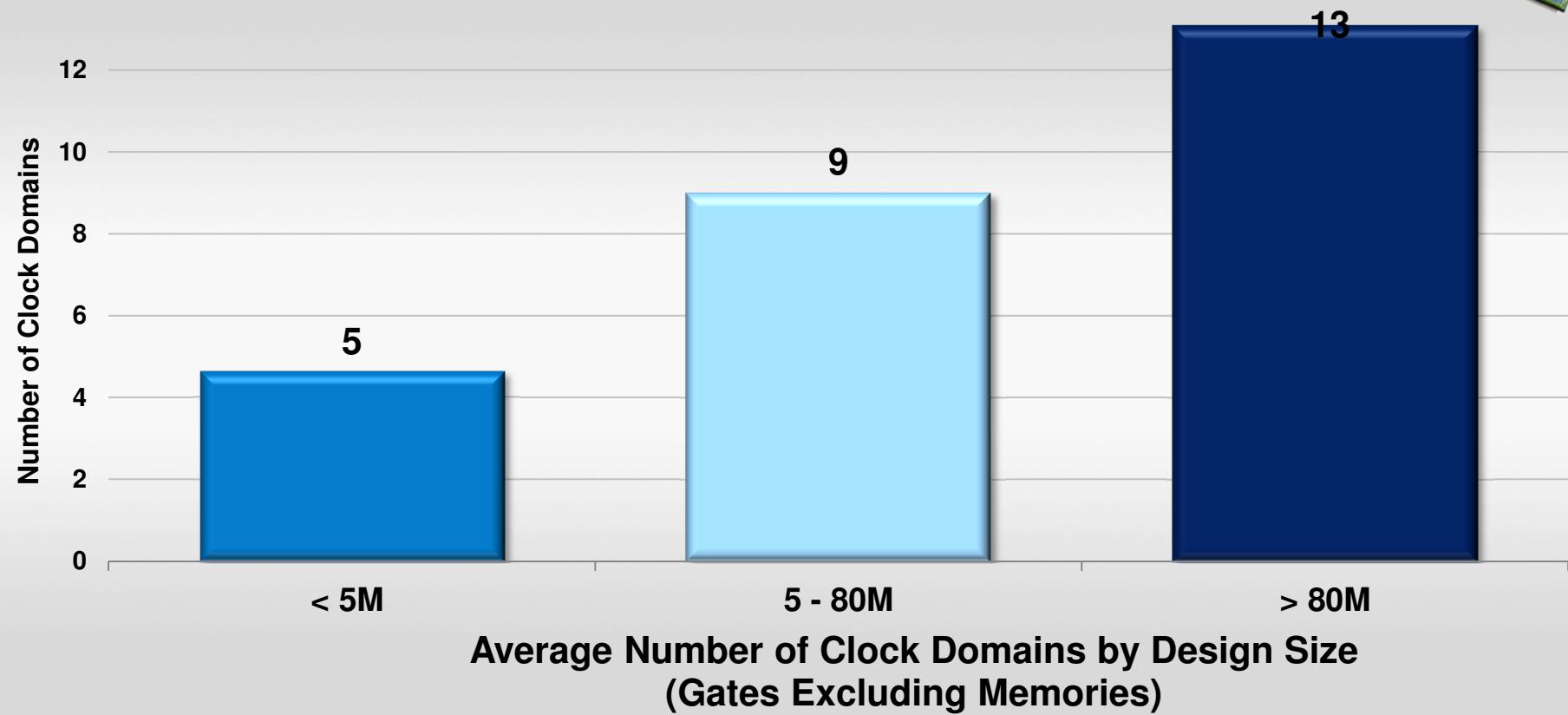
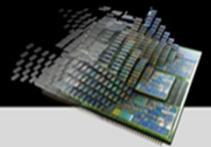
**Functional**

# Multiple Asynchronous Clock Domain Trends



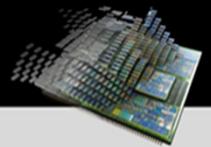
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Large the Design the More Clock Domains



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Verification Layer Trends



**Software**

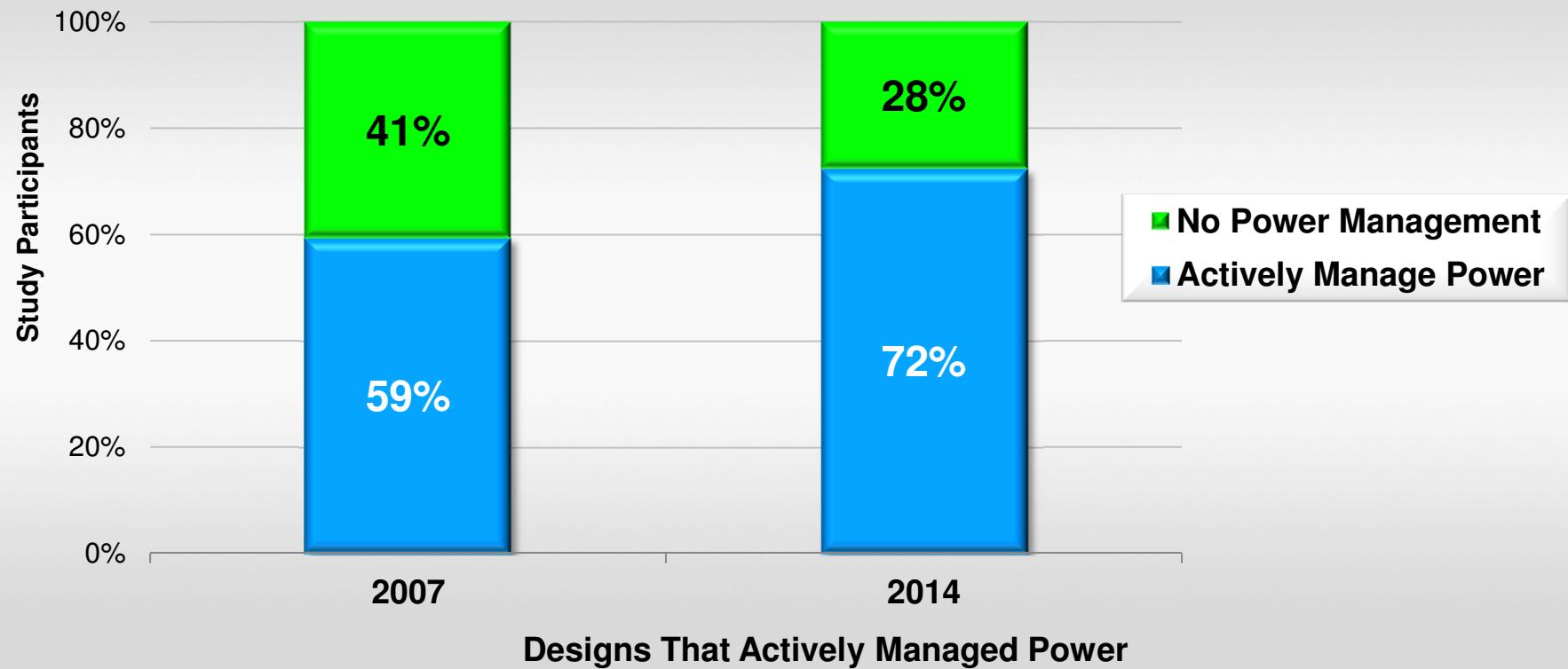
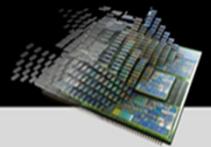
**Security Domains**

**Power Domains**

**Clock Domains**

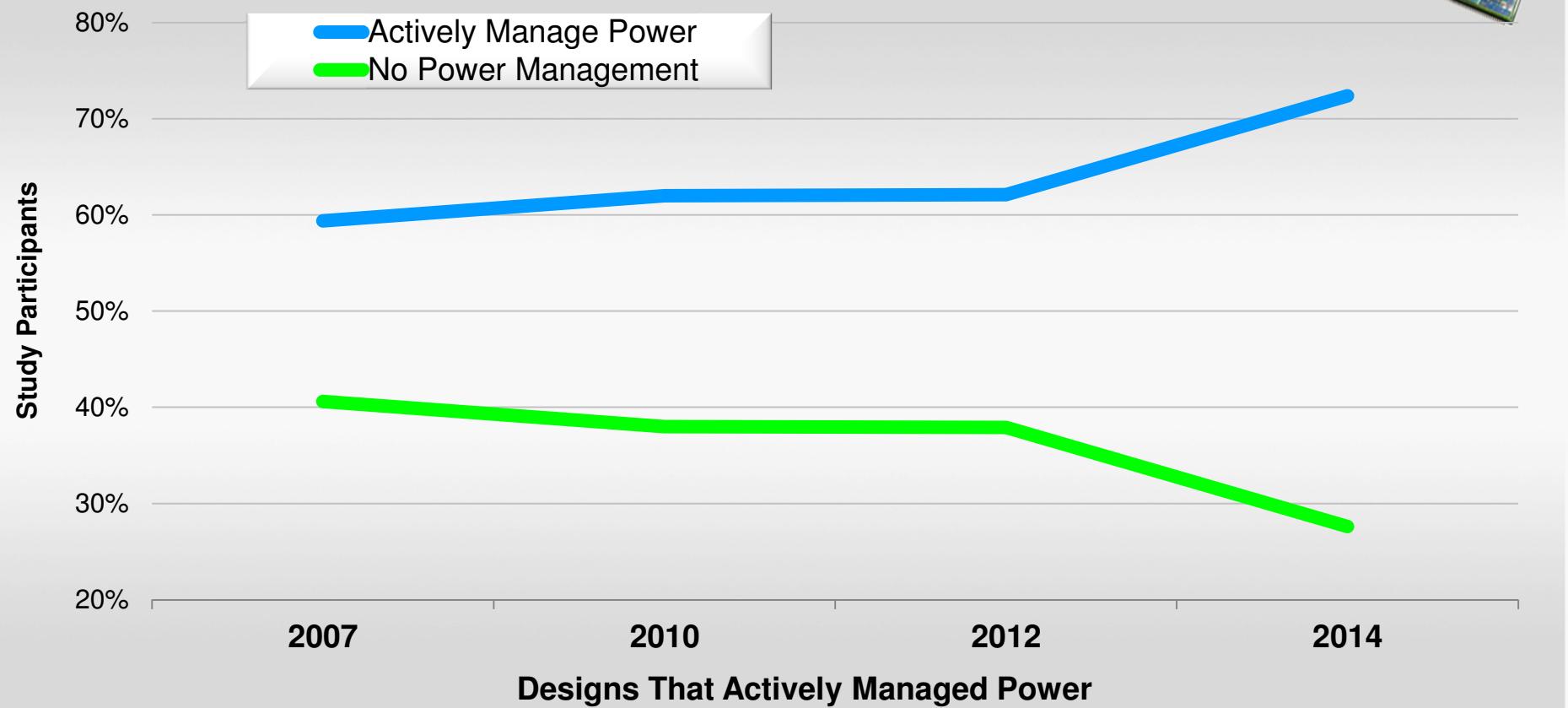
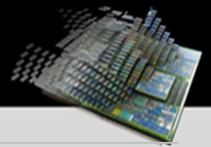
**Functional**

# More Designs Actively Manage Power



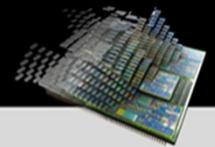
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# 19% Increase in the Past Two Years!

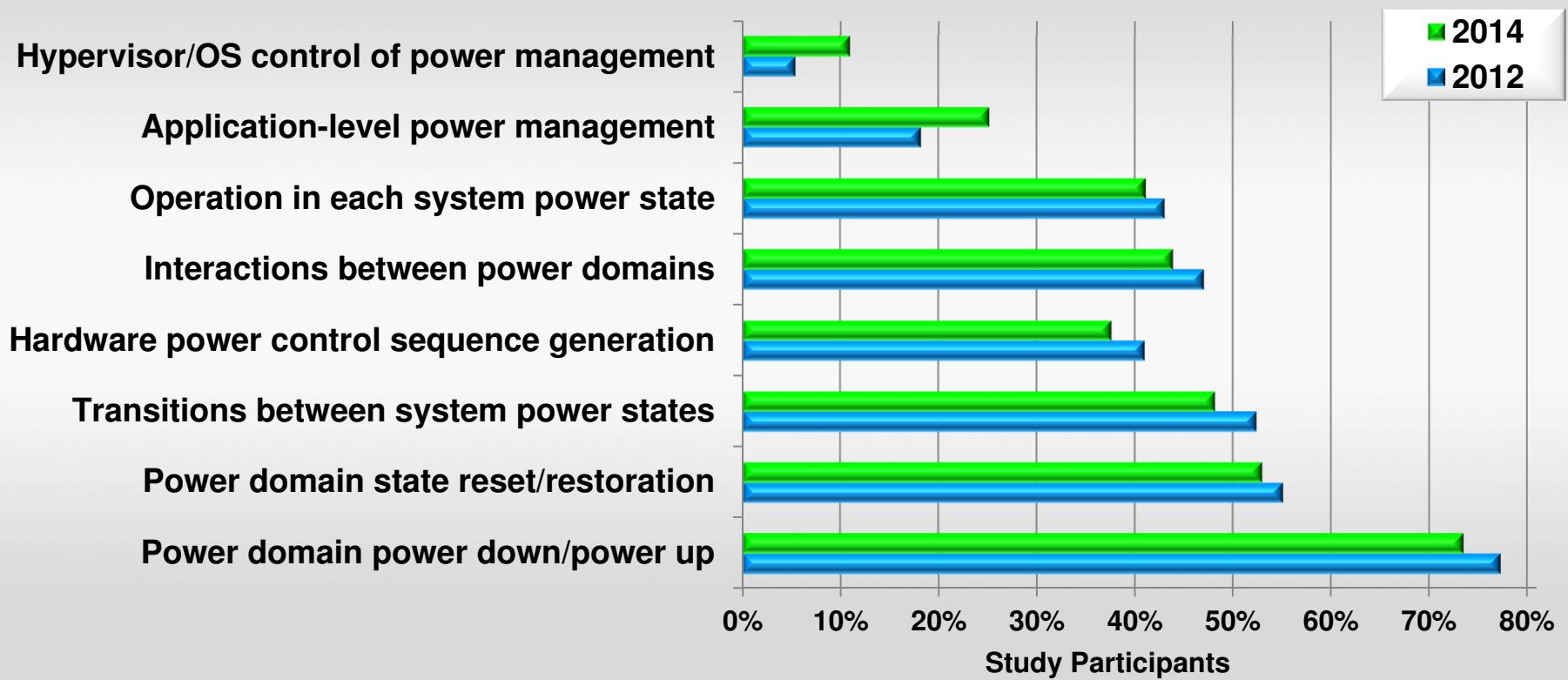


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Power Verification Challenges

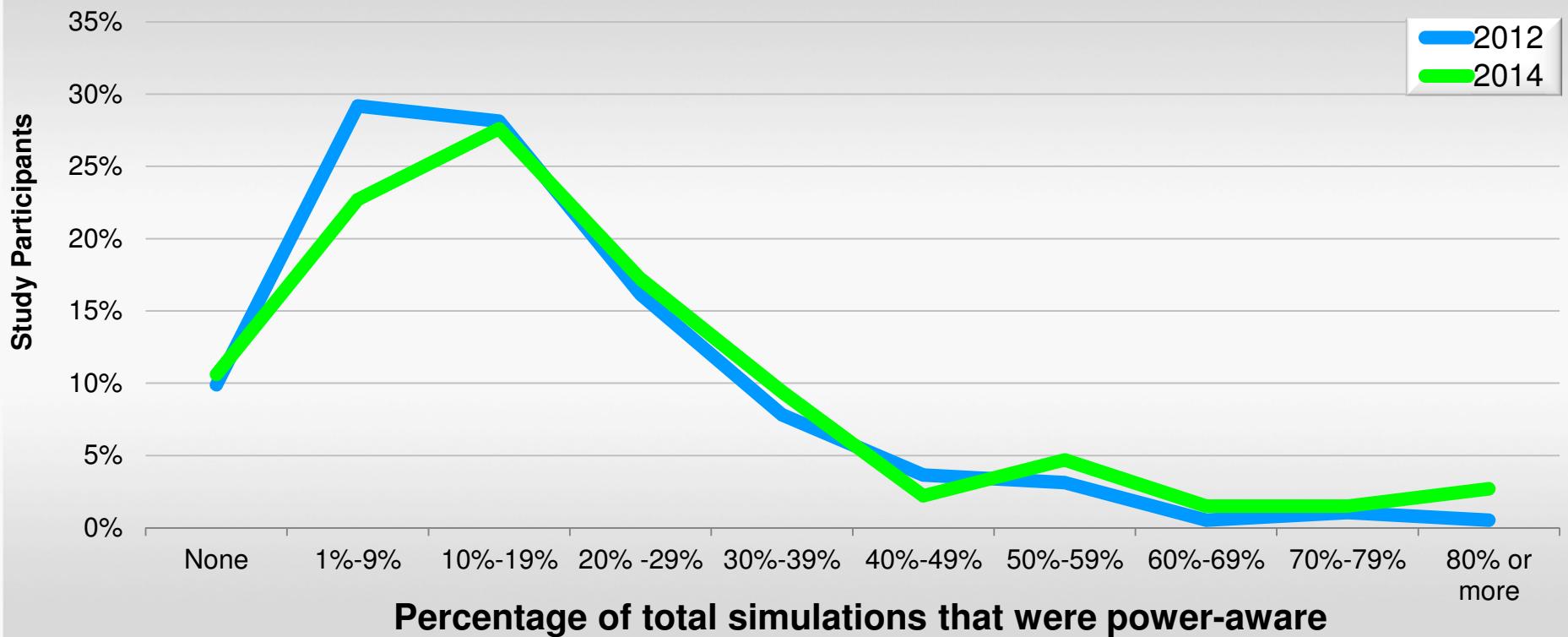


## Aspects of Power Managed Design that are Verified



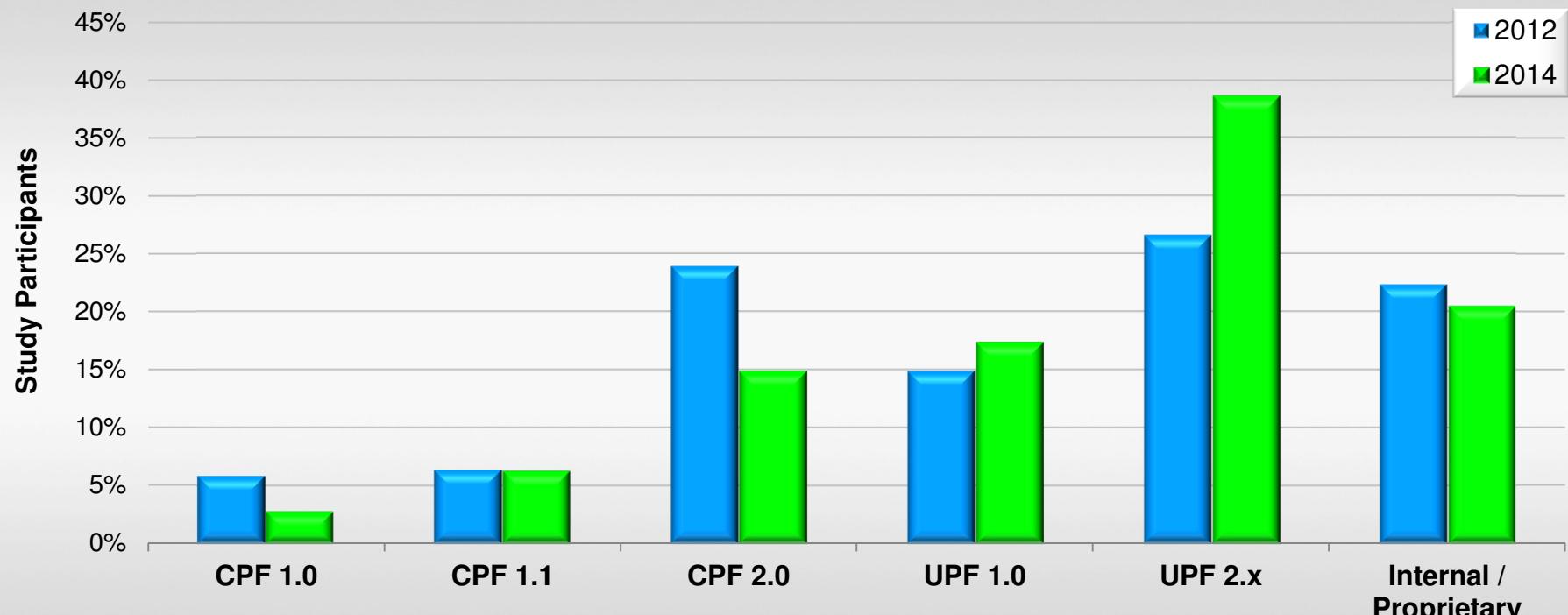
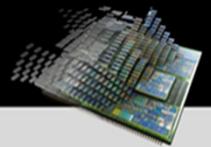
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Number of Simulations Focused on Power Verification



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

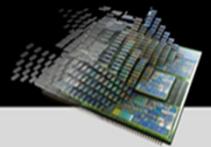
# Power Intent Standards Trends



## Notation Used to Describe Power Intent

Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Verification Layer Trends



Software

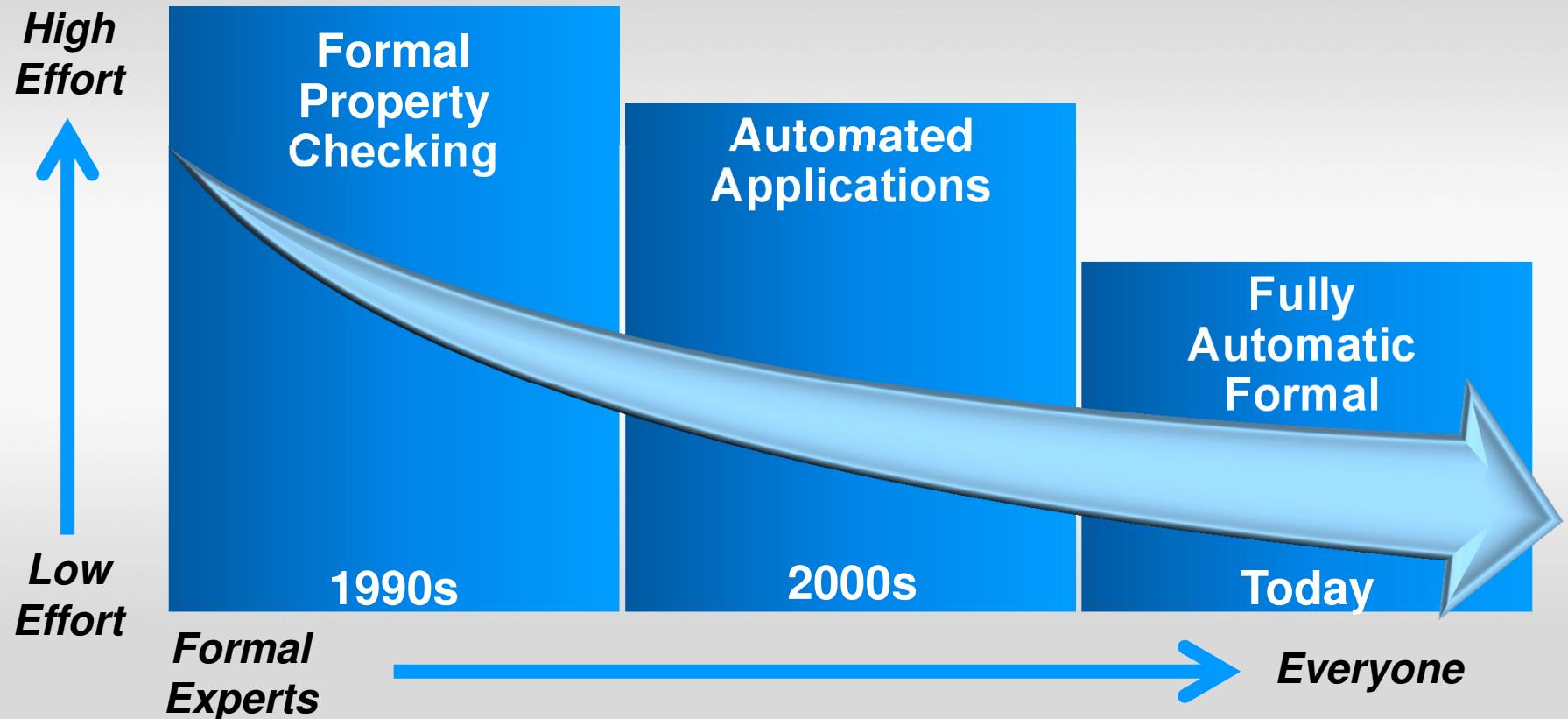
**Security Domains**

Power Domains

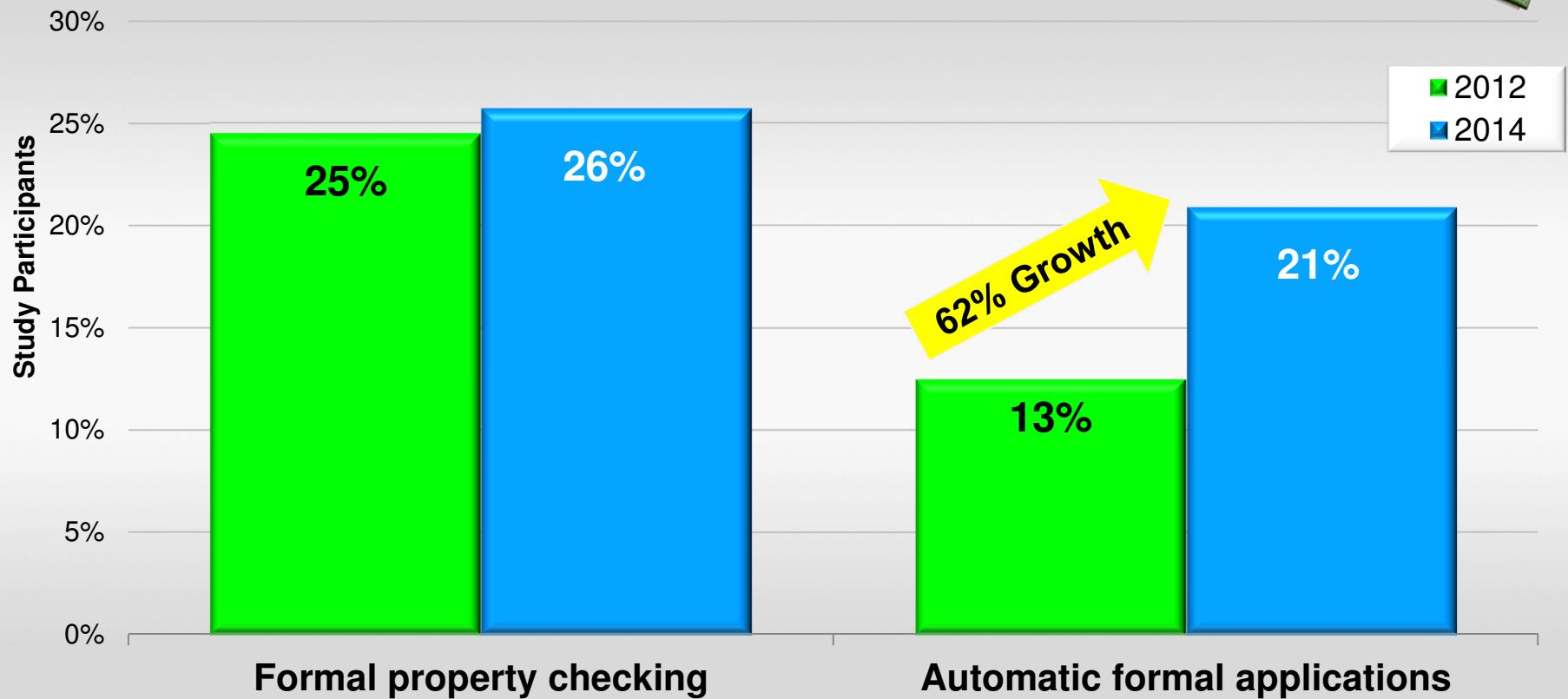
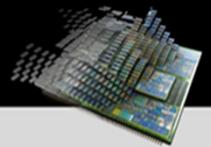
Clock Domains

Functional

# Formal Verification—Not Just for Experts Anymore!



# Formal Technology Adoption



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

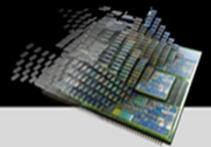
51

H Foster, HVC, November 2014

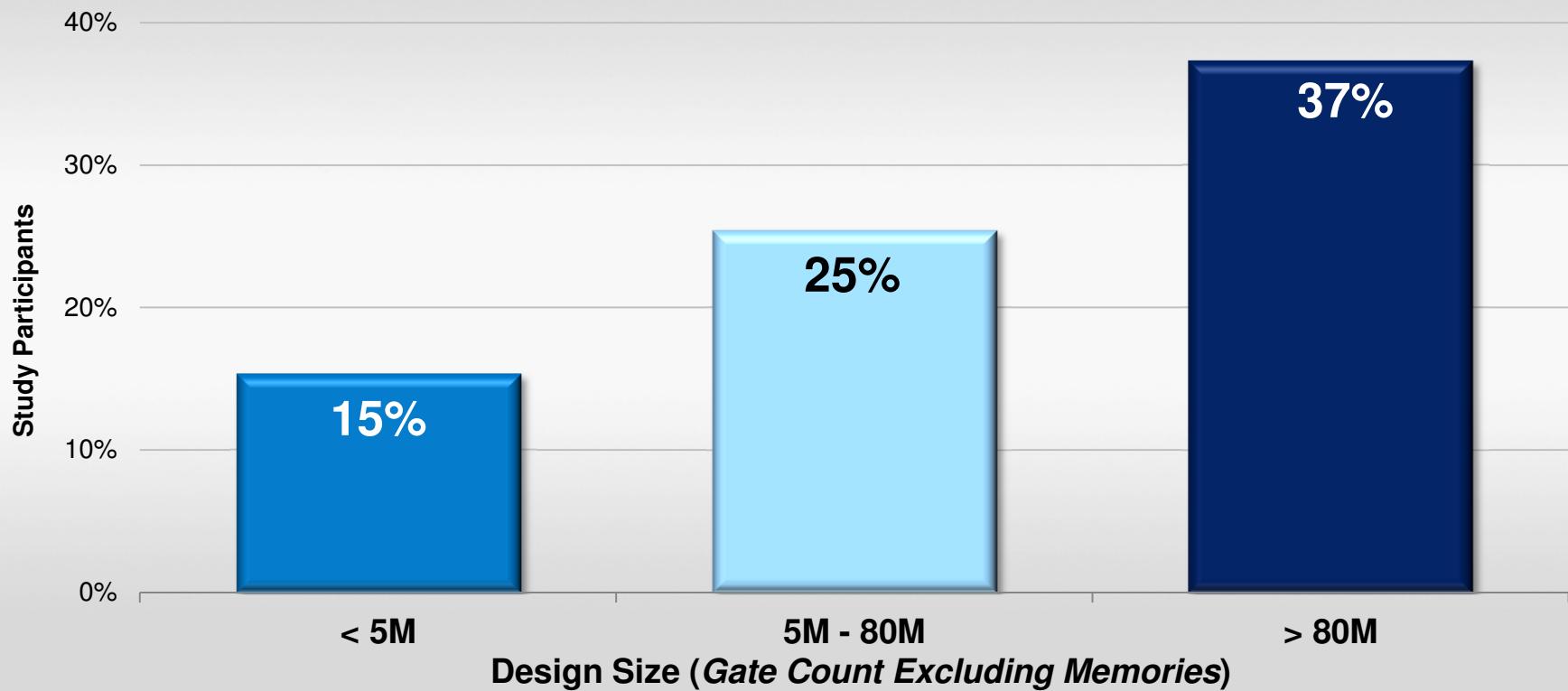
\* Multiple answers possible

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# Formal Property Checking Adoption

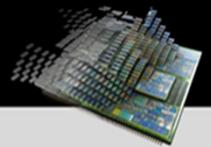


## Formal Property Checking Adoption by Design Size



Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Verification Layer Trends



**Software**

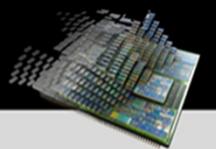
**Security Domains**

**Power Domains**

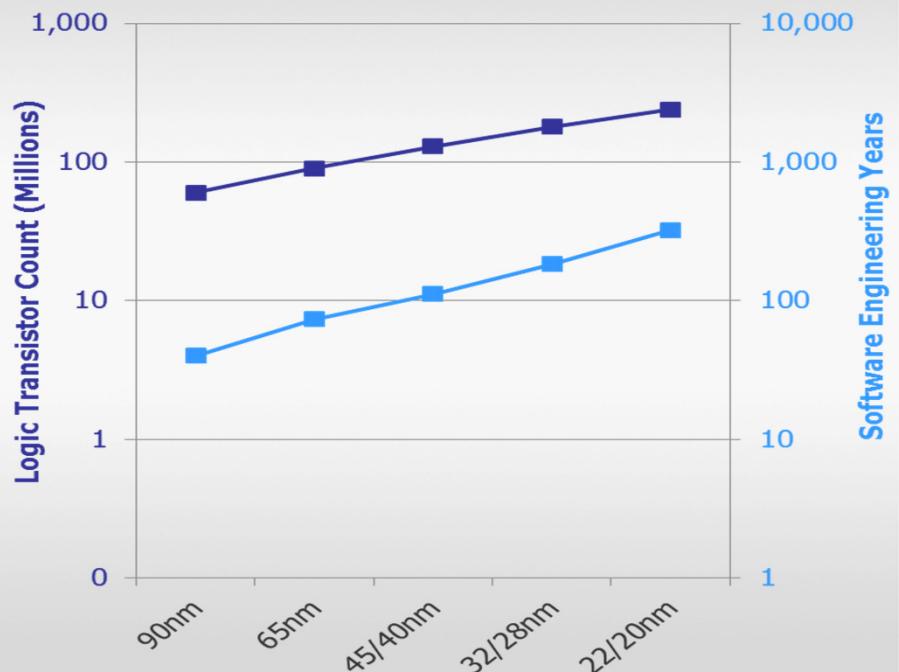
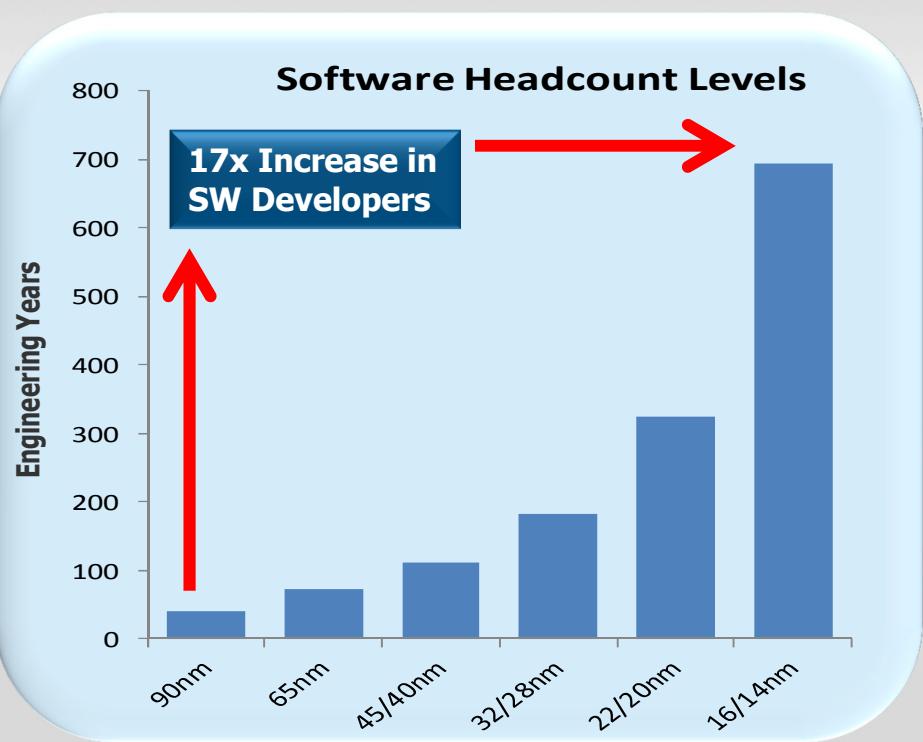
**Clock Domains**

**Functional**

# Embedded SW Headcount Surges with New Node

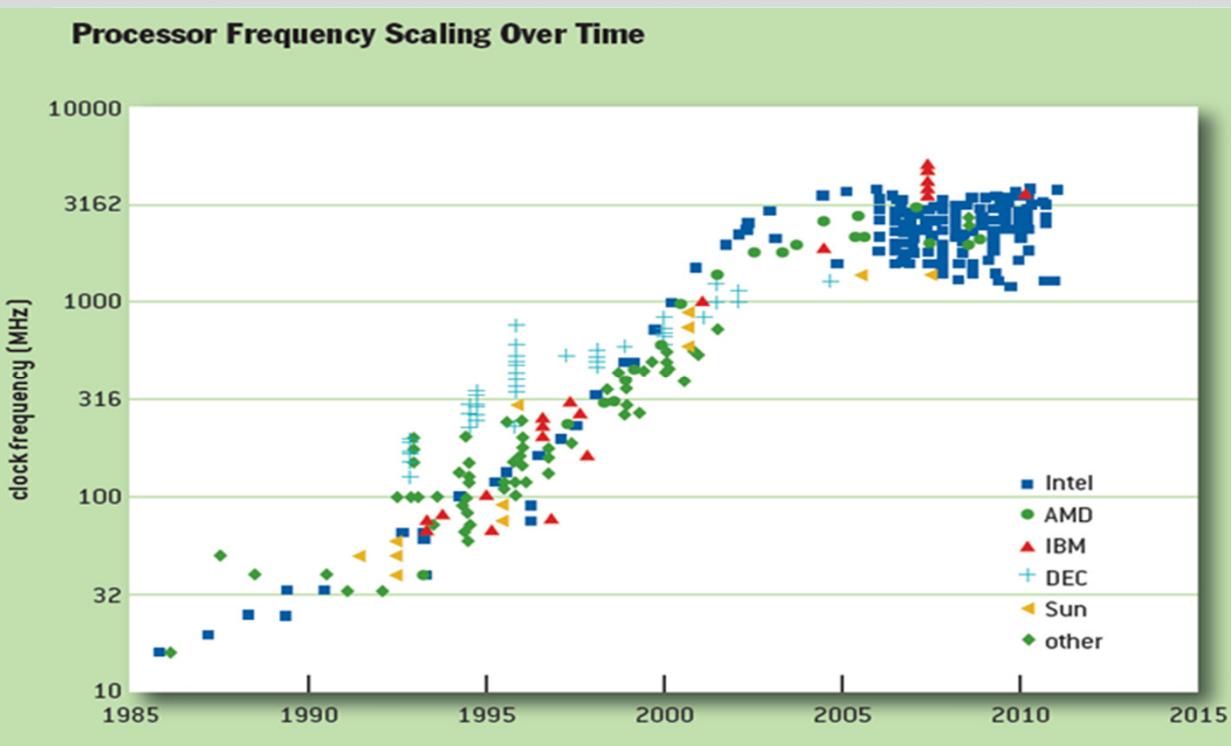
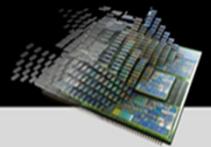


## Primary Chip Design



Source: IBS, April 2013

# Clock Speed Scaling Stalls

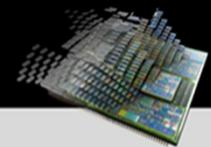


**Emulation Required to Extend Performance**

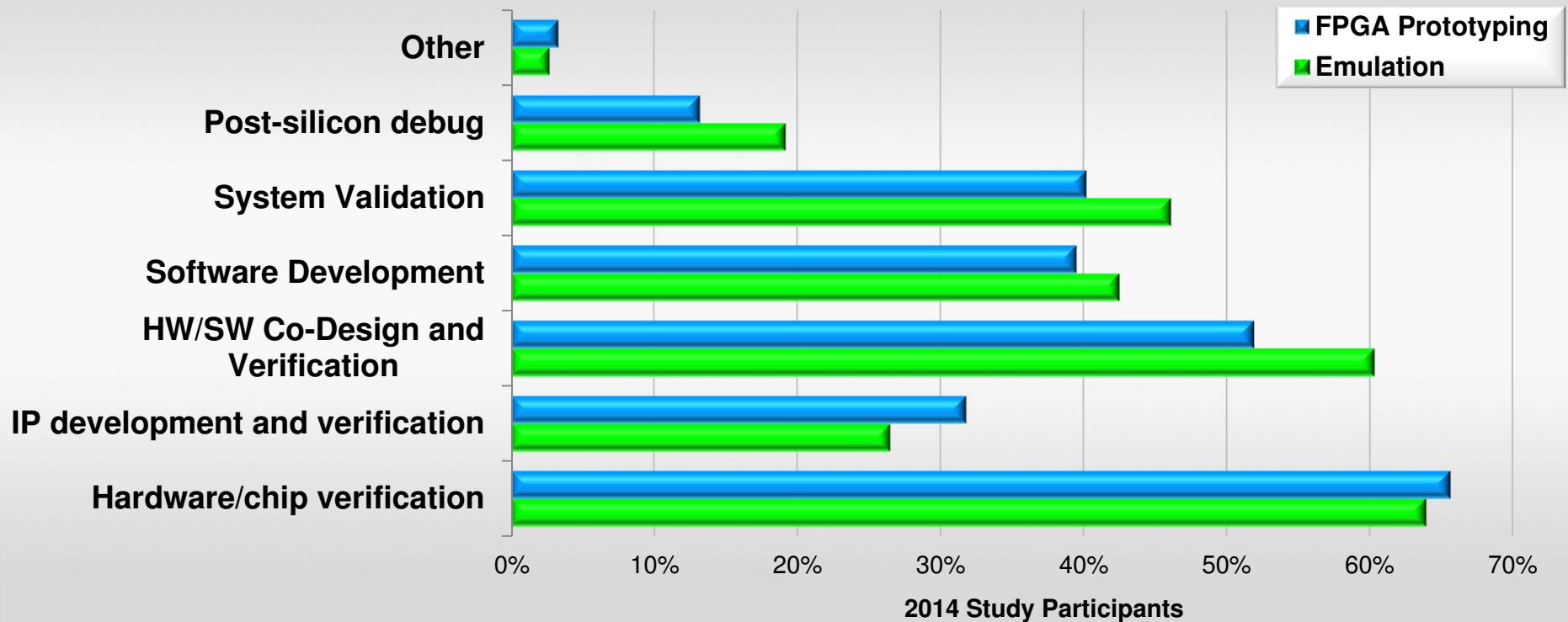


Source: Recording Microprocessor History 4/6/2012 Andrew Danowitz, Kyle Kelley, James Mao, John P. Stevenson, Mark Horowitz <http://queue.acm.org/detail.cfm?id=2181798>

# System-Level Verification Objectives

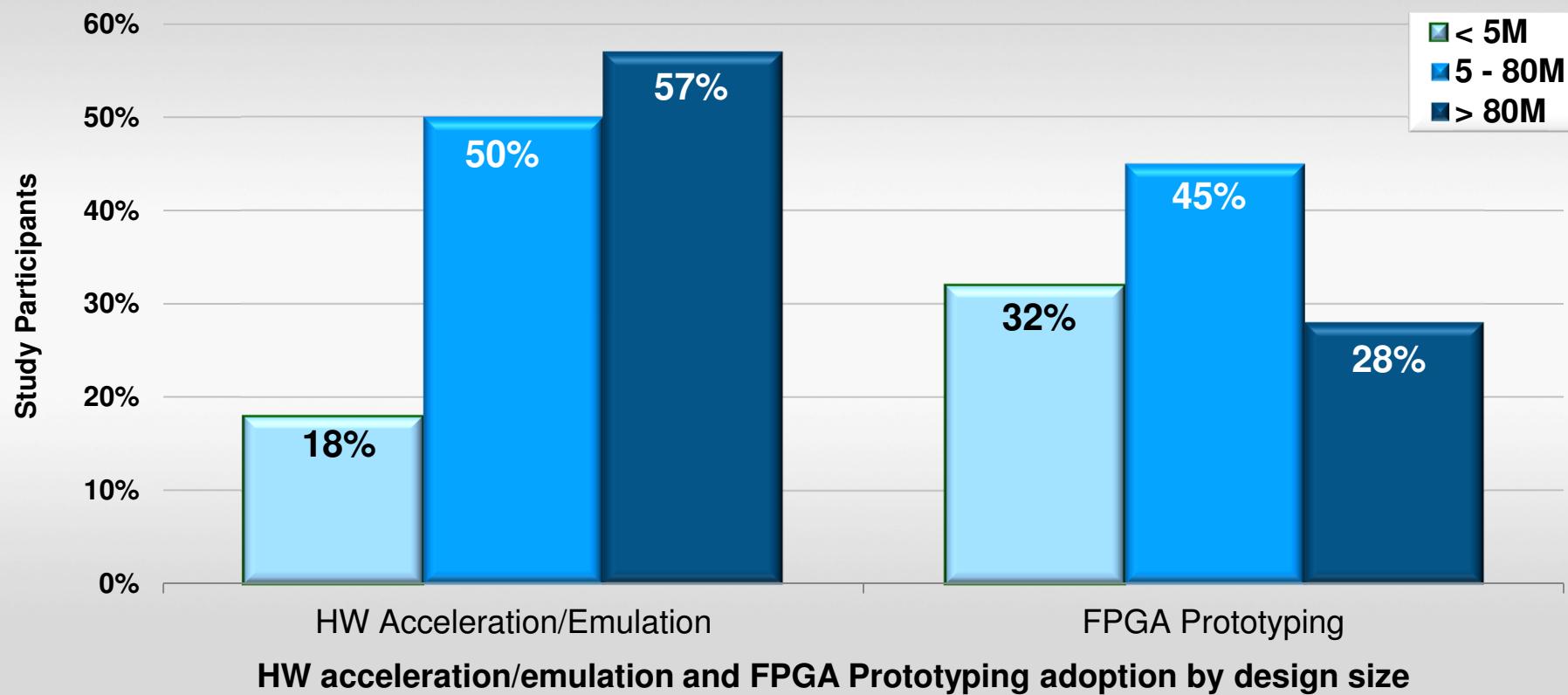
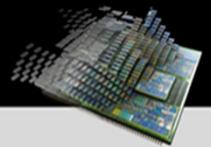


## Why was emulation or FPGA prototyping performed?



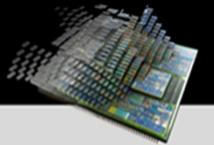
Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study (Preliminary Results)

# Emulation & FPGA Prototyping Adoption by Size

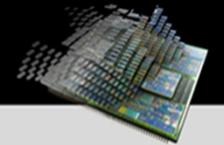


Source: Wilson Research Group and Mentor Graphics, 2014 Functional Verification Study

# Navigating the Perfect Storm



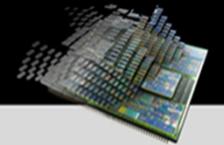
# Charting a New Course for Verification



*From increasing*

**Cycles**      of      **Verification**

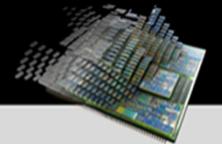
# Charting a New Course for Verification



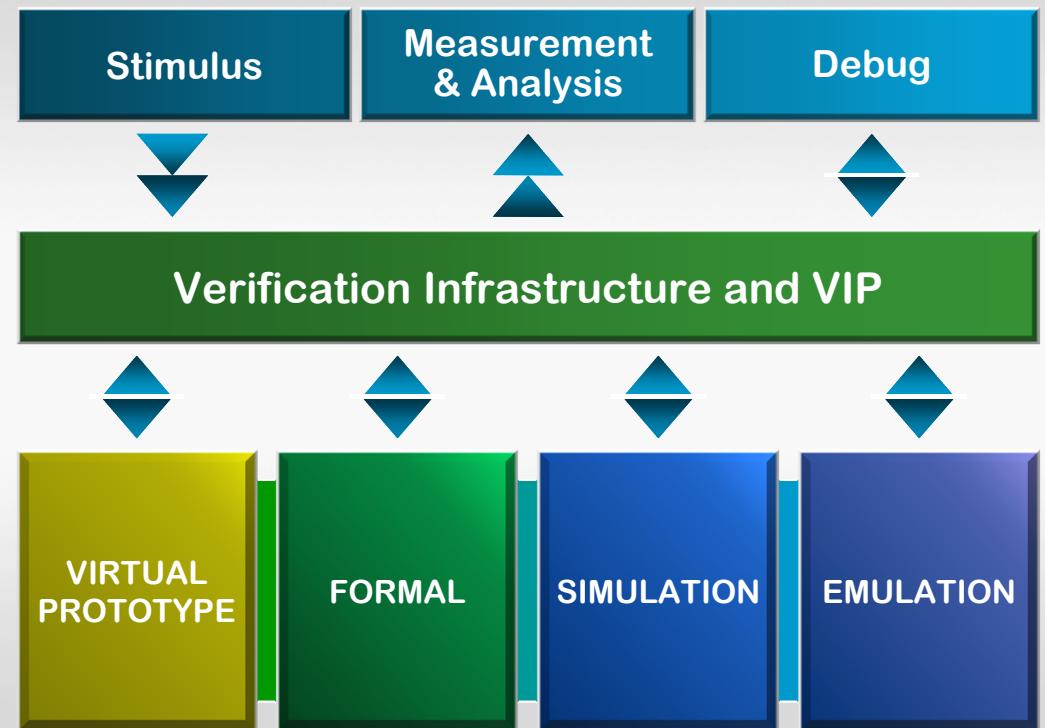
*To maximizing*

**Verification per Cycles**

# Enterprise Verification Platform



An environment where the verification process is completely abstracted from the underlying verification engines



# Verification Academy



## Navigating the Perfect Storm

*Trends in Functional Verification*

*Harry Foster*

*Chief Verification Scientist*

*info@verificationacademy.com* | *www.verificationacademy.com*

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