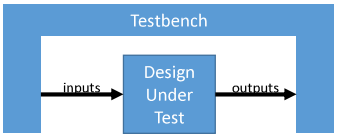
Example System Verilog Testbench

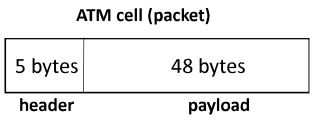
Chris Spear and G Tumbush: *SystemVerilog for Verification (ECE 571 text)*

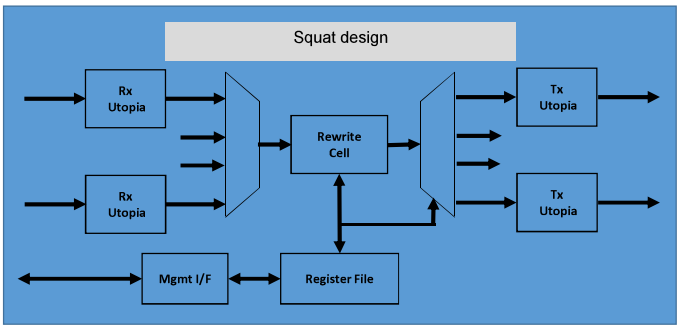
http://chris.spear.net/systemverilog

Test bench Example

- Layered
  - Structured with abstraction/reuse/maintenance in mind
- Constrained random stimulus
- Functional coverage



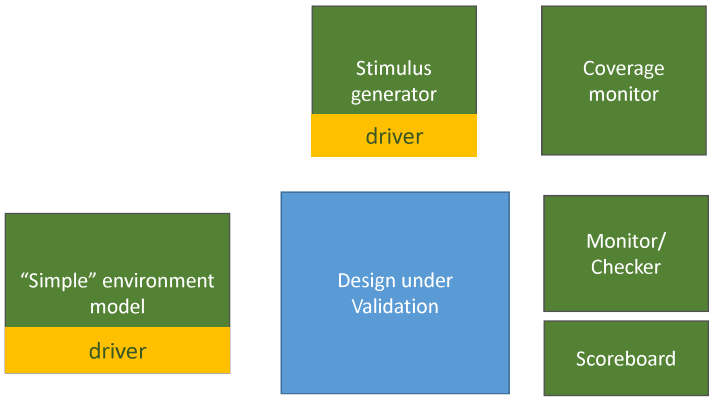


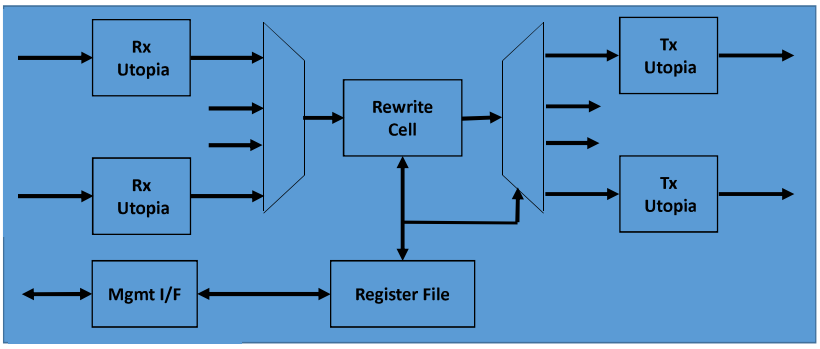


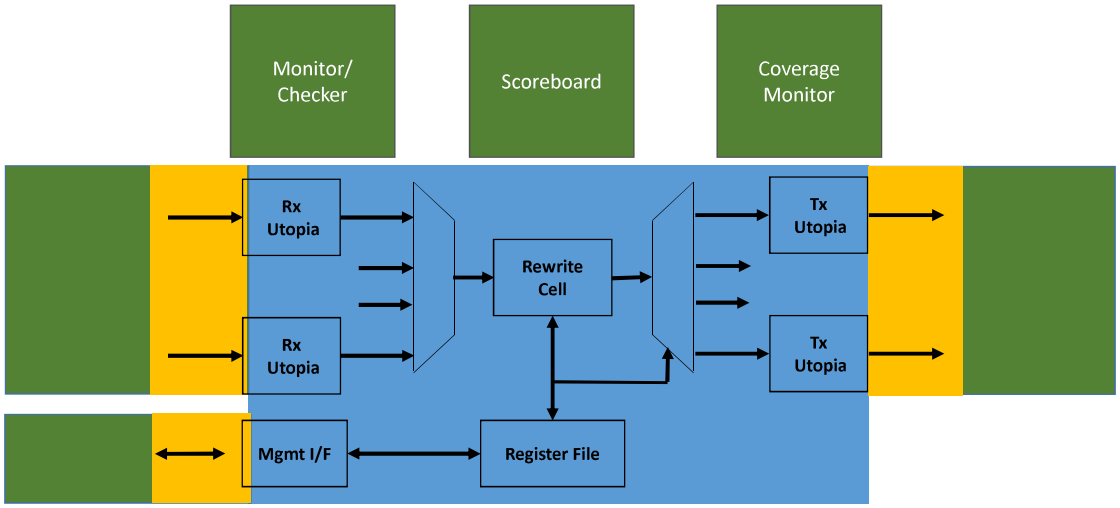
(Virtual Path Indicator lookup table)

UNI formatted cells → NNI formatted Cells

User Network Interface — Network-Network Interface


Stimulus generator
driver
Coverage monitor
"Simple" environment model
driver
Design under Validation
Monitor/ Checker
Scoreboard


Rx Utopia
Rx Utopia
Mgmt I/F
Rewrite Cell
Register File
Tx Utopia
Tx Utopia



Callbacks to checker, scoreboard, coverage monitor whenever

- Data sent to DUT
- Received from DUT