SCEMI Pipe Based Example

Transaction Pipes

- Transaction pipes are unidirectional FIFOs based on Transaction Level Modeling (TLM)
- SCEMI 2.0 standard compliant
- These are written in SystemVerilog and provided as a xtlm package in Veloce
- Provide communication channel between SV HVL and HDL
- Suitable for streaming data

SCEMI (Pronounced SKI-MI)

- Standard Co-Emulation Modeling Interface
- Acellera Standard
- Two Models
  - Function Call Based Transaction (Reactive Model)
  - Transaction Pipe Based Transaction (Streaming Model)

The SCEMI pipe is instantiated in the HDL transactor with appropriate width and buffer size. The handle of the pipe instance is used in HVL to reference it.