Sample Adaptive Offset Filter

VLSI System Design & Implementation Final Project

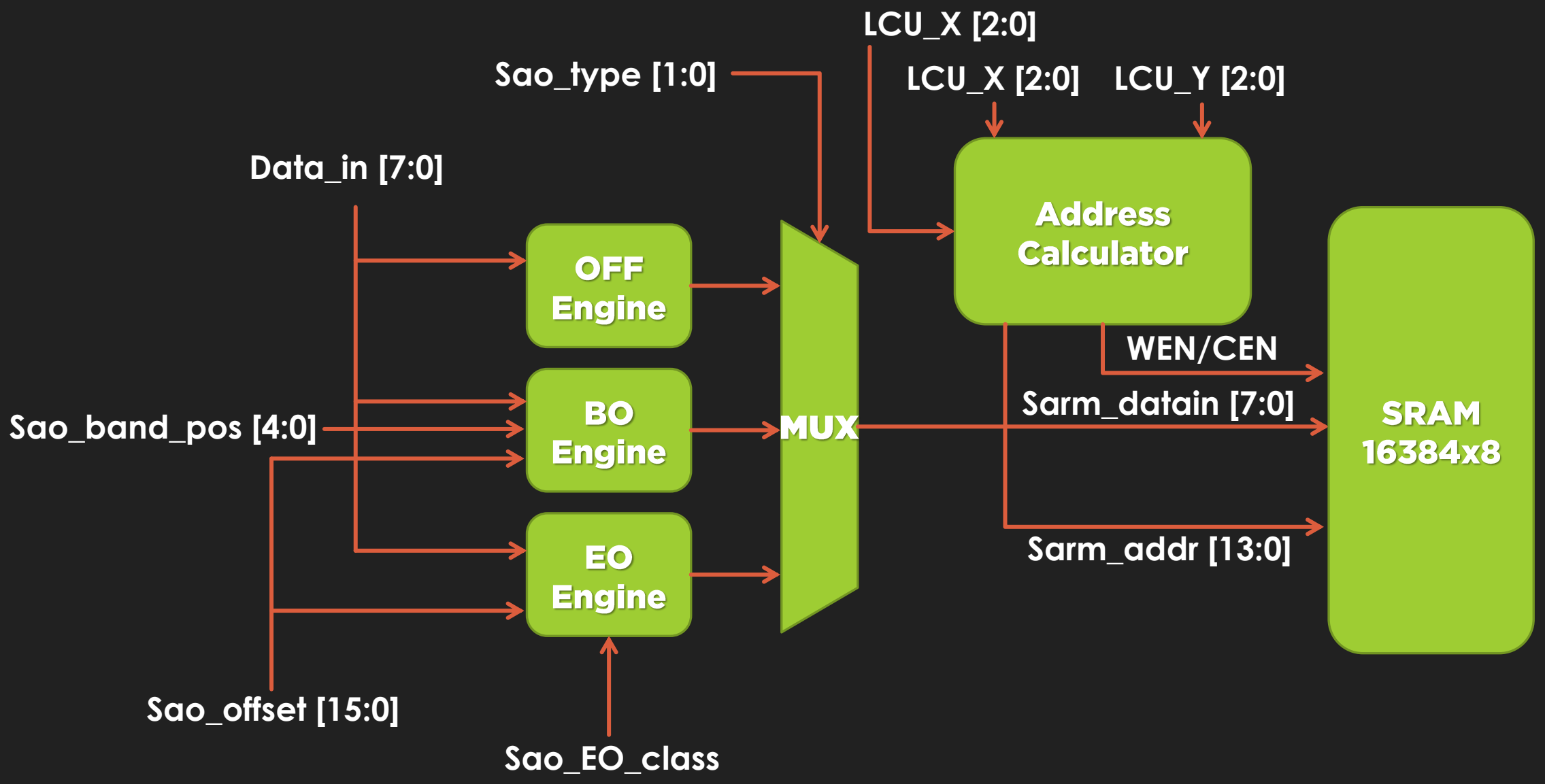
105062600 Yi-Cheng, Chao

Outline

- Design Concept
- Simulation Result
- Result Display
- Difficulty Encounter

Outline

- Design Concept
  - Basic Architecture
  - Band Offset & Edge Offset Engine
  - Overflow/Underflow Handling
  - Address Calculator
- Simulation Result
- Result Display
- Difficulty Encounter



Design Concept – Basic Architecture

Outline

- Design Concept
  - Basic Architecture
  - Band Offset & Edge Offset Engine
  - Overflow/Underflow Handling
  - Address Calculator
- Simulation Result
- Result Display
- Difficulty Encounter

OFF Engine

- Off operation is directly written data_in in SRAM, so just send data in buffer_0 to sram_datain.

BO Engine

- Capture the top five MSB to determine which beginning of continuous band is.
  - Plus one for its next three bands. (There are four bands totally.)

```
assign din_shift = buffer_0[7:3];

assign BO_continuous_band_0 = (din_shift == sao_band_pos_next);
assign BO_continuous_band_1 = (din_shift == sao_band_pos_next+1);
assign BO_continuous_band_2 = (din_shift == sao_band_pos_next+2);
assign BO_continuous_band_3 = (din_shift == sao_band_pos_next+3);

assign bo_offset = BO_continuous_band_0 ? sao_offset_next[15:12] : 0 +
                   BO_continuous_band_1 ? sao_offset_next[11:8] : 0 +
                   BO_continuous_band_2 ? sao_offset_next[7:4] : 0 +
                   BO_continuous_band_3 ? sao_offset_next[3:0] : 0 ;
```

  - If data belong to these band, calculate the golden data which SRAM needed.

EO Engine

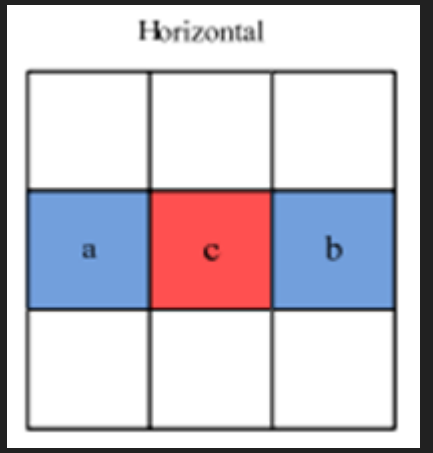
- Before calculate EO category, use four signed registers (two for horizontal edge filter, and two for vertical edge filter) to store the difference for its horizontal or vertical neighbor pixel data.
- Use these two difference to determine which category is.

(Take horizontal EO for example)

```
assign hor_diff1 = c - a;
assign hor_diff2 = c - b;

assign hor_category1 = hor_diff1[8] && hor_diff2[8];
assign hor_category2 = (hor_diff1[8] && (hor_diff2 == 0)) || (hor_diff2[8] && (hor_diff1 == 0));
assign hor_category3 = ((hor_diff1 > 0) && (hor_diff2 == 0)) || ((hor_diff2 > 0) && (hor_diff1 == 0));
assign hor_category4 = (hor_diff1 > 0) && (hor_diff2 > 0);
```

Table 1. Sample classification rules for edge offset.

Category	Condition
1	c<a && c<b
2	(c < a && c==b) ||(c==a&&c < b)
3	(c > a && c==b) ||(c==a&&c > b)
4	c > a && c > b
0	None of the above



EO Engine

- Use 128 D filp-flops instead of using SRAM to hold data, therefore, I can use data to calculate required difference directly.

```
//data in
always@(posedge clk or posedge reset)
        if(reset)
            buffer_0 <= 0;
        else if(in_en) buffer_0 <= din;
```

```
always @ (posedge clk, posedge reset) begin
    if (reset) begin
        buffer_1 <= 0; buffer_2 <= 0; buffer_3 <= 0; buffer_4 <= 0; buffer_5 <= 0; buffer_6 <= 0; buffer_7 <= 0; buffer_8 <= 0; buffer_9 <= 0; buffer_10 <= 0;
        buffer_11 <= 0; buffer_12 <= 0; buffer_13 <= 0; buffer_14 <= 0; buffer_15 <= 0; buffer_16 <= 0; buffer_17 <= 0; buffer_18 <= 0; buffer_19 <= 0; buffer_20 <= 0;
        buffer_21 <= 0; buffer_22 <= 0; buffer_23 <= 0; buffer_24 <= 0; buffer_25 <= 0; buffer_26 <= 0; buffer_27 <= 0; buffer_28 <= 0; buffer_29 <= 0; buffer_30 <= 0;
        buffer_31 <= 0; buffer_32 <= 0; buffer_33 <= 0; buffer_34 <= 0; buffer_35 <= 0; buffer_36 <= 0; buffer_37 <= 0; buffer_38 <= 0; buffer_39 <= 0; buffer_40 <= 0;
        buffer_41 <= 0; buffer_42 <= 0; buffer_43 <= 0; buffer_44 <= 0; buffer_45 <= 0; buffer_46 <= 0; buffer_47 <= 0; buffer_48 <= 0; buffer_49 <= 0; buffer_50 <= 0;
        buffer_51 <= 0; buffer_52 <= 0; buffer_53 <= 0; buffer_54 <= 0; buffer_55 <= 0; buffer_56 <= 0; buffer_57 <= 0; buffer_58 <= 0; buffer_59 <= 0; buffer_60 <= 0;
        buffer_61 <= 0; buffer_62 <= 0; buffer_63 <= 0; buffer_64 <= 0; buffer_65 <= 0; buffer_66 <= 0; buffer_67 <= 0; buffer_68 <= 0; buffer_69 <= 0; buffer_70 <= 0;
        buffer_71 <= 0; buffer_72 <= 0; buffer_73 <= 0; buffer_74 <= 0; buffer_75 <= 0; buffer_76 <= 0; buffer_77 <= 0; buffer_78 <= 0; buffer_79 <= 0; buffer_80 <= 0;
        buffer_81 <= 0; buffer_82 <= 0; buffer_83 <= 0; buffer_84 <= 0; buffer_85 <= 0; buffer_86 <= 0; buffer_87 <= 0; buffer_88 <= 0; buffer_89 <= 0; buffer_90 <= 0;
        buffer_91 <= 0; buffer_92 <= 0; buffer_93 <= 0; buffer_94 <= 0; buffer_95 <= 0; buffer_96 <= 0; buffer_97 <= 0; buffer_98 <= 0; buffer_99 <= 0; buffer_100 <= 0;
        buffer_101 <= 0; buffer_102 <= 0; buffer_103 <= 0; buffer_104 <= 0; buffer_105 <= 0; buffer_106 <= 0; buffer_107 <= 0; buffer_108 <= 0; buffer_109 <= 0; buffer_110 <= 0;
        buffer_111 <= 0; buffer_112 <= 0; buffer_113 <= 0; buffer_114 <= 0; buffer_115 <= 0; buffer_116 <= 0; buffer_117 <= 0; buffer_118 <= 0; buffer_119 <= 0; buffer_120 <= 0;
        buffer_121 <= 0; buffer_122 <= 0; buffer_123 <= 0; buffer_124 <= 0; buffer_125 <= 0; buffer_126 <= 0; buffer_127 <= 0; buffer_128 <= 0;
    end else begin
        buffer_1 <= buffer_next_1; buffer_2 <= buffer_next_2; buffer_3 <= buffer_next_3; buffer_4 <= buffer_next_4; buffer_5 <= buffer_next_5; buffer_6 <= buffer_next_6; buffer_7
        buffer_11 <= buffer_next_11; buffer_12 <= buffer_next_12; buffer_13 <= buffer_next_13; buffer_14 <= buffer_next_14; buffer_15 <= buffer_next_15; buffer_16 <= buffer_next_1
        buffer_21 <= buffer_next_21; buffer_22 <= buffer_next_22; buffer_23 <= buffer_next_23; buffer_24 <= buffer_next_24; buffer_25 <= buffer_next_25; buffer_26 <= buffer_next_2
        buffer_31 <= buffer_next_31; buffer_32 <= buffer_next_32; buffer_33 <= buffer_next_33; buffer_34 <= buffer_next_34; buffer_35 <= buffer_next_35; buffer_36 <= buffer_next_3
        buffer_41 <= buffer_next_41; buffer_42 <= buffer_next_42; buffer_43 <= buffer_next_43; buffer_44 <= buffer_next_44; buffer_45 <= buffer_next_45; buffer_46 <= buffer_next_4
        buffer_51 <= buffer_next_51; buffer_52 <= buffer_next_52; buffer_53 <= buffer_next_53; buffer_54 <= buffer_next_54; buffer_55 <= buffer_next_55; buffer_56 <= buffer_next_5
        buffer_61 <= buffer_next_61; buffer_62 <= buffer_next_62; buffer_63 <= buffer_next_63; buffer_64 <= buffer_next_64; buffer_65 <= buffer_next_65; buffer_66 <= buffer_next_6
        buffer_71 <= buffer_next_71; buffer_72 <= buffer_next_72; buffer_73 <= buffer_next_73; buffer_74 <= buffer_next_74; buffer_75 <= buffer_next_75; buffer_76 <= buffer_next_7
        buffer_81 <= buffer_next_81; buffer_82 <= buffer_next_82; buffer_83 <= buffer_next_83; buffer_84 <= buffer_next_84; buffer_85 <= buffer_next_85; buffer_86 <= buffer_next_8
        buffer_91 <= buffer_next_91; buffer_92 <= buffer_next_92; buffer_93 <= buffer_next_93; buffer_94 <= buffer_next_94; buffer_95 <= buffer_next_95; buffer_96 <= buffer_next_9
        buffer_101 <= buffer_next_101; buffer_102 <= buffer_next_102; buffer_103 <= buffer_next_103; buffer_104 <= buffer_next_104; buffer_105 <= buffer_next_105; buffer_106 <= bu
        buffer_111 <= buffer_next_111; buffer_112 <= buffer_next_112; buffer_113 <= buffer_next_113; buffer_114 <= buffer_next_114; buffer_115 <= buffer_next_115; buffer_116 <= bu
        buffer_121 <= buffer_next_121; buffer_122 <= buffer_next_122; buffer_123 <= buffer_next_123; buffer_124 <= buffer_next_124; buffer_125 <= buffer_next_125; buffer_126 <= bu
    end
```

EO Engine

- For horizontal EO, difference is determined by the current pixel and its left and right neighbor pixels.
- For vertical EO, difference is determined by the current pixel and its top and bottom neighbor pixels.
  - Use LCU block size 16 x 16 for exapmle, we need to make use of data store in buffer_0, buffer_16, buffer_32.

Outline

- Design Concept
  - Basic Architecture
  - Band Offset & Edge Offset Engine
  - Overflow/Underflow Handling
  - Address Calculator
- Simulation Result
- Result Display
- Difficulty Encounter
- Experience & Conclusion

Overflow/Underflow Handling

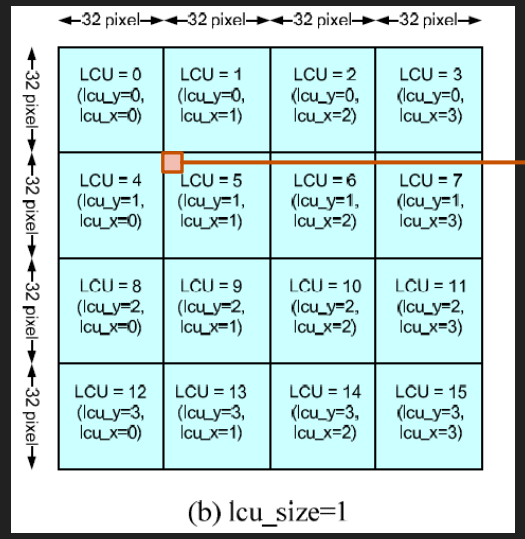
- Use signed extension for calculation, hence we can judge overflow/underflow or not by MSB of result.
  - In BO operation, underflow only appear in BO_continuous_band_0, and overflow only happen in BO_continuous_band_3.
  - In EO operation, underflow appear when the EO_offset is negative, and overflow while positive EO_offset.
- If overflow then assign 8'd255, and 8'd0 for underflow.

Outline

- Design Concept
  - Basic Architecture
  - Band Offset & Edge Offset Engine
  - Overflow/Underflow Handling
  - Address Calculator
- Simulation Result
- Result Display
- Difficulty Encounter

Address Calculator

- Take advantage of two flags to detect LCU block starting wriring and termination, so as to recalculate the write address.
- For each LCU block start point (the upper left corner), the address can know from LCU_X and LCU_Y.

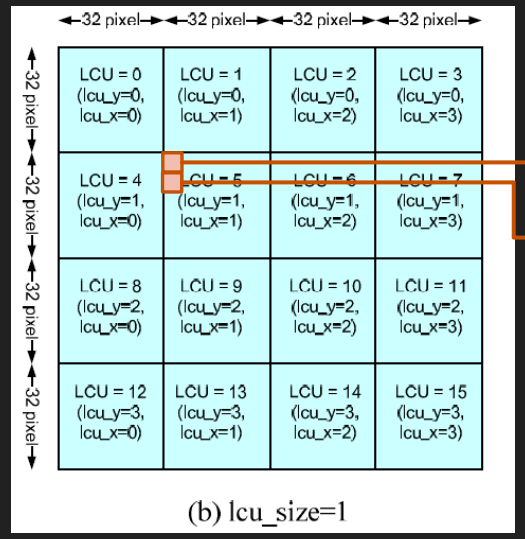


Address = 1* 2^5 + 1 * 2^5 * 128 = 4128

Formula: address = LCU_X * 2^(LCU_size + 4) + LCU_Y * 2(LCU_size + 4) * 128

Address Calculator

- For change to next row in same LCU block, the address will increase 128 – (LCU block edge - 1), and use a counter to detect whether count up a row (i.e LCU block edge size) or not.



Address = 1* 2^5 + 1 * 2^5 * 128 = 4128

Address = 4128 + 16 – 1 = 4241

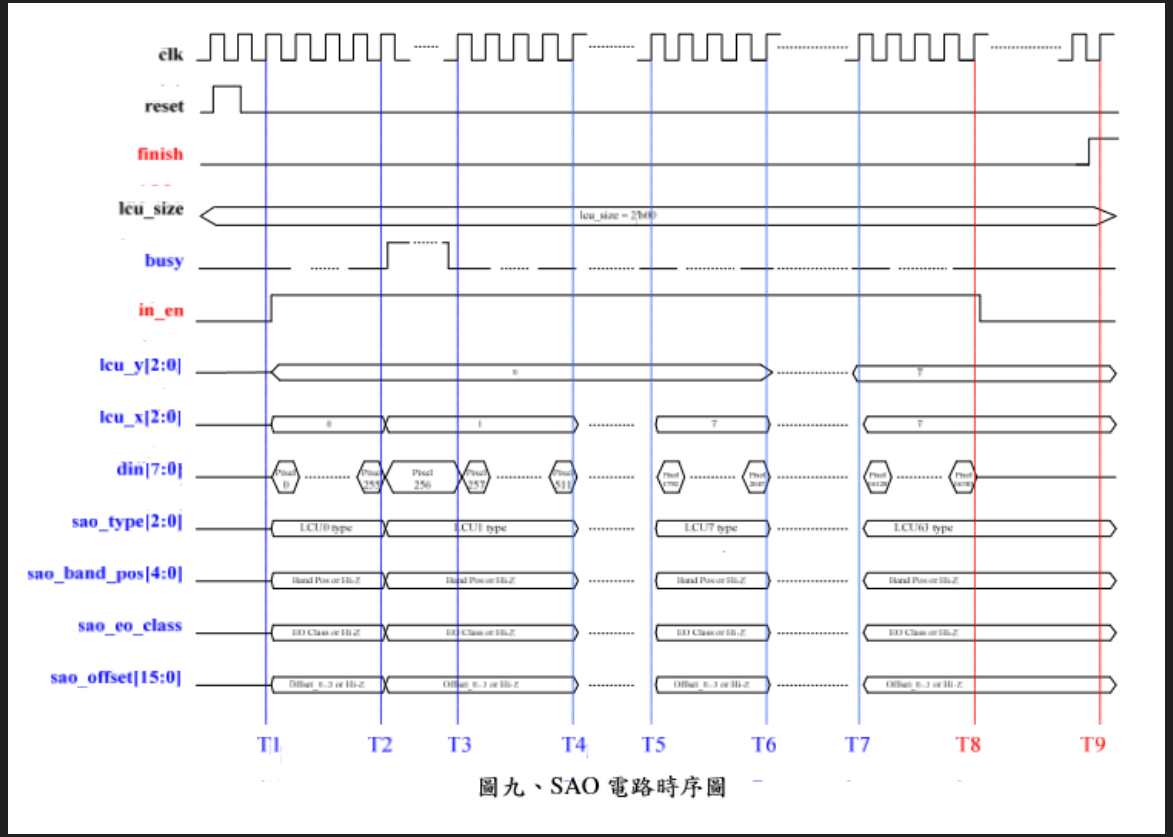
Formula: address = LCU_X * 2^(LCU_size + 4) + LCU_Y * 2(LCU_size + 4) * 128

Outline

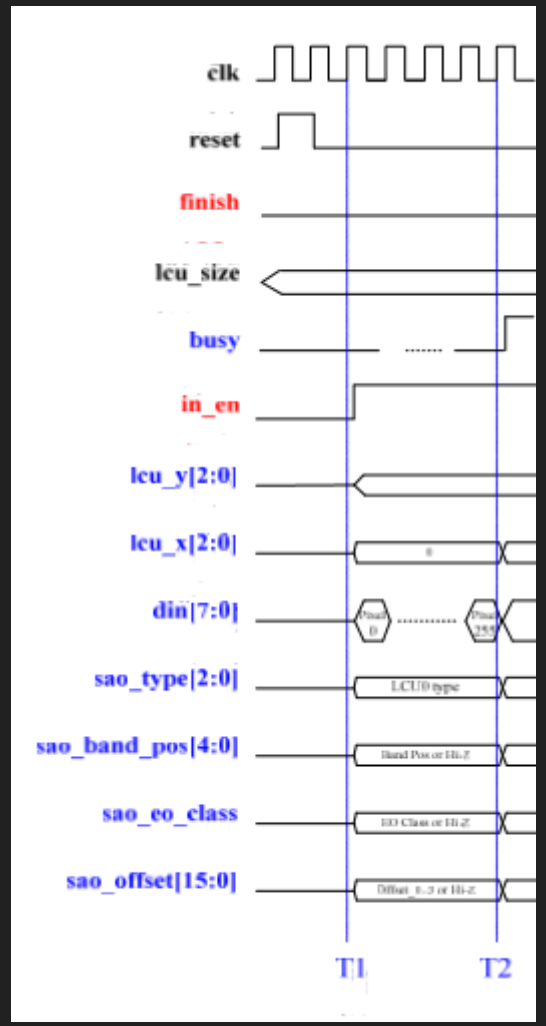
- Design Concept
- Simulation Result
  - RTL Simulation
  - Pre-Layout Simulation
  - Post-Layout Simulation
- Result Display
- Difficulty Encounter

RTL Simulation

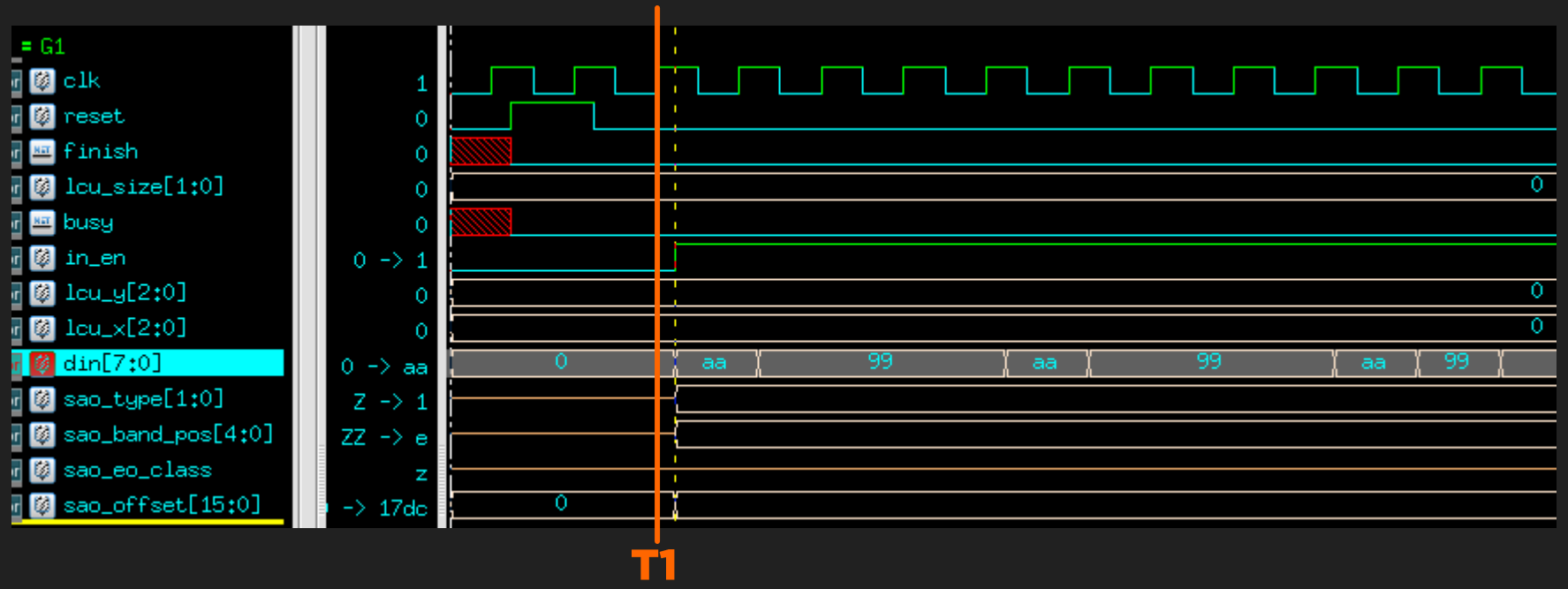
- The time order graph is shown at left hand side, take LCU size 16 for example.
- To check the correctness of my design, I use these graph as criterion to compare with my design.



圖九、SAO 電路時序圖

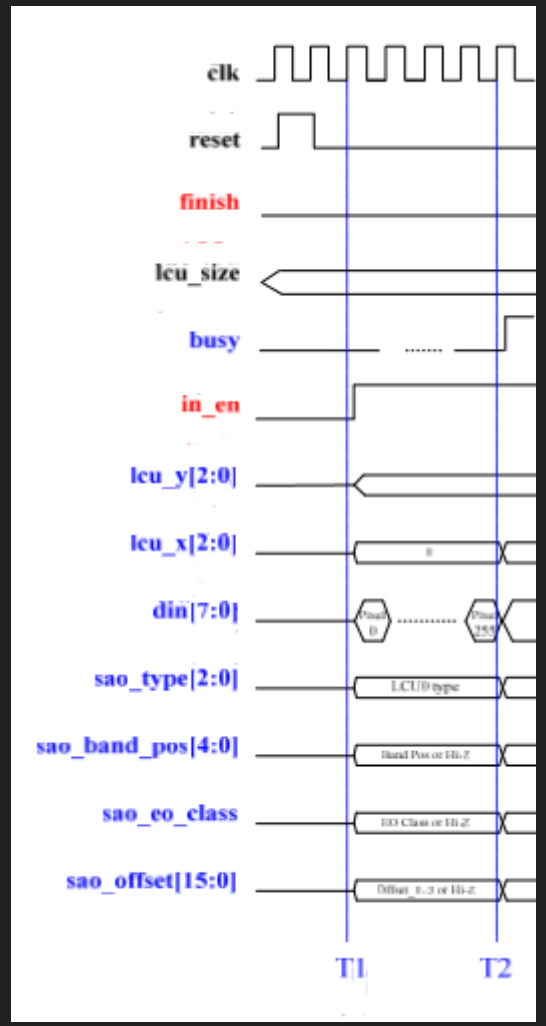


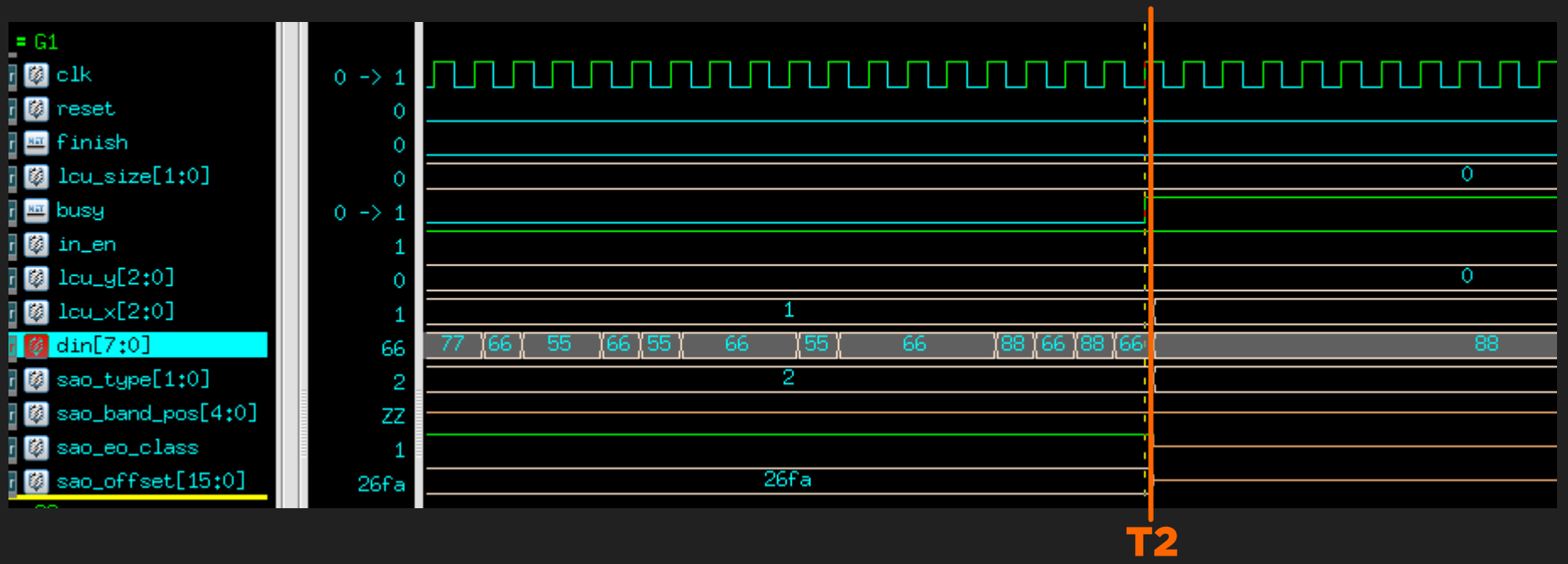
- In the beginning, reset one clock cycle, initialization of SAO is complete. At T1, host detects the busy flag at low level, in_en flag rises and begins to input the first data.



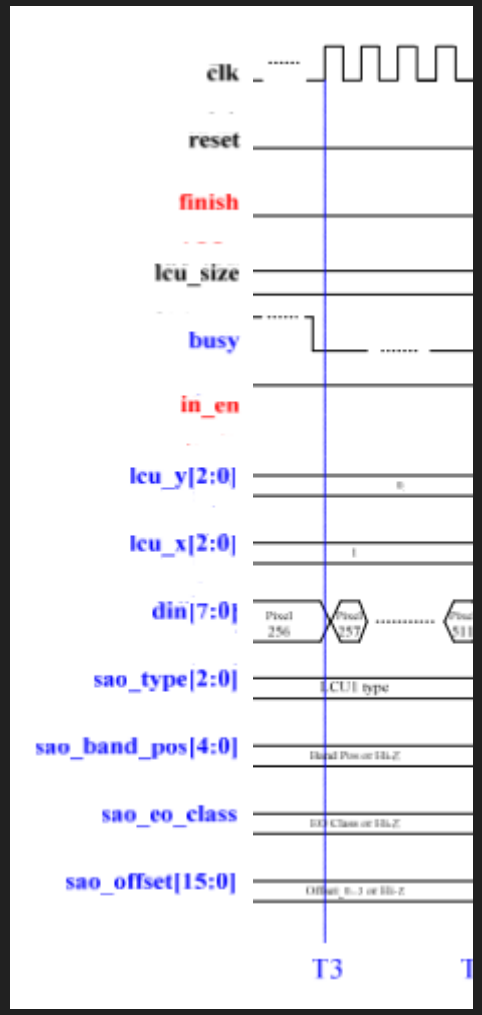
RTL Simulation

- At T2, if the busy flag is rising, host stop importing data. Host will not resume data input until detect the busy flag at low level on rising edge.

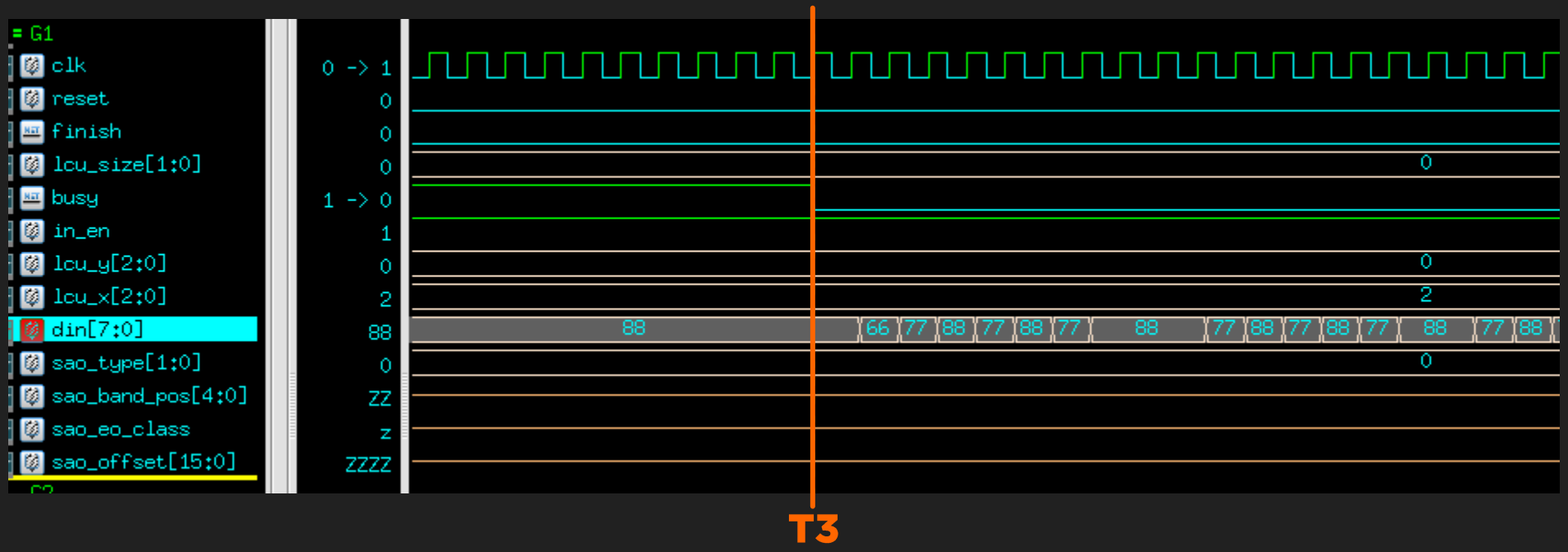




RTL Simulation

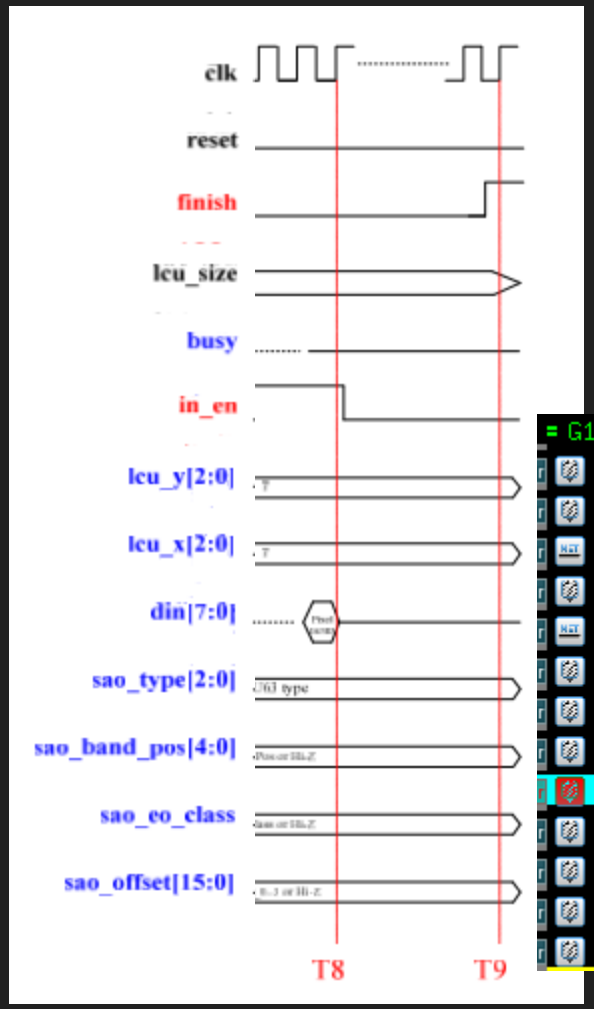


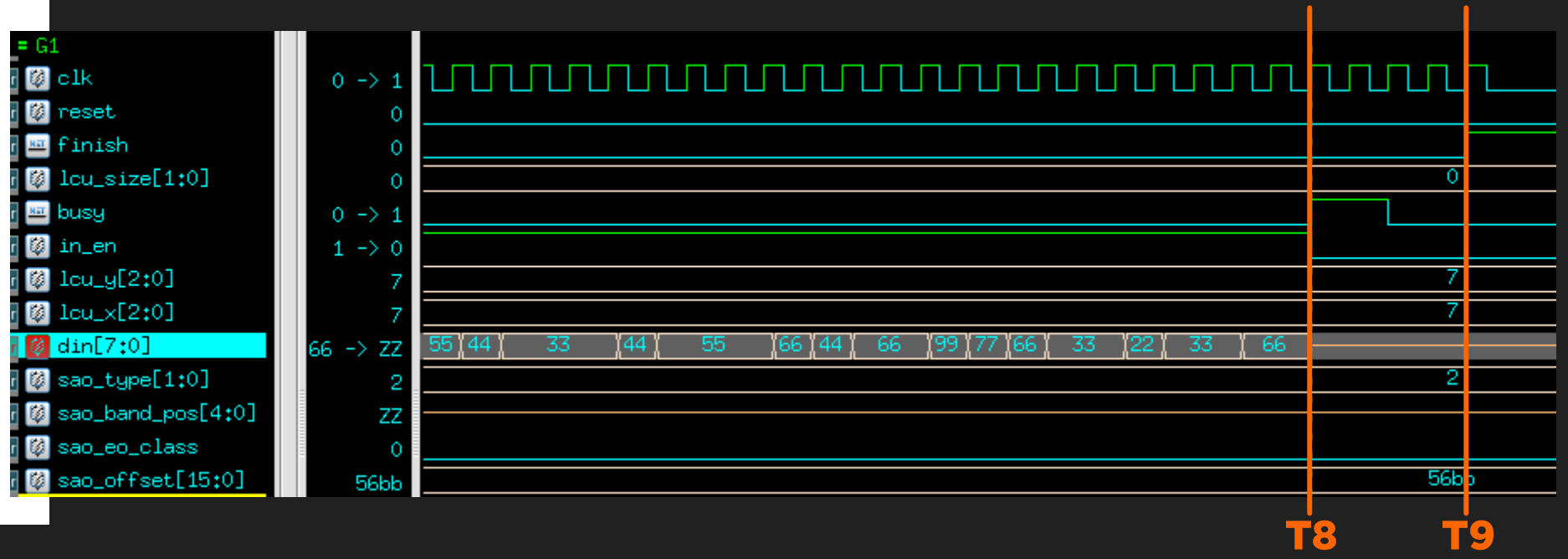
- At T3, host detect busy flag falling on rising edge, resume data input.



RTL Simulation

- At T8, importing data finish, so that in_en flag fall. After calculating data fully, rise the finish flag at T9, then the simulation is complete.





RTL Simulation

RTL Simulation

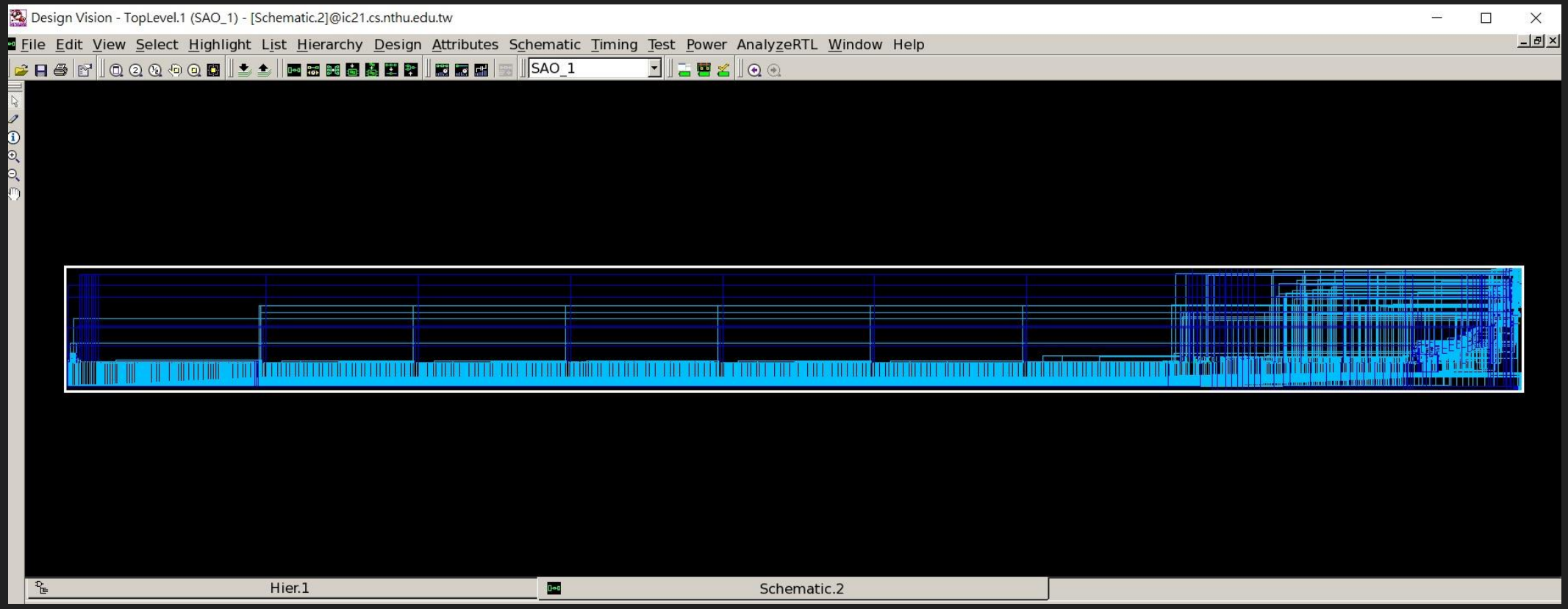
```
SRAM Address:16252 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=12): 33 == expect 33
SRAM Address:16253 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=13): 39 == expect 39
SRAM Address:16254 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=14): 44 == expect 44
SRAM Address:16255 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=14, x=15): 55 == expect 55
SRAM Address:16368 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 0): 55 == expect 55
SRAM Address:16369 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 1): 5b == expect 5b
SRAM Address:16370 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 2): 61 == expect 61
SRAM Address:16371 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 3): 49 == expect 49
SRAM Address:16372 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 4): 61 == expect 61
SRAM Address:16373 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 5): 6c == expect 6c
SRAM Address:16374 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 6): 94 == expect 94
SRAM Address:16375 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 7): 77 == expect 77
SRAM Address:16376 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 8): 66 == expect 66
SRAM Address:16377 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x= 9): 39 == expect 39
SRAM Address:16378 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=10): 2e == expect 2e
SRAM Address:16379 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=11): 27 == expect 27
SRAM Address:16380 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=12): 2e == expect 2e
SRAM Address:16381 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=13): 39 == expect 39
SRAM Address:16382 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=14): 61 == expect 61
SRAM Address:16383 => LCU(lcu_y= 7, lcu_x= 7): Success at Pixel(y=15, x=15): 66 == expect 66
--------------------------------------------------

Congratulations! All data have been generated successfully!

-------------------------PASS-------------------------

Simulation complete via $finish(1) at time 71291100 PS + 0
```

- The clock period for RTL simulation can achieve to very small period.

Outline

- Design Concept
- Simulation Result
  - RTL Simulation
  - Pre-Layout Simulation
  - Post-Layout Simulation
- Result Display
- Difficulty Encounter

Schematic View



Timing/Area Report

```
  clock CLK (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  sram_din_reg[0]/CK (DFFRX1)              0.00      10.00 r
  library setup time                      -0.22       9.78
  data required time                                  9.78
  ----------------------------------------------------------
  data required time                                  9.78
  data arrival time                                  -8.61
  ----------------------------------------------------------
  slack (MET)                                         1.16


design_vision>
Log  History
design_vision>
```

```
  Number of buf/inv:                      213
  Number of references:                    55

  Combinational area:              7752.025793
  Buf/Inv area:                    1218.733181
  Noncombinational area:          36504.283165
  Macro/Black Box area:          438436.062500
  Net Interconnect area:      undefined  (No wire load specified)

  Total cell area:                482692.371458
  Total area:                 undefined
  design_vision>
Log  History
design_vision>
```

Power Report

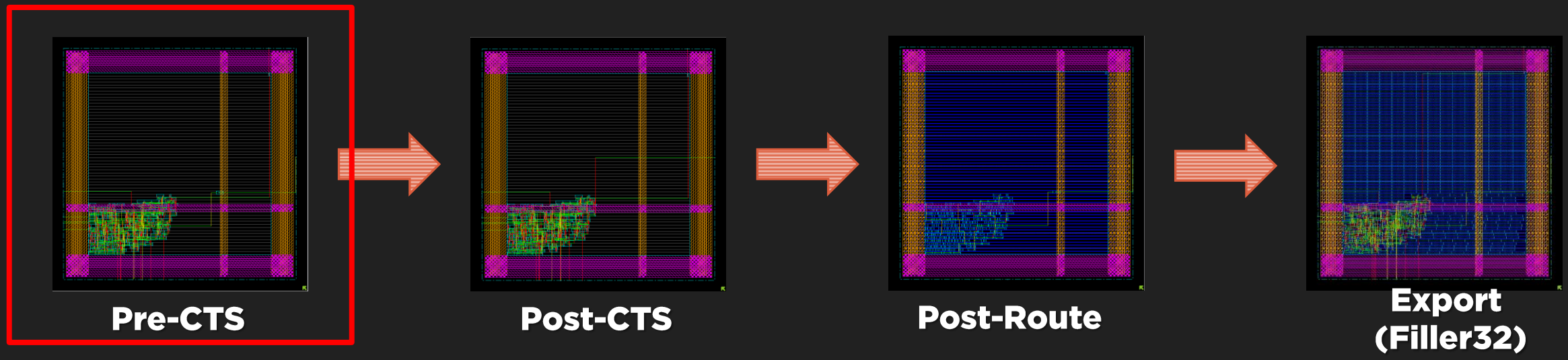
```
                 Internal         Switching           Leakage             Total
Power Group      Power            Power               Power               Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000              0.0000  (   0.00%)
memory             0.6150           0.0000          9.8000e+07              0.7130  (  22.64%)
black_box          0.0000           0.0000              0.0000              0.0000  (   0.00%)
clock_network      0.0000           0.0000              0.0000              0.0000  (   0.00%)
register           2.3280        4.3188e-03          3.3602e+07              2.3659  (  75.12%)
sequential         0.0000           0.0000              0.0000              0.0000  (   0.00%)
combinational   2.6016e-02        3.7533e-02          6.9936e+06          7.0543e-02  (   2.24%)
--------------------------------------------------------------------------------------------------
Total              2.9689 mW     4.1852e-02 mW     1.3860e+08 pW           3.1494 mW
design_vision>
```

Log | History

design_vision>

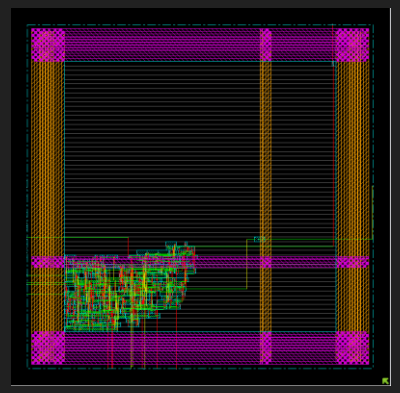
Outline

- Design Concept
- Simulation Result
  - RTL Simulation
  - Pre-Layout Simulation
  - Post-Layout Simulation
- Result Display
- Difficulty Encounter
- Experience & Conclusion

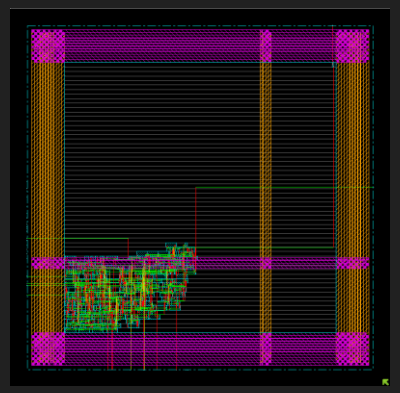



```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.614  |  5.657  |  5.614  |  7.634  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      1 (1)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 8.880%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

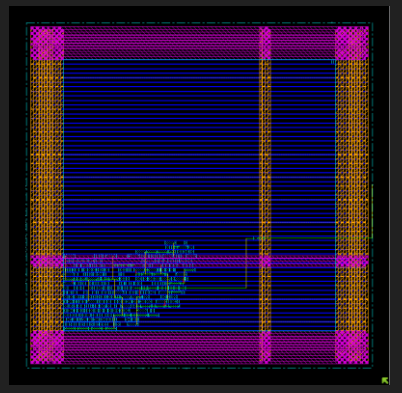
Post Layout APR Flow



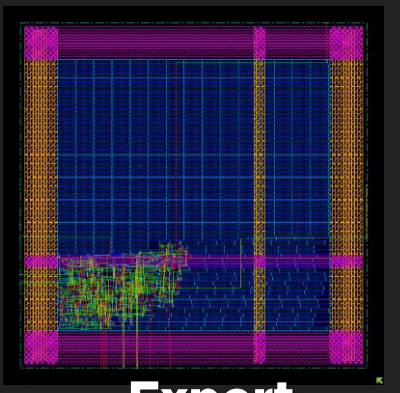
Pre-CTS



Post-CTS



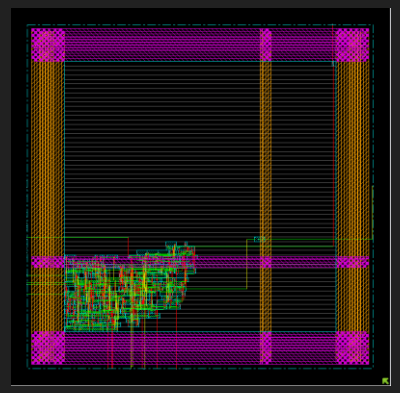
Post-Route



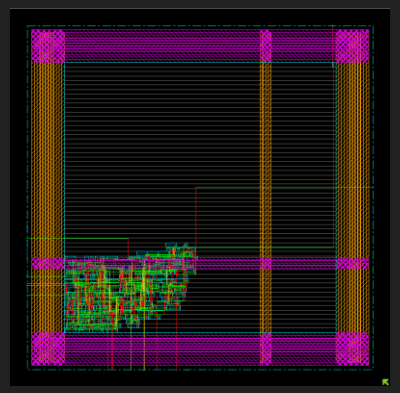
Export
(Filler32)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.308  |  5.657  |  5.308  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 9.011%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

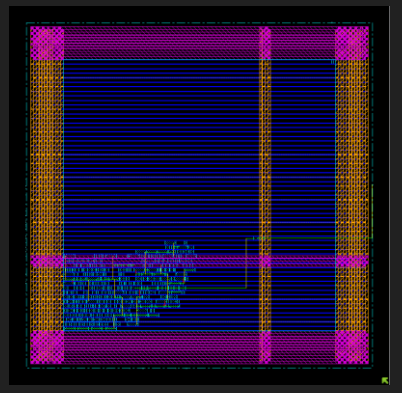
Post Layout APR Flow



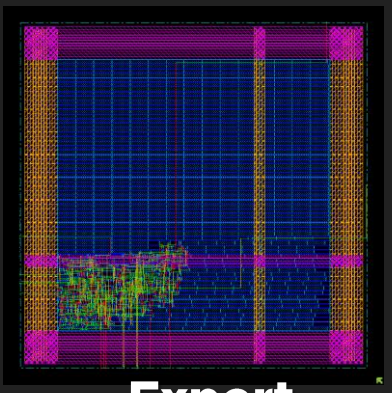
Pre-CTS



Post-CTS



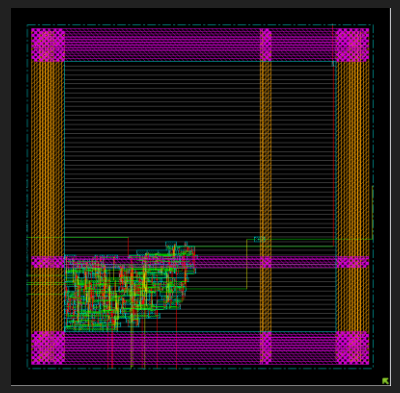
Post-Route



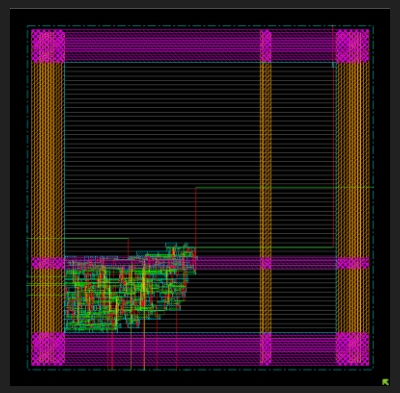
Export (Filler32)

```
------------------------------------------------------------
     optDesign Final Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.307  |  5.646  |  5.307  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.089  |  0.089  |  1.327  |  1.036  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 8.973%
Routing Overflow: 0.00% H and 0.00% V
------------------------------------------------------------
```

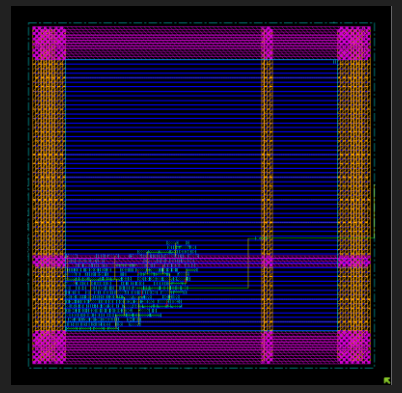
Post Layout APR Flow



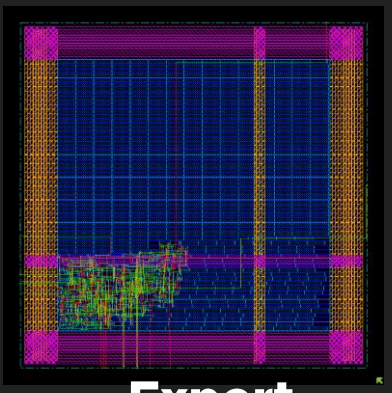
Pre-CTS



Post-CTS



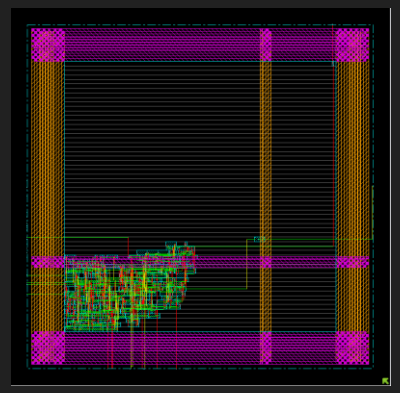
Post-Route



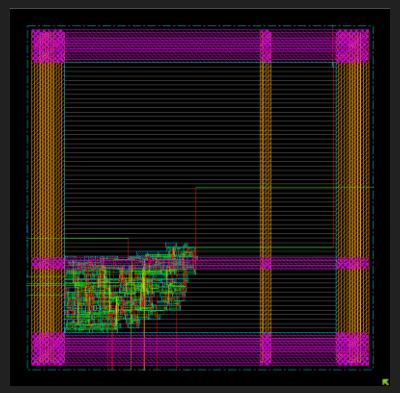
Export
(Filler32)

```
------------------------------------------------------------
          timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.288  |  5.656  |  5.288  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 8.973%
Total number of glitch violations: 0
------------------------------------------------------------
```

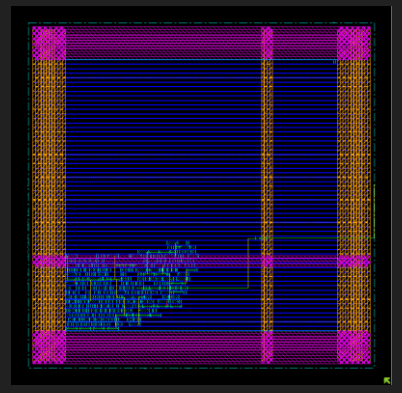
Post Layout APR Flow



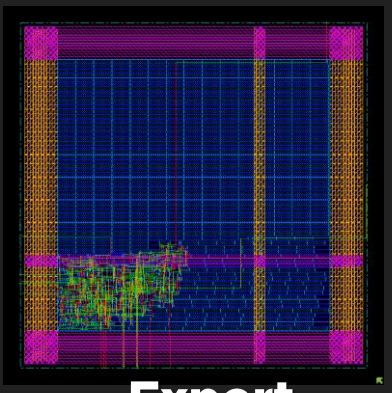
Pre-CTS



Post-CTS



Post-Route



Export (Filler32)

```
------------------------------------------------------------
     optDesign Final SI Timing Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  5.288  |  5.656  |  5.288  |  7.948  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+--------------------+---------+---------+---------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate |
+--------------------+---------+---------+---------+---------+---------+---------+
|           WNS (ns):|  0.091  |  0.091  |  1.329  |  1.036  |   N/A   |   N/A   |
|           TNS (ns):|  0.000  |  0.000  |  0.000  |  0.000  |   N/A   |   N/A   |
|    Violating Paths:|    0    |    0    |    0    |    0    |   N/A   |   N/A   |
|          All Paths:|   100   |   46    |   76    |    2    |   N/A   |   N/A   |
+--------------------+---------+---------+---------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |              Real             |       Total      |
|    DRVs        +------------------+------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+------------------+------------+------------------+
|   max_cap      |      0 (0)       |   0.000    |      0 (0)       |
|   max_tran     |      0 (0)       |   0.000    |      0 (0)       |
|   max_fanout   |      0 (0)       |     0      |      0 (0)       |
|   max_length   |      0 (0)       |     0      |      0 (0)       |
+----------------+------------------+------------+------------------+

Density: 8.973%
Total number of glitch violations: 0
------------------------------------------------------------
```

Post Layout APR Flow

DRC/LVS Verify

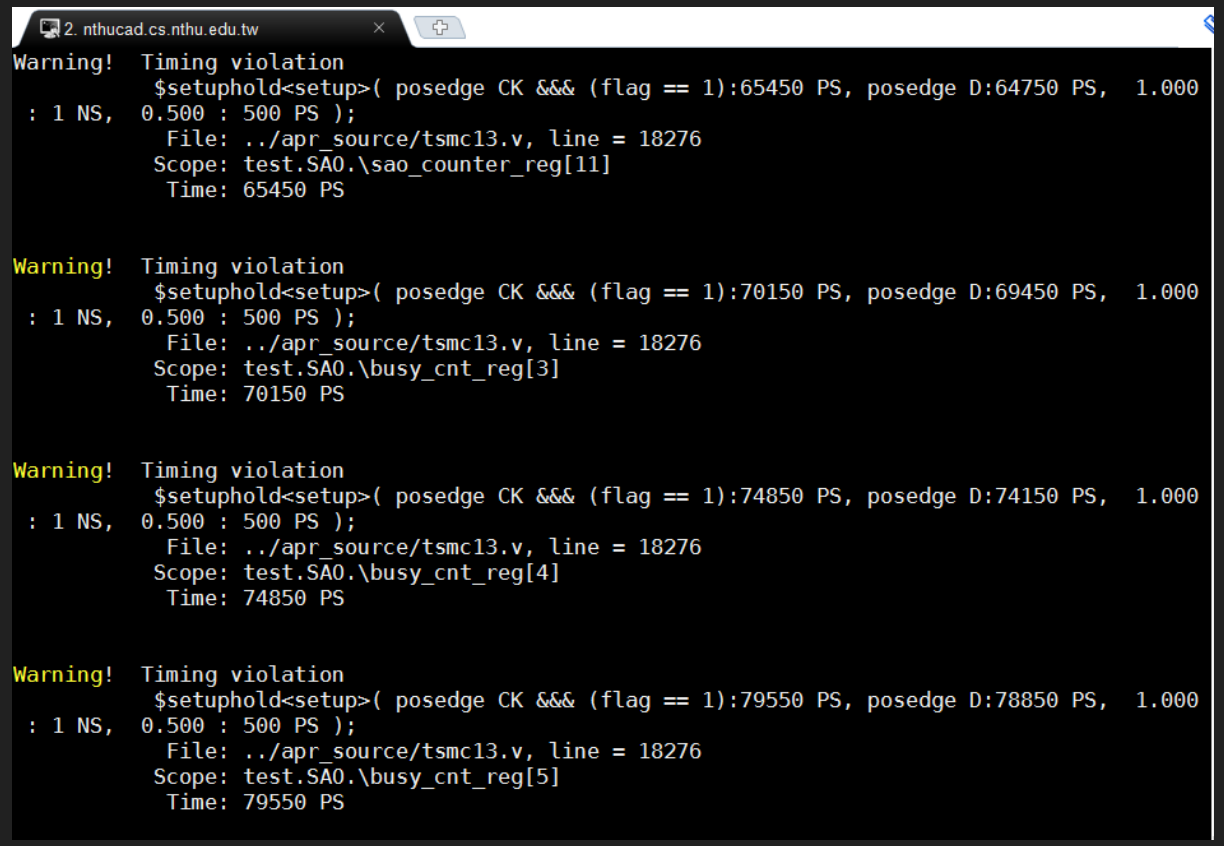
```
******** Start: VERIFY CONNECTIVITY ********
Start Time: Tue Jan 10 13:35:57 2017

Design Name: SAO_1
Database Units: 2000
Design Boundary: (0.0000, 0.0000) (282.4650, 281.7400)
Error Limit = 1000; Warning Limit = 50
Check all nets

Begin Summary
  Found no problems or warnings.
End Summary

End Time: Tue Jan 10 13:35:58 2017
Time Elapsed: 0:00:01.0

******** End: VERIFY CONNECTIVITY ********
  Verification Complete : 0 Viols.  0 Wrngs.
  (CPU Time: 0:00:00.0  MEM: 0.000M)
```

```
encounter 2>  *** Starting Verify Geometry (MEM: 837.6) ***

  VERIFY GEOMETRY ..... Starting Verification
  VERIFY GEOMETRY ..... Initializing
  VERIFY GEOMETRY ..... Deleting Existing Violations
  VERIFY GEOMETRY ..... Creating Sub-Areas
                  ..... bin size: 8320
  VERIFY GEOMETRY ..... SubArea : 1 of 1
  VERIFY GEOMETRY ..... Cells          :  0 Viols.
  VERIFY GEOMETRY ..... SameNet        :  0 Viols.
  VERIFY GEOMETRY ..... Wiring         :  0 Viols.
  VERIFY GEOMETRY ..... Antenna        :  0 Viols.
  VERIFY GEOMETRY ..... Sub-Area : 1 complete 0 Viols. 0 Wrngs.
VG: elapsed time: 0.00
Begin Summary ...
  Cells       : 0
  SameNet     : 0
  Wiring      : 0
  Antenna     : 0
  Short       : 0
  Overlap     : 0
End Summary

  Verification Complete : 0 Viols.  0 Wrngs.

**********End: VERIFY GEOMETRY**********
 *** verify geometry (CPU: 0:00:00.3  MEM: 15.6M)
```

Report Area

```
encounter 2> analyzeFloorplan
Start to collect the design information.
Build netlist information for Cell SAO_1.
Finished collecting the design information.
Average module density = 0.952.
Density for the design = 0.952.
       = stdcell_area 27523 sites (46718 um^2) / alloc_area 28920 sites (49089 um^2).
Pin Density = 0.049.
           = total # of pins 1335 / total Instance area 27523.
************************** Analyze Floorplan **************************
    Die Area(um^2)             : 79581.69
    Core Area(um^2)            : 49174.05
    Chip Density (Counting Std Cells and MACROs and IOs): 58.704%
    Core Density (Counting Std Cells and MACROs): 95.004%
    Average utilization        : 95.169%
    Number of instance(s)      : 1121
    Number of Macro(s)         : 0
    Number of IO Pin(s)        : 45
    Number of Power Domain(s) : 0
************************** Estimation Results **************************
************************************************************************
```

Post-Layout Simulation



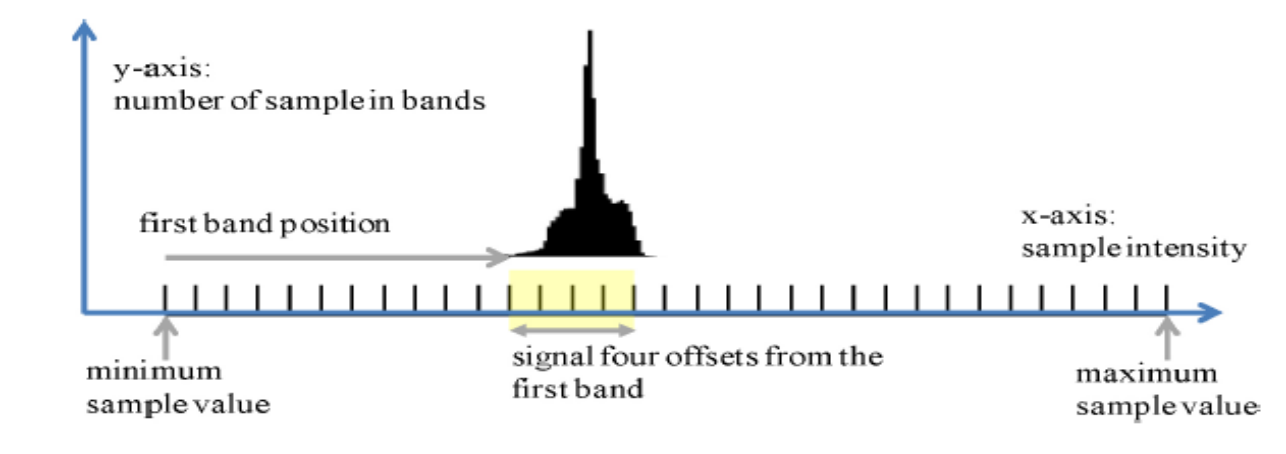
- Unfortunately, the simulation is error due to some problems…
- The reason why I forget to set some steps might be the lack of knowledge of APR flow.

Outline

- Design Concept
- Simulation Result
- Result Display
- Difficulty Encounter

Result Display (BO)

- The main reason for using four consecutive bands is that in the smooth areas artifacts can appear.



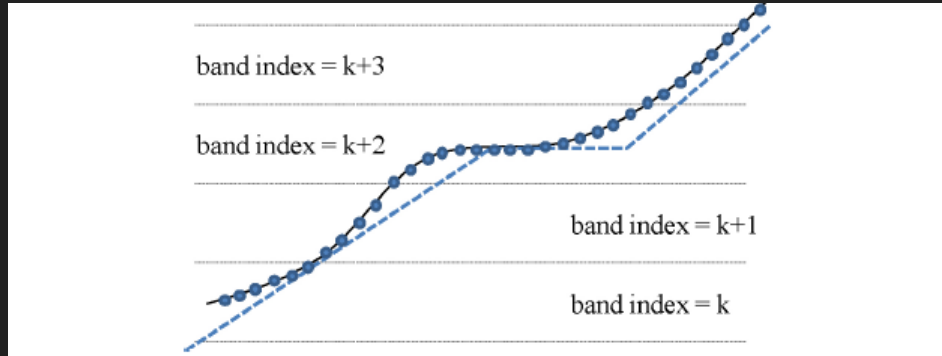
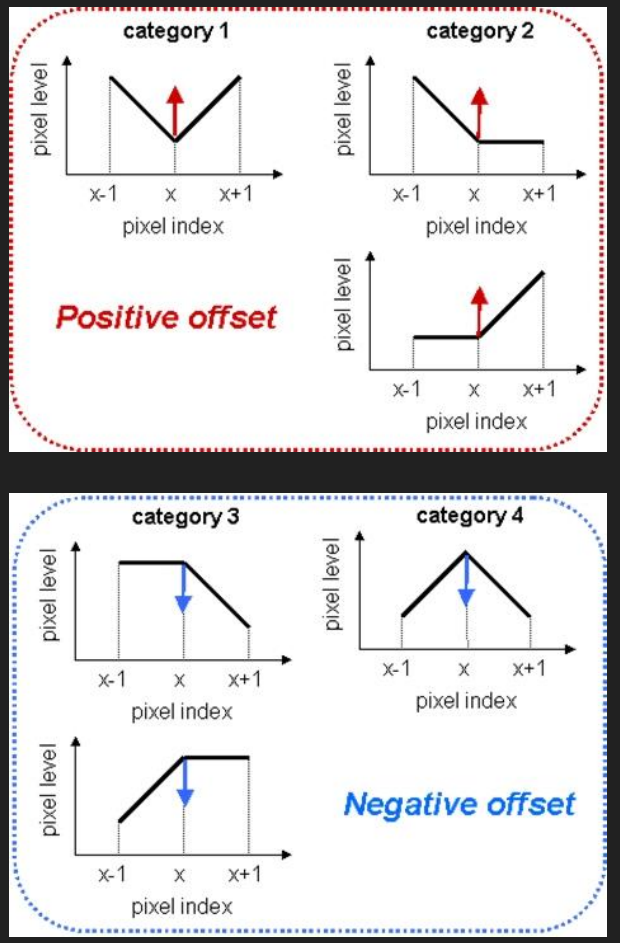


Fig. 6. Example of BO, where the dotted curve is the original samples and the solid curve is the reconstructed samples.

Result Display (EO)

- Categories 1 and 4 are associated with a local valley and a local peak along the selected 1-D pattern, respectively.
- Categories 2 and 3 are associated with concave and convex corners along the selected 1-D pattern, respectively.



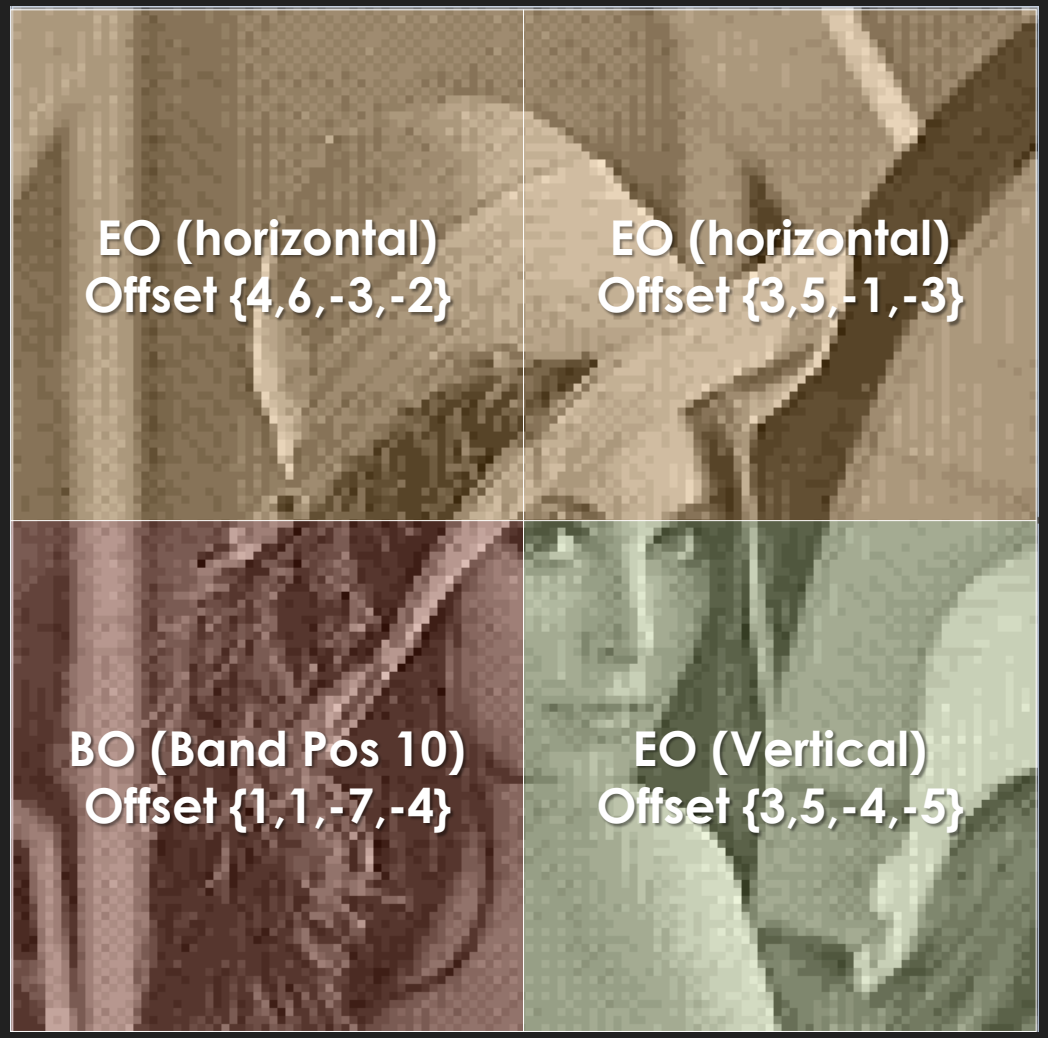
Original Image

Processed Image

Use pattern LCU size 64 x 64

Result Display

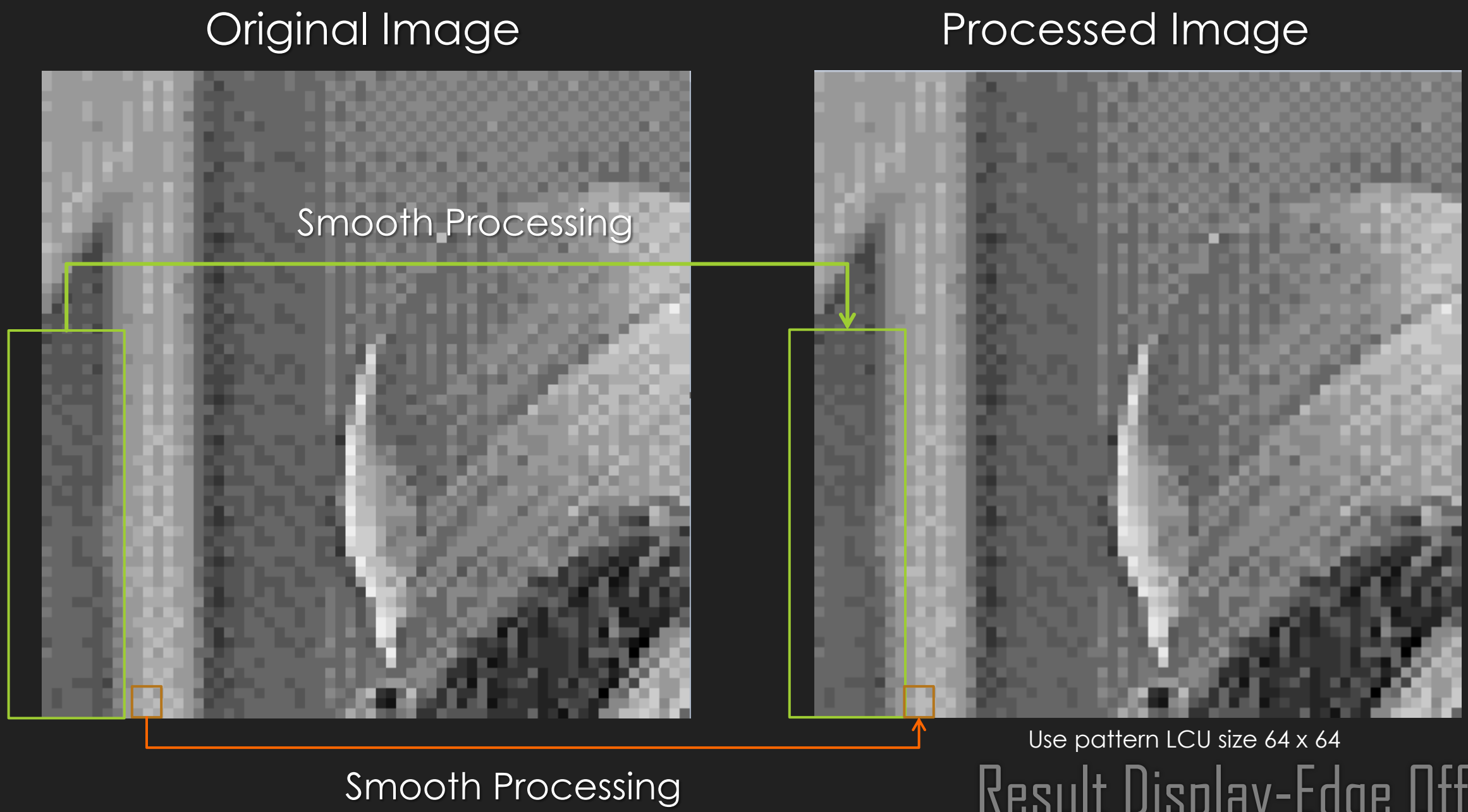
Original Image



Processed Image

Use pattern LCU size 64 x 64

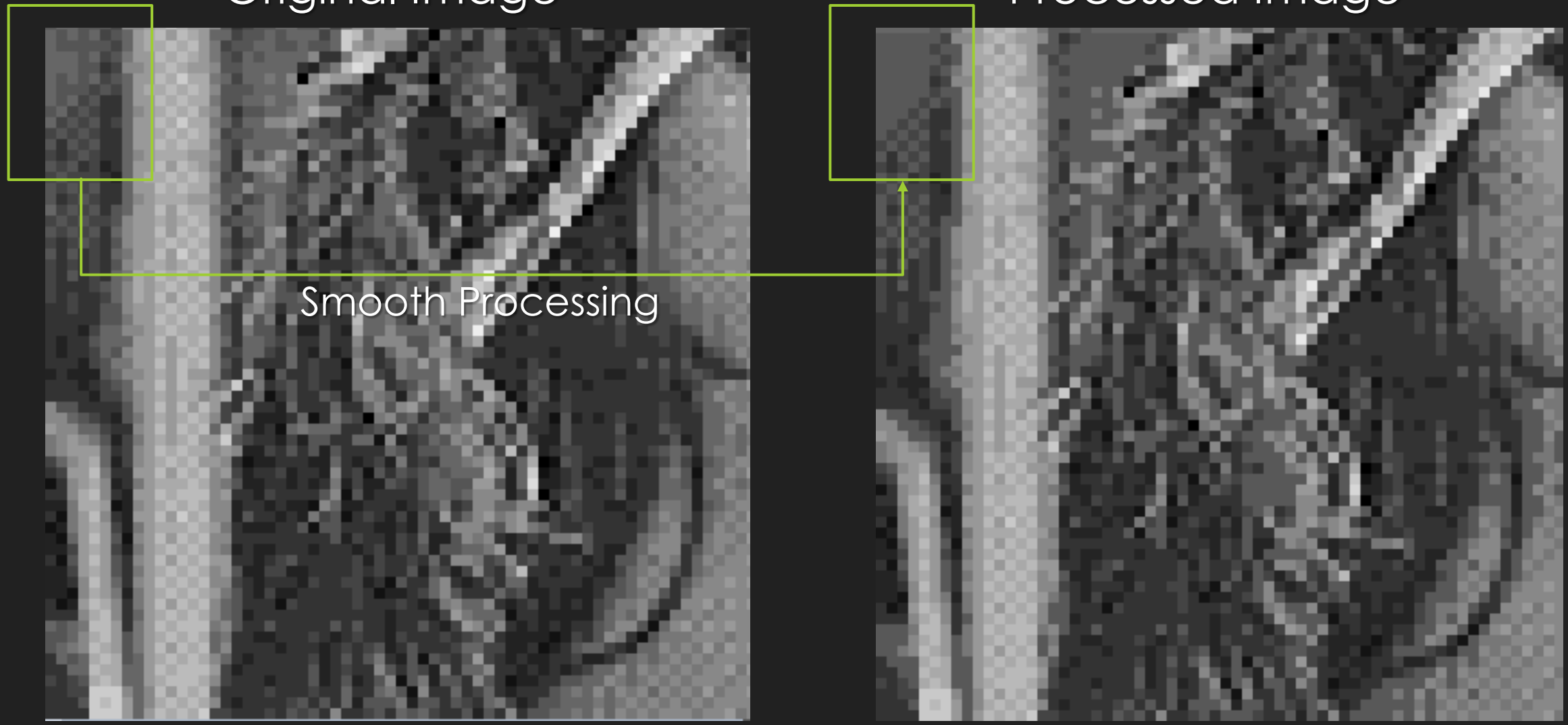
Result Display



Result Display-Edge Offset

Original Image

Processed Image



Use pattern LCU size 64 x 64

Result Display-Band Offset

Outline

- Design Concept
- Simulation Result
- Result Display
- Difficulty Encounter

Difficulty Encounter

- The usage of 1-D register/wire cannot show signal on nWave, which is hard to debug, so I extend 1-D register/wire to single register/wire separately in the end.
- Because I just follow the tutorial flow at Lab4, I cannot set some parameter by myself, like setting timing library (.lib)/ physical library (.lef/.vcleg) of SRAM 16384x8 on MMMC, perhaps some steps lacking lead to my false post-layout simulation.

Outline

- Design Concept
- Simulation Result
- Result Display
- Difficulty Encounter

Special Thanks

T.A. Wu

- The help to deal with tons of problems ,which I encountered on either lab assignment or design concept.

Special Thanks

Eric

- The help to display image through python, and the usage of pillow library.

Special Thanks

Gary

- The help to display image through matlab.

Special Thanks

Lily

- The help of grammar checking in my demo slides.

Thanks for listening