5-Line-to-32 line-Decoder/Demultiplexer

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***Abstract*—The circuit is designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems, this decoder can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast enable circuit, the delay times of this decoder and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.**

Keywords—decoder

I. INTRODUCTION

Decoder Discrete quantities of information are represented in digital system with binary codes. A binary code of n bits is capable of representing up to distinct elements of the coded information. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines. If the n-bit decoded information has unused or don't-care combinations, the decoder output will have less then 2n outputs [2].

II. TRUTH TABLE

Input			Output							
X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Table 1. Truth table of 3-to-8 line decoder.

III. CIRCUIT DIAGRAM

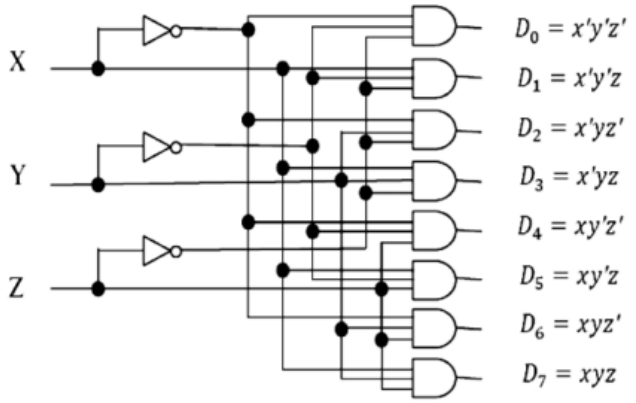
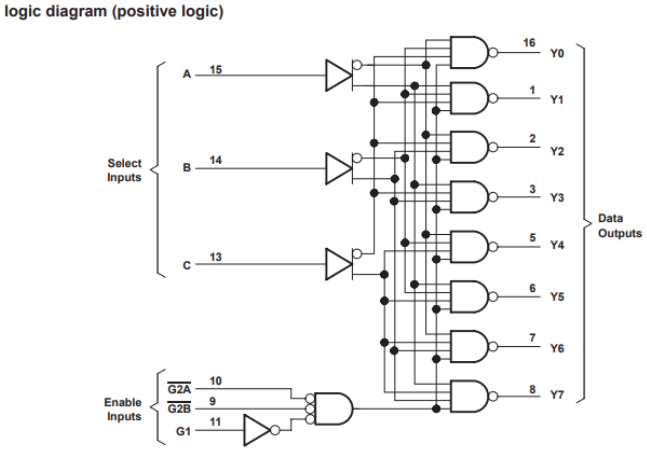


Figure 1. 3-to-8 line decoder.



IV. APPLICATION

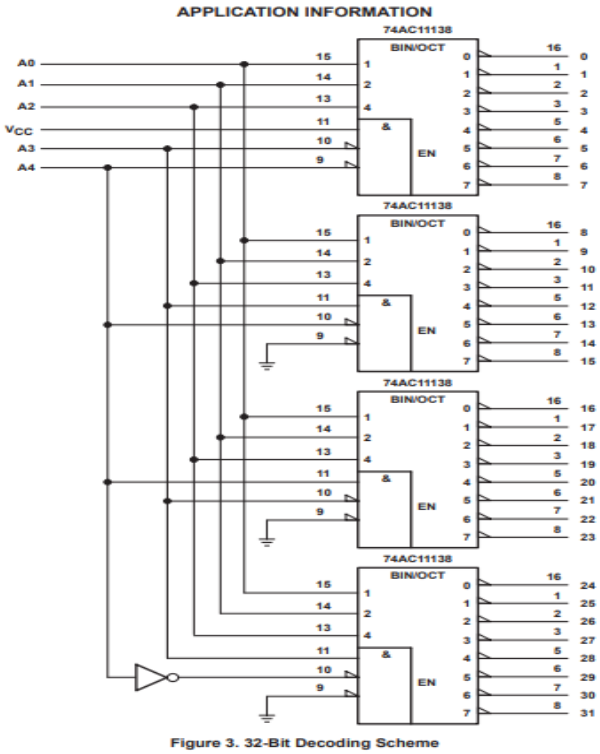


Figure 3. 32-Bit Decoding Scheme

References

[1] Texas Instrument 3:8 decoder/demultiplexer using IC 74AC11138

[2] M. M. Mano, Digital Design, Prentice Hall, 1984, pp. 167-175

[3] Design of a Qubit and a Decoder in Quantum Computing Based on a Spin Field Effect A. A. Suratgar1 , S. Rafiei*2 , A. A. Taherpour3 , A.Babaei4