1.4 pC Charge Injection, 100 pA Leakage, Quad SPST Switches

DESCRIPTION

The DG611E, DG612E, and DG613E contain four independently selectable SPST switches. They offer improved performance over the industry standard DG611 series. The DG611E and DG612E have all switches normally closed and normally open respectively, while the DG613E has 2 normally open and 2 normally closed switches.

They are designed to operate from a 3 V to 12 V single supply or from ± 3 V to ± 5 V dual supplies and are fully specified at +3 V, +5 V and ± 5 V. All control logic inputs have guaranteed 2 V logic high limits when operating from +5 V or ± 5 V supplies and 1.4 V when operating from a +3 V supply.

The DG611E, DG612E, and DG613E switches conduct equally well in both directions and offer rail to rail analog signal handling.

1.4 pC low charge injection, coupled with very low switch capacitance: 3 pF, fast switching speed: t_{on}/t_{off} 23 ns/14 ns and excellent 3 dB bandwidth: 1 GHz, make these products ideal for precision instrumentation, high-end data acquisition, automated test equipment and high speed communication applications.

Operation temperature is specified from -40 °C to +125 °C.

The DG611E, DG612E, and DG613E are available in 16 lead SOIC, TSSOP and the space saving 1.8 mm x 2.6 mm miniQFN packages.

FEATURES

- Low charge injection (1.4 pC typ.)
- Leakage current < 0.25 nA at 85 °C
- Low switch capacitance (C_{soff} 3 pF typ.)
- Low $R_{DS(on)}$ - 115 Ω max.
- Fully specified with single supply operation at 3 V, 5 V, and dual supplies at ± 5 V
- Low voltage, 2.5 V CMOS/TTL compatible
- 1 GHz, 3 dB bandwidth
- Excellent isolation performance (-59 dB at 10 MHz)
- Excellent crosstalk performance (-74 dB at 10 MHz)
- Fully specified from -40 °C to +85 °C and -40 °C to +125 °C
- 16 lead SOIC, TSSOP and miniQFN package (1.8 mm x 2.6 mm)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free

RoHS COMPLIANT

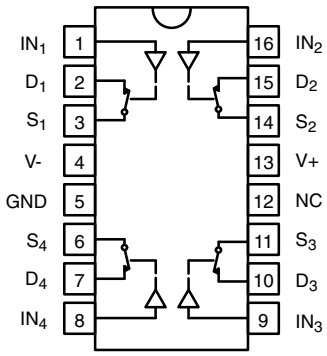
HALOGEN FREE

APPLICATIONS

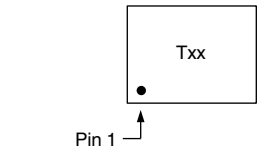
- Precision instrumentation
- Medical instrumentation
- Automated test equipment
- High speed communications applications
- High-end data acquisition
- Sample and hold applications
- Sample and hold systems

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG611E
SOIC/TSSOP

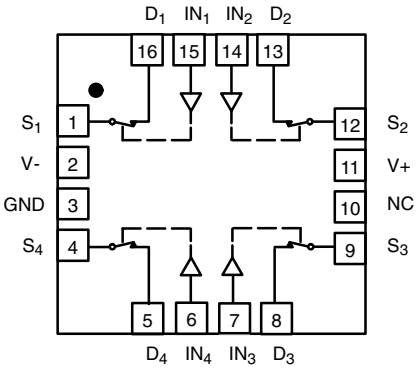


Top View



Device Marking: Txx for DG611E
(miniQFN16) Uxx for DG612E
Vxx for DG613E
xx = Date/Lot Traceability Code

DG611E
miniQFN

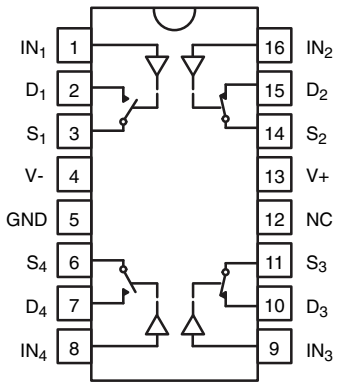


Top View

TRUTH TABLE		
LOGIC	**DG611E**	**DG612E**
0	On	Off
1	Off	On

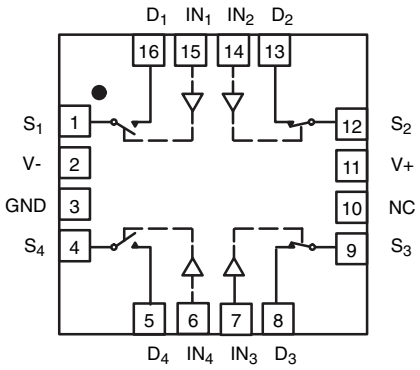
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG613E
SOIC/TSSOP

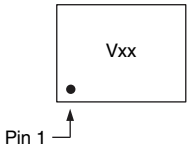


Top View

DG613E
miniQFN



Top View



Device Marking: Vxx for DG613E
(miniQFN16)

TRUTH TABLE		
LOGIC	**SW1, SW4**	**SW2, SW3**
0	Off	On
1	On	Off

ORDERING INFORMATION		
TEMP. RANGE	**PACKAGE**	**PART NUMBER**
-40 °C to +125 °C [a]	16-pin TSSOP	DG611EEQ-T1-GE4 DG612EEQ-T1-GE4 DG613EEQ-T1-GE4
	16-pin narrow SOIC	DG611EEY-T1-GE4 DG612EEY-T1-GE4 DG613EEY-T1-GE4
	16-pin miniQFN	DG611EEN-T1-GE4 DG612EEN-T1-GE4 DG613EEN-T1-GE4

Note

a. -40 °C to +85 °C datasheet limits apply

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)			
PARAMETER		**LIMIT**	**UNIT**
V+ to V-		14	V
GND to V-		7	
Digital inputs [a], V_S, V_D		(V-) - 0.3 V to (V+) + 0.3 V or 30 mA, whichever occurs first	
Continuous current (any terminal)		30	mA
Peak current, S or D (pulsed 1 ms, 10 % duty cycle)		100	
Storage temperature		-65 to +150	°C
Power dissipation (package) [b]	16-pin TSSOP [c]	450	mW
	16-pin miniQFN [d]	525	
	16-pin narrow SOIC [e]	640	
Thermal resistance (package) [b]	16-pin TSSOP	178	°C/W
	16-pin miniQFN	152	
	16-pin narrow SOIC	125	
ESD / HBM	EIA / JESD22-A114-A	2k	V
ESD / CDM	EIA / JESD22-C101-A	1k	
Latch up	JESD78	300	mA

Notes

a. Signals on SX, DX, or INX exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings
b. All leads welded or soldered to PC board
c. Derate 5.6 mW/°C above 70 °C
d. Derate 6.6 mW/°C above 70 °C
e. Derate 8 mW/°C above 70 °C
f. Manual soldering with iron is not recommended for leadless components. The miniQFN-16 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

SPECIFICATIONS FOR DUAL SUPPLIES (V+ = +5 V, V- = -5 V)									
PARAMETER	**SYMBOL**	**TEST CONDITIONS UNLESS OTHERWISE SPECIFIED** V + = +5 V, V - = - 5 V V_{IN} = 2 V, 0.8 V [a]	**TEMP.** [b]	**LIMITS**					**UNIT**
				TYP. [c]	**-40 °C to +125 °C**		**-40 °C to +85 °C**		
					MIN. [d]	**MAX.** [d]	**MIN.** [d]	**MAX.** [d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	- 5	5	- 5	5	V
Drain-source On-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	72	-	115	-	115	Ω
			Full	-	-	160	-	140	
On-resistance match	$\Delta R_{DS(on)}$	I_S = 1 mA, V_D = ± 3 V	Room	0.6	-	2.5	-	2.5	
			Full	-	-	5	-	4.5	
On-resistance flatness	$R_{flat(on)}$	I_S = 1 mA, V_D = -3 V, 0 V, +3 V	Room	15	-	20	-	20	
			Full	-	-	30	-	25	
Switch off leakage current	$I_{S(off)}$	V+ = 5.5 V, V- = -5.5 V V_D = +4.5 V / -4.5 V V_S = -4.5 V / +4.5 V	Room	± 0.0005	-0.1	0.1	-0.1	0.1	nA
			Full	-	-2	2	-0.25	0.25	
	$I_{D(off)}$		Room	± 0.006	-0.1	0.1	-0.1	0.1	
			Full	-	-2	2	-0.25	0.25	
Switch on leakage current	$I_{D(on)}$	V+ = 5.5 V, V- = -5.5 V V_D = V_S = ± 4.5 V	Room	± 0.008	-0.1	0.1	-0.1	0.1	
			Full	-	-6	6	-0.25	0.25	
Digital Control									
Input current, V_{IN} low	I_{IL}	V_{IN} under test = 0.8 V	Full	0.01	-0.1	0.1	-0.1	0.1	µA
Input current, V_{IN} high	I_{IH}	V_{IN} under test = 2 V	Full	0.01	-0.1	0.1	-0.1	0.1	
Input capacitance [e]	C_{IN}	f = 1 MHz	Room	3	-	-	-	-	pF
Dynamic Characteristics									
Turn-on time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = ± 3 V	Room	23	-	50	-	50	ns
			Full	-	-	75	-	60	
Turn-off time	t_{OFF}		Room	14	-	35	-	35	
			Full	-	-	50	-	45	
Break-before-make time delay	t_{BBM}	DG613E only, V_S = 3 V R_L = 300 Ω, C_L = 35 pF	Room	15	-	-	-	-	
			Full	-	2	-	2	-	
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	1.4	-	-	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 10 MHz	Room	-59	-	-	-	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-74	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	1	-	-	-	-	GHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz; V_S = 0 V	Room	3	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	3	-	-	-	-	
Drain on capacitance [e]	$C_{D(on)}$	f = 1 MHz; V_S = V_D = 0 V	Room	7	-	-	-	-	
Total harmonic distortion [e]	THD	Signal = 1 V_{RMS}, 20 Hz to 20 kHz, R_L = 600 Ω	Room	0.13	-	-	-	-	%
Power Supplies									
Power supply current	I+	V+ = +5 V, V- = -5 V V_{IN} = 0 V or 5 V	Room	0.001	-	0.1	-	0.1	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	

SPECIFICATIONS FOR SINGLE SUPPLIES (V+ = +5 V, V- = 0 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V+ = +5 V, V- = 0 V V_{IN} = 2 V, 0.8 V [a]	TEMP.[b]	LIMITS					UNIT
				TYP.C	-40 °C to +125 °C		-40 °C to +85 °C		
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	0	5	0	5	V
Drain-source On-resistance	$R_{DS(on)}$	V+ = 5 V, V- = 0 V I_S = 1 mA, V_D = +3.5 V	Room	130	-	170	-	170	Ω
			Full	-	-	235	-	215	
On-resistance match	$\Delta R_{DS(on)}$	V+ = 5 V, V- = 0 V, I_S = 1 mA, V_D = 3.5 V	Room	0.6	-	5	-	5	
			Full	-	-	12	-	10	
On-resistance flatness	$R_{flat(on)}$	V+ = 5 V, V- = 0 V, I_S = 1 mA, V_D = 0 V, 3.5 V	Room	29	-	50	-	50	
			Full	-	-	100	-	90	
Switch off leakage current	$I_{S(off)}$	V+ = 5.5 V, V- = 0 V V_D = 4.5 V / 1 V V_S = 1 V / 4.5 V	Room	± 0.0005	-0.1	0.1	-0.1	0.1	nA
			Full	-	-2	2	-0.25	0.25	
	$I_{D(off)}$		Room	± 0.006	-0.1	0.1	-0.1	0.1	
			Full	-	-2	2	-0.25	0.25	
Switch on leakage current	$I_{D(on)}$	V+ = 5.5 V, V- = 0 V V_D = V_S = 1 V / 4.5 V	Room	± 0.008	-0.1	0.1	-0.1	0.1	
			Full	-	-6	6	-0.25	0.25	
Digital Control									
Input current, V_{IN} low	I_{IL}	V_{IN} under test = 0.8 V	Full	0.01	-0.1	0.1	-0.1	0.1	µA
Input current, V_{IN} high	I_{IH}	V_{IN} under test = 2 V	Full	0.01	-0.1	0.1	-0.1	0.1	
Input capacitance [e]	C_{IN}	f = 1 MHz	Room	4	-	-	-	-	pF
Dynamic Characteristics									
Turn-on time [e]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 3 V	Room	33	-	60	-	60	ns
			Full	-	-	90	-	80	
Turn-off Time [e]	t_{OFF}		Room	14	-	35	-	35	
			Full	-	-	45	-	40	
Break-before-make time delay [e]	t_{BBM}	DG613E only, V_S = 3 V R_L = 300 Ω, C_L = 35 pF	Room	19	-	-	-	-	
			Full	-	2	-	2	-	
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Full	1.5	-	-	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 10 MHz	Room	-59	-	-	-	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-70	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	880	-	-	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz; V_S = 0 V	Room	3	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	3	-	-	-	-	
Drain on capacitance [e]	$C_{D(on)}$	f = 1 MHz; V_S = V_D = 0 V	Room	7	-	-	-	-	
Power Supplies									
Power supply current	I+	V_{IN} = 0 V or 5 V	Room	0.001	-	0.1	-	0.1	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	

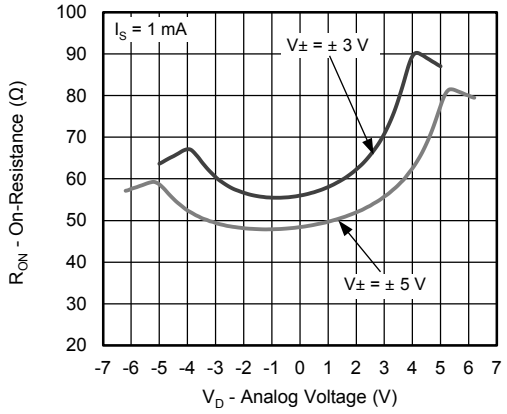
SPECIFICATIONS FOR SINGLE SUPPLIES (V+ = +3 V, V- = 0 V)									
PARAMETER	SYMBOL	TEST CONDITIONS UNLESS OTHERWISE SPECIFIED V + = +3 V, V - = - 0 V V_{IN} = 1.4 V, 0.6 V [a]	TEMP. [b]	LIMITS					UNIT
				TYP. [c]	-40 °C to +125 °C		-40 °C to +85 °C		
					MIN. [d]	MAX. [d]	MIN. [d]	MAX. [d]	
Analog Switch									
Analog signal range [e]	V_{ANALOG}		Full	-	0	3	0	3	V
Drain source On-resistance	$R_{DS(on)}$	I_S = 1 mA, V_D = +1.5 V	Room	305	-	420	-	420	Ω
			Full	-	-	600	-	500	
Switch off leakage current	$I_{S(off)}$	V+ = 3.3 V, V- = 0 V V_D = 3 V / 0.3 V V_S = 0.3 V / 3 V	Room	± 0.0005	-0.1	0.1	-0.1	0.1	nA
			Full	-	-2	2	-0.25	0.25	
	$I_{D(off)}$		Room	± 0.006	-0.1	0.1	-0.1	0.1	
			Full	-	-2	2	-0.25	0.25	
Switch on leakage current	$I_{D(on)}$	V+ = 3.3 V, V- = 0 V V_D = V_S = 0.3 V / 3 V	Room	± 0.008	-0.1	0.1	-0.1	0.1	
			Full	-	-6	6	-0.25	0.25	
Digital Control									
Input current, V_{IN} low	I_{IL}	V_{IN} under test = 0.6 V	Full	0.01	-0.1	0.1	-0.1	0.1	µA
Input current, V_{IN} high	I_{IH}	V_{IN} under test = 1.4 V	Full	0.01	-0.1	0.1	-0.1	0.1	
Input capacitance [e]	C_{IN}	f = 1 MHz	Room	4	-	-	-	-	pF
Dynamic Characteristics									
Turn-on time	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_S = 2 V	Room	76	-	115	-	115	ns
			Full	-	-	180	-	155	
Turn-off time	t_{OFF}		Room	31	-	58	-	58	
			Full	-	-	65	-	60	
Break-before-make time delay	t_{BBM}	DG613 only, V_S = 2 V R_L = 300 Ω, C_L = 35 pF	Room	60	-	-	-	-	
			Full	-	10	-	10	-	
Charge injection [e]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room	1.4	-	-	-	-	pC
Off isolation [e]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 10 MHz	Room	-59	-	-	-	-	dB
Channel-to-channel crosstalk [e]	X_{TALK}		Room	-71	-	-	-	-	
Bandwidth [e]	BW	R_L = 50 Ω, C_L = 5 pF	Room	830	-	-	-	-	MHz
Source off capacitance [e]	$C_{S(off)}$	f = 1 MHz; V_S = 0 V	Room	3	-	-	-	-	pF
Drain off capacitance [e]	$C_{D(off)}$		Room	4	-	-	-	-	
Drain on capacitance [e]	$C_{D(on)}$	f = 1 MHz; V_S = V_D = 0 V	Room	7	-	-	-	-	
Power Supplies									
Power supply current	I+	V_{IN} = 0 V or 3 V	Room	0.001	-	0.1	-	0.1	µA
			Full	-	-	1	-	1	
Negative supply current	I-		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	
Ground current	I_{GND}		Room	-0.001	-0.1	-	-0.1	-	
			Full	-	-1	-	-1	-	

Notes

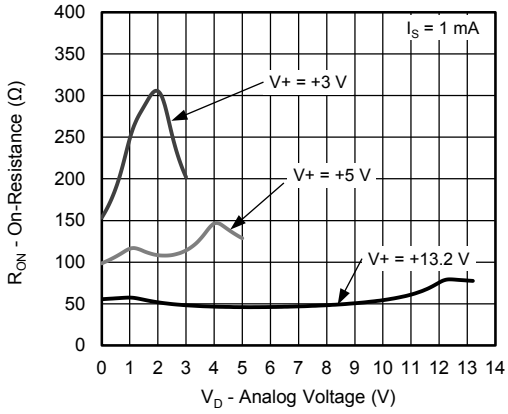
a. V_{IN} = input voltage to perform proper function
b. Room = 25 °C, Full = as determined by the operating temperature suffix
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet
e. Guaranteed by design, not subject to production test

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

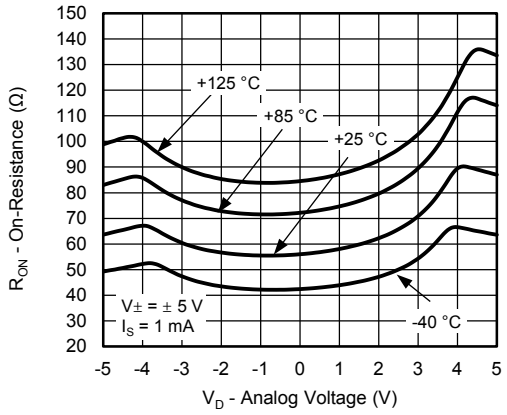
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



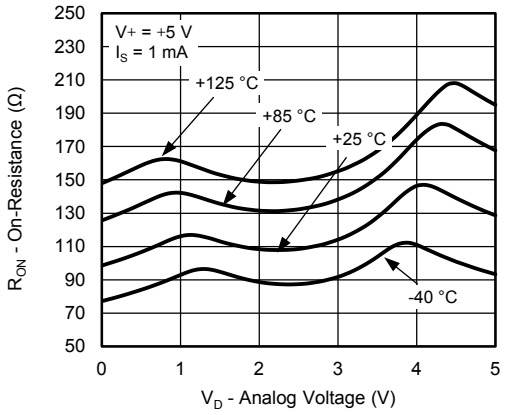
On-Resistance vs. V_D (Dual Supply)



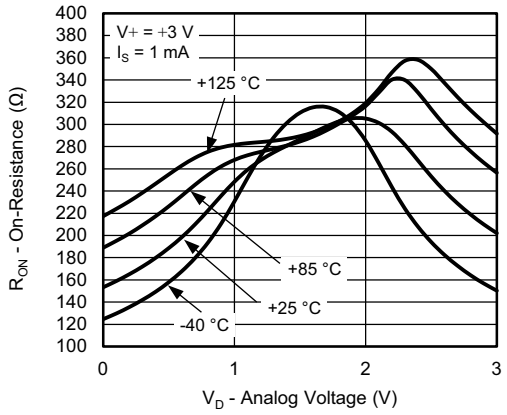
On-Resistance vs. V_D (Single Supply)



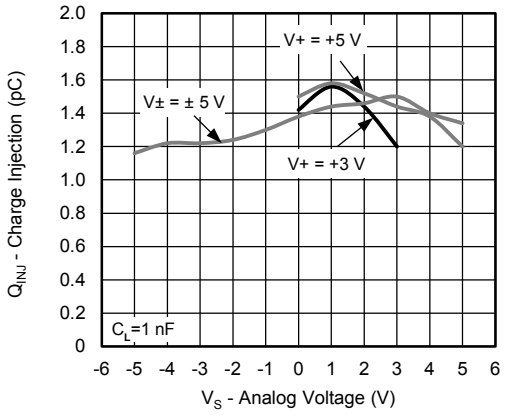
On-Resistance vs. Temperature (Dual Supply)



On-Resistance vs. Temperature (Single Supply)

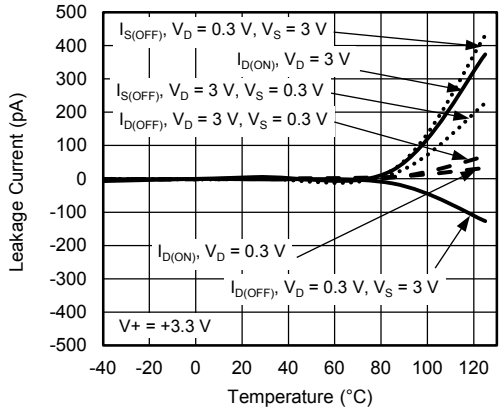


On-Resistance vs. Temperature (Single Supply)

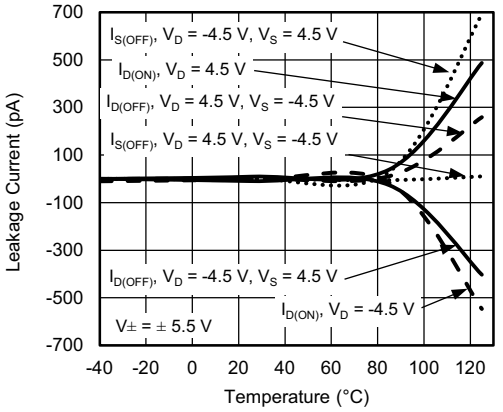


Charge Injection vs. Analog Voltage

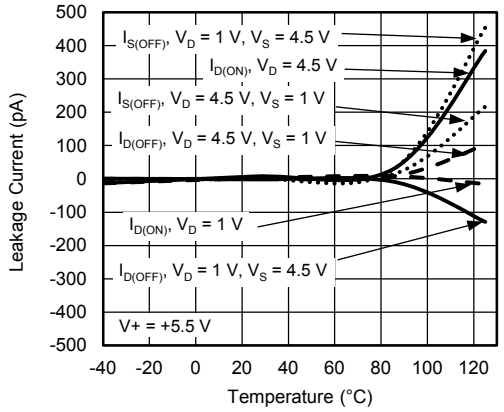
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



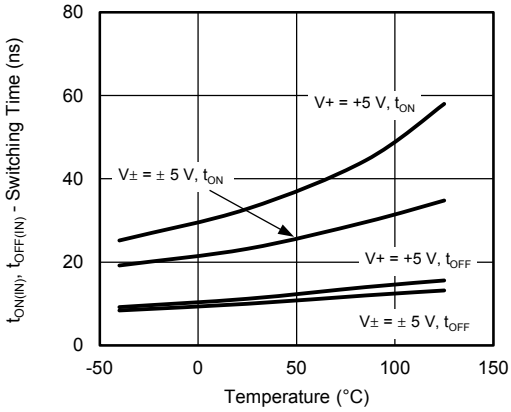
Leakage Current vs. Temperature



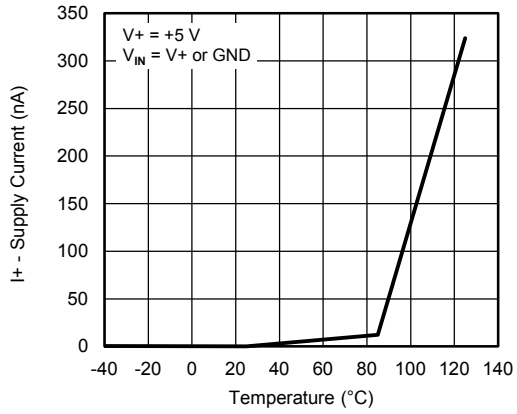
Leakage Current vs. Temperature



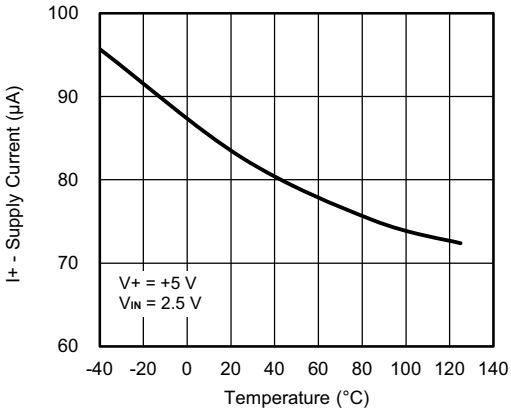
Leakage Current vs. Temperature



Switching Time vs. Temperature

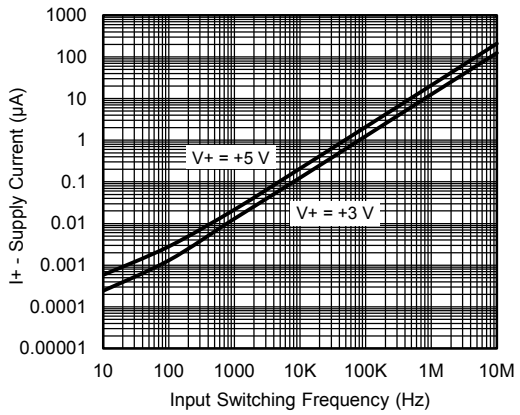


Supply Current vs. Temperature

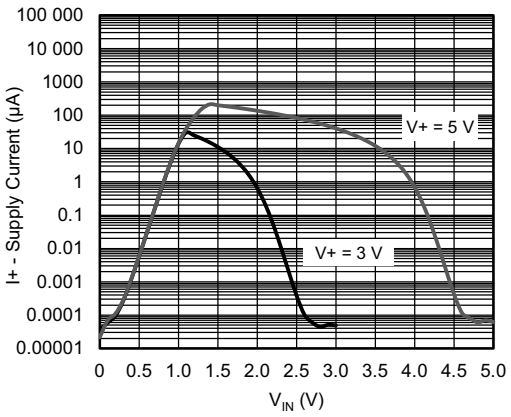


Supply Current vs. Temperature

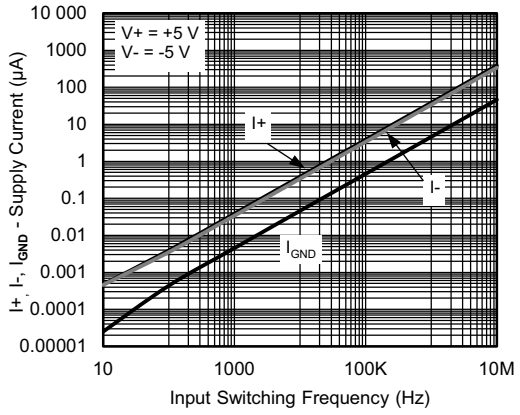
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



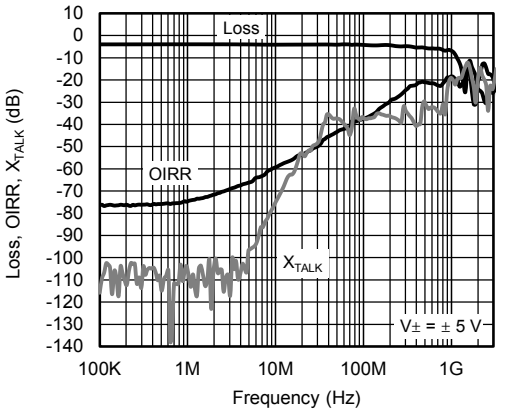
Supply Current vs. Switching Frequency



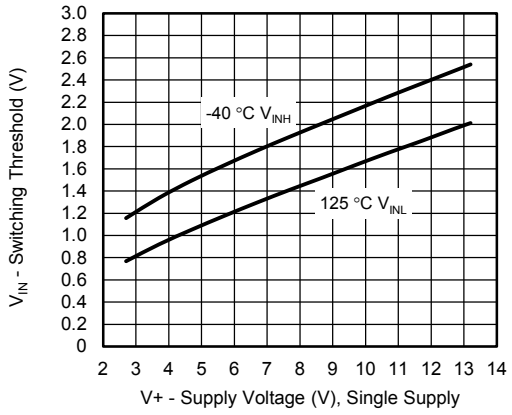
Supply Current vs. Input Voltage



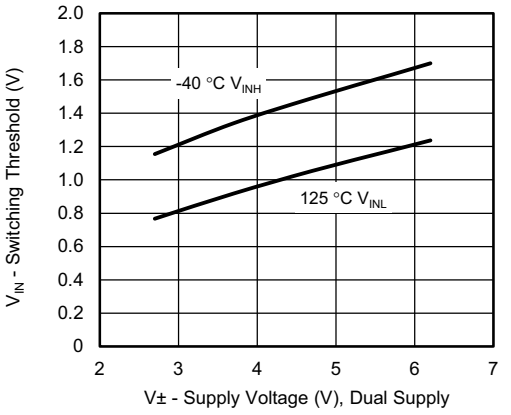
Supply Current vs. Switching Frequency



Insertion Loss, Off-Isolation, Crosstalk vs. Frequency

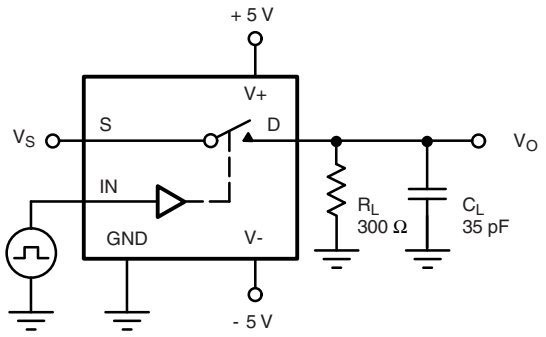


Switching Threshold vs. Supply Voltage (Single Supply)



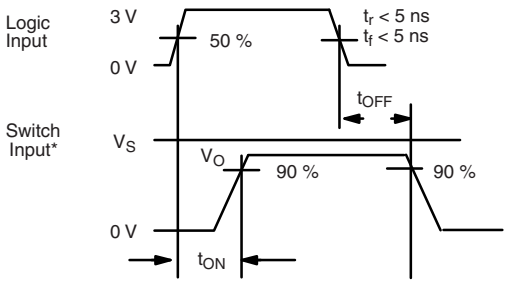
Switching Threshold vs. Supply Voltage (Dual Supply)

TEST CIRCUITS



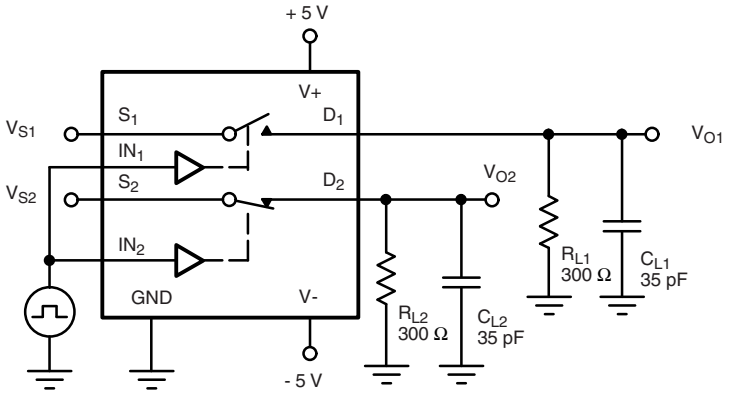
C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Fig. 1 - Switching Time



C_L (includes fixture and stray capacitance)

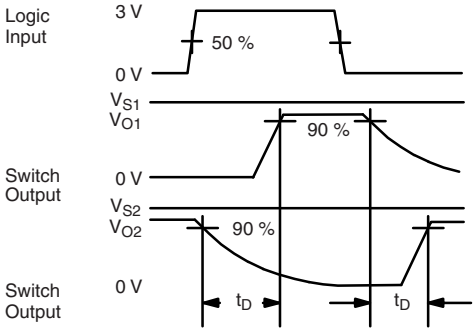
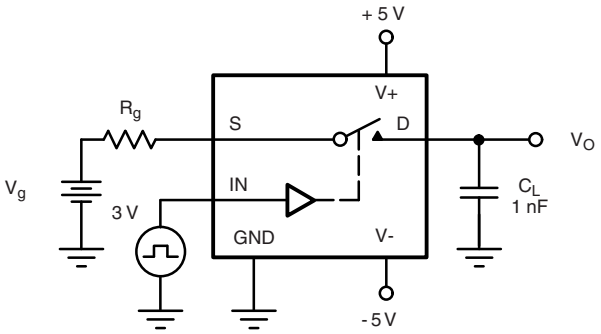


Fig. 2 - Break-Before-Make (DG613E)



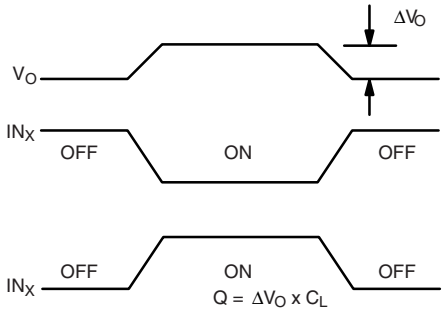


Fig. 3 - Charge Injection

TEST CIRCUITS

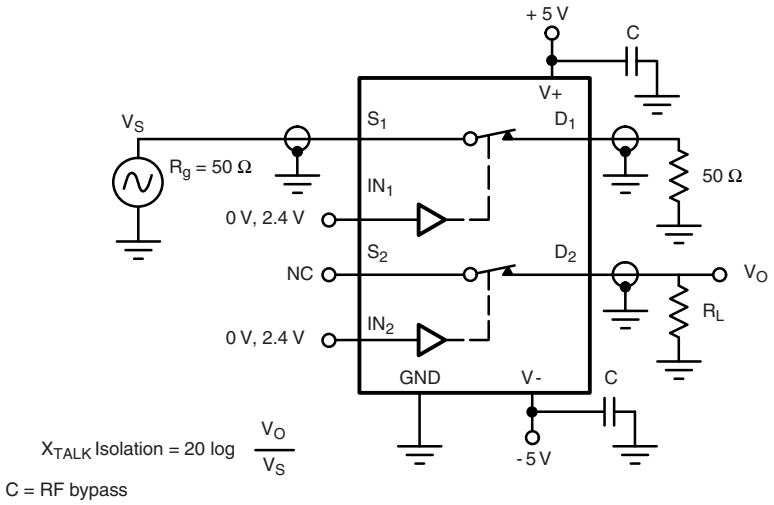


Fig. 4 - Crosstalk

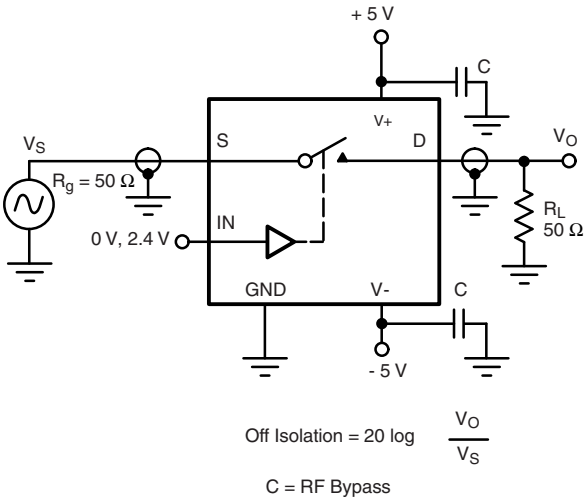


Fig. 5 - Off-Isolation

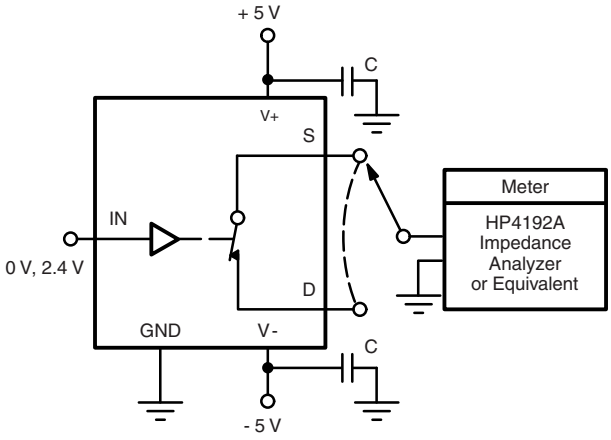
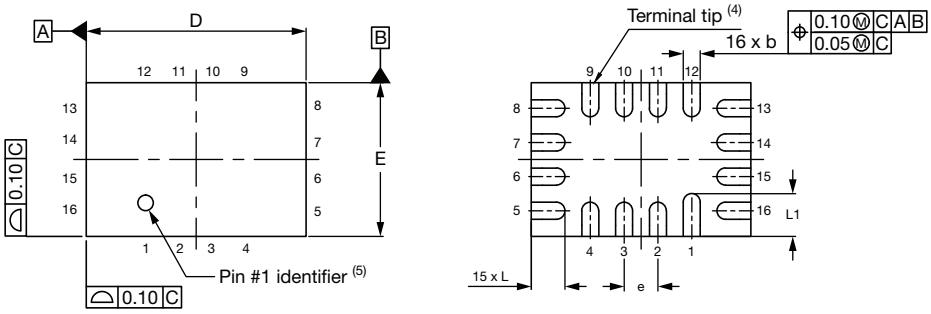


Fig. 6 - Source / Drain Capacitances

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?78910.

Thin miniQFN16 Case Outline



DIMENSIONS	MILLIMETERS (1)			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0	-	0.05	0	-	0.002
A3	0.15 ref.			0.006 ref.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.50	2.60	2.70	0.098	0.102	0.106
e	0.40 BSC			0.016 BSC		
E	1.70	1.80	1.90	0.067	0.071	0.075
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.45	0.50	0.55	0.018	0.020	0.022
N (3)	16			16		
Nd (3)	4			4		
Ne (3)	4			4		

Notes

(1) Use millimeters as the primary measurement.

(2) Dimensioning and tolerances conform to ASME Y14.5M. - 1994.

(3) N is the number of terminals. Nd and Ne is the number of terminals in each D and E site respectively.

(4) Dimensions b applies to plated terminal and is measured between 0.15 mm and 0.30 mm from terminal tip.

(5) The pin 1 identifier must be existed on the top surface of the package by using identification mark or other feature of package body.

(6) Package warpage max. 0.05 mm.

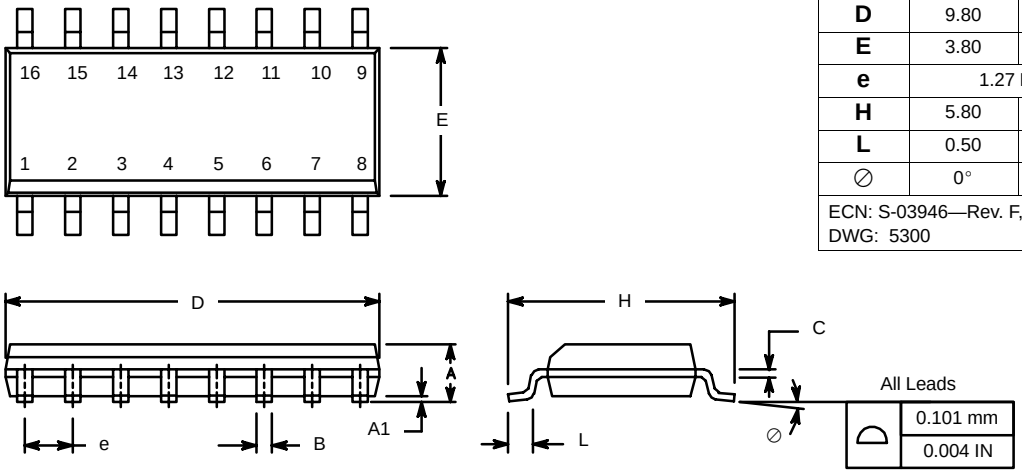
ECN: T16-0226-Rev. B, 09-May-16
DWG: 6023

SOIC (NARROW): 16-LEAD

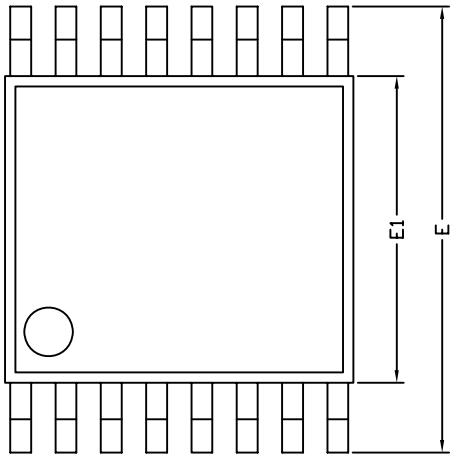
JEDEC Part Number: MS-012

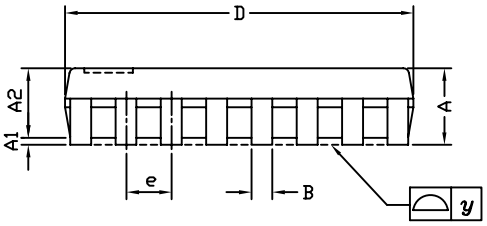
Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.38	0.51	0.015	0.020
C	0.18	0.23	0.007	0.009
D	9.80	10.00	0.385	0.393
E	3.80	4.00	0.149	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
L	0.50	0.93	0.020	0.037
⊘	0°	8°	0°	8°

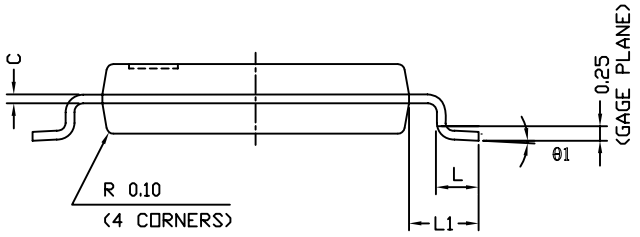
ECN: S-03946—Rev. F, 09-Jul-01
DWG: 5300



TSSOP: 16-LEAD

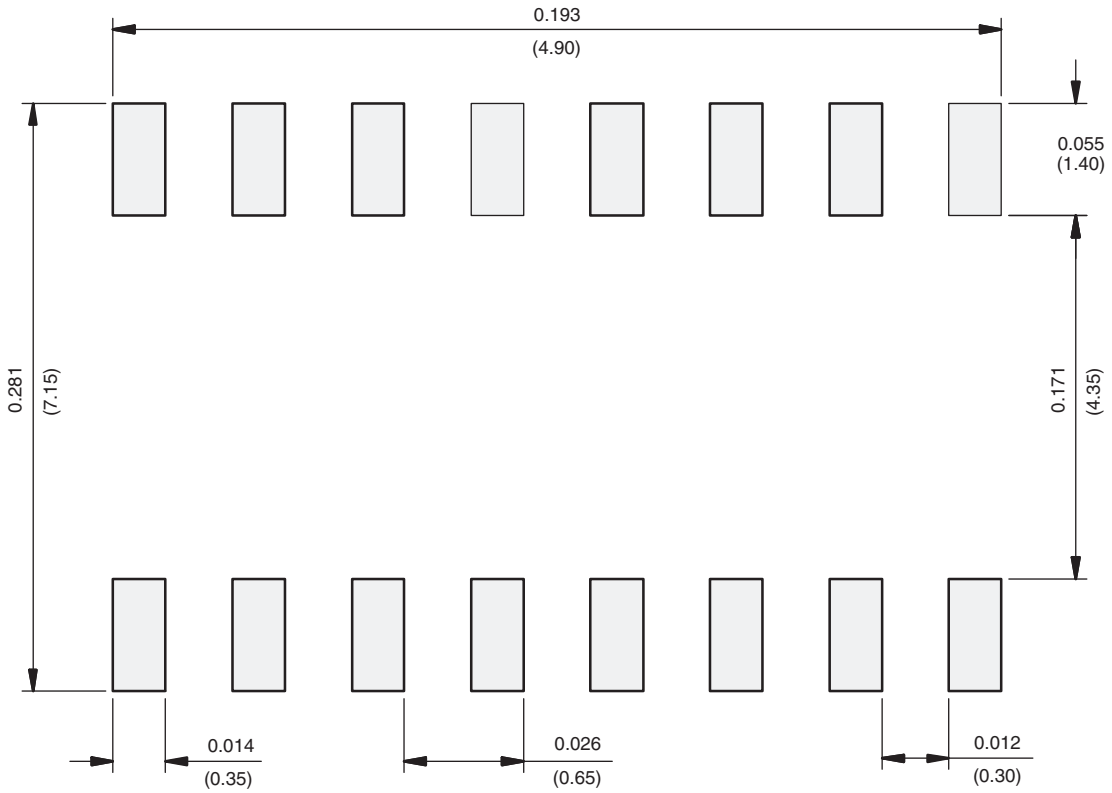






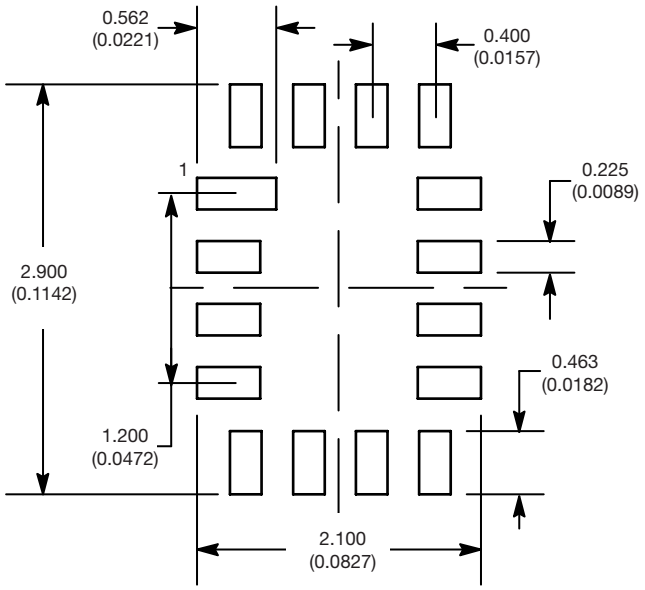
Symbols	DIMENSIONS IN MILLIMETERS		
	Min	Nom	Max
A	-	1.10	1.20
A1	0.05	0.10	0.15
A2	-	1.00	1.05
B	0.22	0.28	0.38
C	-	0.127	-
D	4.90	5.00	5.10
E	6.10	6.40	6.70
E1	4.30	4.40	4.50
e	-	0.65	-
L	0.50	0.60	0.70
L1	0.90	1.00	1.10
y	-	-	0.10
θ1	0°	3°	6°
ECN: S-61920-Rev. D, 23-Oct-06 DWG: 5624			

RECOMMENDED MINIMUM PAD FOR TSSOP-16



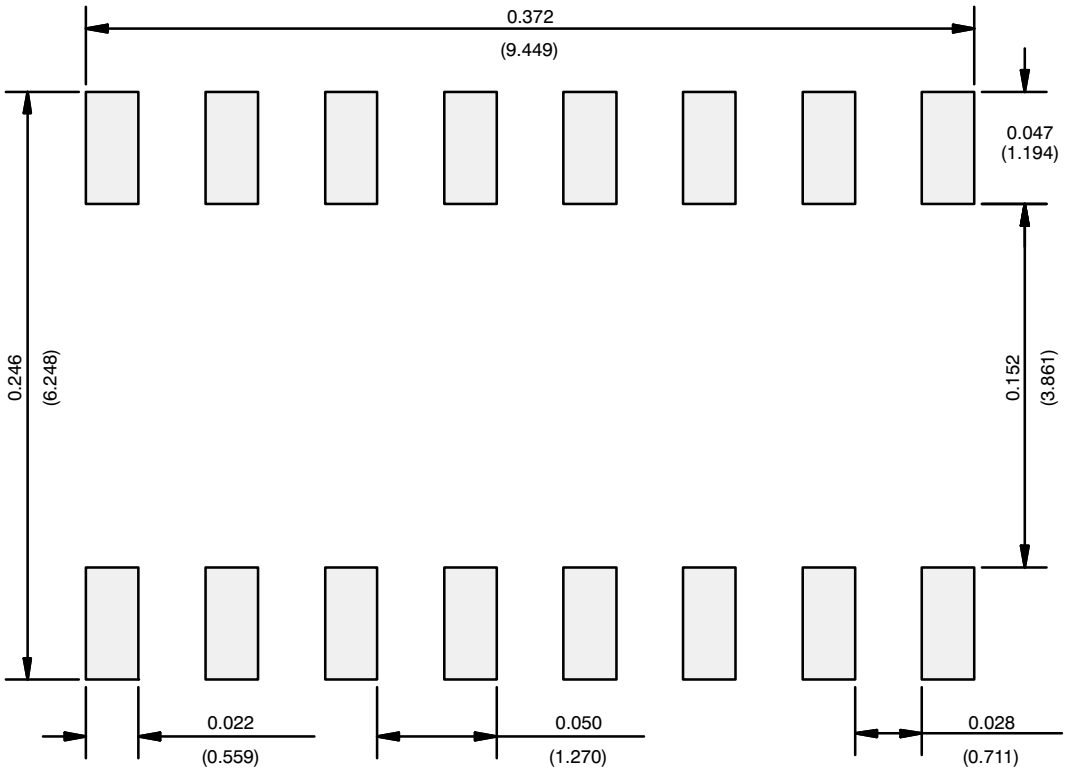
Recommended Minimum Pads
Dimensions in inches (mm)

RECOMMENDED MINIMUM PADS FOR MINI QFN 16L



Mounting Footprint
Dimensions in mm (inch)

RECOMMENDED MINIMUM PADS FOR SO-16



Recommended Minimum Pads
Dimensions in Inches/(mm)

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