Digital Logic Design

Assignment 02

For problems 1-6, Draw the truth table, write the corresponding Boolean Function in Sum of Min-terms form, simplify the Boolean Function using K-Map, draw the logic circuits using AND/OR/NOT gates and finally write down the HDL code.

Problem 1:
Design a combinational circuit that takes a four-bit input and determines whether the input binary number is a Fibonacci number. You can consider zero as the first Fibonacci number. In case if the number represents a Fibonacci number, then logic 1 is generated else logic 0 is generated.

Problem 2:
Consider a transmission system that transmits four data bits at a time. For achieving reliability both the systems decide to work on even parity. **Design** a circuit that generates the required parity bit at the emitter side. Also design a circuit that checks the parity at the receiving side.

Problem 3:
Design a combinational circuit with three inputs x, y, and z and three outputs A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

Problem 4:
Design a combinational circuit that converts a three-bit binary number to a three-bit Gray code

Problem 5:
a. **Design** a Half-subtractor
b. **Design** a Full-subtractor circuit.
c. **Design** an Adder-Subtractor circuit.

Problem 6:
Design a 3x8 Decoder

Problem 7:
Draw the block level logic diagram of a higher order decoder using lower order decoders:
a. A 4x16 decoder using two 3x8 decoders.
b. A 5x32 decoder using four 3x8 decoders and a 2x4 decoder.

Problem 8:
Implement the following combinational circuits using decoders.
a. Write down truth table for a Full Subtractor. Write down the Boolean functions in sum of min-terms form. Draw the logic circuit using decoder of appropriate size.
b. Write down truth table for a combinational circuit that converts a 4-bit Gray Code to 4-bit binary number. Write down the Boolean functions for outputs in sum of min-terms form. Draw the logic circuit using a decoder of appropriate size.

Problem 9:
An encoder has two limitations. An output of all zeros may mean that all inputs are zero or may mean that d_0 is one. To solve this issue, we can have an additional output 'v' of the encoder, which will be zero when all the inputs are zero. Second limitation is if more than one input lines are high the encoder generates unpredictable output. Design a 4x2 low high priority encoder that handles both these limitations. Construct truth table using all 16 combinations and explain how this truth table can be reduced to a smaller truth table and how you can derive the min-terms for the outputs from the reduced truth table. Draw the circuit diagram

Problem 10:

a. Draw block level logic diagram of a 2x1 Multiplexer, draw its truth table, derive its Boolean function, draw its gate level diagram and finally write down HDL code for the Mux chip.
b. Draw block level logic diagram of a Mux4way chip (using three 2x1 Mux chips) and write down its HDL code.

Problem 11:

a. Draw block level logic diagram of a MUX16 chip using sixteen 2x1 MUX chips. The chip receives two 16 bit numbers and outputs one out of them depending on the single selection line. Write down its HDL to implement this chip.
b. Draw block level logic diagram of a MUX4way16 chip using three MUX16 chips (designed in part a). The chip receives four single bits as input and outputs one out of them depending on the two selection lines. Write down its HDL to implement this chip.
c. Draw block level logic diagram of a MUX8way16 chip using two MUX4way16 chips (designed in part c) and a MUX16 chip (designed in part a). The chip receives eight 16-bit inputs and outputs one 16-bit number out of the eight numbers, depending on the three selection lines. Write down its HDL to implement this chip.

Problem 12:

Draw the block diagram of the following combinational circuits using appropriate size multiplexers. Highlight how you find the size of multiplexer for each circuit

a. Full Subtractor
b. $F(A,B,C,D) = \Sigma(2, 4, 6, 7, 8, 9, 10)$

Problem 13:

a. Design a 1x8 DEMUX and finally write down HDL code for that chip.
b. Draw block diagram of a 1x16 DEMUX using two 1x8 DEMUX and one 1x2 DEMUX.
c. Draw logic circuit of a Full Adder using appropriate size DEMUX

Submission Instructions:

- **Solutions to all the parts must be your own hard work. DON'T let anyone copy your assignment. In case of a copy both students will be awarded a ZERO may be some negative marks as well.**
- **You have to submit your assignment in HAND written form on plain A4 Sheets.**
- **Attach a cover sheet showing the assignment title, course and your personal information.**

TIME IS JUST LIKE MONEY.
THE LESS WE HAVE IT;
THE MORE WISELY WE SPEND IT.
Manage your time and Good Luck