SCL 0.18µm (Analog) PDK

User Guide

Advanced VLSI Design Lab

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Revision History

Rev.	Author	Last updated on
1.0	Samiran Dam	6th Nov., 2015

1. Basic Setup

1.1. Setup your working directory

Step 1: Copy the working directory from the following path into your home directory -

Command:

cp ~design_installer/scl/scl180_analog.zip .

Step 2: Unzip the **scl180_analog.zip** and enter into **scl180_analog** directory (it is the working directory <**WORKING_DIR**>).

1.2. Working directory structure

<**WORKING_DIR**>
- **cdl_netlists**
  - *scale.cdl*
- **DEMO**
- **Docs**
- **physical_verification**
  - **drc**
    - **rsf**
      - *drc.rsf*
      - *DRC.header*
    - **temp**
  - **antenna**
    - **rsf**
      - *antenna.rsf*
      - *ANTENNA.header*
    - **temp**
  - **lvs**
    - **rsf**
      - *lvs.rsf*
      - *LVS.header*
    - **temp**
  - **pex**
    - **rsf**
      - *pex.rsf*
      - *RCX_4LM.header*
    - **temp**
- **simulation**
  - **spice_files**
    - *inverter_testcase.sp*
  - **results**
- *cds.lib*
- *.cdsinit*
- *.bashrc*
- *user_guide.pdf*

Description of the above items are as follows.

- **cdl_netlist** directory contains the cdl netlists which will be required for LVS. It also contains *scale.cdl* file which is used during LVS and PEX run.
- **DEMO** is a a user design library. It is used to demonstrate various steps throughout this document.
- **Docs** contains two documents which are -
  DR2_0018SL_SCL_Rev1.pdf >> Design Rules for TS18 Standard Logic Process for SCL
  DRS2_0018SL_SCL_manual.pdf >> SPICE Models for TS18 Standard Logic Process
- **physical_verification** contains four separate directories for DRC, antenna, LVS and PEX run using **Calibre**.
- **simulation** contains two directories – **spice_files** and **results**. **spice_files** contains one sample spice netlist for a CMOS inverter circuit (which is inside the DEMO library). This spice netlist (*inverter_testcase.sp*) is used to run the post-layout simulation using Synopsis's **HSPICE** simulator. **results** directory is used to store the simulation output files.

1.3. Change the paths

Replace the string <WORKING_DIR> with the actual path in the following files *antenna.rsf*, *drc.rsf*, *lvs.rsf* and *pex.rsf.*

1.4. About “cds.lib”

cds.lib file contains

- SCL 0.18um PDK library (**ts018_scl_prim**)
- 1.8V I/O library (**CIO150**)
- 3.3V I/O library (**CIO250**)
- HSPICE compatible analogLib (**analogLib_hspice**)

2. Schematic simulation

2.1. Launch cadence

Step-1: Open a terminal window in <WORKING_DIR>.

Step-2: run *.bashrc* [command >> **source .bashrc**]

Step-3: run virtuoso [command >> **virtuoso**]

2.2. Simulate in ADE-L

Step-1: Open **Tools > Library Manager**. Go to the **DEMO** library and open **testinv_testbench** schematic.

Step-2: Launch **ADE-L**.

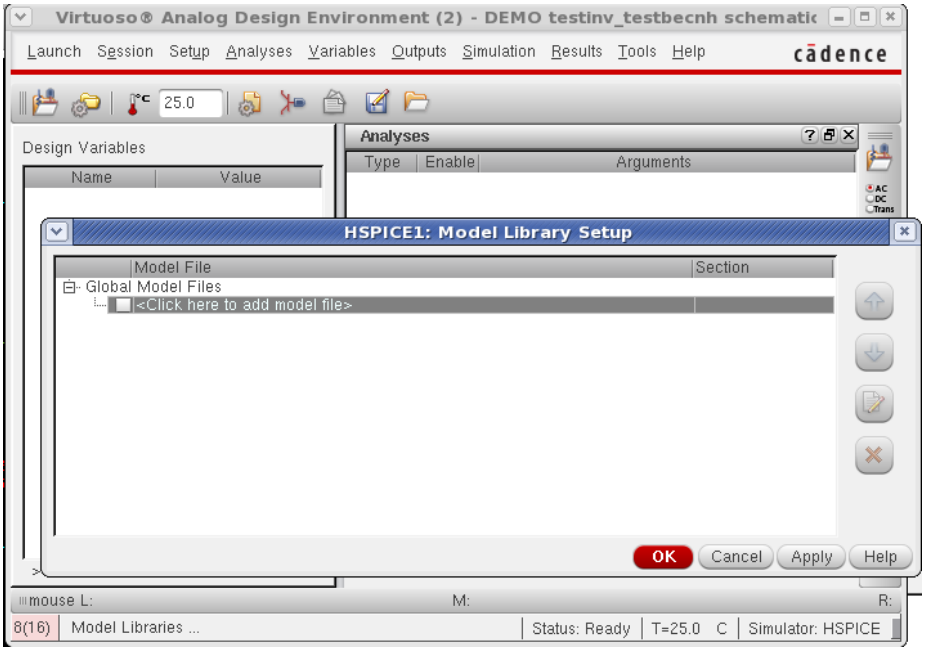
2.2.1. Add model file path

Step-1: Open **Setup > Model Libraries**

Step-2: Enter the following path of the model files.

/designPackages/design_installer/scl/scl_pdk/design_kit/models/hspice/ts18sl_scl.lib

Step-3: Choose appropriate *Section* from the drop-down list. For this demo example, choose **tt_hv**.

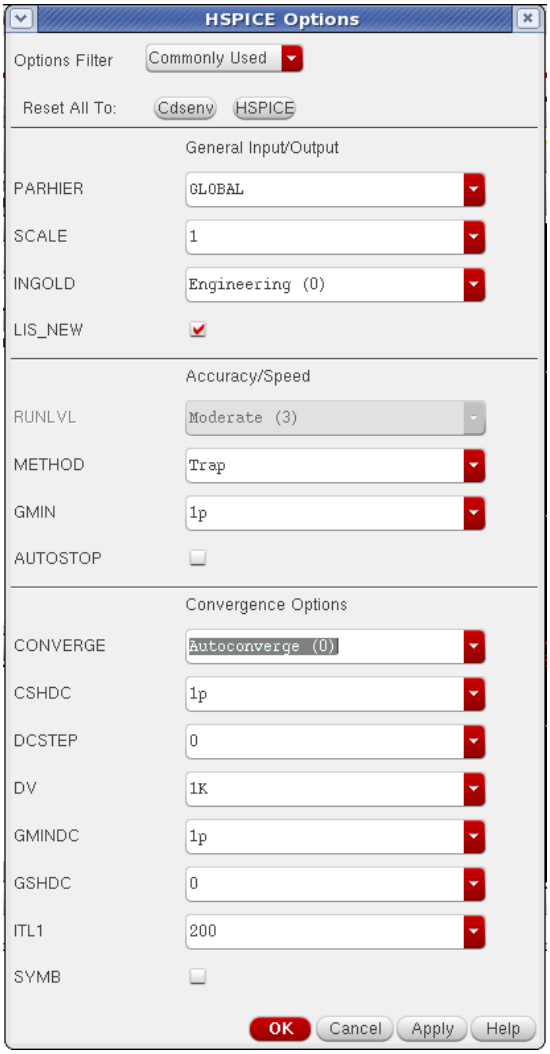


2.2.2. Change scale factor

In SCL process, dimensions of the devices are assumed to be in *micrometer* scale. However, in by default the HSPICE simulator assumes all the dimension to be in *meter*. Therefore, it is necessary to change the default setting.

Step-1: Open **Simulation > Options > Analog > Commonly Used... I**t will open a window (HSPICE Options)

Step-2: In **HPICE Options** window, change the default value of the parameter, **Scale** from **1** to to **1u**.



3. Physical verification

Open the **testinv** schematic from the **DEMO** library. Launch **Layout-XL**.

3.1. DRC

Step-1: Launch **Calibre > DRC**

Step-2: Go to **File > Load Runset** and browse to the ***drc.rsf*** file.

Step-3: Run **DRC**

3.2. Antenna rule check

Step-1: Launch **Calibre > DRC**

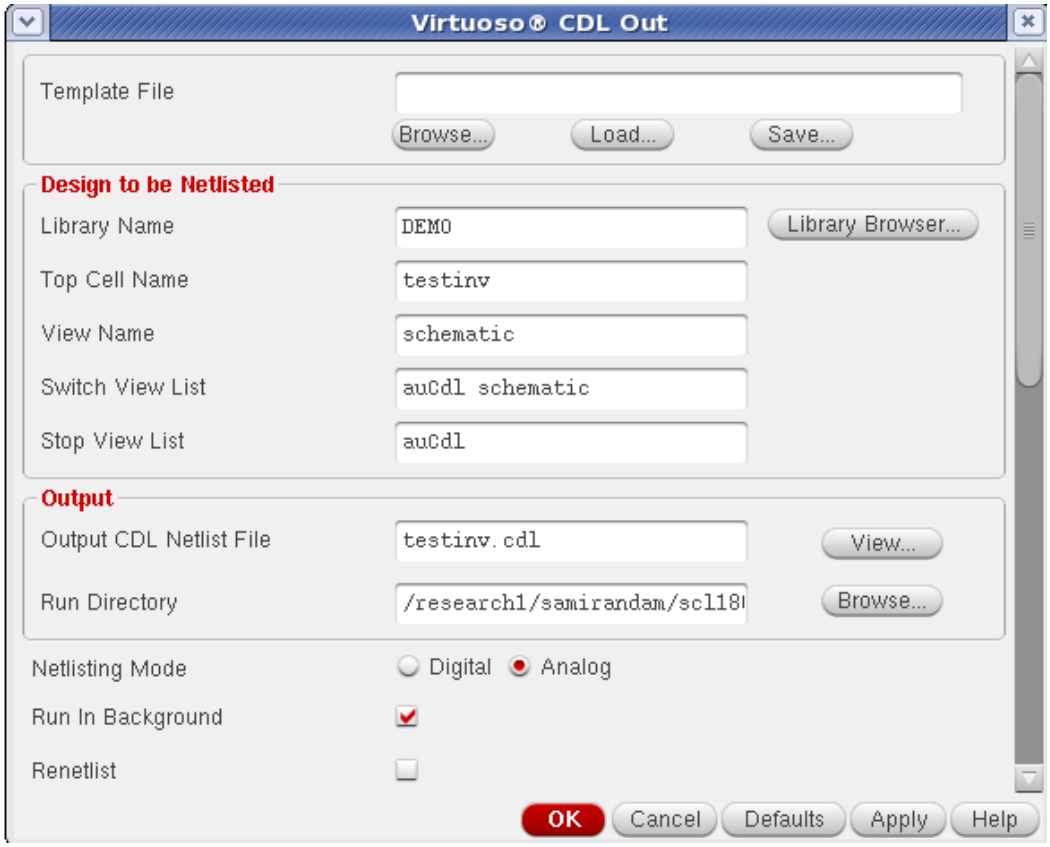
Step-2: Go to **File > Load Runset** and browse to the ***antenna.rsf*** file.

Step-3: Run **DRC**

3.3. LVS

Step-1: Create the **CDL netlist** of the schematic.

- Go to the **CIW** window.
- Go to **File > Export > CDL**
- In the window that appears, click on the button **"Library Browser"** and browse to the schematic of the **testinv** cell.



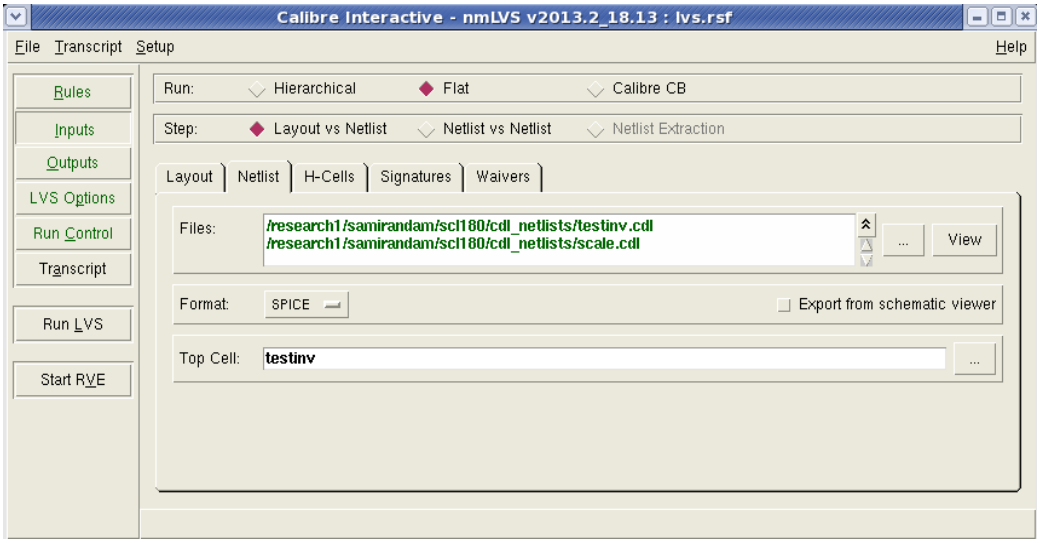
- In the Output section of the window, specify the **"Run Directory"** as the **cdl_netlist** directory in the <WORKING_DIR>. And specify the **"Output CDL Netlist File"** as the name of the cell, which for this example is **testinv.cdl**.

Step-2: Launch **Calibre > LVS**

Step-3: Go to **File > Load Runset** and browse to the ***lvs.rsf*** file.

Step-4: In the **"Inputs"** section of the LVS window, select the **Netlist** tab. And in the Files section browse to the **cdl_netlist** directory and select the **testinv.cdl** and **scale.cdl** files and add them in the list of files.

Step-5: Run **LVS**



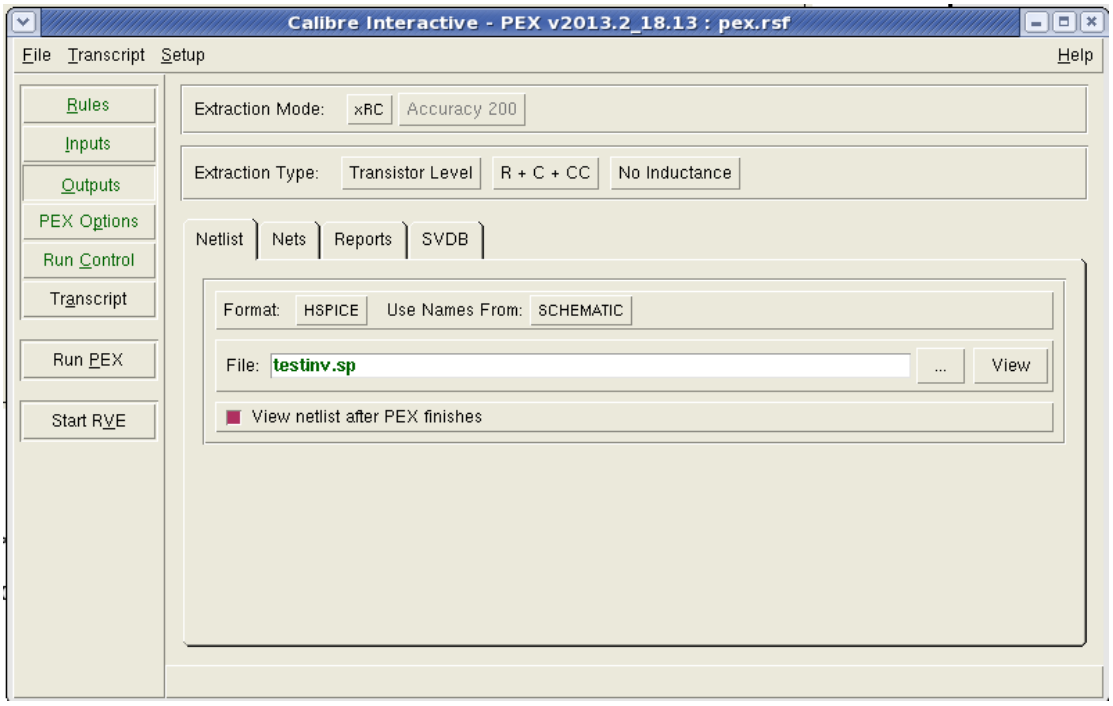
3.4. PEX

Step-1: Launch **Calibre > PEX**

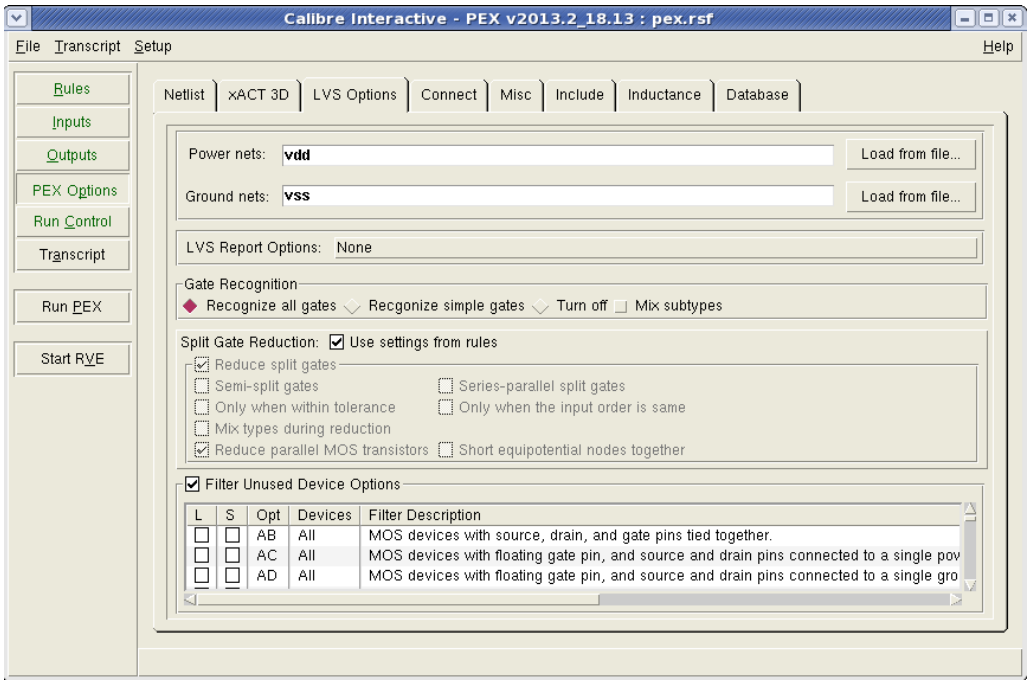
Step-2: Go to **File > Load Runset** and browse to the ***pex.rsf*** file.

Step-3: In the **"Inputs"** section of the PEX window, select the **Netlist** tab. And in the Files section browse to the **cdl_netlist** directory and select the **testinv.cdl** and **scale.cdl** files and add them in the list of files.

Step-4: Go to the **"Outputs"** section of the PEX window and choose **"Format"** as **HSPICE** and change the **"File"** name to ***testinv.sp***. This file will be saved in - *<WORKING_DIR>/physical_verification/pex/temp/testinv.sp* path



Step-5: Go the **"PEX Options"** and then select the tab **"LVS Options"** and enter **vdd** in the field **Power nets** and **vss** in the field **Ground nets**.



Step-6: Run **PEX**

4. Post-layout simulation

Post-layout simulation is done using HSPICE in command-mode. A sample spice netlist for transient simulation of the our example inverter is saved in -

<WORKING_DIR>/simulation/spice_files/inverter _testcase.sp

Before starting the simulation, modify the *inverter_testcase.sp* to include the extracted netlist

.include <WORKING_DIR>/physical_verification/pex/temp/testinv.sp

4.1. Simulation using HSPICE

Execute the following command to run HSPICE on the spice netlist.

hspice64 -mt 2 -i <WORKING_DIR>/simulation/spice_file/inverter_testcase.sp -o <WORKING_DIR>/simulation/results/testinv_sim &

Note: *<WORKING_DIR>/simulation/spice_file/inverter_testcase.sp* is the path of the spice netlist of the testbench

<WORKING_DIR>/simulation/results/testinv_sim is the path of the simulation result directory

4.2. Viewing simulated waveforms

Run the following command to open the waveform window.

wv &

Browse to the simulation result directory (**File > Import Waveform File**) and select ***inverter_testcase.tr0*** file.

5. Monte-Carlo simulation

...to be updated in the next revision.

6. I/O Library

...to be updated in the next revision.