Trabalho Prático

Cofre de Pão de Queijos

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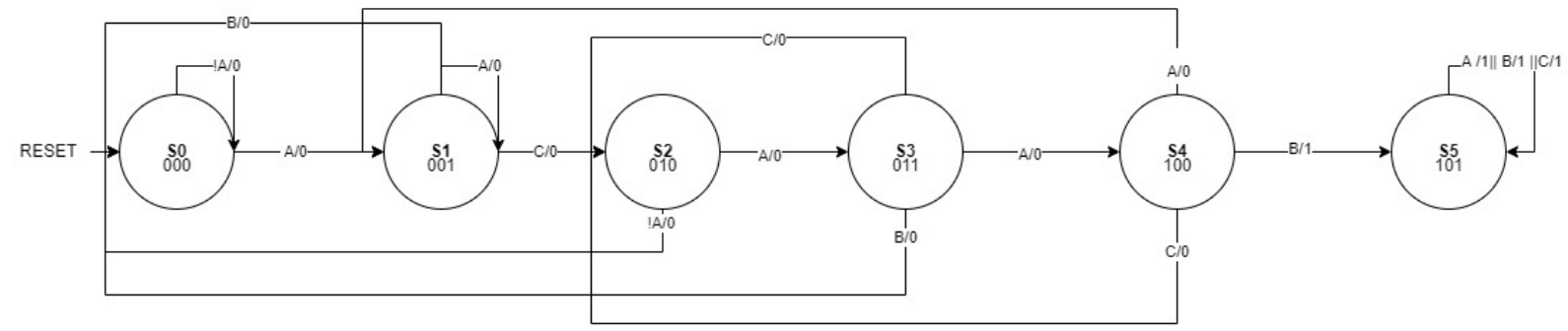
Atenção: Todos os arquivos desta documentação estão separados em pastas no diretório desse projeto. É **ALTAMENTE RECOMENDADO** que esses arquivos sejam analisados separadamente.

1. Email:

Michele Nogueira Lima (via Portal Minhas Turmas) <naoresponder@ufmg.br>
para Lucas

Prezado Lucas, o código a ser usado por você para o circuito de abertura do cofre de pão de queijo é: ACAAB. Cordialmente, Fabricante de Pão de Queijo

2. Diagrama de Estados:



3. Tabela de Estados Próximos:

Bits de Entrada		Estado Atual			Próximo Estado			Output
X0	X1	Q0	Q1	Q2	Q0+	Q1+	Q2+	Y
0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	1	0
1	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	0
0	1	0	0	1	0	0	1	0
1	0	0	0	1	0	0	0	0
1	1	0	0	1	0	1	0	0
0	0	0	1	0	0	1	0	0
0	1	0	1	0	0	1	1	0
1	0	0	1	0	0	0	0	0
1	1	0	1	0	0	0	0	0
0	0	0	1	1	0	1	1	0
0	1	0	1	1	1	0	0	0
1	0	0	1	1	0	0	0	0
1	1	0	1	1	0	1	0	0
0	0	1	0	0	1	0	0	0
0	1	1	0	0	0	0	1	0
1	0	1	0	0	1	0	1	1
1	1	1	0	0	0	1	0	0
0	0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	1	1
1	0	1	0	1	1	0	1	1
1	1	1	0	1	1	0	1	1
0	0	x	x	x	x	x	x	x
0	1	x	x	x	x	x	x	x
1	0	x	x	x	x	x	x	x
1	1	x	x	x	x	x	x	x
0	0	x	x	x	x	x	x	x
0	1	x	x	x	x	x	x	x
1	0	x	x	x	x	x	x	x
1	1	x	x	x	x	x	x	x

4. Mapas de Karnaugh:

Q0+

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$\overline{Q_{0+} Q_{1+} Q_{2+}}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+} Q_{1+}} Q_{2+}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} Q_{2+}$	**0**	**1**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} \overline{Q_{2+}}$	**0**	**0**	**0**	**0**

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$Q_{0+} \overline{Q_{1+} Q_{2+}}$	**1**	**0**	**0**	**1**
$Q_0 \overline{Q_{1+}} Q_{2+}$	**1**	**1**	**1**	**1**
$Q_{0+} Q_{1+} Q_{2+}$	**X**	**X**	**X**	**X**
$Q_{0+} Q_{1+} \overline{Q_{2+}}$	**X**	**X**	**X**	**X**

Q0+ Equação:

$$y = Q_0 X_2' + Q_0 Q_2 + Q_1 Q_2 X_1' X_2$$

Q1+

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$\overline{Q_{0+} Q_{1+} Q_{2+}}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+} Q_{1+}} Q_{2+}$	**0**	**0**	**1**	**0**
$\overline{Q_{0+}} Q_{1+} Q_{2+}$	**1**	**0**	**1**	**0**
$\overline{Q_{0+}} Q_{1+} \overline{Q_{2+}}$	**1**	**1**	**0**	**0**

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$Q_{0+} \overline{Q_{1+} Q_{2+}}$	**0**	**0**	**1**	**0**
$Q_0 \overline{Q_{1+}} Q_{2+}$	**0**	**0**	**0**	**0**
$Q_{0+} Q_{1+} Q_{2+}$	**X**	**X**	**X**	**X**
$Q_{0+} Q_{1+} \overline{Q_{2+}}$	**X**	**X**	**X**	**X**

Q1+ Equação:

$$y = Q_1 Q_2 {X_1}' + Q_1 X_1 {X_2}' + {Q_0}' Q_2 X_1 X_2 + Q_0 {Q_2}' X_1 X_2$$

Q2+

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$\overline{Q_{0+} Q_{1+} Q_{2+}}$	**0**	**1**	**0**	**0**
$\overline{Q_{0+} Q_{1+}} Q_{2+}$	**1**	**1**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} Q_{2+}$	**1**	**0**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} \overline{Q_{2+}}$	**0**	**1**	**0**	**0**

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$Q_{0+} \overline{Q_{1+} Q_{2+}}$	**0**	**1**	**0**	**1**
$Q_0 \overline{Q_{1+}} Q_{2+}$	**1**	**1**	**1**	**1**
$Q_{0+} Q_{1+} Q_{2+}$	**X**	**X**	**X**	**X**
$Q_{0+} Q_{1+} \overline{Q_{2+}}$	**X**	**X**	**X**	**X**

Q2+ Equação:

$$y = Q_0 Q_2 + Q_1{}' X_1{}' X_2 + Q_2{}' X_1{}' X_2 + Q_2 X_1{}' X_2{}' + Q_0 X_1 X_2{}'$$

OUTPUT (Y)

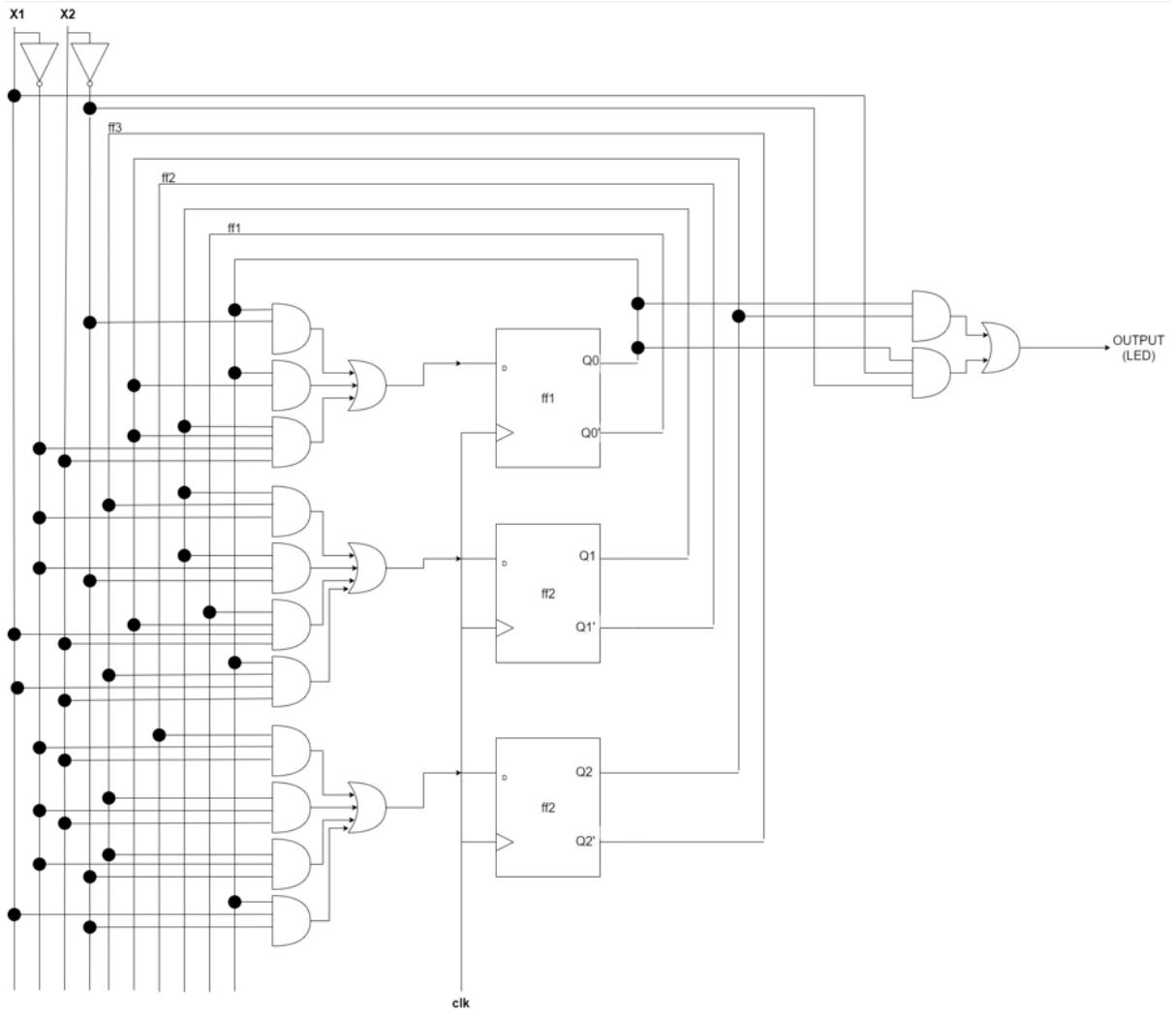
	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$\overline{Q_{0+} Q_{1+} Q_{2+}}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+} Q_{1+}} Q_{2+}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} Q_{2+}$	**0**	**0**	**0**	**0**
$\overline{Q_{0+}} Q_{1+} \overline{Q_{2+}}$	**0**	**0**	**0**	**0**

	$\overline{X_1 X_2}$	$\overline{X_1} X_2$	$X_1 X_2$	$X_1 \overline{X_2}$
$Q_{0+} \overline{Q_{1+} Q_{2+}}$	**0**	**0**	**0**	**1**
$Q_0 \overline{Q_{1+}} Q_{2+}$	**1**	**1**	**1**	**1**
$Q_{0+} Q_{1+} Q_{2+}$	**X**	**X**	**X**	**X**
$Q_{0+} Q_{1+} \overline{Q_{2+}}$	**X**	**X**	**X**	**X**

OUTPUT Equação:

$$y = Q_0 Q_2 + Q_0 X_1 X_2'$$

5. Circuito lógico:

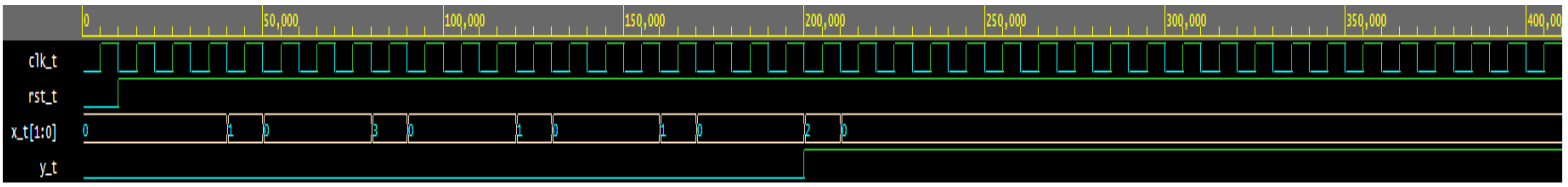


6. Verilog:

Código:

- *mealy_tb.v* é o arquivo de implementação do programa.
- *teste_mealy.v* é o arquivo de testes, ou seja, é o testbench

Saída EPWave:



Log:

```
[2022-07-21 18:53:44 EDT] vlib work && vlog '-timescale' '1ns/1ns' design.sv
testbench.sv  && vsim -c -do "vsim +access+r; run -all; exit"
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: fsm_teste."
MESSAGE "$root top modules: fsm_teste."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line
breakpoints and assertion debug will not be available.
done
# Aldec, Inc. Riviera-PRO version 2020.04.130.7729 built for Linux64 on June
10, 2020.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2020 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 100ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
```

```
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 0 primitives and 5 (100.00%) other processes in SLP
# SLP: 9 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is reduced.
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4683 kB (elbread=427 elab2=4122 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# RUNTIME: Info: RUNTIME_0070 testbench.sv (59): $stop called.
# KERNEL: Time: 410 ns, Iteration: 0, Instance: /fsm_teste, Process: @INITIAL#12_0@.
# KERNEL: Stopped at time 410 ns + 0.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2022-07-21 18:53:46 EDT] Opening EPWave...
Done
```