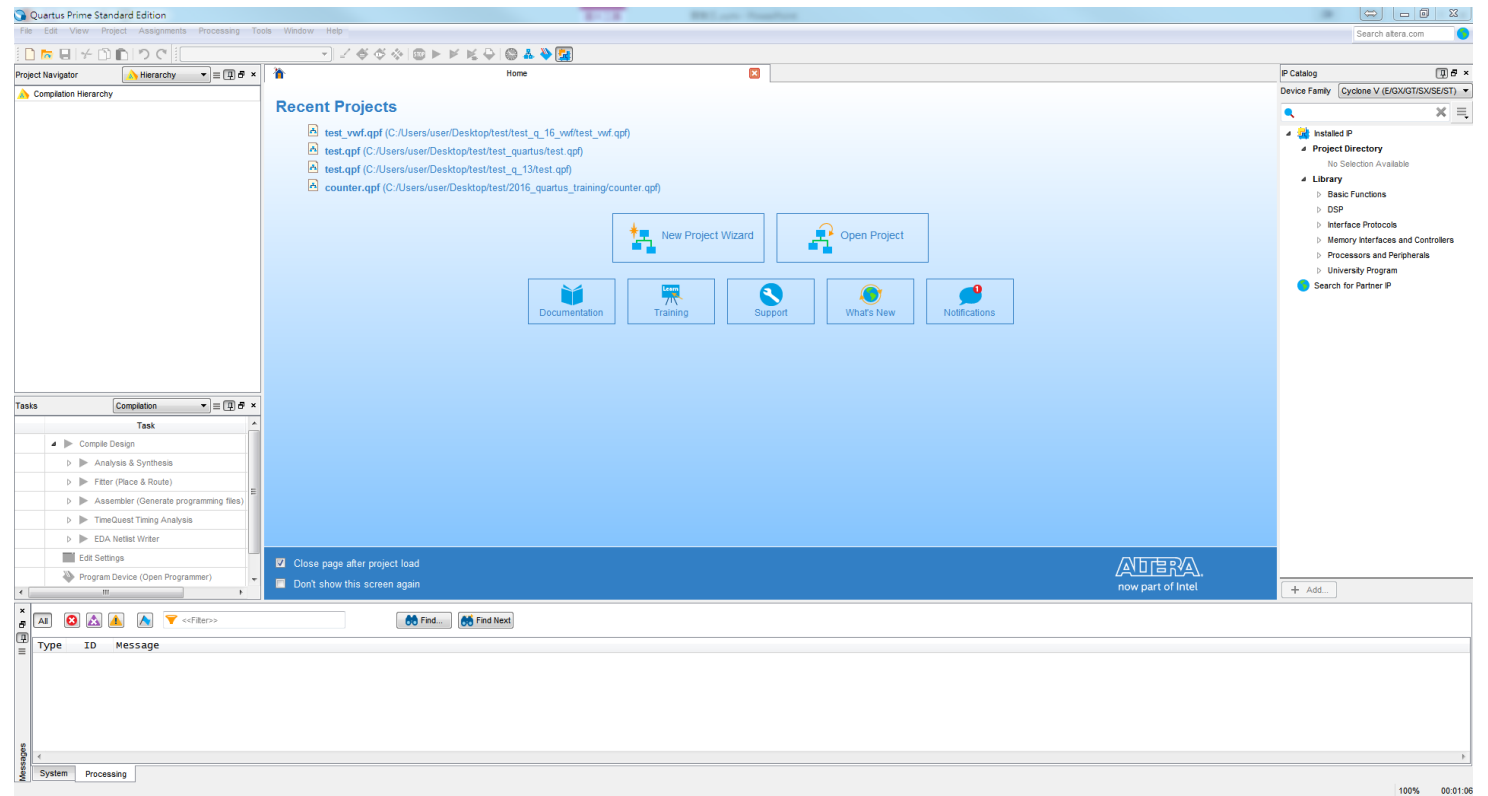
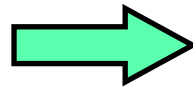
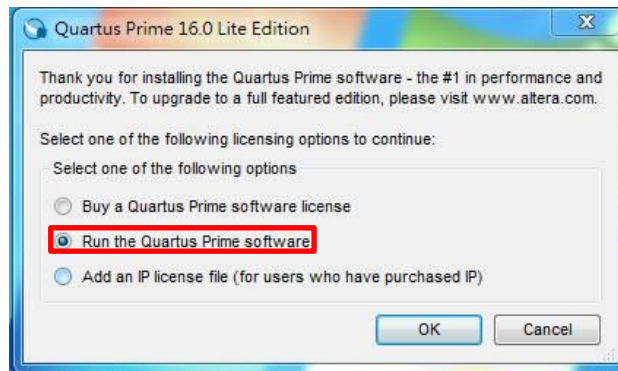


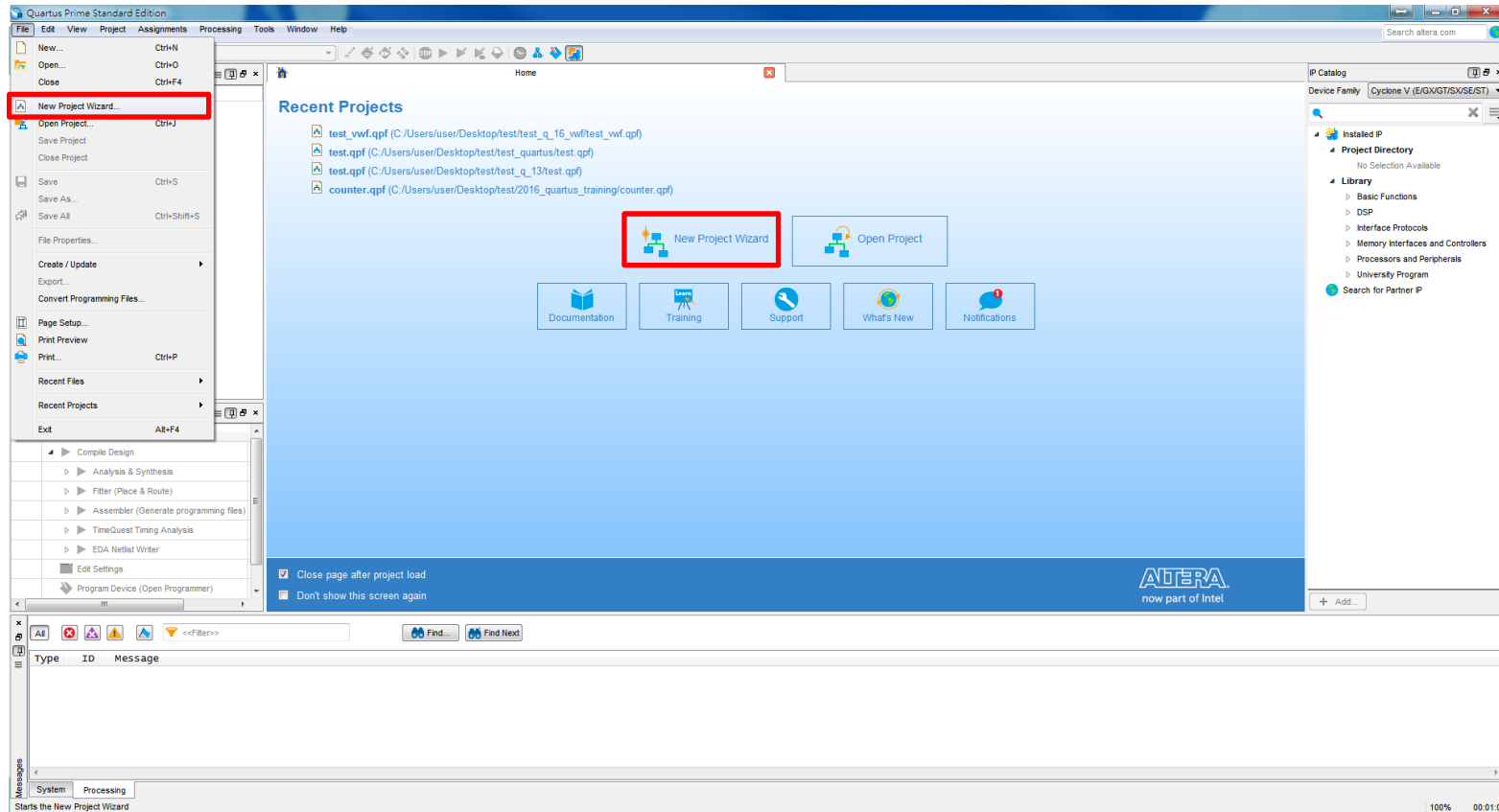
Quartus II Tutorial (1/10)

- Getting Started –
 - Start the Quartus II software



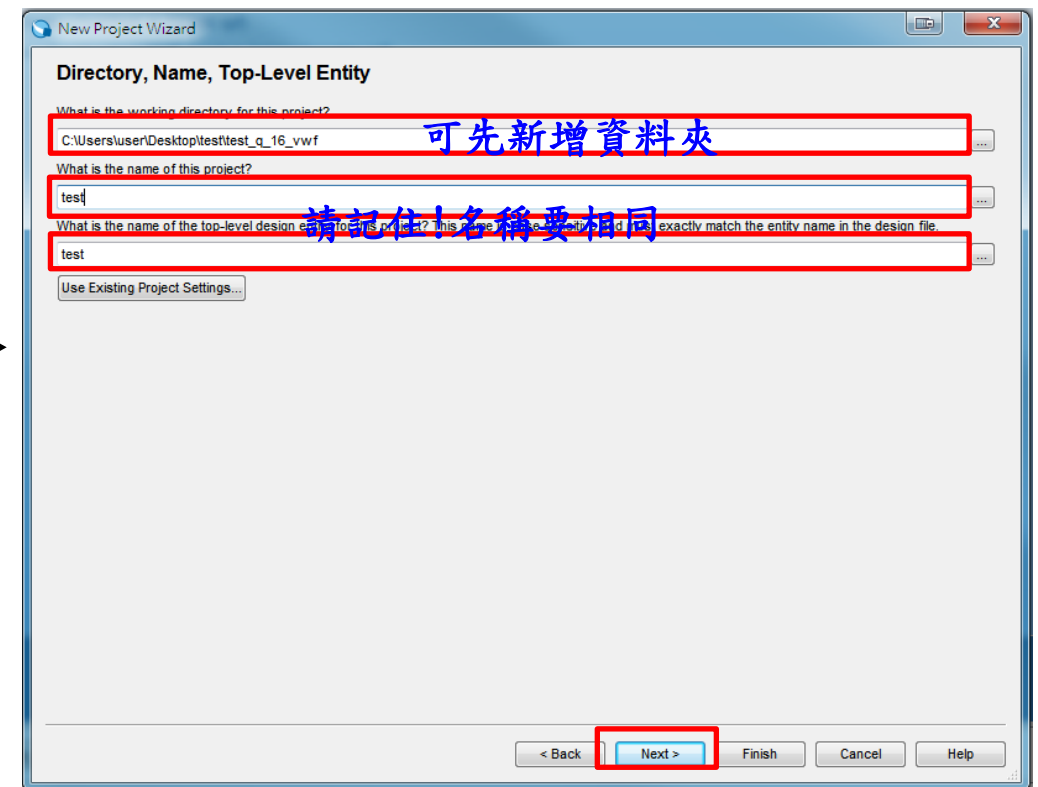
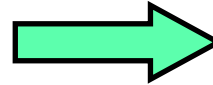
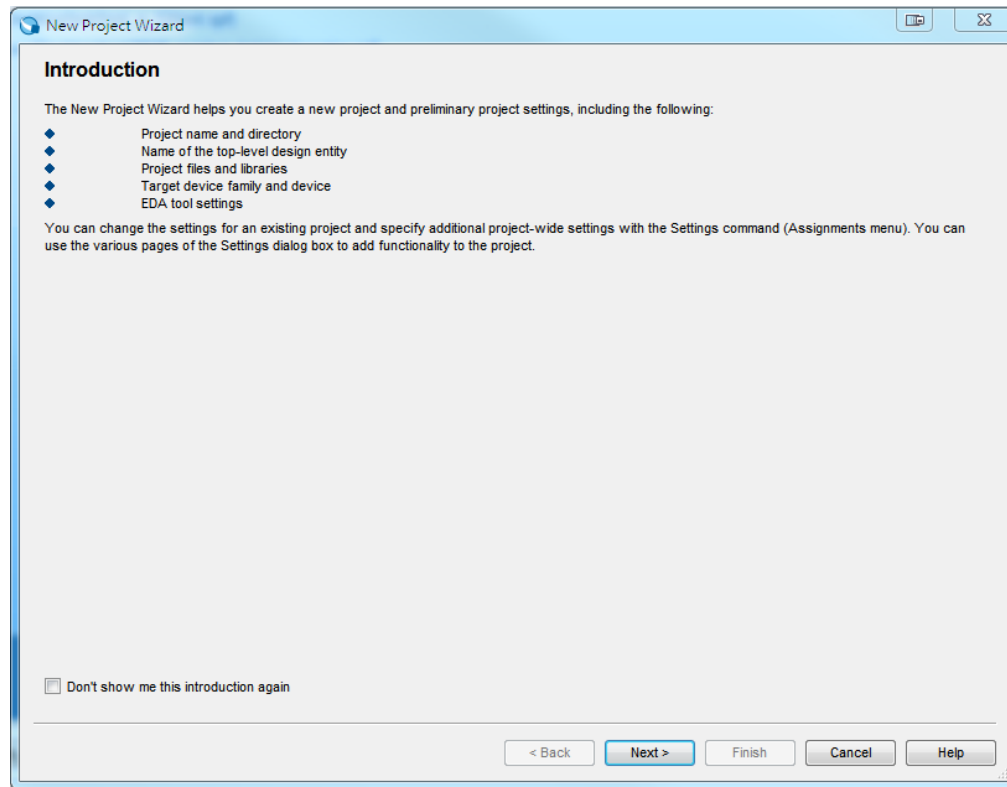
Quartus II Tutorial (2/10)

- Create a New Project –
 - Open New Project Wizard (File → New Project Wizard...)



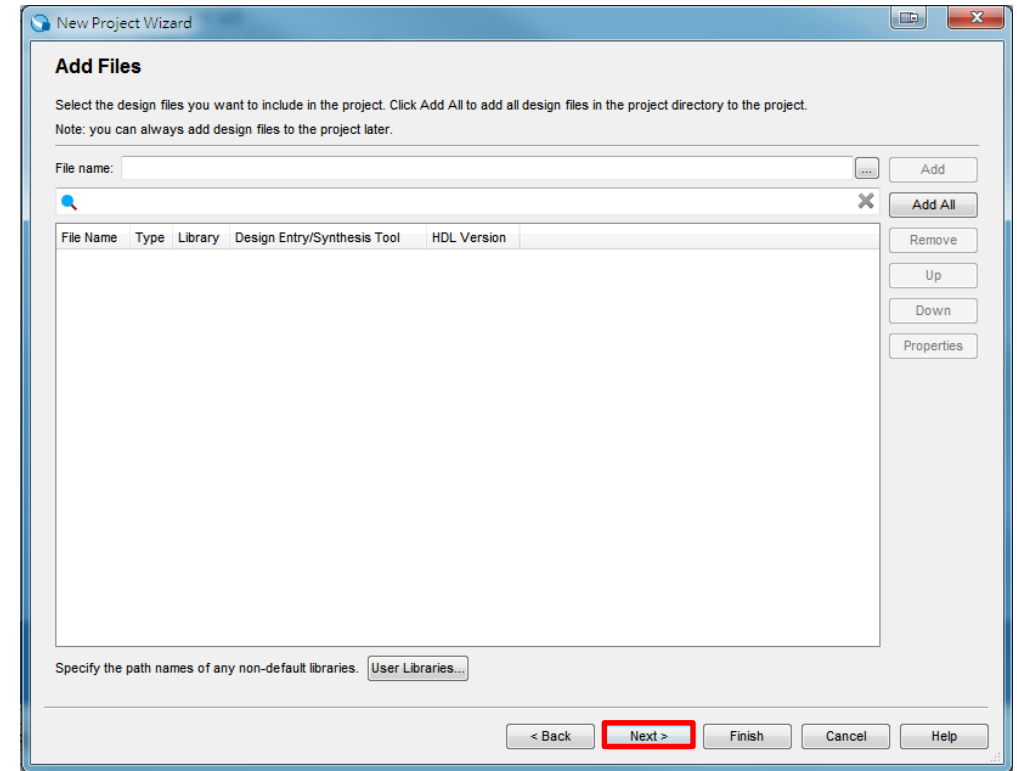
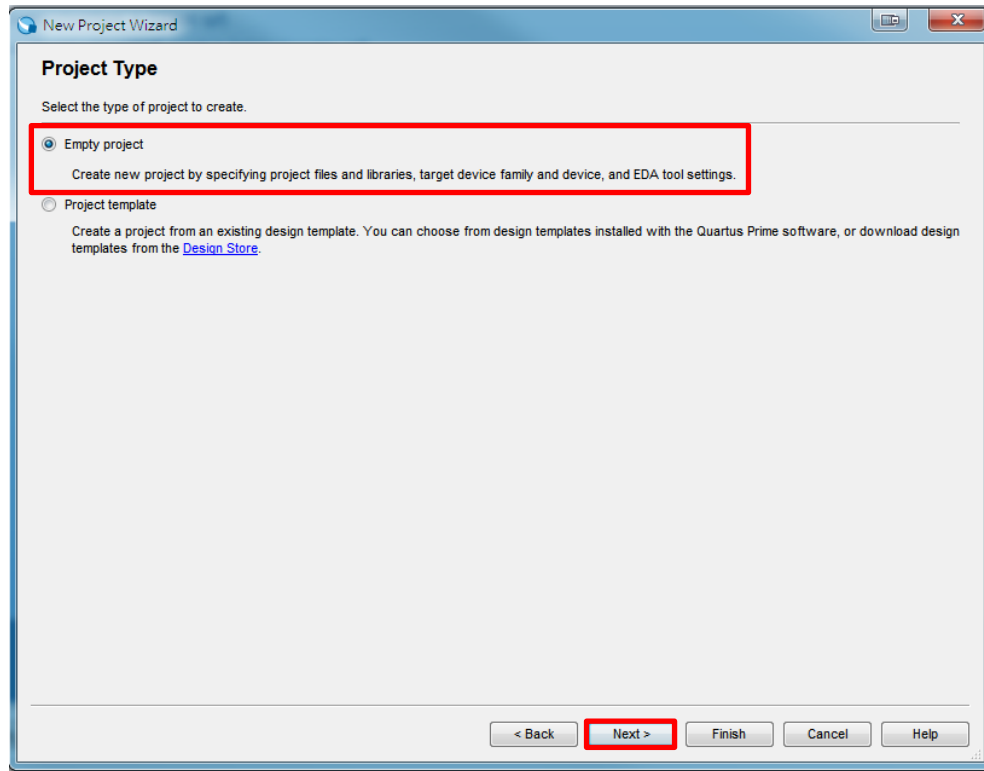
Quartus II Tutorial (3/10)

- Specify the working directory and the name of the project



Quartus II Tutorial (4/10)

- Select “Empty project”. Then, click “Next”.
- Select design files. Or click “Next” to skip this step.



Quartus II Tutorial (5/10)

- Specify device settings - **(DE0-CV Device family are used)**. Click “Next.”

5CEFA4F23C7

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)

Devices: All

Target device

☐ Auto device selected by the Fitter

☒ Specific device selected in 'Available devices' list

☐ Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 484

Core Speed grade: 7

Name filter:

☒ Show advanced devices

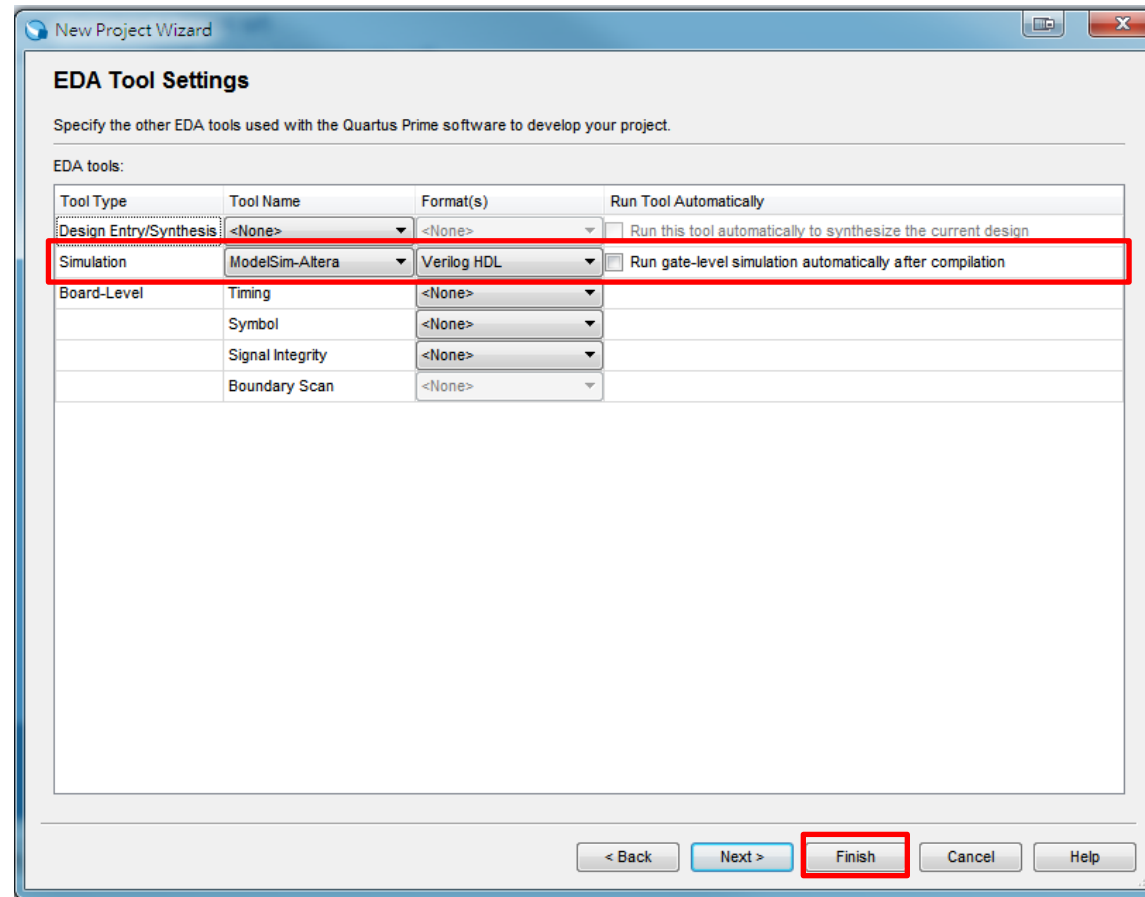
Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	PCIe Hi
5CEFA2F23I7	1.1V	9430	224	224	0	0	0
5CEFA4F23C7	1.1V	18480	224	224	0	0	0
5CEFA4F23I7	1.1V	18480	224	224	0	0	0
5CEFA5F23C7	1.1V	29080	240	240	0	0	0
5CEFA5F23I7	1.1V	29080	240	240	0	0	0

< Back Next > Finish Cancel Help

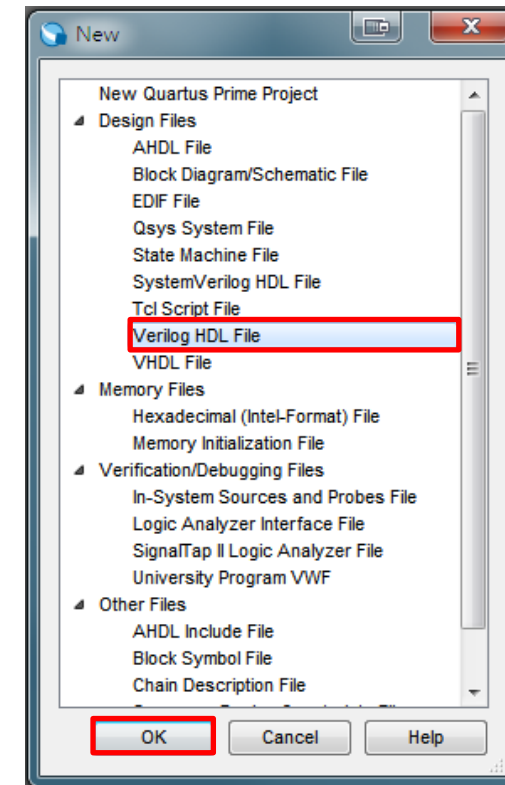
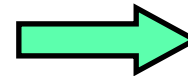
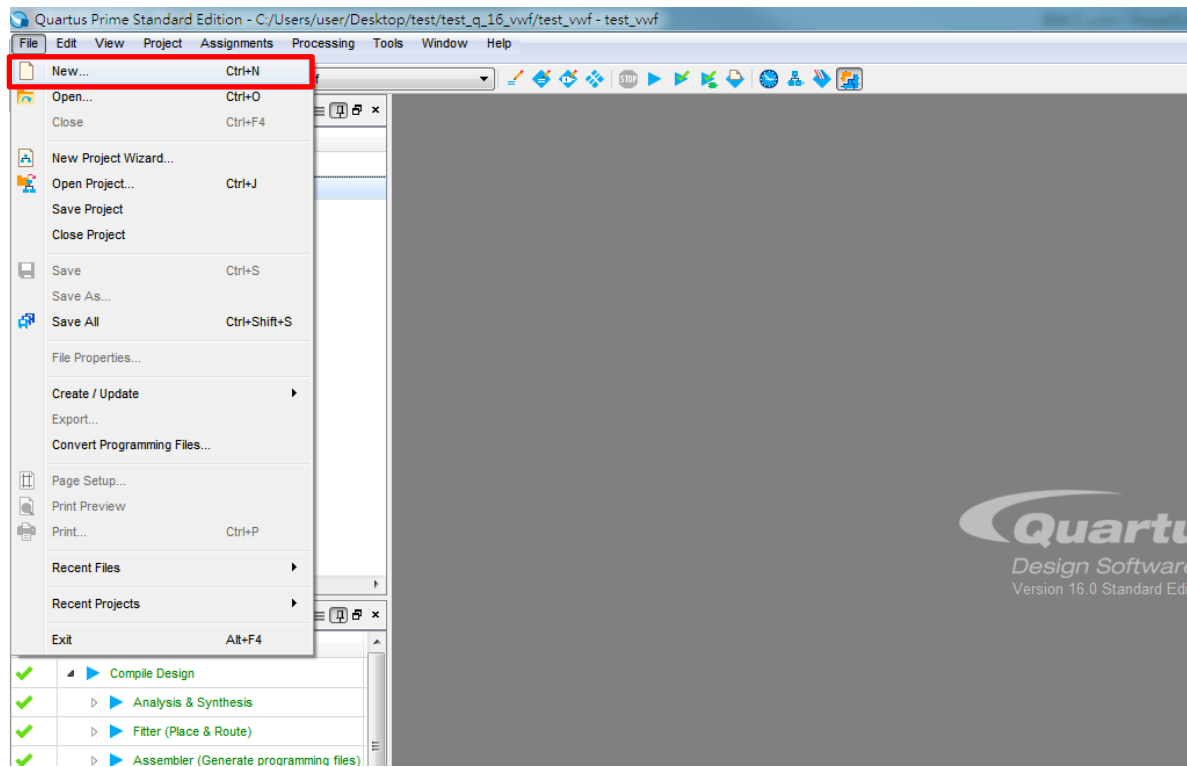
Quartus II Tutorial (6/10)

- Specify EDA Tool – (**Modelsim-Altera** is selected for simulation). Click “Finish.”



Quartus II Tutorial (7/10)

- Edit a new file by opening a Verilog HDL file
 - (File → New → **Verilog HDL File** → OK)



Quartus II Tutorial (8/10)

■ Write Verilog code

Top module name 一定要跟 Project name 相同 !!

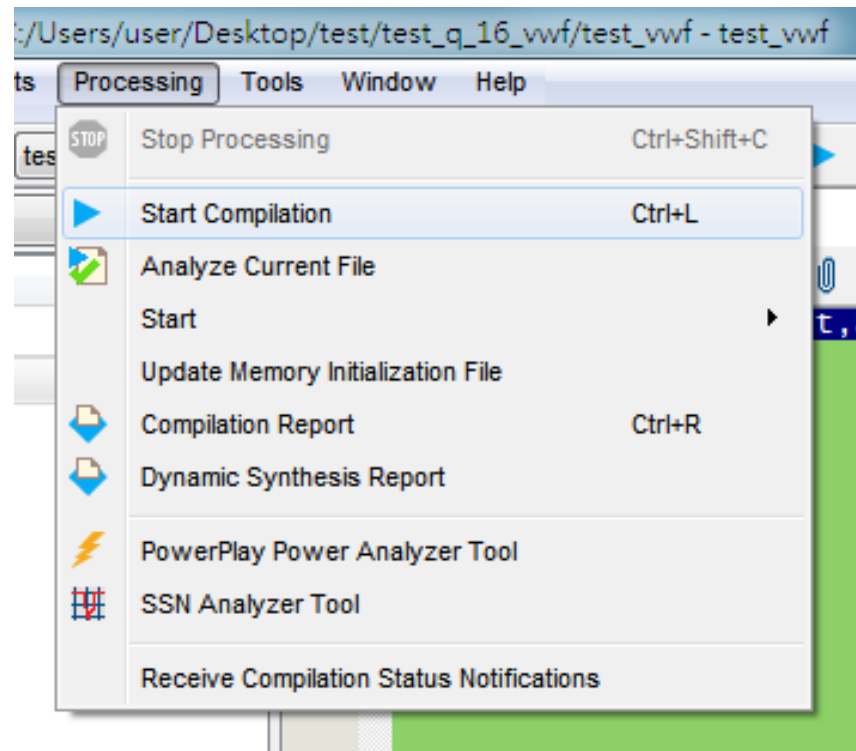
1:	//File Name : Half_Adder.v
2:	module Half_Adder(a, b, sum, carry);
3:	input a, b;
4:	output sum, carry;
5:	
6:	assign sum = a ^ b;
7:	assign carry = a & b;
8:	
9:	endmodule

輸入(input)		輸出(output)	
被加數(a)	加數(b)	和(sum)	進位(carry)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



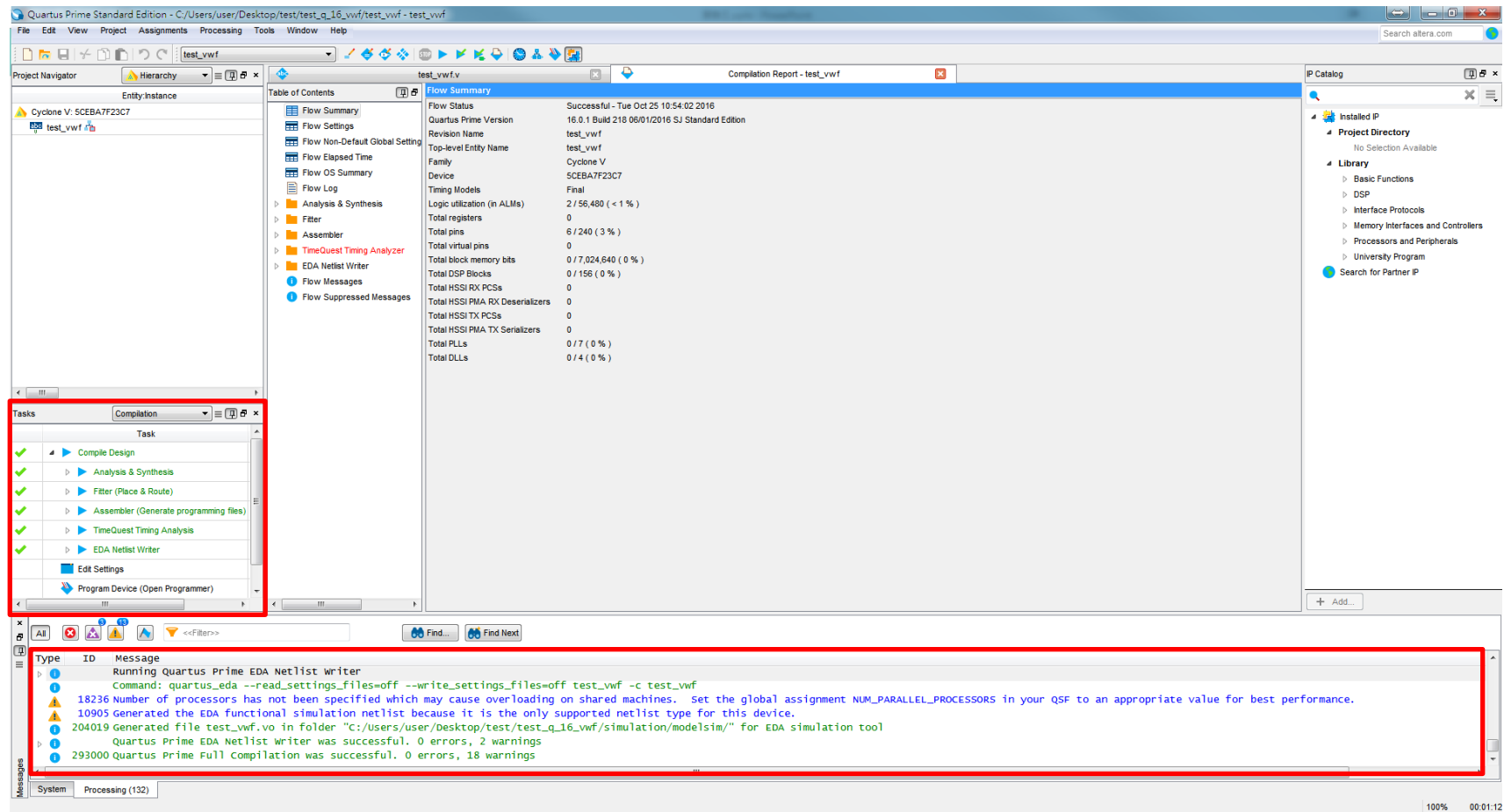
Quartus II Tutorial (9/10)

- **Compiling the Designed Circuit** (synthesis 合成)
 - (Processing → Start Compilation)



Quartus II Tutorial (10/10)

■ Successful compilation

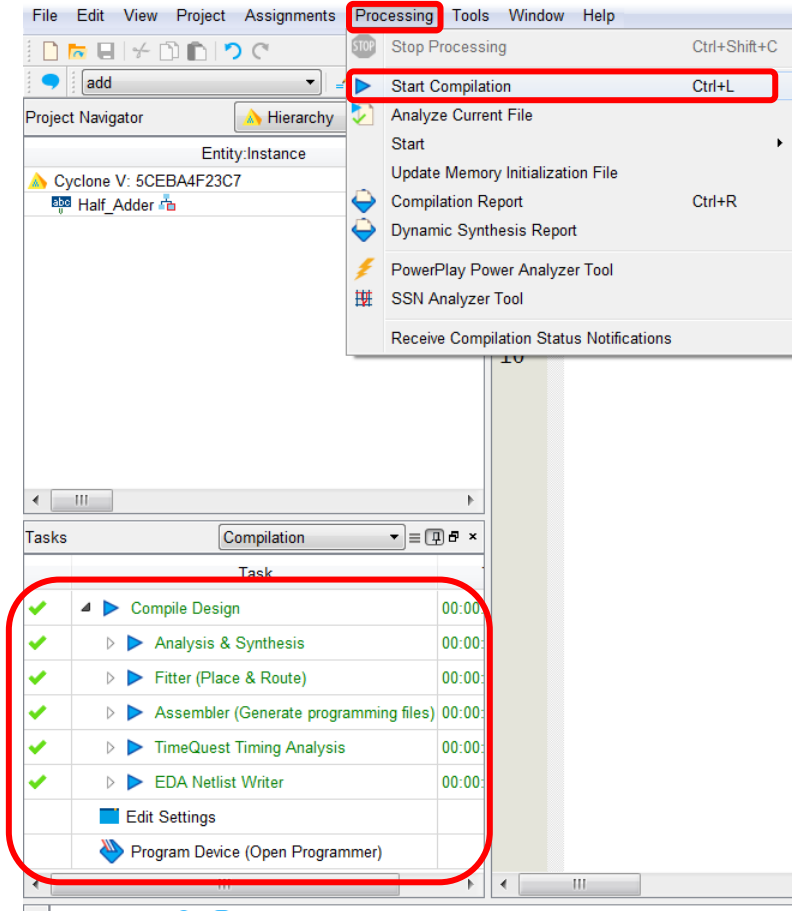


Programming DE0-CV (1/13)

```
1 module Half_Adder(a, b, sum, carry);  
2  
3 input a,b;  
4 output sum, carry;  
5  
6 and(carry,a,b);  
7 xor(sum,a,b);  
8  
9 endmodule  
10
```

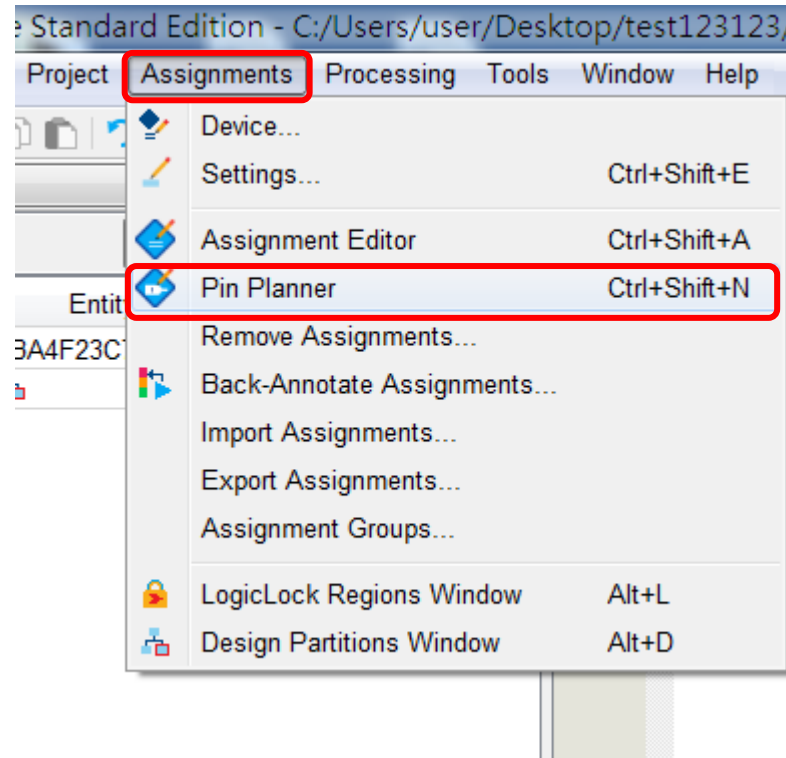
Programming DE0-CV (2/13)

■ Start compilation



Programming DE0-CV (3/13)

- Open Pin Planner



Programming DE0-CV (4/13)

■ Pin assignment

Top View - Wire Bond
Cyclone V - 5CEBA4F23C7

Report not available

Groups Report

Tasks

- Early Pin Planning
- Early Pin Planning...
- Run I/O Assignment Ana...

Named: * Edit: PIN_AA2 Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
a	Input	PIN U13	4A	B4A N0	PIN M16	2.5 V (default)
b	Input	PIN V13	4A	B4A N0	PIN N21	2.5 V (default)
carry	Output	PIN AA1	2A	B2A N0	PIN N16	2.5 V (default)
sum	Output	PIN AA2				
<<new node>>						





Pin Legend

Symbol	Pin Type
○	User I/O
●	User assigne...
●	Fitter assigne...
○	Unbonded pad
○	Reserved pin
E	DEV_OE
n	DIFF_n
p	DIFF_p
n	DIFF_n output
p	DIFF_p output

Double click

Programming DE0-CV (5/13)

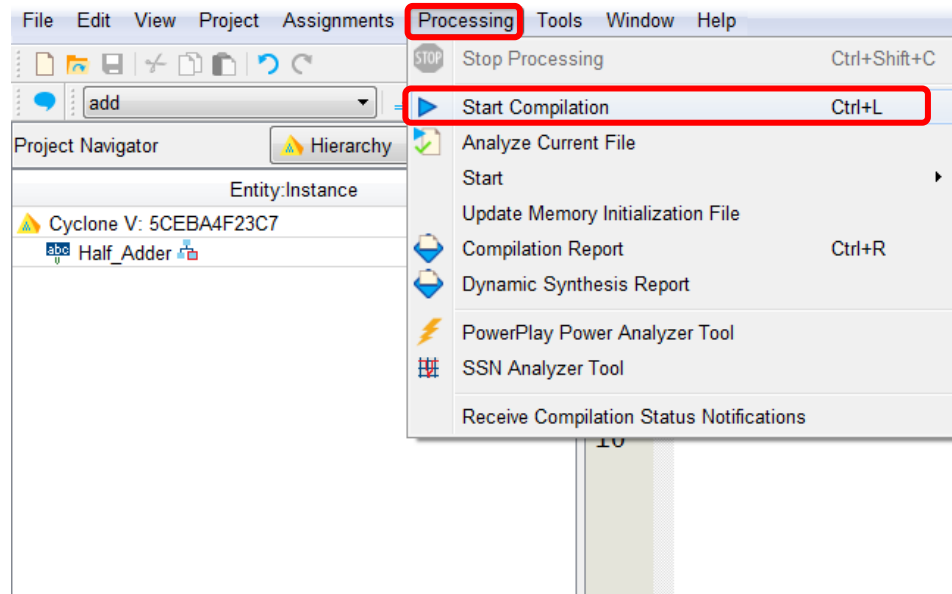
- Assign pin location to all inputs and outputs

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard
 a	Input	PIN U13 SW0	4A	B4A N0	PIN M16	2.5 V (default)
 b	Input	PIN V13 SW1	4A	B4A N0	PIN N21	2.5 V (default)
 carry	Output	PIN AA1 LED1	2A	B2A N0	PIN N16	2.5 V (default)
 sum	Output	PIN AA2 LED0				

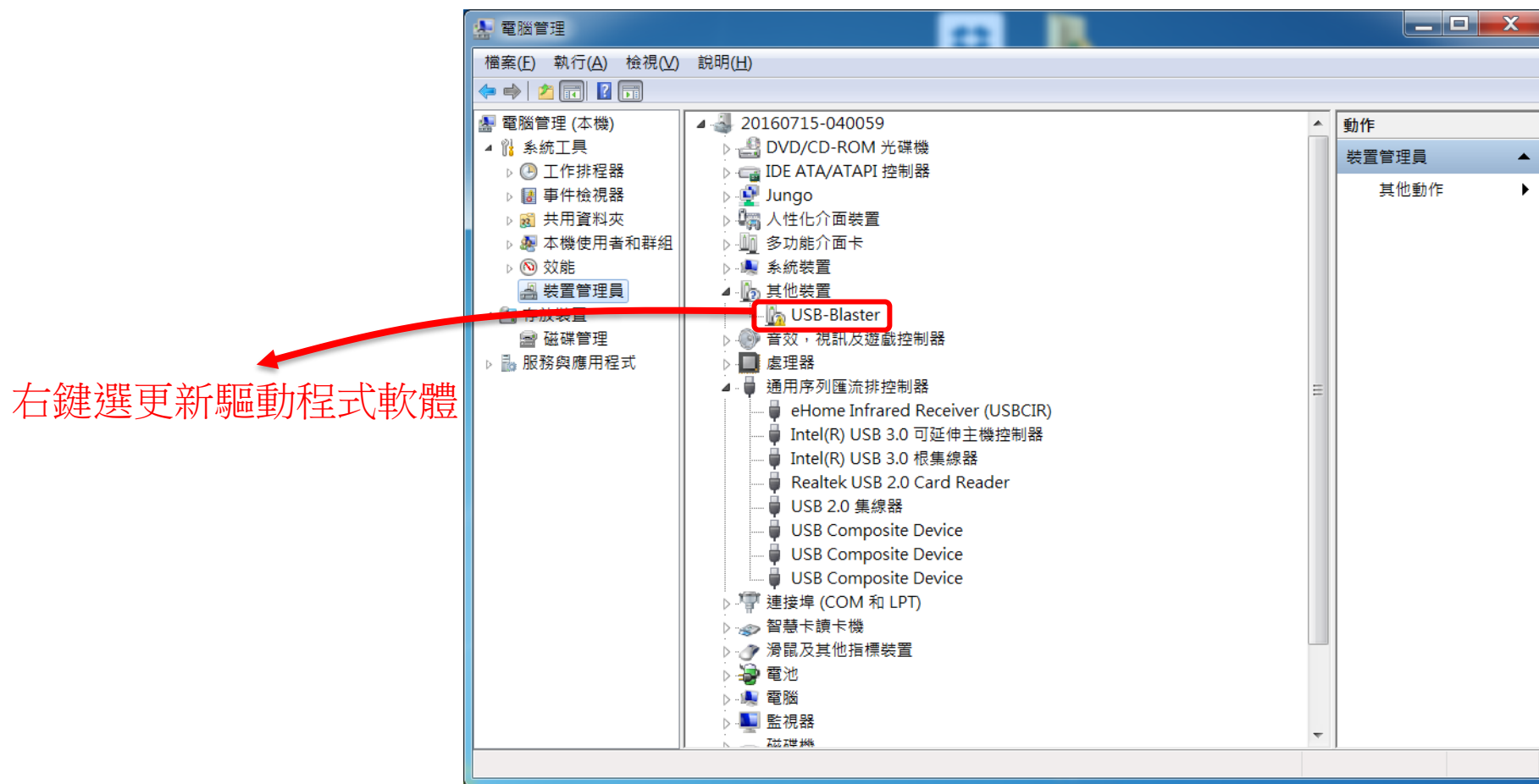
- Please refer to DE0_pin.xls for pin location assignment

Programming DE0-CV (6/13)

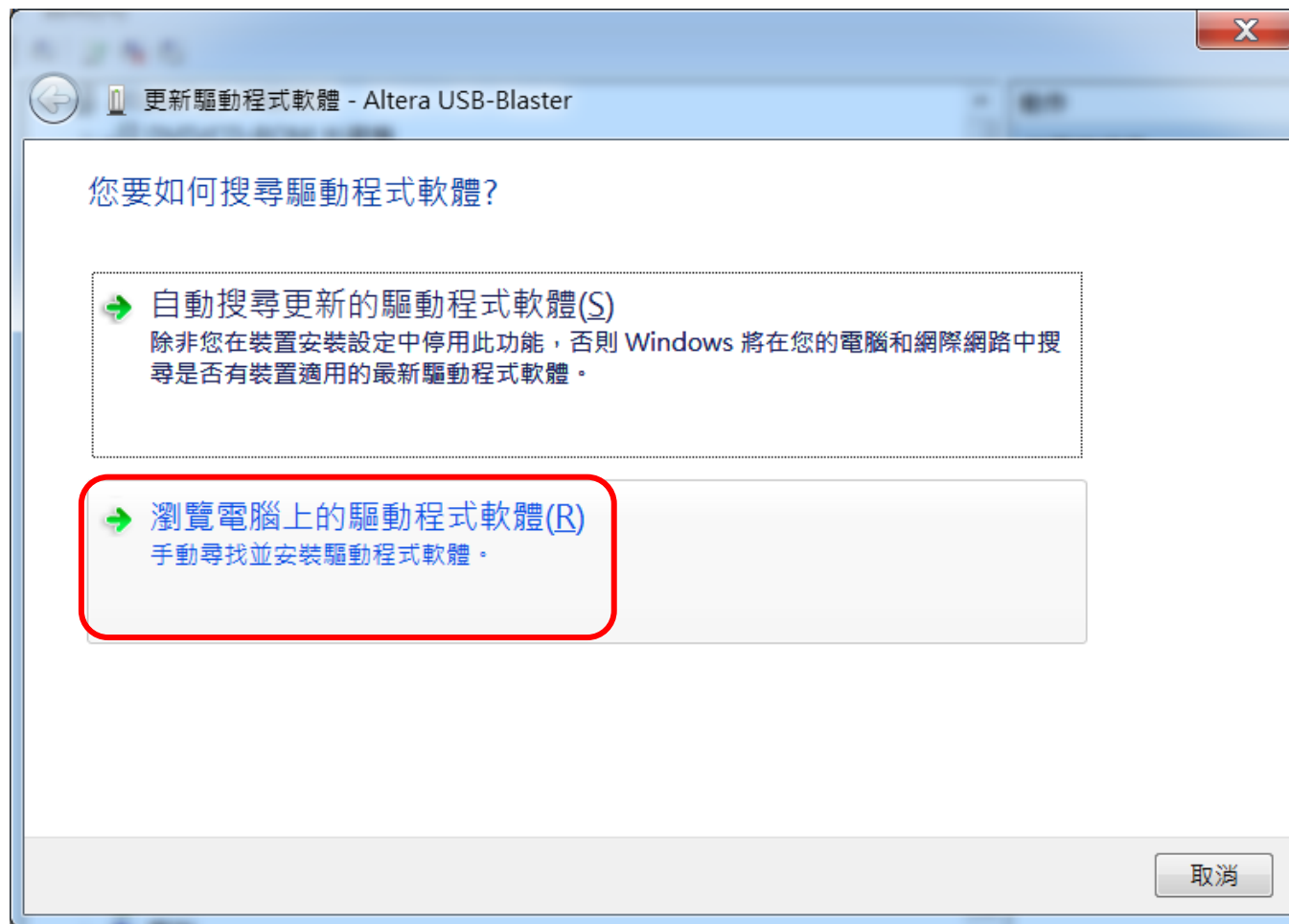
- Start compilation



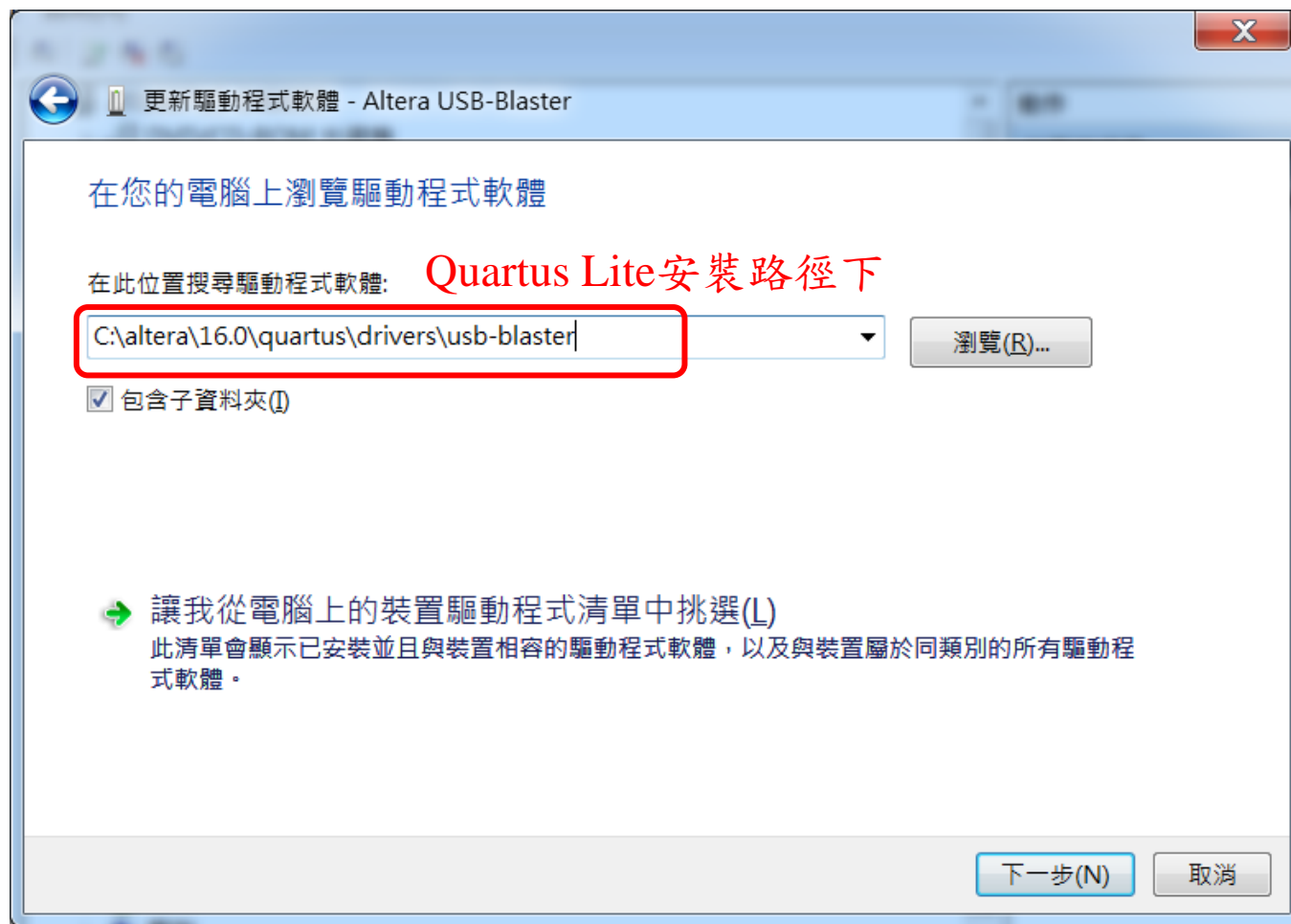
Programming DE0-CV (7/13)



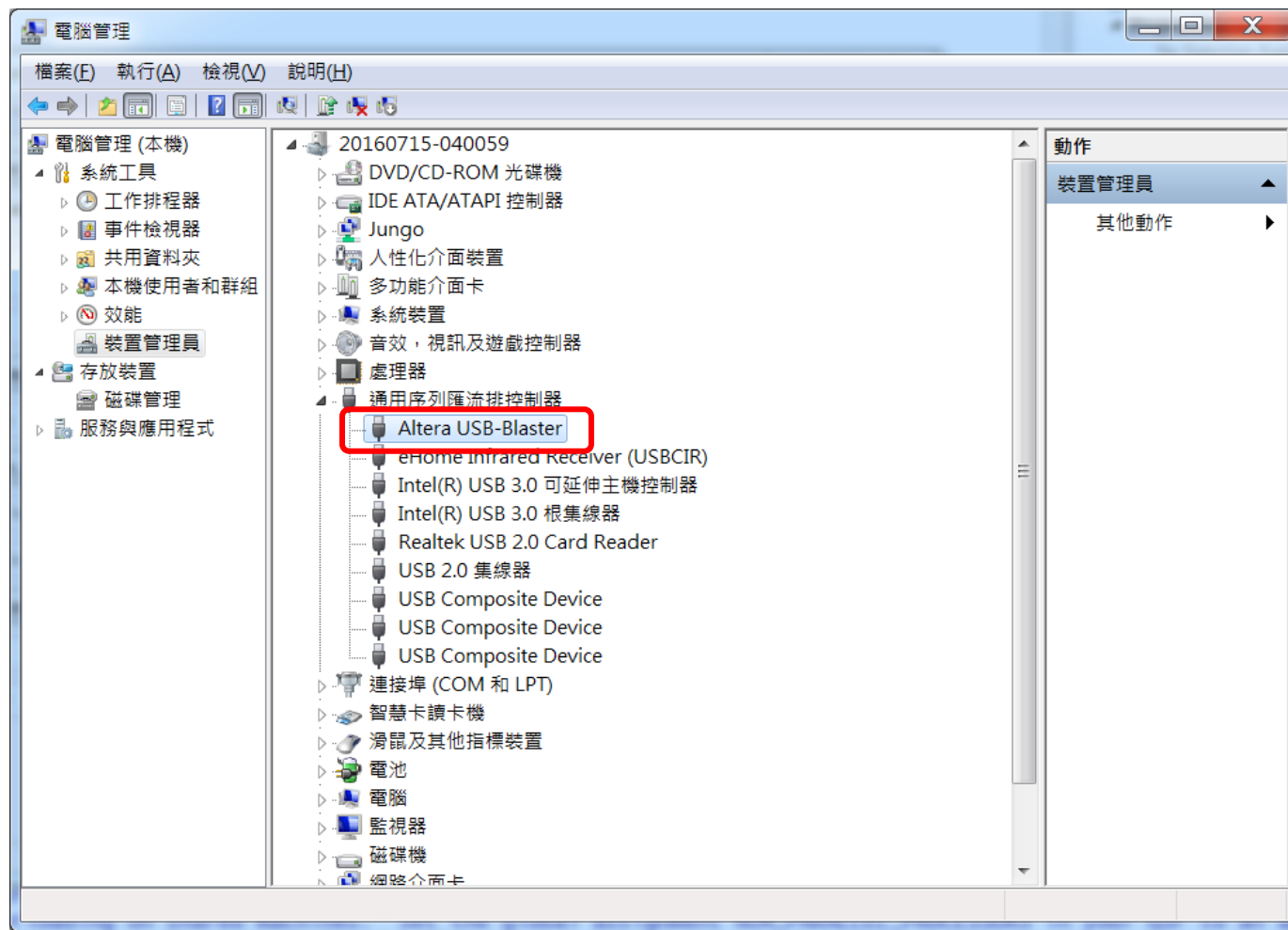
Programming DE0-CV (8/13)



Programming DE0-CV (9/13)

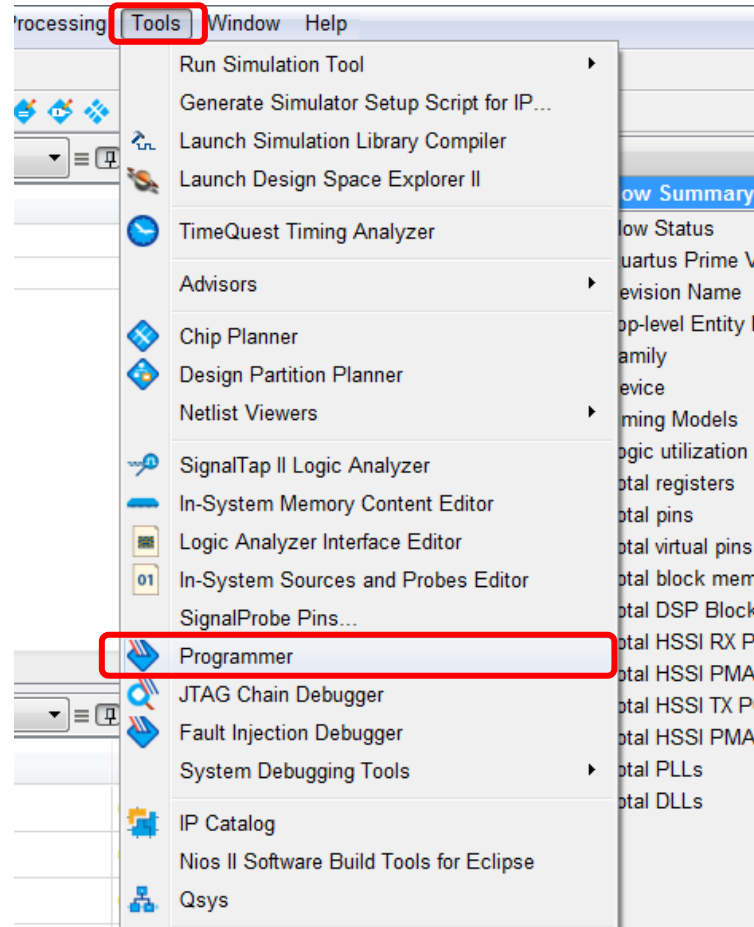


Programming DE0-CV (10/13)



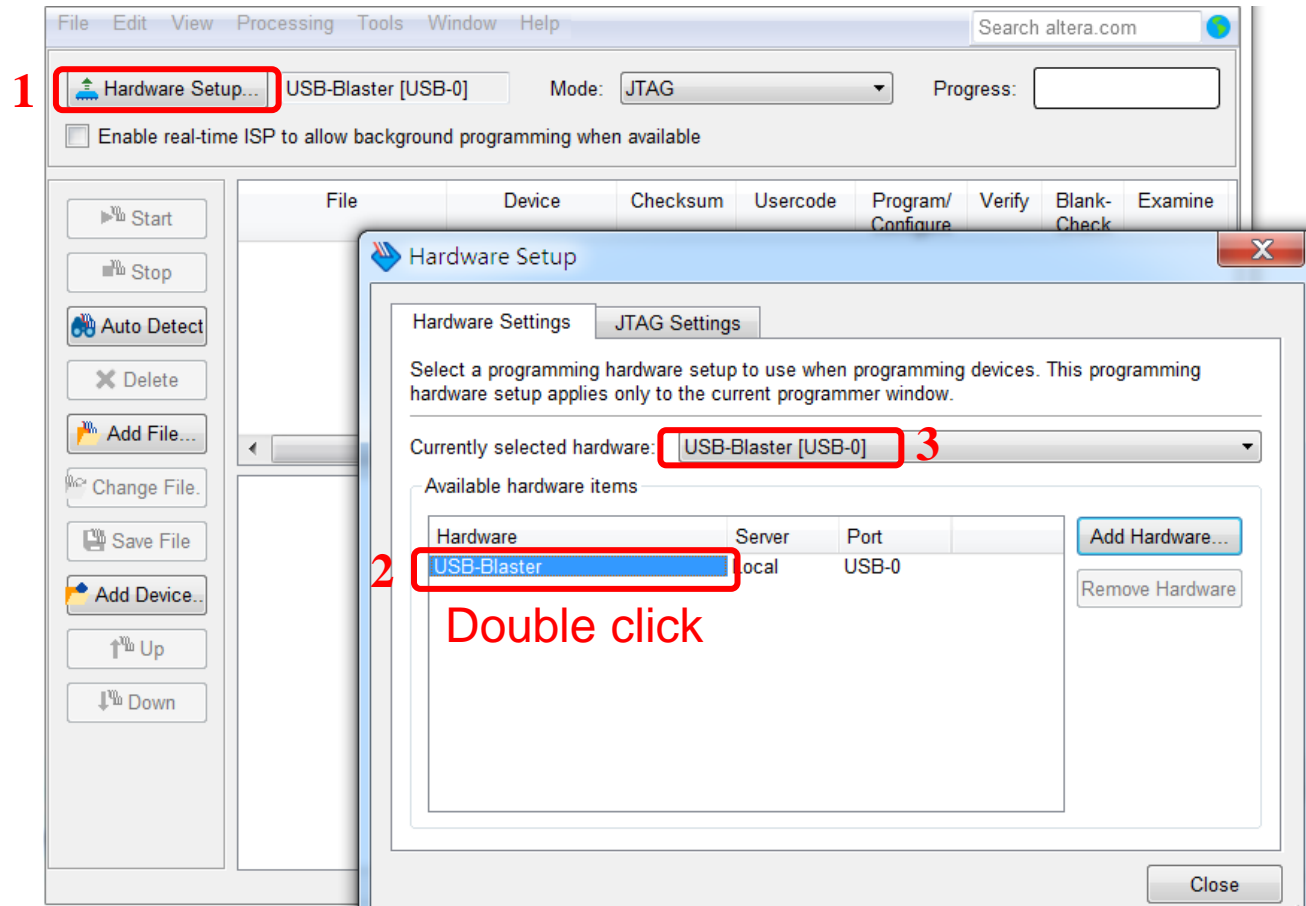
Programming DE0-CV (11/13)

■ Programming device



Programming DE0-CV (12/13)

- Hardware setup: add **USB-Blaster**



Programming DE0-CV (13/13)

■ Programming device

