

HDB Signal Layout:
Avoid running HDB signals in parallel with host interface control signals (eq. RESET_L, HCS_L, HD/C, HWE_L, HRD_L) without ground shielding separating them on a 2-layer board.

Mechanical parts

Quantity	Discription
PCB	

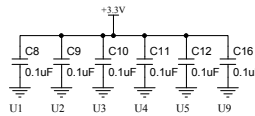
SID13522 Host Interface Mode Configuration

I/F Mode	CNF0	HDB15
16-bit Parallel	0	N/A
8-bit Parallel	1	0
Serial	1	1

Note: For reference only, use SW1 to configure this board for different Host I/F modes.

Host I/F	SW1-1	SW1-2	SW1-3
16-bit Parallel	On	On	D/C
8-bit Parallel	Off	On	D/C
Serial - SPI1	Off	Off	On
Serial - SPI2	Off	Off	Off

Note: D/C = don't care



Note: HDB(7:3) can only be driven low during serial interface modes.

Note: HDB(14:8) can only be driven low during 8-bit parallel or serial interface modes.

E-paper Display Epson PICtail(TM) Plus Board

Size: C

03-60377

Rev: D

MICROCHIP

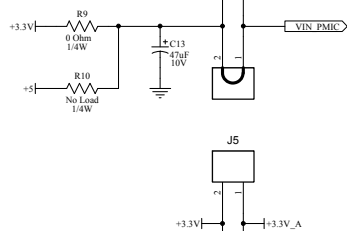
Date 2/27/2012

File: 03-60377 Page 1 REV D.SchDoc

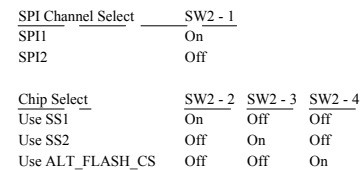
Eng R. Roussant

Drawn by: S. Humbert

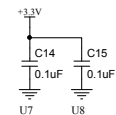
Sheet 1 of 2




Male header Right Angle



Note: Only 1 of SW2-2, SW2-3, SW2-4 should be On at any time. Make sure Flash Memory SPI channel selection not conflict with Host I/F in serial mode.



Quantity		Discription	
JUMPER	1	Jumper	LOAD AT J3 1-2

E-paper Display Epson PICtail(TM) Plus Board			
Size:		03-60377	Rev:
C			D
		Eng R. Roiviyant	
Date: 2/27/2012		Drawn by: S. Humbler	
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