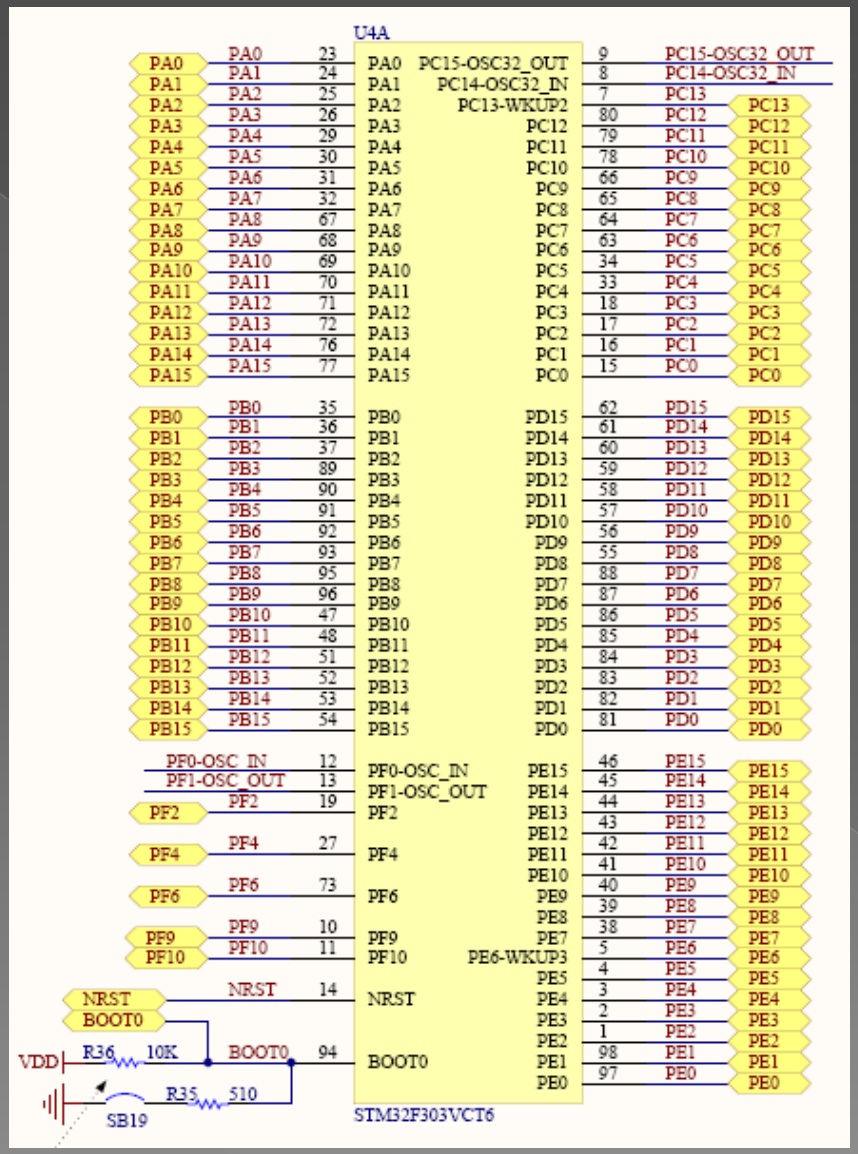
STM32F3 GPIOs

Cuauhtémoc Carbajal
ITESM CEM
06/02/2014

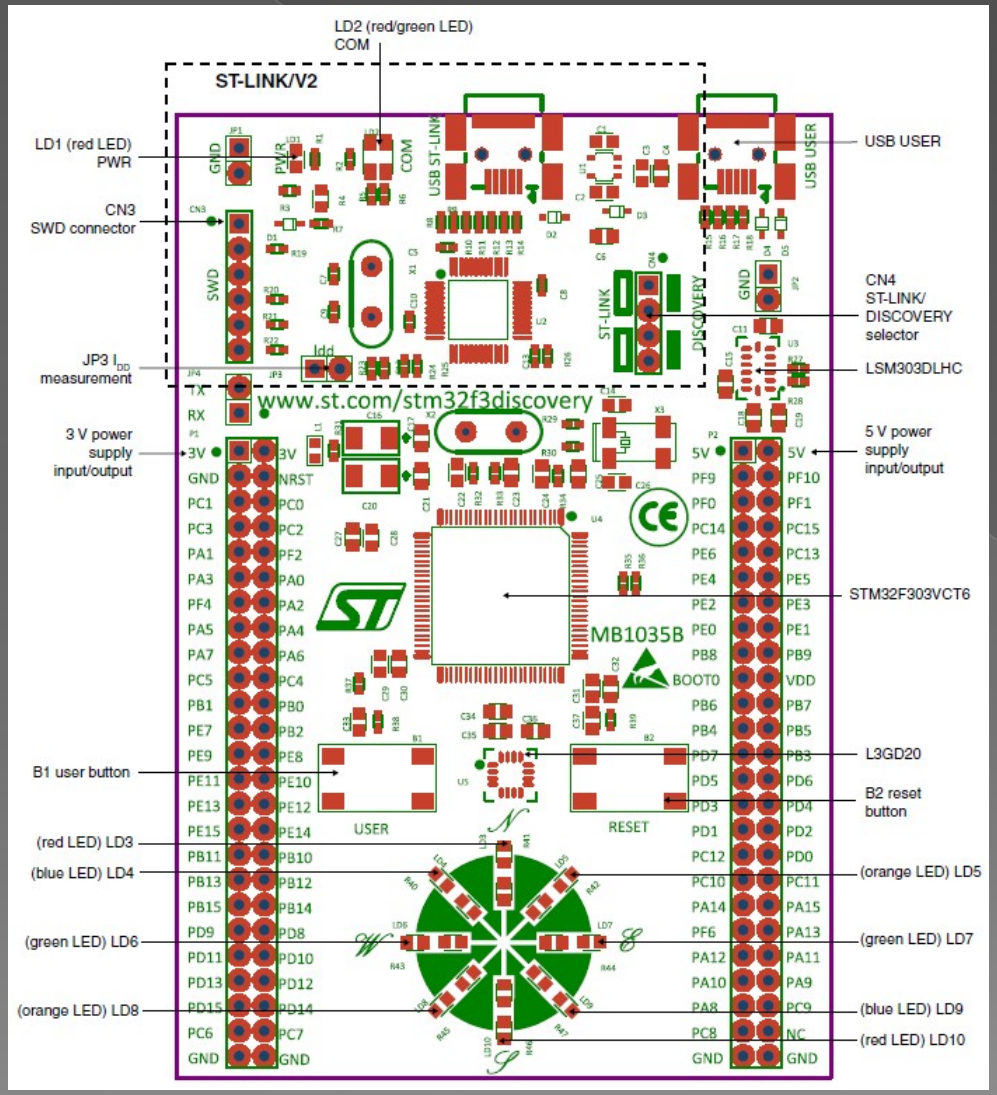
- STM32 F3Discovery board demonstration
- STM32F3Discovery-Based Quadcopter

STM32F303VCT6 Pinout



STM32F3Discovery Board Schematic, page 1

What's on the STM32F3DISCOVERY?



STM32F303VCT6:

- This ARM Cortex-M4 32-bit MCU with FPU has 256 KB Flash, 48 KB SRAM, 4 ADCs, two DAC channels, seven comparators, four PGAs, 13 timers, 2.0-3.6 V operation.

MEMS:

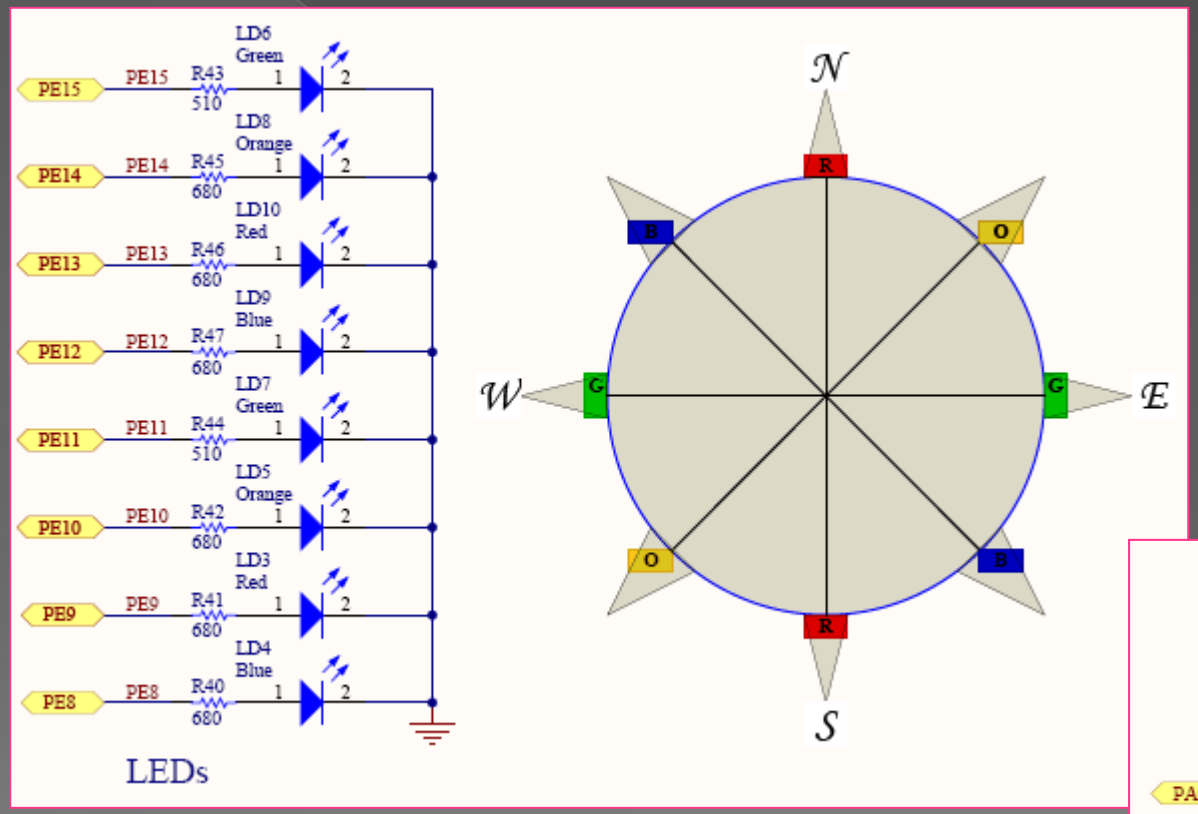
- LSM303DLHC: E-compass/accelerometer
- L3GD20: Gyroscope

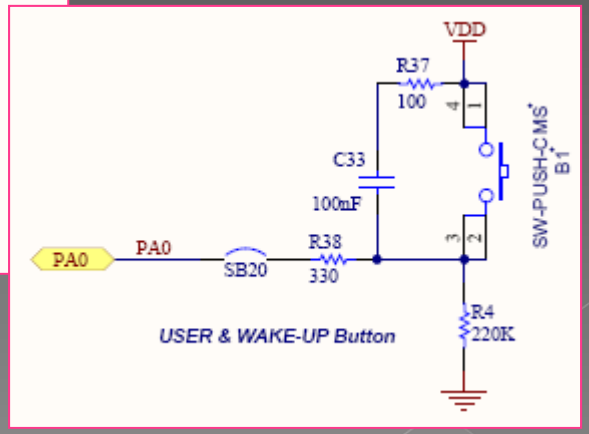
Extension connectors:

- GPIOs are available on these connectors.
- When using the GPIO pins, care must be taken for avoiding conflict with existing connections.

STM32F3DISCOVERY - Discovery kit for STM32F303xx microcontrollers, pages 21-29

LEDs and User Button





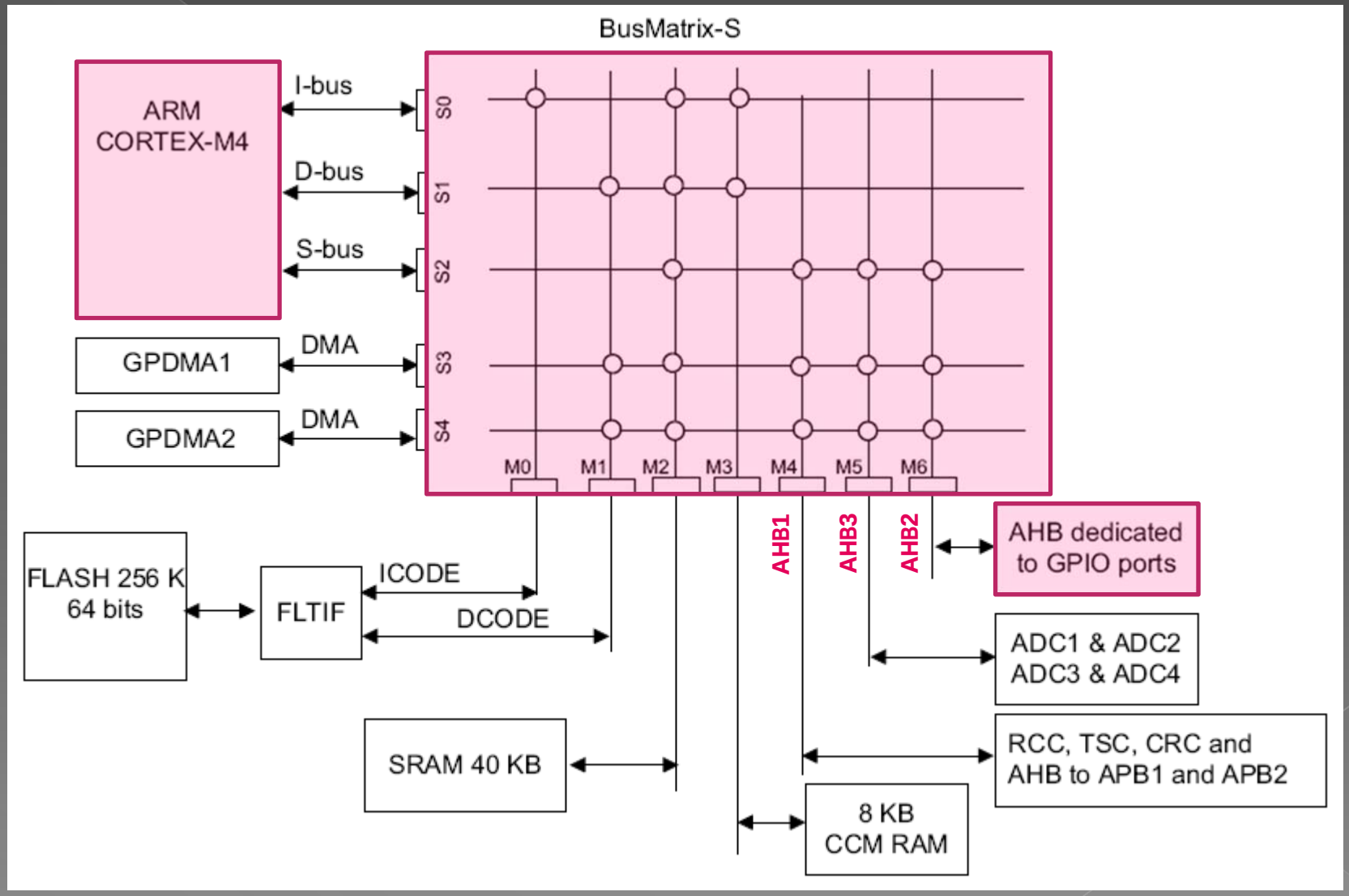
STM32F303 MCU pin description versus board function

MCU pin			Board function											
Main function	Alternate functions	LQFP100 pin num.	LSM303DLHC	L3GD20	Pushbutton	LED	SWD	USB	OSC	Free I/O	Power supply	CN3	P1	P2
BOOT0		94												19
NRST		14			RESET		NRST					5	4	
PA0	TIM2_CH1_ETR, G1_IO1, USART2_CTS, COMP1_OUT, TIM8_BKIN, TM8_ETR	23			USER								12	
PA1	TIM2_CH2, G1_IO2, USART2_RTS, TIM15_CH1N	24											9	
PA2	TIM2_CH3, G1_IO3, USART2_TX, COMP2_OUT, TIM15_CH1, AOP1_OUT	25											14	
PA3	TIM2_CH4, G1_IO4, USART2_RX, TIM15_CH2	26											11	
PA4	TIM3_CH2, G2_IO1, SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK	29											16	
PA5	TIM2_CH1_ETR, G2_IO2, SPI1_SCK	30		SCL/SPC									15	

- It is highly recommended to use only those pins which are listed as "Free I/O."

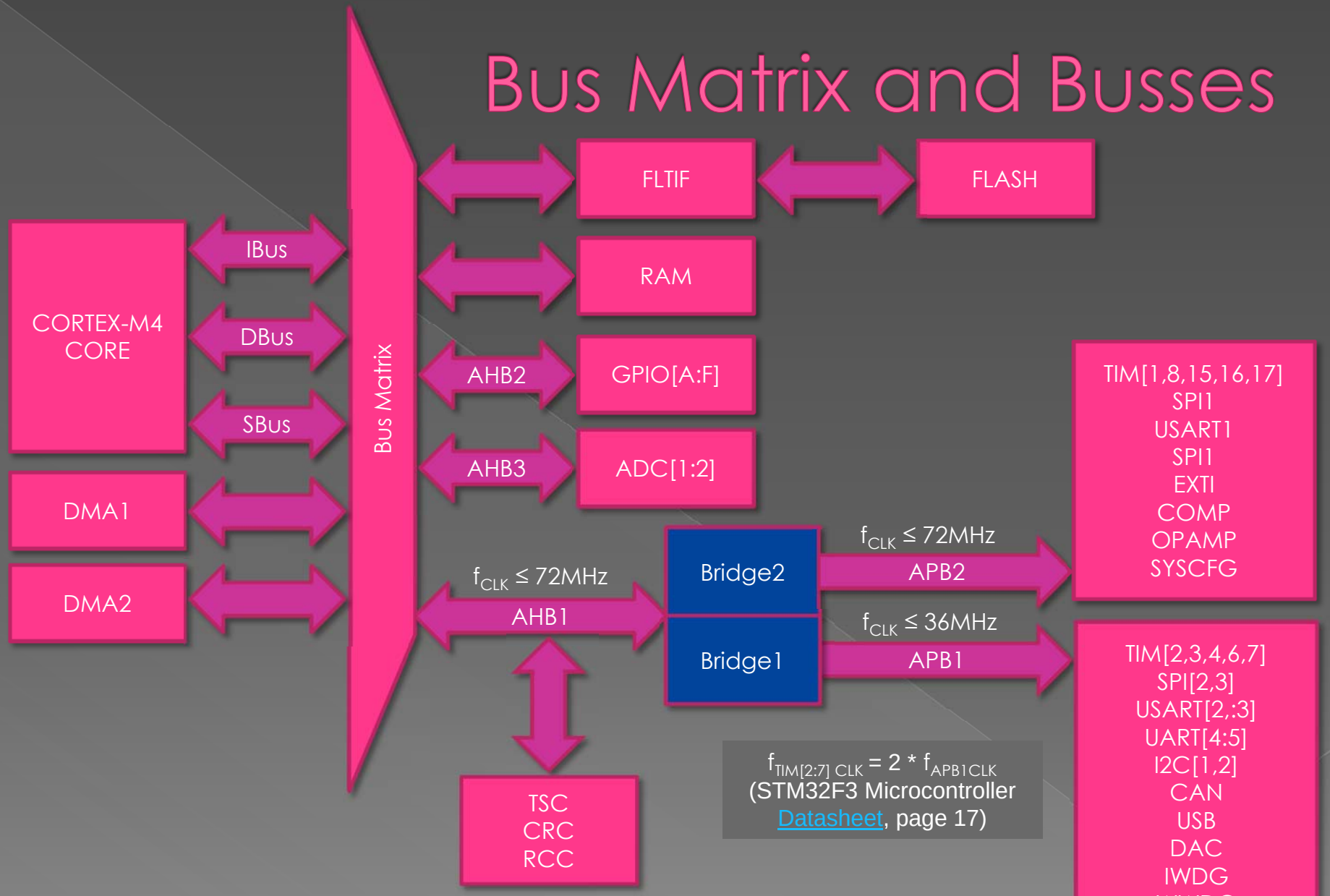
STM32F3DISCOVERY - Discovery kit for STM32F303xx microcontrollers , pages 21-29

Bus matrix



STM32F3 Microcontroller Reference Manual, page 39

Bus Matrix and Busses



$f_{TIM[2:7]\ CLK} = 2 * f_{APB1CLK}$
(STM32F3 Microcontroller Datasheet, page 17)

AHB[1;3]: Advanced High-performance Bus
APB: Advanced Peripheral Bus
RCC: Reset and Clock Control

STM32F3 Microcontroller Reference Manual, pages 41-44

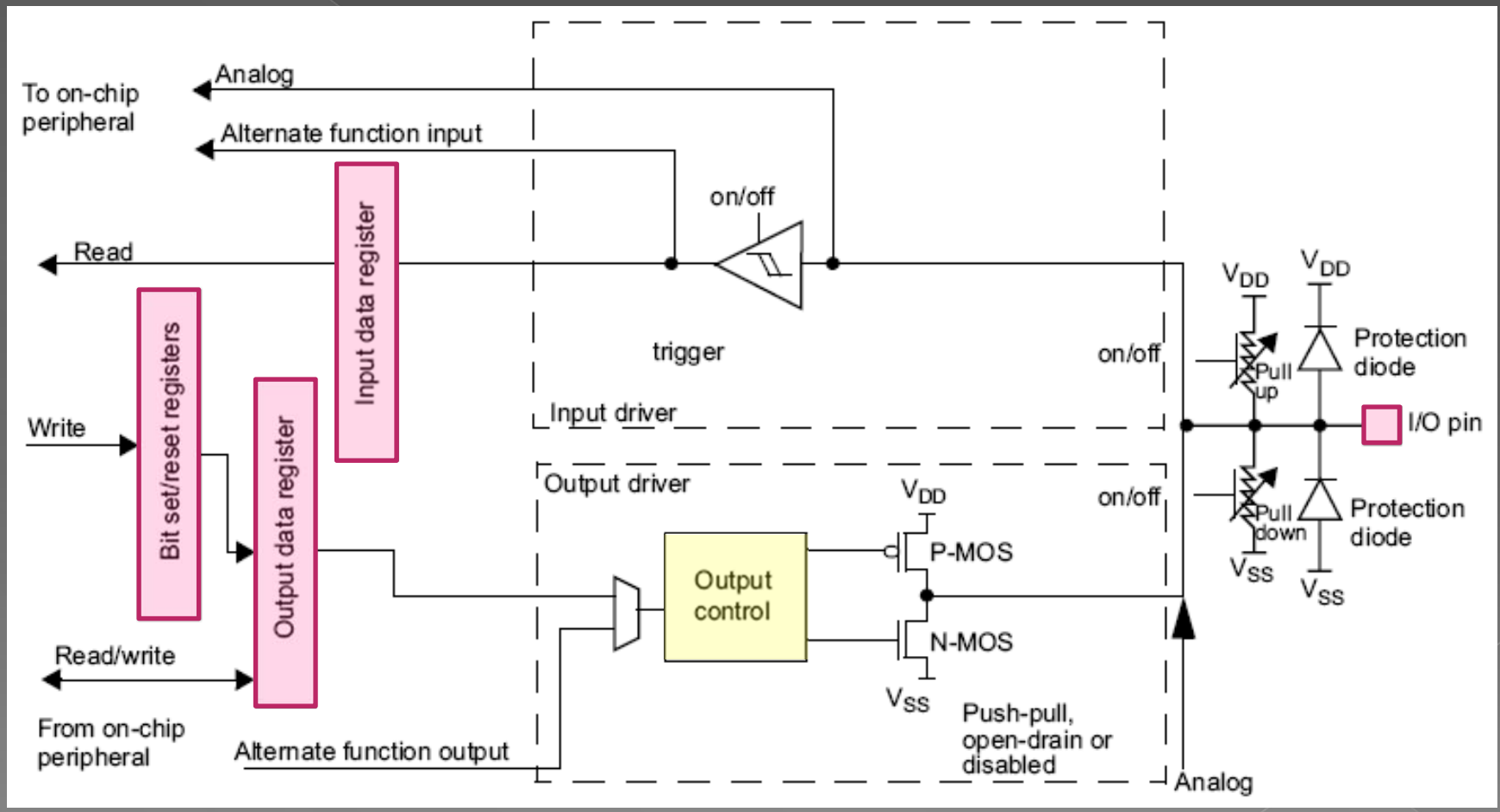
GPIO functional description

Subject to the specific hardware characteristics of each I/O port, each port bit of the general-purpose I/O (GPIO) ports can be individually configured by software in several modes:

- Digital Input
- Digital Output
- Alternate function
- Analog

STM32F3 Microcontroller Reference Manual, page 135

Basic structure of a standard I/O port bit



STM32F3 Microcontroller Reference Manual, page 136

Memory map and peripheral register boundary addresses (partial)

Bus	Boundary address	Size (bytes)	Peripheral
AHB2	0x4800 1400 - 0x4800 17FF	1 K	GPIOF
	0x4800 1000 - 0x4800 13FF	1 K	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 K	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 K	GPIOC
	0x4800 0400 - 0x4800 07FF	1 K	GPIOB
	0x4800 0000 - 0x4800 03FF	1 K	GPIOA
AHB1	0x4002 1000 - 0x4002 13FF	1 K	RCC

RCC: Reset and clock control

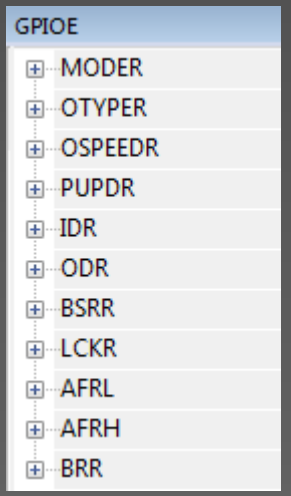
STM32F3 Microcontroller Reference Manual, page 41

GPIO registers

x = {A, B, ... F}

configuration registers

Register		Offset
GPIO port mode	GPIOx->MODER	0x00
GPIO port output type	GPIOx->OTYPER	0x04
GPIO port output speed	GPIOx->OSPEEDR	0x08
GPIO port pull-up/pull-down	GPIOx->PUPDR	0x0C
GPIO port input data	GPIOx->IDR	0x10
GPIO port output data	GPIOx->ODR	0x14
GPIO port bit set/reset	GPIOx->BSRR	0x18
GPIO port configuration lock	GPIOx->LCKR	0x1C
GPIO alternate function low	GPIOx->AFRL	0x20
GPIO alternate function high	GPIOx->AFRH	0x24
GPIO Port bit reset	GPIOx->BRR	0x28



STM32F3 Microcontroller Reference Manual, pages 145-152

Port bit configuration table

MODER(i) [1:0]	OTYPER(i)	OSPEEDR(i) [B:A]		PUPDR(i) [1:0]		I/O configuration	
01	0	SPEED [B:A]		0	0	GP output	PP
	0			0	1	GP output	PP + PU
	0			1	0	GP output	PP + PD
	0			1	1	Reserved	
	1			0	0	GP output	OD
	1			0	1	GP output	OD + PU
	1			1	0	GP output	OD + PD
	1			1	1	Reserved (GP output OD)	
10	0	SPEED [B:A]		0	0	AF	PP
	0			0	1	AF	PP + PU
	0			1	0	AF	PP + PD
	0			1	1	Reserved	
	1			0	0	AF	OD
	1			0	1	AF	OD + PU
	1			1	0	AF	OD + PD
	1			1	1	Reserved	
00	x	x	x	0	0	Input	Floating
	x	x	x	0	1	Input	PU
	x	x	x	1	0	Input	PD
	x	x	x	1	1	Reserved (input floating)	
11	x	x	x	0	0	Input/output	Analog
	x	x	x	0	1	Reserved	
	x	x	x	1	0		
	x	x	x	1	1		

GP = general-purpose
PP = push-pull
PU = pull-up
PD = pull-down
OD = open-drain
AF = alternate function

MODER(i)[1:0]: (i = 0..15)
00: Input mode (reset state)
01: General purpose output mode
10: Alternate function mode
11: Analog mode

OTYPER(i)[0]:
0: Output push-pull (reset state)
1: Output open-drain

OSPEEDR(i)[1:0]:
x0: 2 MHz, low speed
01: 10 MHz, medium speed
11: 50 MHz, high speed

PUPDR(i)[1:0]:
00: No pull-up, pull-down
01: Pull-up
10: Pull-down
11: Reserved

STM32F3 Microcontroller Reference Manual, page 137

GPIO register map and reset values

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	GPIOx_MODER (where x = **B..F**	MODER15[1:0]		MODER14[1:0]		MODER13[1:0]		MODER12[1:0]		MODER11[1:0]		MODER10[1:0]		MODER9[1:0]		MODER8[1:0]		MODER7[1:0]		MODER6[1:0]		MODER5[1:0]		MODER4[1:0]		MODER3[1:0]		MODER2[1:0]		MODER1[1:0]		MODER0[1:0]	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x04	GPIOx_OTYPER (where x = **A..F**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	OT15	OT14	OT13	OT12	OT11	OT10	OT9	OT8	OT7	OT6	OT5	OT4	OT3	OT2	OT1	OT0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x08	GPIOx_OSPEEDR (where **x = A..F**)	OSPEEDR15[1:0]		OSPEEDR14[1:0]		OSPEEDR13[1:0]		OSPEEDR12[1:0]		OSPEEDR11[1:0]		OSPEEDR10[1:0]		OSPEEDR9[1:0]		OSPEEDR8[1:0]		OSPEEDR7[1:0]		OSPEEDR6[1:0]		OSPEEDR5[1:0]		OSPEEDR4[1:0]		OSPEEDR3[1:0]		OSPEEDR2[1:0]		OSPEEDR1[1:0]		OSPEEDR0[1:0]	
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x0C	GPIOx_PUPDR	PUPDR15[1:0]		PUPDR14[1:0]		PUPDR13[1:0]		PUPDR12[1:0]		PUPDR11[1:0]		PUPDR10[1:0]		PUPDR9[1:0]		PUPDR8[1:0]		PUPDR7[1:0]		PUPDR6[1:0]		PUPDR5[1:0]		PUPDR4[1:0]		PUPDR3[1:0]		PUPDR2[1:0]		PUPDR1[1:0]		PUPDR0[1:0]	
	Reset value	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

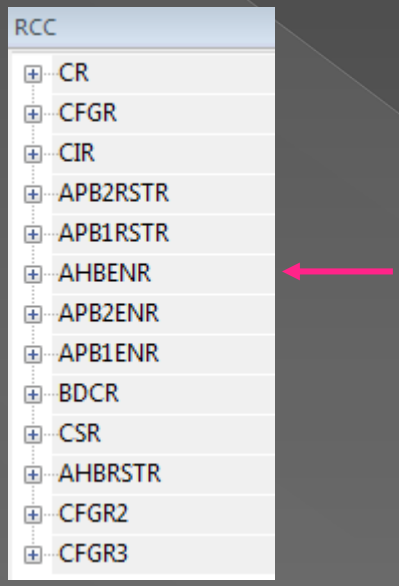
STM32F3 Microcontroller Reference Manual, page 151

GPIO register map and reset values (continued)

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x10	GPIOx_IDR (where x = **A..F**)	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	IDR15	IDR14	IDR13	IDR12	IDR11	IDR10	IDR9	IDR8	IDR7	IDR6	IDR5	IDR4	IDR3	IDR2	IDR1	IDR0
	Reset value																	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
0x14	GPIOx_ODR (where x = **A..F**)	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ODR15	ODR14	ODR13	ODR12	ODR11	ODR10	ODR9	ODR8	ODR7	ODR6	ODR5	ODR4	ODR3	ODR2	ODR1	ODR0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x18	GPIOx_BSRR (where x = **A..F**)	BRr5	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0	BS15	BS14	BS13	BS12	BS11	BS10	BS9	BS8	BS7	BS6	BS5	BS4	BS3	BS2	BS1	BS0
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x1C	GPIOx_LCKR (where x = **A..F**)	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	LCKK	LCK15	LCK14	LCK13	LCK12	LCK11	LCK10	LCK9	LCK8	LCK7	LCK6	LCK5	LCK4	LCK3	LCK2	LCK1	LCK0
	Reset value																0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x20	GPIOx_AFRL (where x = **A..F**)	AFRL7[3:0]				AFRL6[3:0]				AFRL5[3:0]				AFRL4[3:0]				AFRL3[3:0]				AFRL2[3:0]				AFRL1[3:0]				AFRL0[3:0]			
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x24	GPIOx_AFRH (where x = **A..F**)	AFRH15[3:0]				AFRH14[3:0]				AFRH13[3:0]				AFRH12[3:0]				AFRH11[3:0]				AFRH10[3:0]				AFRH9[3:0]				AFRH8[3:0]			
	Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x28	GPIOx_BRR (where x = **A..F**)	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	BR15	BR14	BR13	BR12	BR11	BR10	BR9	BR8	BR7	BR6	BR5	BR4	BR3	BR2	BR1	BR0
	Reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

STM32F3 Microcontroller Reference Manual, page 152

AHB peripheral clock enable register (RCC->AHBENR)



IOPxN
1: GPIOx clock enabled
0: GPIOx clock disabled

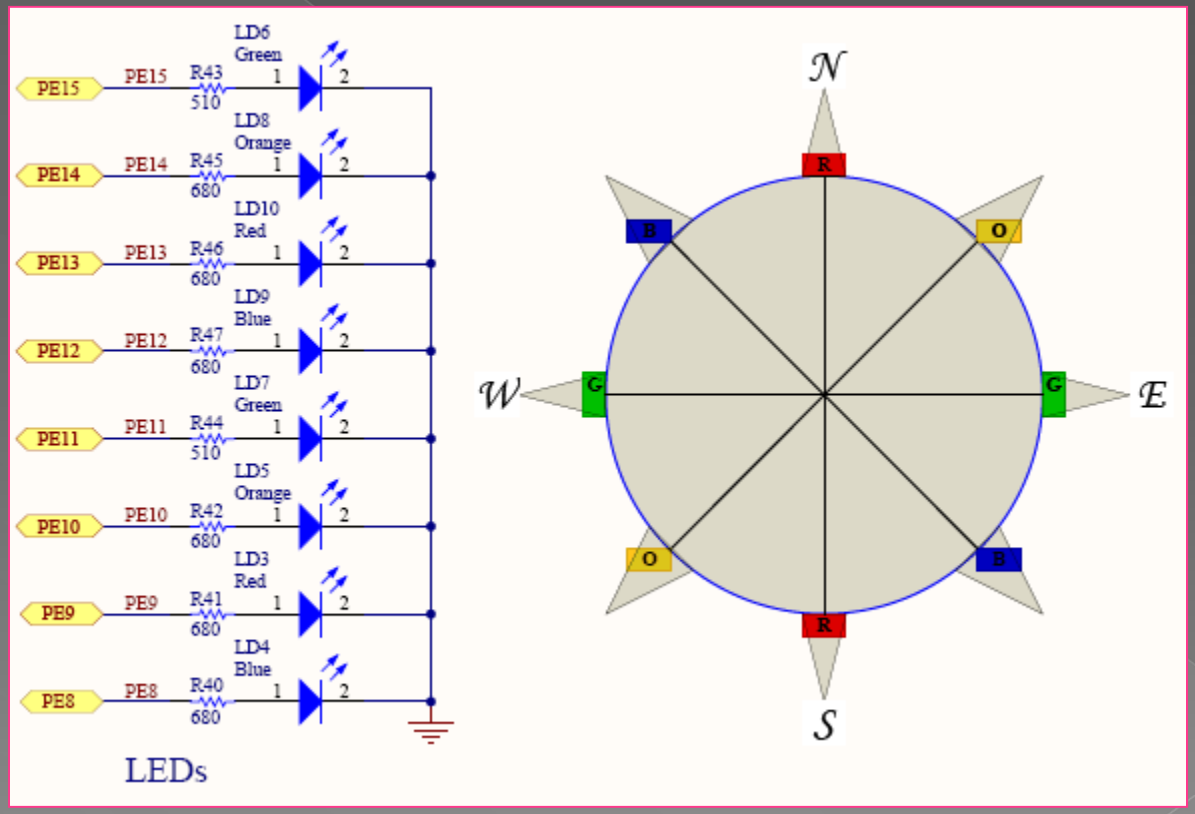
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res	Res	ADC34EN	ADC12EN	Res	Res	Res	TSCEN	Res	IOPFEN	IOPEEN	IOPDEN	IOPCEN	IOPBEN	IOPAEN	Res
							rw		rw		rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	Res	Res	Res	Res	Res	Res	Res	Res	CRCEN	Res	FLITFEN	Res	SRAMEN	DMA2EN	DMA1EN
									rw		rw		rw		rw

STM32F3 Microcontroller Reference Manual, page 117

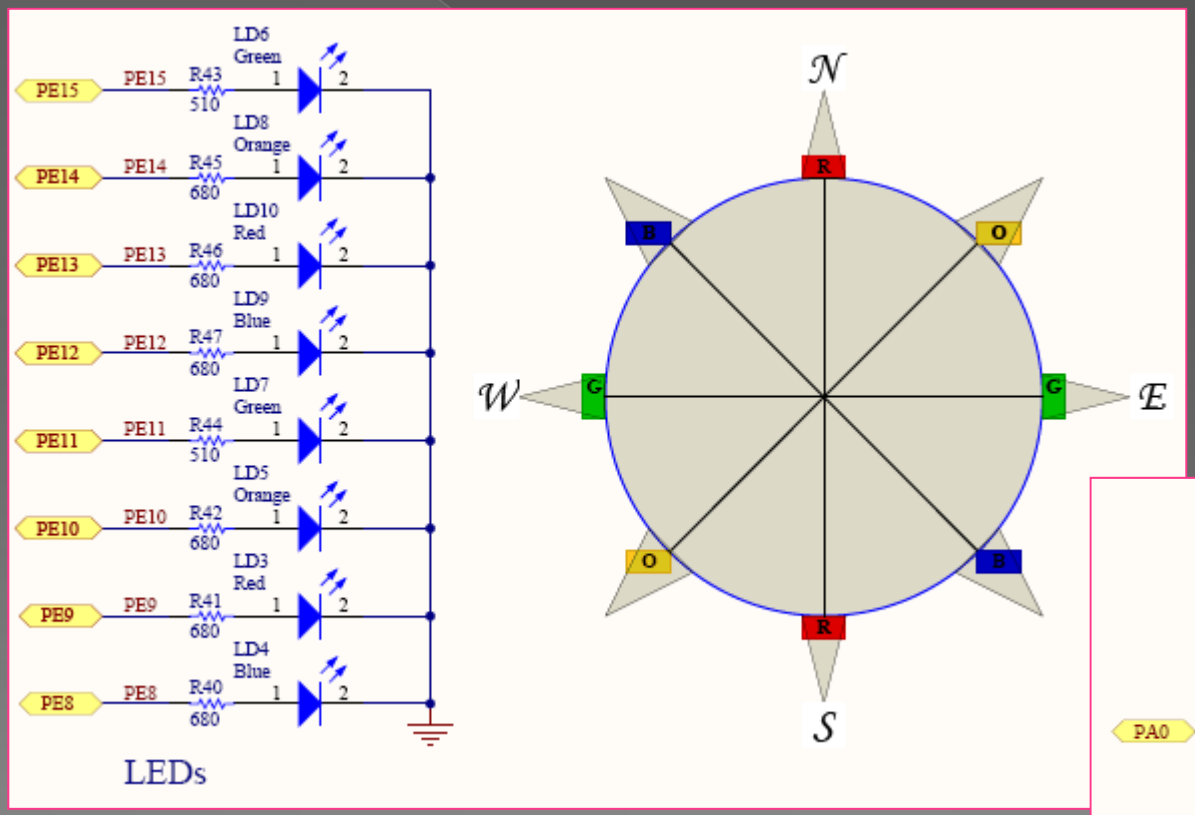
Exercise: LEDs blinking

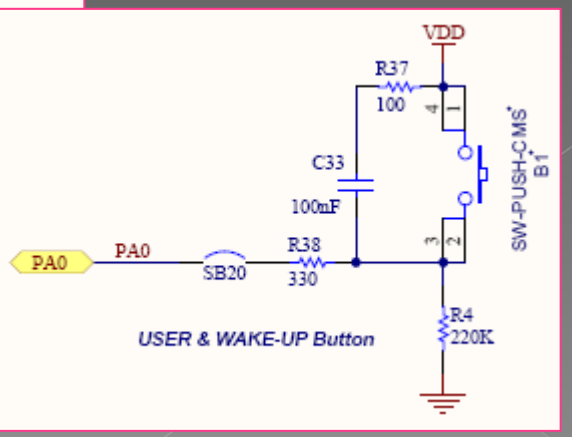
- Forever, turn LED6 & LED7 high during 500 ms, then low during 500 ms.



Exercise: LED6 Controlled by a Push Button

- If the user PB is pressed then turn LED6 on; else, turn it off.





I/O alternate function selection

- Two registers (GPIOx_AFRL, GPIO_AFRH) are provided to select one of the alternate function inputs/outputs available for each I/O.
- With these registers, you can connect an alternate function to some other pin as required by your application.
  - a number of possible peripheral functions are multiplexed on each GPIO

Alternate functions for GPIOA pins[0:7]

AF n°	Port & Pin Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
7	PA0		TIM2_CH1_ETR		TSC_G1_IO1				USART2_CTS	COMP1_OUT	TIM8_BKIN	TIM8_ETR					EVENTOUT
5	PA1		TIM2_CH2		TSC_G1_IO2				USART2_RTS		TIM15_CH1N						EVENTOUT
6	PA2		TIM2_CH3		TSC_G1_IO3				USART2_TX	COMP2_OUT	TIM15_CH1						EVENTOUT
5	PA3		TIM2_CH4		TSC_G1_IO4				USART2_RX		TIM15_CH2						EVENTOUT
6	PA4			TIM3_CH2	TSC_G2_IO1		SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK								EVENTOUT
4	PA5		TIM2_CH1_ETR		TSC_G2_IO2		SPI1_SCK										EVENTOUT
8	PA6		TIM16_CH1	TIM3_CH1	TSC_G2_IO3	TIM8_BKIN	SPI1_MISO	TIM1_BKIN		COMP1_OUT							EVENTOUT
8	PA7		TIM17_CH1	TIM3_CH2	TSC_G2_IO4	TIM8_CH1N	SPI1_MOSI	TIM1_CH1N		COMP2_OUT							EVENTOUT

STM32F3 Microcontroller Datasheet, pages 41-48

I/O structure

FT	5 V tolerant I/O
FTf	5 V tolerant I/O, FM+ capable
TTa	3.3 V tolerant I/O directly connected to ADC
TC	Standard 3.3V I/O
B	Dedicated BOOT0 pin
RST	Bidirectional reset pin with embedded weak pull-up resistor

STM32F3 Microcontroller Datasheet, pages 35-40

Thank you

STM32 Releasing your **creativity**