

# **INTERMODEM PROCESSOR SYSTEM**

## **Instruction Manual**

**January 1970**

**Prepared for:**

**Bolt, Beranek and Newman, Inc.  
Cambridge, Massachusetts**

**Honeywell**

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## SECTION I INTRODUCTION

This manual contains the description of the Intermodem Processor (IMP) System, manufactured by Honeywell Inc., Computer Control Division, Framingham, Massachusetts, for Bolt, Beranek and Newman Inc., Cambridge, Massachusetts.

### EQUIPMENT SUPPLIED

The IMP system consists of a ruggedized DDP-516 high-boy general purpose computer with a 12K memory, a 16-channel direct multiplex control (DMC) option, and 16 priority interrupt (PI) lines. A typical system contains a full duplex IMP-host option and three full duplex IMP-modem options which are mounted in two option assemblies within the CPU cabinet. The system configuration can be expanded to include a maximum of five IMP-modem options and two IMP-host options. Each system contains a special real time clock (RTC) option, watch dog timer (WDT) option, memory lockout option, halt inhibit option, and auto-restart option. An ASR-33 Teletype and a portable paper tape reader are supplied with each system, along with the necessary interface cabling.

### APPLICABLE DOCUMENTS

Documents containing supplementary information are:

<i>Title</i>	<i>Doc. No.</i>
Instruction Manual for DDP-516 General Purpose Computer, Vol. I	130071620
Instruction Manual for DDP-516 General Purpose Computer, Vol. II	130071621
Instruction Manual for DDP-516 General Purpose Computer, Vol. III	130071622
Option Manual for RP-61/62 Ruggedized Power Supply	130071933
FORTRAN IV Manual	130071364
Option Manual for DMC	130071647
Instruction Manual for DDP-516 Ruggedized Computer	70130072185
Priority Interrupt and Memory Increment Option Manual	130071644
Technical Manuals for Automatic Send-Receive (ASR)	
Teletypewriter Set, Teletype Corp. Model 33,	
Bulletin 273-B, Vol. I	70130071453
Bulletin 273-B, Vol. II	70130071455
Bulletin 1184-B, Teletype Parts	70130071454

### GENERAL DESCRIPTION

The BB&N IMP system provides the storage, buffering and switching capabilities which allow communications between computer centers located throughout the world. Incoming and outgoing data transfers are handled on a time sharing basis according to priorities. A typical IMP system is shown in Figure 1-1.

Incoming data from a modem data set is received serially at the IMP-modem option, and a 16-bit data word is formed. After forming the data word, the IMP-modem option bids for service via its associated PI line. The DMC option breaks into the program sequence at the end of the current instruction (depending upon priority), addresses the interrupting IMP-modem option and transfers the 16-bit data word in parallel, into the DDP-516 CPU memory, where it is stored. Then, the next data word is formed, transferred, and stored. This action is repeated until the incoming transfer is completed.

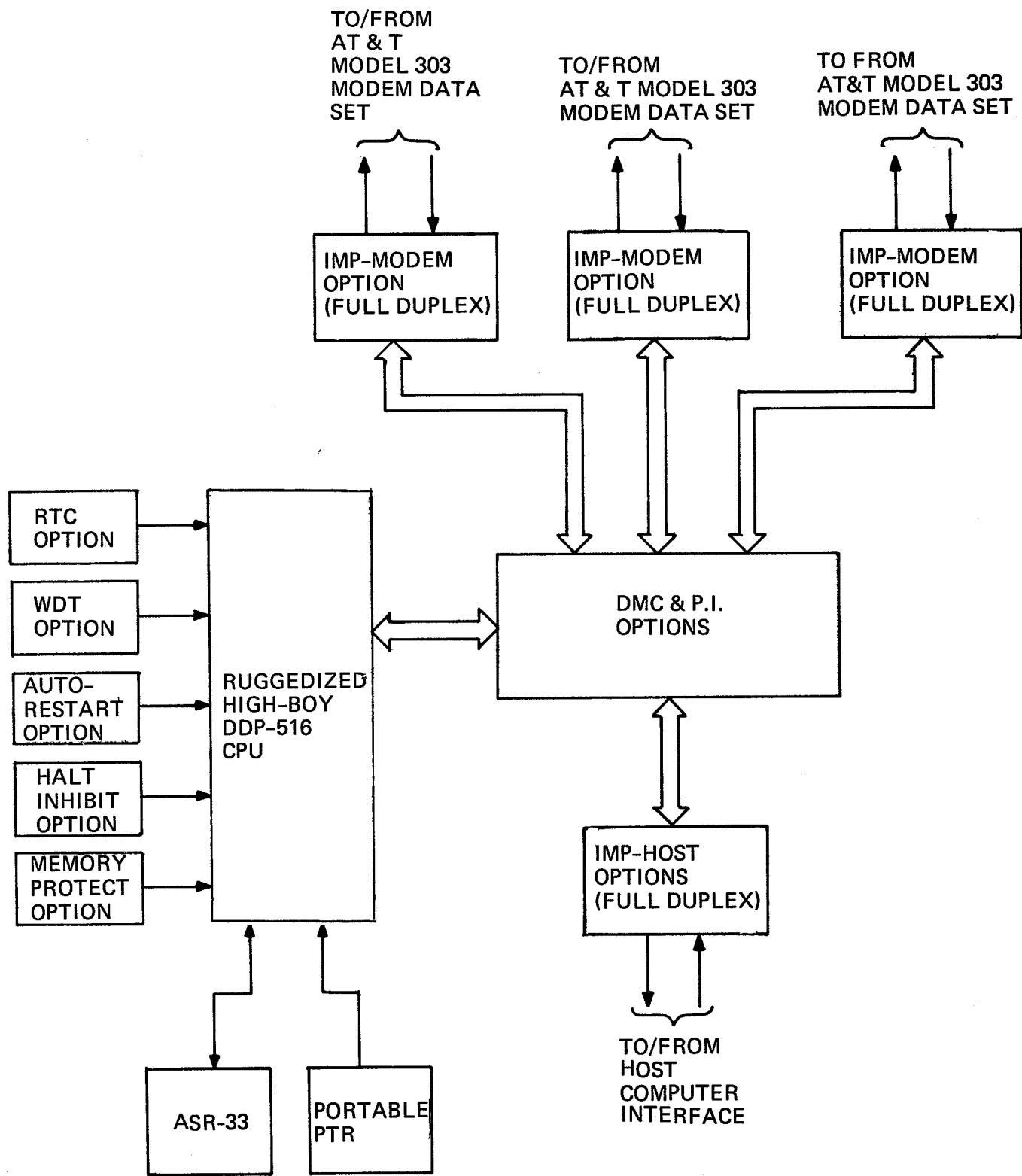


Figure 1-1. Typical BB&N IMP System Block Diagram

A block of outgoing data is transferred out of the DDP-516 memory in 16-bit data words. The IMP-modem option is addressed, the DMC channel is enabled, and the first data word is stored when the IMP-modem option is ready. Then, the data word is shifted serially out of the IMP-modem option and into the modem data set. This action is repeated until the complete block of data is transferred, and the DMC end-of-range is reached.

The modem data sets and the host computer can communicate via the DDP-516. An incoming data transfer for the host computer is first stored in the DDP-516 memory. Then, the IMP-host option is addressed, its associated DMC channel is enabled, and the limits of the message are established by setting up the DMC end of range. When the IMP-host option is ready, the data is transferred out of memory in 16-bit bytes. After storage in the IMP-host option, the 16-bit data word is shifted serially to the host computer interface. When the serial transfer is completed, the next byte is loaded into the IMP-host option and shifted to the host computer interface. This action is repeated until the data transfer is completed, and the DMC end of range is reached.

When the host computer outputs data, the IMP-host option receives the data from the host computer interface serially and forms a 16-bit data word. When a 16-bit data word is formed, the IMP-host option bids for service by enabling its priority interrupt line. The IMP-host logic is enabled, and the data word is loaded into the DDP-516 via the associated DMC channel.

The actual configuration of an IMP system can vary from the configuration shown in Figure 1-1. Provisions have been made to increase the number of IMP-modem options to five and IMP-host options to two. The expected demands of each host computer site determine the actual system configuration.

Additional optional equipment, such as the real time clock, watch dog timer, etc., are provided and interfaced with the DDP-516 CPU. Input/output devices, such as the ASR-33 and a portable paper tape reader, are provided to allow communications with the DDP-516 CPU.

## **SECTION II INSTALLATION**

This section contains a general physical description of the equipment supplied with the IMP system. System interconnections and  $\mu$ -PAC complement lists for the optional equipment are also provided. Specific instructions pertaining to CPU installation are contained in the Instruction Manual for the DDP-516 Ruggedized General Purpose Computer.

### **PHYSICAL DESCRIPTION**

The assemblies of the IMP system are contained in a DDP-516 ruggedized high-boy cabinet. Figure 2-1 identifies the location of the assemblies within the cabinet. The CPU logic is contained in tilt-out assemblies A1 and A4-A5. Logic for the optional equipment added for the IMP system are mounted in option assemblies B1-B2 and B3-B4, which are also tilt-out assemblies. The location of the power supplies, power distribution, and auto-restart relays are also identified.

Each IMP-modem option occupies a 3 x 3  $\mu$ -BLOC, and the IMP-host option occupies a 2 x 3  $\mu$ -BLOC. The WDT, RTC, and display logic is contained on a 2 x 3  $\mu$ -BLOC, and the other control logic is contained on three separate 1 x 3  $\mu$ -BLOCs. Eight spare 1 x 3 spaces are available for system expansion. The locations of the logic within the tilt-out assemblies are identified in Figure 2-2. Hinge location on tilt-out assemblies aids in equipment location. Actual  $\mu$ -PAC locations for the optional equipment are shown on the PAC layout drawings presented at the rear of this manual.

### **SYSTEM INTERCONNECTIONS**

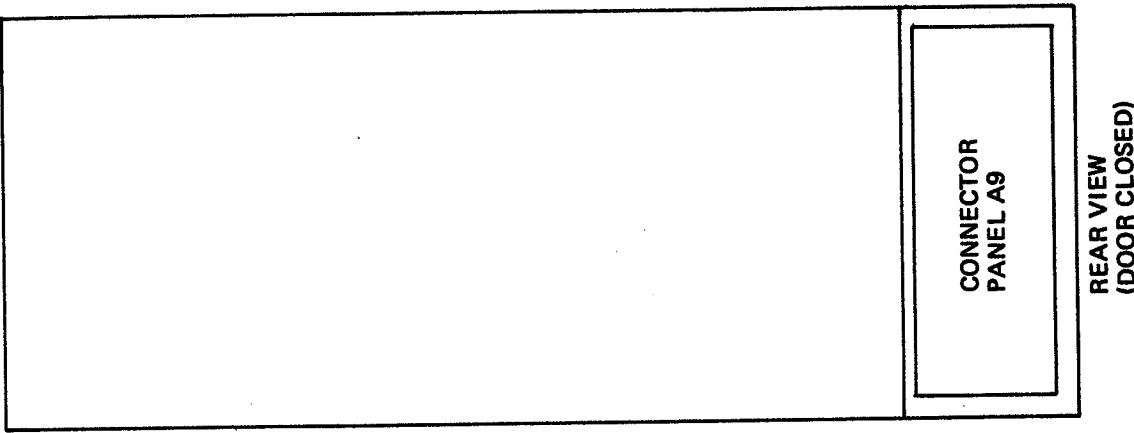
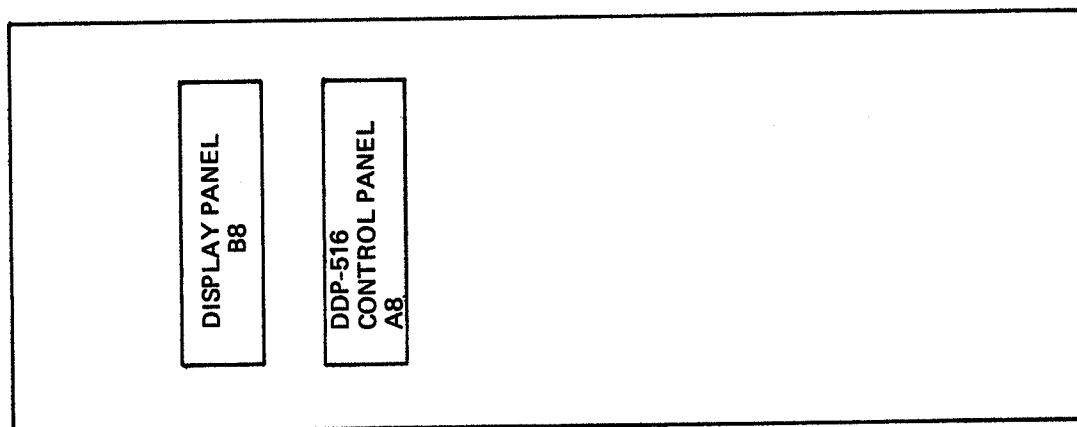
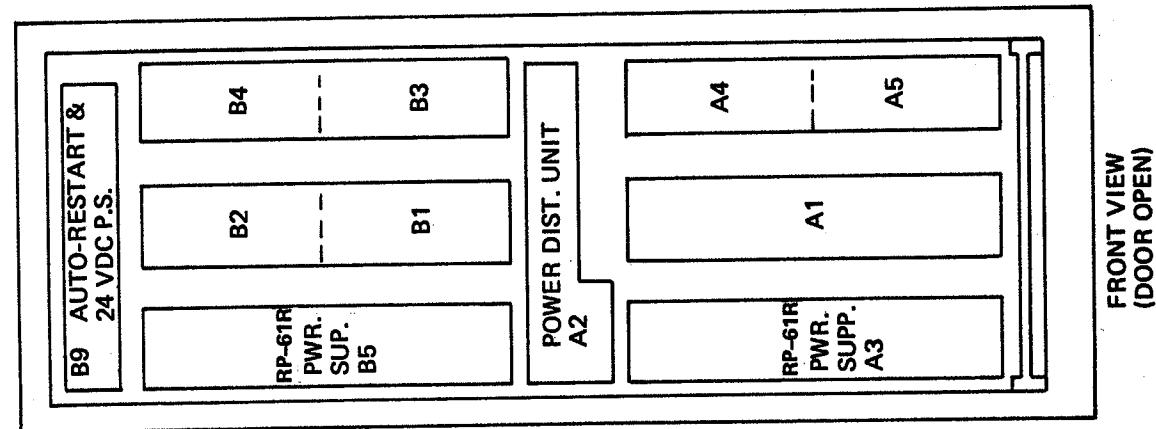
The cables which interconnect the various system components are interfaced with the DDP-516 CPU via the connector panel located at the lower rear of the ruggedized high-boy enclosure. Figure 2-3 shows the connector panel for a typical system of three IMP-modem options and one IMP-host option. For a larger system, blank covers are removed, and the required connectors are inserted. Cables from the modem data sets go to the IMP-modem connectors, and the cable from the host computer interface is connected to the IMP-host connector. The ASR connector receives the cable from the ASR-33, and the PTR connector receives the cable from the portable PTR.

Power to the PTR, ASR, and DDP-516 CPU is obtained via separate power cables which connect to a 120 Vac prime power source. To control the PTR and ASR prime power from the DDP-516 control panel, cables from the 24 Vdc connector are connected into the ASR-33 and PTR power control circuits. A 24 Vdc signal present when the CPU is turned on enables the power control circuits and allows power application.

### **$\mu$ -PAC COMPLEMENT**

The  $\mu$ -PAC complement lists for the BB&N IMP system optional equipment are contained in Tables 2-1 through 2-3. Refer to the DDP-516 Instruction Manual for the basic computer  $\mu$ -PAC complement.

Figure 2-1. Typical BB&N IMP System, Assembly Location Diagram



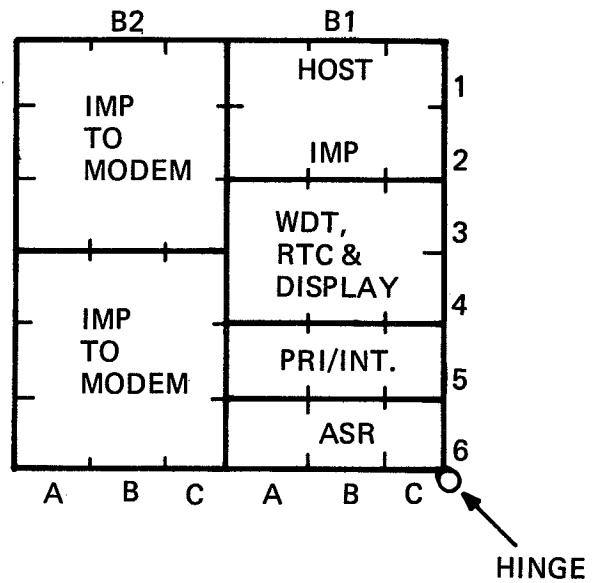
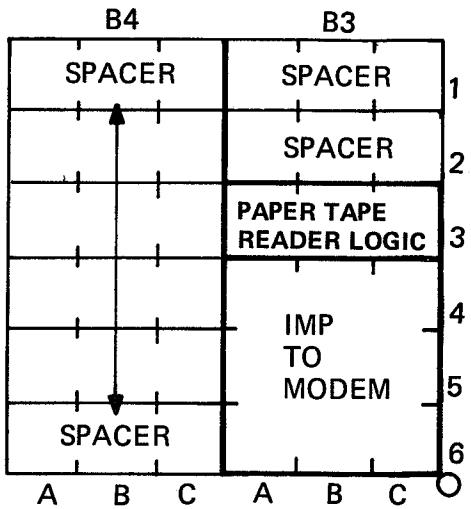
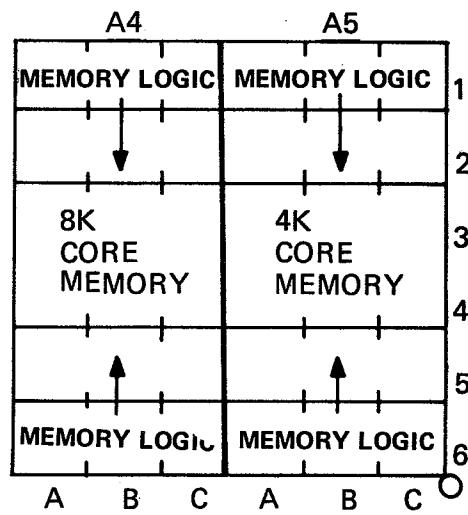
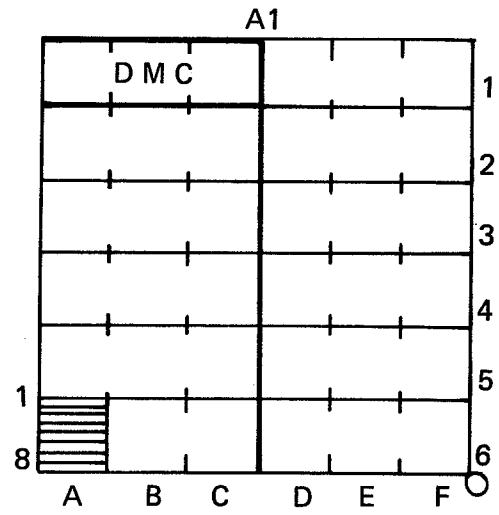
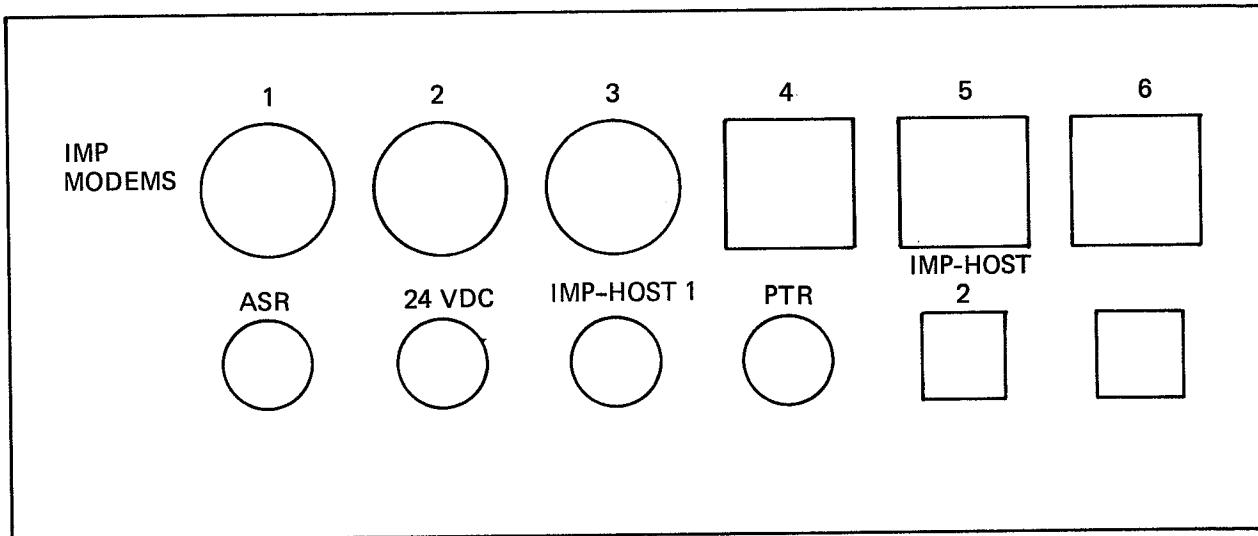


Figure 2-2. Typical BB&N IMP System, Option Location Diagram



**Figure 2-3. BB&N IMP Connector Panel**

**TABLE 2-1.  
μ-PAC COMPLEMENT FOR IMP-MODEM OPTION**

Model No.	Quantity	Model No.	Quantity
BC-335	2	EO-335	6
BR-320	9	FA-320	1
*CC-152	2	FA-335	4
*CC-253	2	FF-335	2
DE-335	2	MV-335	1
DI-320	2	OD-335	3
DI-335	4	PA-336	3
DL-335	2	SR-335	1
DM-335	3	SR-336	1
DN-320	4	TG-320	9

**TABLE 2-2.  
μ-PAC COMPLEMENT FOR IMP-HOST OPTION**

Model No.	Quantity	Model No.	Quantity
BC-335	2	FA-335	3
*CC-152	1	OD-335	1
DC-335	1	PA-336	1
DI-335	5	SR-335	1
DL-335	1	SR-336	2
DM-335	3	TG-320	4
DM-337	1	XD-336	1
DN-335	1		

\*Special μ-PAC

**TABLE 2-3.**  
 **$\mu$ -PAC COMPLEMENT FOR RTC, WDT & DISPLAY**

Model No.	Quantity	Model No.	Quantity
BC-335	2	FA-335	2
BC-336	1	LD-330	2
BR-320	4	MC-335	1
*CC-152	1	MV-335	1
DC-335	2	RC-330	1
DI-335	4	SD-330	1
DM-335	1	TG-335	4

\*Special  $\mu$ -PAC

### SECTION III OPERATION AND PROGRAMMING NOTES

The CPU operation and programming considerations for the DDP-516 IMP system are similar to those of the standard DDP-516 CPU and the ruggedized DDP-516 CPU. Therefore, the instruction manuals, user guide and programming manuals for the standard DDP-516 and ruggedized DDP-516 provide the necessary operating information. This section provides the necessary supplementary information for the optional equipment in this system.

#### OPERATION

The operational controls and indicators for the CPU are located on the CPU control panel and power distribution unit. The functions of these controls and indicators are described in the instruction manual for the ruggedized DDP-516 general purpose computer.

Figure 3-1 shows the controls and indicators mounted on the IMP system display panel. Table 3-1 lists the function and designations of the controls and indicators.

#### PROGRAMMING NOTES

This section contains a list of OCP instructions assigned to the IMP system.

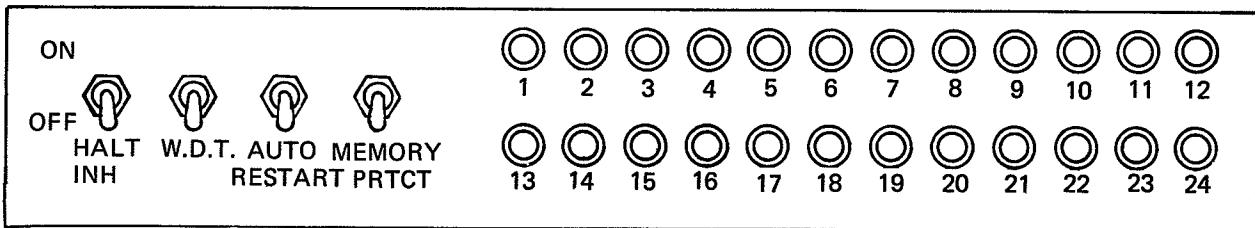


Figure 3-1. Display Panel

## **IMP-Modem Instructions**

The following OCPs are assigned to the IMP-modem option.

OCP '007X*	Enables modem output mode.
OCP '017X*	Resets modem output mode.
OCP '027X*	Crosspatches the modem data set.
OCP '037X*	Crosspatches the interface.
OCP '047X*	Enables modem input mode.
OCP '057X*	Not used.

\* X indicates address selection for modem data sets (e.g., Modem Data Set 3 would be assigned OCP '0073, OCP '0173, etc.)

**TABLE 3-1.  
DISPLAY PANEL CONTROLS AND INDICATORS**

Designation	Type	Function
1 through 24	Indicators	Indicators 1 through 16 display the data on the output transfer bus (OTBXX).
HALT INH	SPDT Toggle Switch	Enables the halt inhibit logic when set to the ON position.
W.D.T.	SPDT Toggle Switch	Allows the watch dog timer option to be enabled when in the ON position.
AUTO RESTART	DPDT Toggle Switch	Enables the automatic restart circuit when set to the ON position.
MEMORY PRTCT	SPDT Toggle Switch	Enables the memory lockout logic when set to the ON position.

## **IMP-Host Instructions**

The following instructions are assigned to the IMP-Host 1 option\*\*.

OCP '0070	Enables host computer output mode.
OCP '0170	Enables host computer input mode.
OCP '0270	Sets end of transmission.
OCP '0370	Enables host computer crosspatch address.
OCP '0470	Unpatches host computer address.
OCP '0570	Enables host computer address.

## **Real Time Clock Instructions**

The following instructions are assigned to the real time clock option.

OCP '0040	Enables the real time clock.
OCP '0041	Enables the task interrupt.
OCP '1040	Disables the real time clock.

## **Watch Dog Timer Instruction**

The following instruction is assigned to the watch dog timer option.

OCP '0026	Resets counter in watch dog timer if W.D.T. switch on display panel is in the up position.
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\*\*IMP-Host 2 instruction codes have a "60" in the last two digits.

## SECTION IV THEORY OF OPERATION

The IMP system contains a number of special options packaged within a ruggedized DDP-516 enclosure. In this section, the theory of operation for each special option is described in individual subsections. Refer to the DDP-516 General Purpose Computer instruction manuals for CPU theory of operation and to the DDP-516 Ruggedized Computer instruction manual for a general discussion of the ruggedized packaging.

### DETAILED DESCRIPTION

#### Real Time Clock

The real time clock option (LBD 01.01), contained in the IMP system, is a 320 kHz clock enabled by an OCP '0040 generating CLOCK+ (zone J2).\* This signal triggers a 1.3  $\mu$ s delay (zone A12) generating a 160 kHz square wave (CLOCK+A). A five-stage counter (zones E9 through L9) counts CLOCK+A down by a factor of five, generating RTCLK-, which strobes a 16-bit binary counter (zone C10). The eighth bit (CNT08+) of the binary counter is connected to PI Line 15 (PIL15). When CNT08+ goes from 0V to +6V, the CPU interrupts to location 102 in the program counter.

This option has the capability of forcing a program interrupt on the lowest PI line (PIL16-). An OCP '0041 causes PIL16- to go to 0V (zone H6). The CPU jumps out of the program, according to priorities, and performs an indirect JST instruction to location 103. This capability is called the task interrupt.

The real time clock option is disabled via an OCP '1040. When this instruction is executed, the ENABL flip-flop (zone D3) is reset, and the negative-going transition of ENABL+ resets the 5-stage and 16-stage counters.

#### IMP-Modem Option

The IMP-modem option is a full duplex device which interfaces an AT&T Model 303 Modem Data Set with the DDP-516 CPU via the DMC option. Logic for the three IMP-modem options supplied with this system are mounted in option assemblies within the DDP-516 cabinet. The transfer of data across the IMP-modem interface is performed via the DDP-516 DMC option and controlled via OCP instructions. Each option is assigned two DMC channels and two PI lines. These assignments are shown in Table 4-1.

Self-test features have been designed into this option. The transmit and receive modes are tested by looping the output directly to the input and the lines to modem are also checked by looping the data. Testing is also accomplished via OCP instructions.

*Transmit Mode (See Figure 4-1).*—Before starting the transmit cycle, the DMC channel pointers are set for the required number of transfers. Then, the assigned OCP which enables the output mode is executed. The OCP is decoded (LBD 00.07/A1 through J6) generating MODCP+ and MODOT+. These signals are ANDed and the resultant signal direct sets the REQOT flip-flop (LBD 00.01/P6). REQOT+ conditions the set control of the SNREQ flip-flop (LBD 00.01/J9) and the next LDSTR+ pulse (LBD 00.01/J4) sets the SNREQ flip-flop.

\*Zone numbers refer to areas on logic block diagrams.

**TABLE 4-1.**  
**DMC AND PI ASSIGNMENTS FOR IMP SYSTEM**

Option	DMC Channel	PI Line
Receive Mode 1	1	1
Receive mode 2	2	2
Receive Mode 3	3	3
Receive Mode 4*	4	4
Receive Mode 5*	5	5
Transmit Mode 1	6	6
Transmit Mode 2	7	7
Transmit Mode 3	8	8
Transmit Mode 4*	9	9
Transmit Mode 5*	10	10
Transmit Host 1	11	11
Transmit Host 2*	12	12
Receive Host 1	13	13
Receive Host 2*	14	14
Spare	15	
Spare	16	
RTC Interrupt		15
Task Interrupt		16

\*Optional.

SNREQ- is inverted and ANDed with FSTLD- (+6V at this time) conditioning the set input of the READY+T flip-flop (LBD 00.01/J6). LDTSR+ strobes the clock input of the READY+T flip-flop. The set output of the READY+T flip-flop is routed to the DMC Data Interrupt Line (DIL) assigned to the option and the DMC cycle is initiated.

Data is routed to the transmit register (LBD 00.02/A1 through N4) via the OTBxx lines. RRLIN+ and DALTN+ are ANDed (LBD 00.01/N11) and the resultant signal (LDTBR-) sets the FSTLD+ flip-flop and resets the READY+T flip-flop. LDTBR- is inverted generating LDTBR+ which strobes the data on the OTBxx lines into the transmit register. The data remains in the transmit register until the SC counter (LBD 00.03/D10 through H10) indicates the message mode is selected.

While the transmit register is being loaded with a 16-bit word, the modem is in the quiescent state and transmits a minimum of two sync characters ('026). After decoding the output request OCP, SNREQ+ goes to +6V conditioning a gate at zone 9A of LBD 00.03. The trailing edge of LDSTR+ increments the SC counter. The octal decoder (LBD 00.03/J6) decodes the contents of the SC counter causing SCDLE- to go to 0V. This indicates the Data Line Escape (DLE) mode and a '020 is transmitted over the line.

As long as the message mode or sync mode is not enabled, MSGSN- increments the SC counter and in this case, steps the option to the STX (Start of Text) mode ('002) and then, into the message mode. The option remains in the message mode until the DMC completes its transmission and the end of range line (ERLXX-) goes to 0V. At this time the DLE character is again transmitted to the modem. This indicates the mode has been changed from the message mode to the end of text mode.

During the message mode, bits 9 through 16 of the transmit register are loaded into the shift register (LBD 00.02/A11 through M11) and shifted out to the modem in a serial transfer. Then, bits 1 through 8 are loaded into the shift register and the second 8-bit serial transfer is performed. The transfer of data from the transmit register and into the shift register is accomplished by the load group strobe pulses (LDGP1+ and LDGP2+, LBD 00.01/F8 and G12). Both of these strobe pulses must be generated before the transmit register is loaded with the next 16-bit word. If the

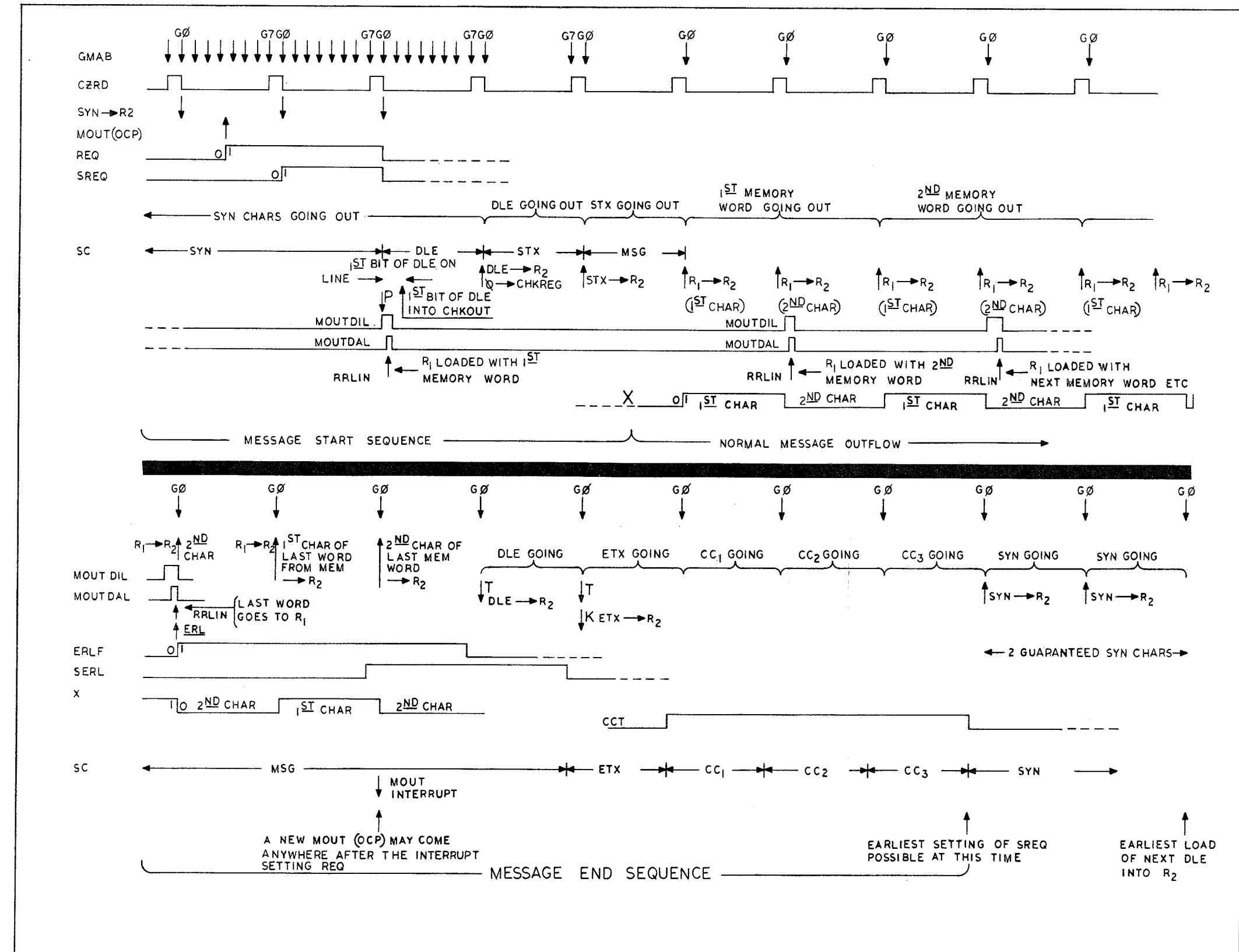


Figure 4-1. IMP-Modem Option –  
Transmit Timing Diagram

modem is in the message mode and the shift register has been filled twice, the transmit control logic is enabled for the next 16-bit DMC transfer. This action continues until the ERLXX- line from the DMC goes to 0V. At this time, the ERLTN flip-flop (LBD 00.01/J10) is set, the set input of the READY+T flip-flop is inhibited and DIL line is held off. ERLTN- generates RSERL+ and steps the SC counter to the end of text mode. ERLTN+ enables the load DLE (LDDLE+) signal. The modem automatically steps from the end of text mode ('203) and into the 24 bits of the check sum register. The formation of the check sum is discussed below in additional detail.

*False DLE Detection.* — From time to time, there may be a combination of bits which appear to be a DLE character ('020). If these bits are not detected as invalid, they will switch the SD counter of the receiving modem prematurely. This will cause the last portion of a message to be lost and inevitably cause a check sum error. Valuable on-line time is lost because a new transmission of the message is required.

To counteract a false DLE character, special DLE detect logic (00.01/K4 through P4) is designed into the IMP-modem option. This logic is utilized in the message mode and is gated with ERLTN- to block several functions. First, another DLE character must be transmitted directly after the first to indicate that this is an invalid end of message.

The FFFFF flip-flop (LBD 00.01/P4) is set by gating DLEDT+ with ERLTN-. FFFFF- goes to 0V disabling the reset control of the FSTLD flip-flop (LBD 00.01/P11). FSTLD- remains at 0V disabling the READY+T flip-flop and blocking the next DIL. With FFFFF- at 0V, both LDGP1+ and LDGP2+ are inhibited. This enables the DLE to be retransmitted and on the next G0007+ pulse the FFFFF flip-flop is reset.

*Receive Mode (See Figure 4-2).* — The receive and transmit modes are regulated by the same clock when the interface is crosspatched (test mode) and by the modem clock when running to the modem and out to the line. The incoming data is routed to the option via the CKTBB+ line and is used to generate DATIN- and DATIN+ (LBD 00.04/E3). Data is shifted through an SR-336 PAC in a serial fashion (LBD 00.05/A1 through A4) and scanned at every shift checking for DLE's, STX's, etc. When the first DLE is detected, the SD counter (LBD 00.03/B6 through G6) is incremented. In the passive state, the SD counter and its associated octal decoder (LBD 00.03/H3) keeps the modem receive portion in the search mode. When a sync character is detected, SYNDT+ is generated (LBD 00.04/P10) and gated with SDSCH+ and LOOKX+ (LBD 00.04/L7) generating NDXSD+. The SD counter is incremented by 1. The option remains in the sync mode until the DLE character is detected. At this time, the option advances to the SDDLE+ mode.

When the start of text character is received, the data is transferred to the option in a serial fashion and loaded into SR-335 PAC (LBD 00.06/G1 through G4). When the SR-335 PAC is filled with 16 bits, the READY+R flip-flop (LBD 00.04/G6) is set and the assigned DIL line goes to a +6V.

The DMC input mode is enabled and DALRC+ goes to +6V. The data in the SR-335 PAC are routed to the memory via the IOBxx bus.

At the end of a complete message, another DLE character is detected which enables the logic to check the received data for valid message bits. If the data corresponds to the same characters that the receive portion made up, they will generate a CHKO0+ indicating a no error condition.

*Check Sum Generation.* — The check sum logic (LBDs 00.08 through 00.11) is used to express a large arithmetic expression in computer terms. Each output bit is shifted through the output check register generating a 24-bit data pattern which is exclusive of the output data. The input check logic receives the 24-bit output data patterns and compares them with the 24-bit data patterns generated from the input data. If the two 24-bit data patterns are equal, the check sum is correct and CHKO- is at the OV level.

### **Watch Dog Timer Option**

This option generates an interrupt to location 62 at regular intervals and turns CPU power off if it is not reset after the third interrupt. To reset the watch dog timer, an OCP '0026 is executed with the WDT switch on the display panel set to the up position. If the WDT switch is placed in the down position, the watch dog timer is disabled and the interrupts are not generated.

The following discussion describes the watch dog timer operation when an OCP '0026 is executed. The OCP is decoded causing ENMVX+ to go to 0V (LBD 01.02/N5) which resets the  $2^{14}$  binary counter (LBD 01.02/P2 through P4 and D11 through L11). When the OCP is completed, ENMVX+ goes to +6V causing ENMVX- to go to 0V. The MV-335 clock PAC (LBD 01.02/A10) is enabled, generating WDCLK+, a 65 Hz clock pulse, which is applied to the binary counter input (LBD 01.02/N1). If a second OCP '0026 is not executed within two minutes, WDIEN- goes true setting the WDTIN flip-flop (LBD 01.02/C5). WDTIN+ is routed to the main frame generating an interrupt to location 62. The CPU acknowledges the interrupt by generating ACKWD+ which resets the WDTIN flip-flop.

If the watch dog timer is not reset by an OCP '0026 following the first interrupt, the binary counter continues to count and interrupts are generated after six-minutes have elapsed and again after ten minutes. The output from the binary counter conditions an interrupt counter (LBD 01.02/M11 through P11) and after 12 minutes have elapsed without an OCP '0026, the interrupt counter outputs cause WD3PS- to go to 0V. This enables a power down circuit (LBD 01.02/F6 through H6), and the power to the CPU is turned off.

### **Halt Inhibit Logic**

The standard DDP-516 control logic DE (Vol. 3, DDP-516 Instruction Manual/LBD 0.125) is modified for the BB&N IMP system by the addition of the HALT INH switch on the display panel and a gate in the CPU control logic (LBD 03.02). If the HALT INH switch is set to the down position, AIF34E-9 (LBD 03.02/C7) is grounded and the normal halt channels are enabled to execute a halt instruction. When the HALT INH switch is set to the up position, AIF34E-9 is allowed to float disabling the halt logic. With the halt logic disabled, the CPU is prevented from executing a halt instruction except during a power failure. If power failure occurs while the halt logic is disabled, the CPU is allowed to override the halt inhibit logic preventing indiscriminate damage to the program.

### **Sector 1 Memory Lockout**

The memory lockout logic (LBD 03.01) for the BB&N IMP system is a modification of the DDP-516 Control Logic H (Vol. 3, DDP-516 Instruction Manual/LBD 0.126). The main function of this option is to protect sector 1 and locations 60 and 62. This option is enabled via the MEMORY PRTCT switch on the display panel. With the switch in the up position, the write cycle of a memory reference instruction is inhibited if a protected location is addressed and the read-regenerate mode is enabled. Therefore, data read during the read cycle is written back into the addressed location unchanged. To accomplish this function, SLOSW+ is used along with the proper decoding of any address using bit 7 (the 1000 bit), not bits 6, 5, 4, and bank A (the lower 4K of memory) to hold RRCXX- at 0V (LBD 03.01/B4). The protection for locations 60 and 62 is accomplished in a similar fashion.

This option is tested by storing all ONEs in a sector 1 location while the MEMORY PRTCT switch is set to the down position. Then, set the switch to the up position and try to store all ZEROs in the same location. If the option is functioning correctly, the location should still contain all ONEs. Locations 60 and 62 can be checked in a similar fashion.

### **Auto-Restart Option**

The auto-restart option consists of two time delay relays mounted on B9 at top of cabinet and a DPDT switch mounted on the display panel. In addition, the program start logic consisting of two  $\mu$ -PACs are located in A1 of the CPU.

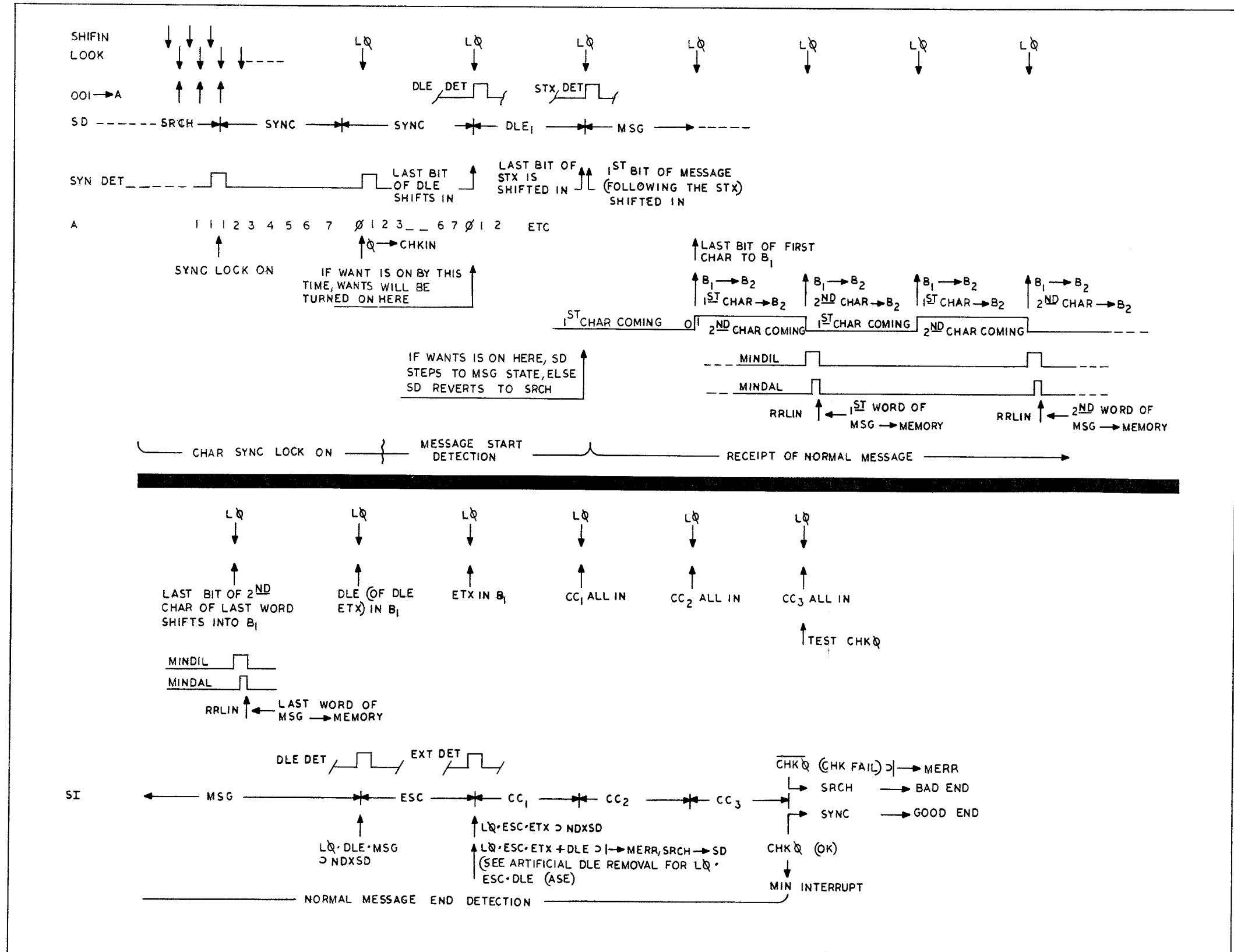


Figure 4-2. IMP-Modem Option --  
Receive Timing Diagram

This option allows complete hands-off power application and program initiation on a ruggedized DDP-516. The DDP-516 must be used in the power failure interrupt mode with a JMP in location 0000<sub>8</sub> to start up the program (customer supplied).

*Modes of Operation.*—This option has two modes of operation which are selected using the AUTO RESTART switch on the display panel. The OFF mode is selected when the switch is placed in the down position and the delayed mode is selected when the switch is placed in the up position. Refer to Figures 4-3 through 4-5 for the following discussions.

*Off Mode.*—In the off mode, the auto-restart option is disabled and normal manual control of power application and program control is allowed.

*Delayed Mode.*—In the delay mode, the two adjustable time delay relays, TD1 and TD2, are wired in cascade with TD1 wired across the load side of the main circuit breaker in the power distribution unit (PDU). When power is applied to TD1, the relay is energized after the adjusted time delay (between 3 and 120 seconds) has been timed out. At the end of the delay, the 24 Vac path to the DDP-516 PDU is completed via a NC contact of TD2 initiating a power on command. At the same time, TD2 is energized starting its time delay. When TD2 times out (adjustable between 1 and 120 seconds), the power on command is removed and a program start (APTX+X+) command is issued to the program start logic located in the main frame. The power on command is removed because the power on circuit is self-latching and the on command must be removed to allow the detection of a power failure.

*Delayed Operation.*—After the first delay, power is automatically applied to the CPU. The internal voltages are allowed to settle and the computer initialization is completed. Then, the instruction in location 0000<sub>8</sub> is automatically executed. If the RUN-SI-MA switch on the control panel is in the RUN position, operations continue as directed by the program. The program may be halted and restarted manually at any time. The manual power control cannot be used in this mode because the auto-restart option will start the CPU automatically after the OFF button has been pressed. If a power failure occurs while the delayed mode is enabled, the CPU is restarted after the adjusted delay has timed out. This delay prevents CPU start up until power has been present for a minimum of three seconds, which allows the power supplies to fully deenergize before turning on again. Therefore, this delay must never be adjusted below three seconds.

#### **IMP-Host Option (See Figure 4-6.)**

The IMP-host option contains the buffering and control necessary to interface the DDP-516 with the host computer interface. The full duplex communication between the DDP-516 and the IMP-host option is performed via the DMC option in parallel while the IMP-host - - host interface is performed serially.

*Transmit Mode.*—The transmit mode is enabled by an OCP '0070 and the appropriate crosspatching OCP. The decoded OCP '0070 generates SETHO- (LBD 02.03/B3) which is gated with HOOPC+ (LBD 02.01/D3) generating STOCP-. The transmit functions are initialized by SNDCP- which is generated by inverting STOCP- (LBD 02.03/E10). SNDCP- also causes STRDY+ to go to +6V (LBD 02.01/C12). The HORDY flip-flop (LBD 02.01/C6) is set by STRDY+, generating the transmit DIL which enables the assigned DMC transmit channel. HODAL+ and RRLIN+ are ANDed (LBD 02.01/B5) generating LDBFR- which strobes the data on the output bus (OTBxx) into the shift register (LBD 02.01/J1 through P11).

The sequence of events for the host transmit mode is timed by signal PULSE+ (LBD 02.01/H5). In the normal transmit mode, RFNIB+A from the host computer interface is ANDed with ENABL+ (LBD 02.02/A10) generating RFNIB+ which triggers the DM-337 PAC to generate PULSE+. In the crosspatch mode, RFNHB+ (LBD 02.02/D2) is used to trigger the DM-337 PAC generating PULSE+. Each PULSE+ generates SHIFT+ (LBD 02.01/B7) which shifts the data out of the shift register as

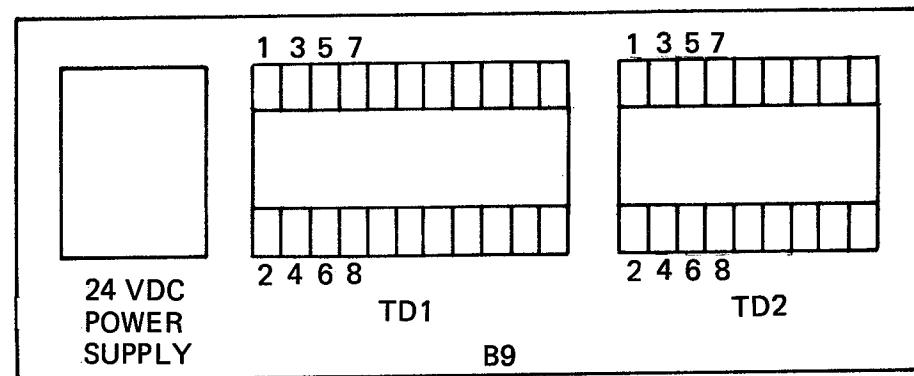
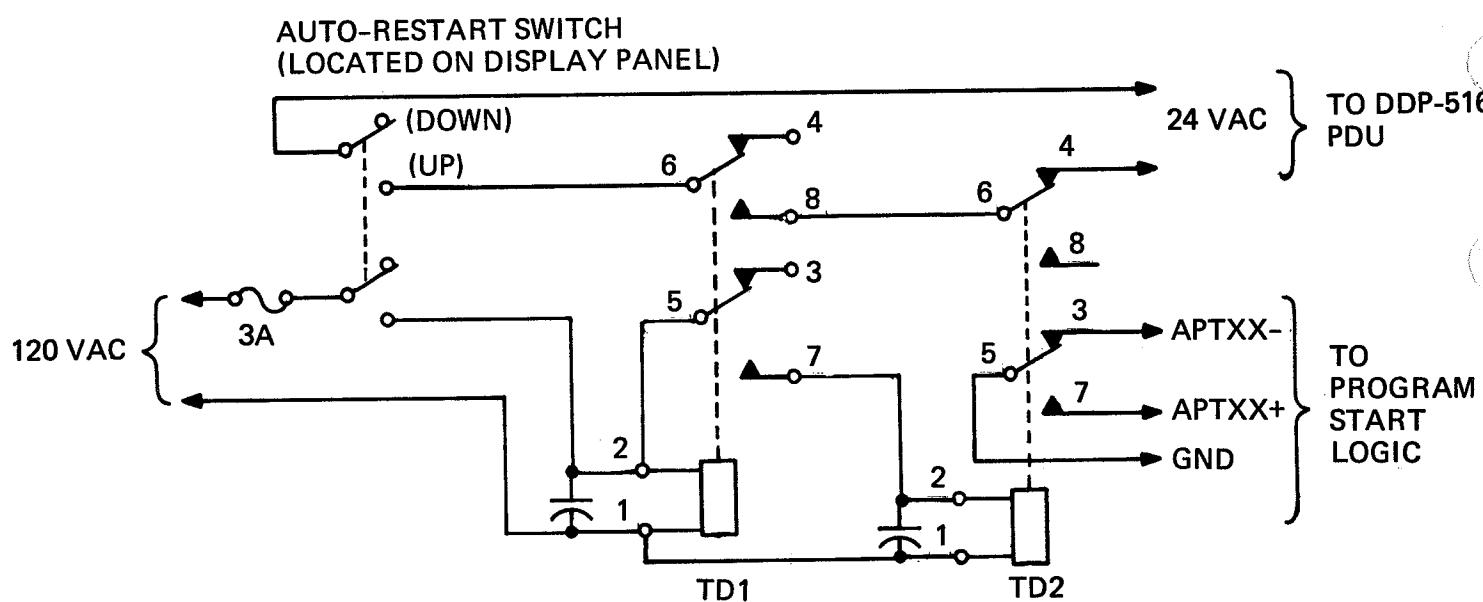


Figure 4-3. Auto-Restart Option Schematic and Layout

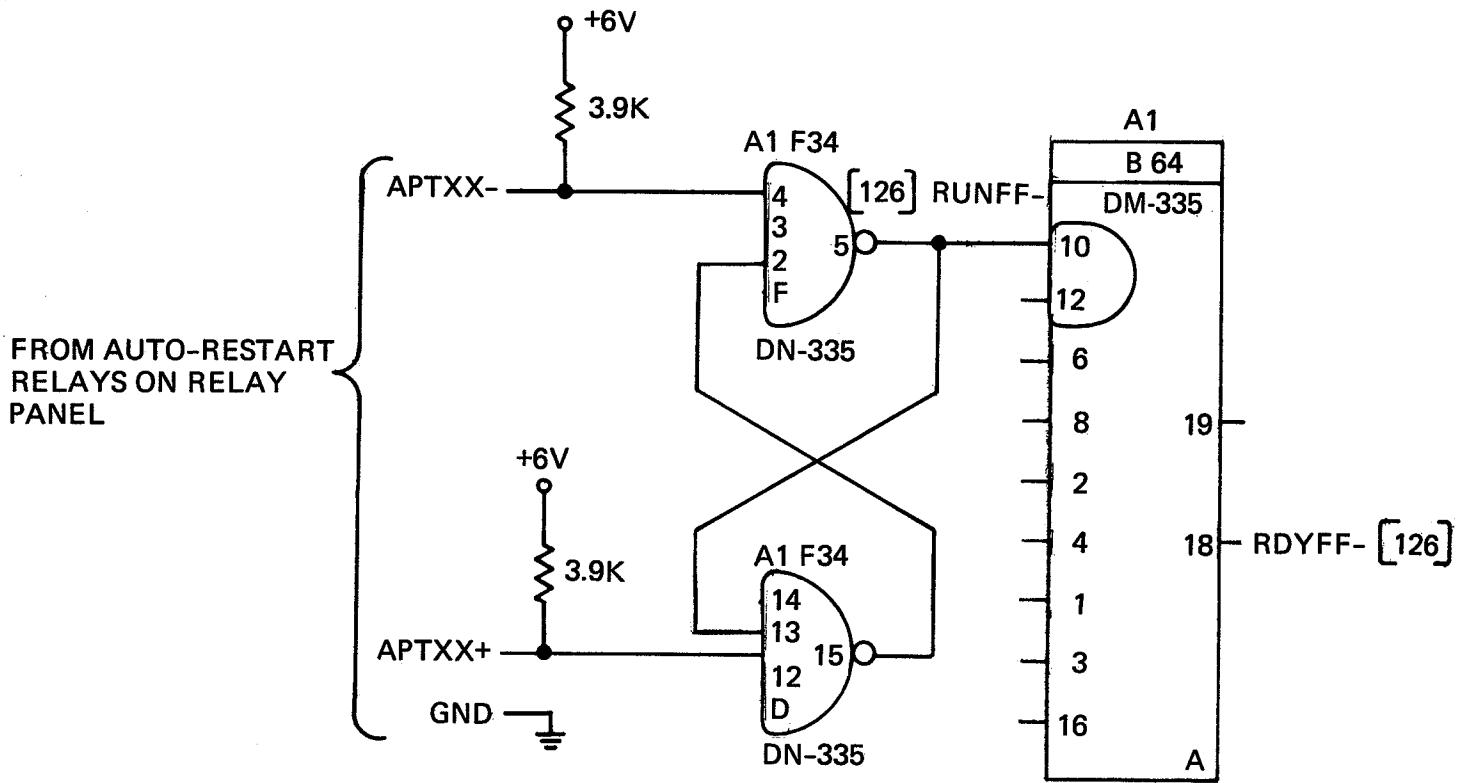


Figure 4-4. Auto-Restart Option -- Program Start Logic

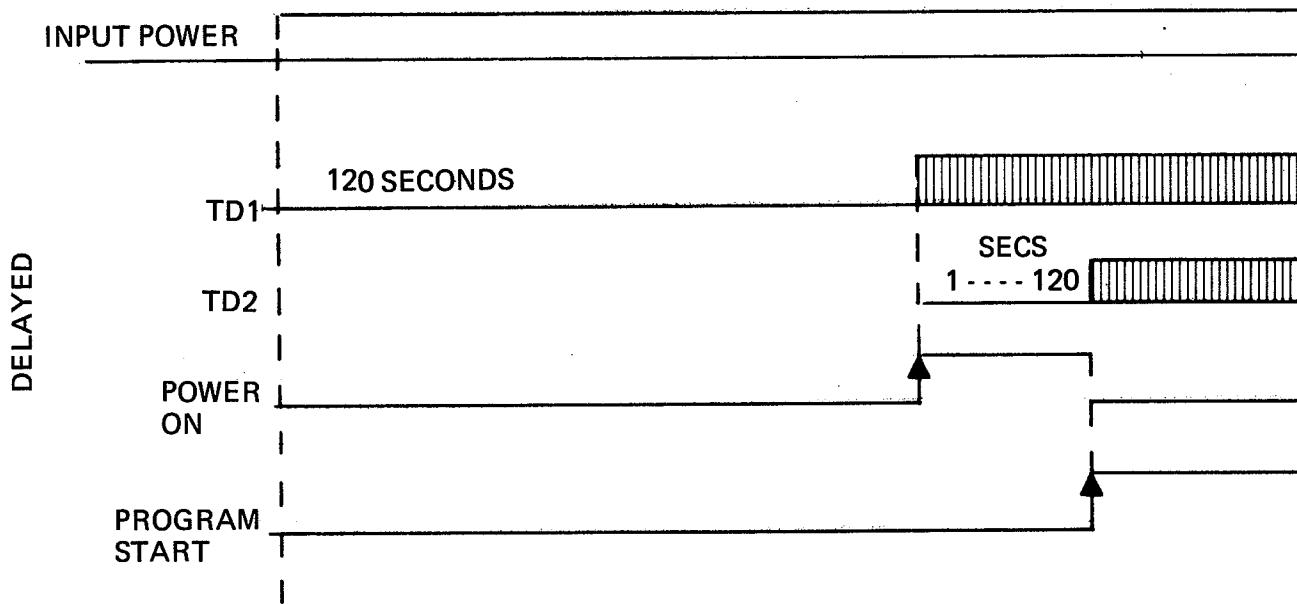


Figure 4-5. Auto-Restart Option – Timing Diagram

DATA0+. This operation continues until the DMC reaches the end of range. At that time, ERLXX+ and HODAL+ are ANDed (LBD 02.01/F3) setting the LSTWD flip-flop. LSTWD+ and ENDHO+ are gated with a count of not zero generating LSHFT+ and setting the LIBIT flip-flop (LBD 02.01/H10). LIBIT+A is routed to the host computer interface indicating the transmission is completed.

*Receive Mode.*—Data from the host computer interface are received in a serial fashion, loaded into a shift register and transferred into the DDP-516 CPU in a parallel fashion when the shift register is filled. If the logic is ready to receive a bit, RFNHB+A (LBD 02.02/F2) is generated and routed to the host computer interface. Chain delay multivibrators (LBD 02.02/D6 through H6) are triggered by RFNHB+. The incoming bit, HSDTA+, is received from the host computer interface and gated with ENABL+ (LBD 02.02/A8) generating DATA1+. This signal is gated with HOEOM- and the resultant signals condition the shift register inputs (LBD 02.02/L2). DELYA- is inverted generating SHAET+ (LBD 02.02/A11) which shifts the data in the shift register and increments the transfer counter (LBD 02.02/B11 through G11). After receiving 16 bits, the ANDing of TZERO+ and DELYB+ generates STIRD+ (LBD 02.02/M12) which sets the HIRDY flip-flop (LBD 02.02/E8) and generates the receive DIL. The DMC channel is enabled, and the transmit DAL generates DALIN+A (LBD 02.03/J2). The outputs from the shift register are routed to the input gating logic (LBD 02.02/N2 through P10) and DALIN+A gates the data onto the input bus (INBxx).

When the last host bit is transferred, LHBIT+A is received. After ANDing LHBIT+A with ENABL+ (LBD 02.02/A5), LHBIT- goes to 0V and the FIXXX flip-flop (LBD 02.02/E4) is set by DELYA+. The next DELYA+ pulse resets the FIXXX flip-flop and sets the HOEOM flip-flop (LBD 02.02/G4). The input gating logic to the shift register is disabled inhibiting any valid incoming data. The HOEOM signal also sets up conditions for a priority interrupt and the program performs an indirect JST instruction to location 100.

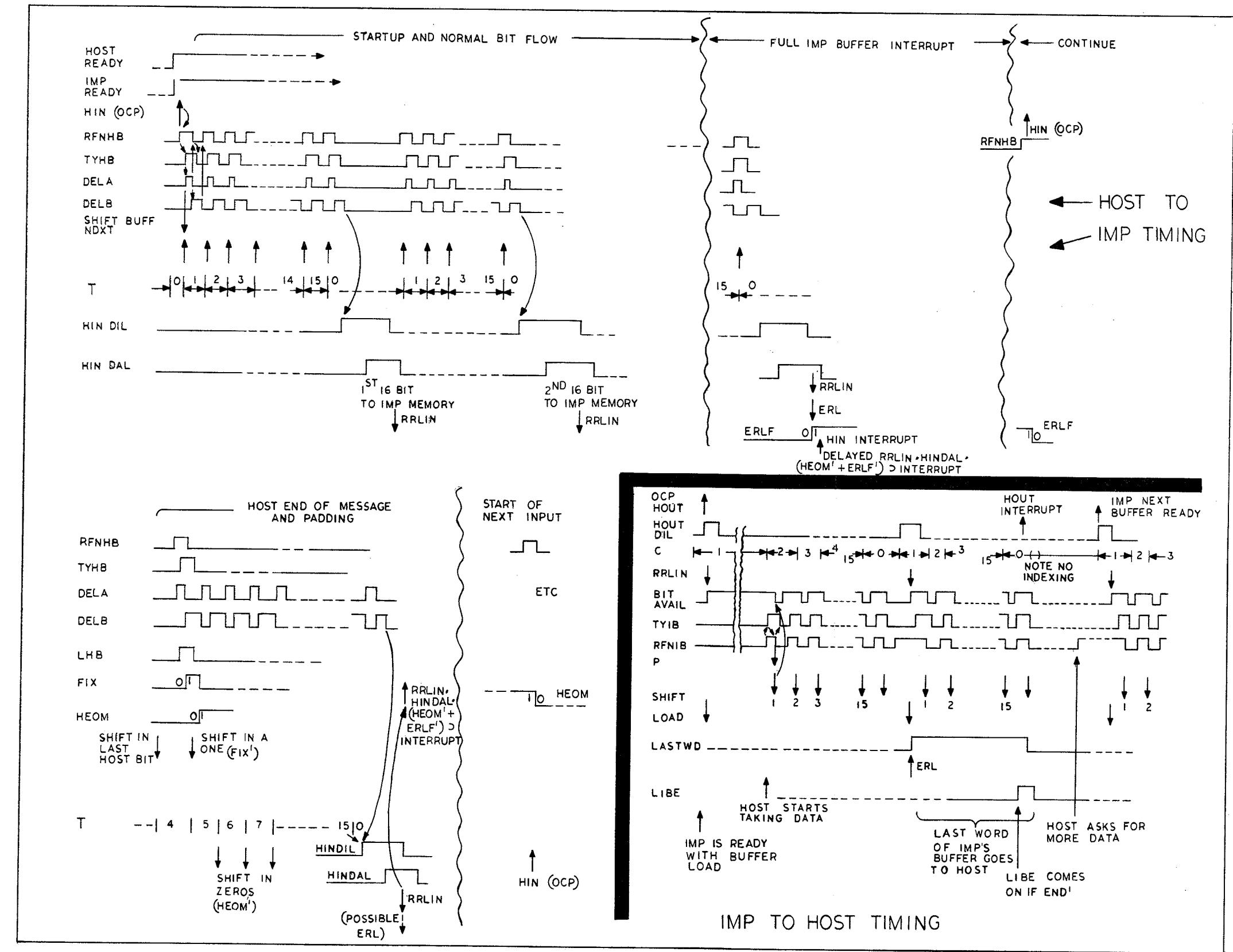


Figure 4-6. IMP Host Option  
Timing Diagram

*Padding Operations.*—Since the IMP-host option must be compatible with host computers of varying word lengths, padding logic has been provided to complete incoming data words. When LHBIT- goes true, the FIXXX flip-flop is set by DELYA+ causing FIXXX- to go to 0V. The input logic to the shift register is conditioned for a ONE transfer by FIXXX-, SHACT+ shifts the shift register and a ONE is loaded into the shift register. The next DELYA+ resets the FIXXX flip-flop causing the HOEOM flip-flop to be set. FIXXX- goes to +6V, the shift register is conditioned for a ZERO transfer, the input to the shift register is conditioned for a ZERO transfer, and ZEROs are shifted into the shift register to complete the data word.

## SECTION V FUNCTION LISTS

The four tables included in this section contain the signal mnemonics used on the system LBDs. Table 5-1 lists the IMP-modem signals, Table 5-2 lists the RTC, WDT, and display signals, Table 5-3 lists the IMP-host signals, and Table 5-4 lists the memory lockout and nonhalt signals.

**TABLE 5-1.  
IMP MODEM MNEMONIC LIST**

<b>Signal</b>	<b>LBD No./Source</b>	<b>Definition</b>
OCPLS	00.12/F5, F10	Output control pulse
OEOxx	00.08	Output check register exclusive ORs
ONETA	00.04/B8	One's to the A-counter
ONLXP	00.07/L5	On-Line cross patch
ONMXP	00.07/L7	Modem cross patch
OTBxx	00.12/D2--F10	Output transfer bus, bits 1 through 16
OTPxx	00.09/B2--P10	Output check register outputs
OTPLS	00.12/D5, D10	Output pulse
IEOxx	00.10/B2--K7	Input check register exclusive ORs
INBxx	00.06/L2--P11	Input transfer bus, bits 1 through 16
INPxx	00.11/B2--P10	Input check register outputs
1TOSD	00.05/B12	ONE to the SD counter
2NDCH	00.04/D10	Second character flip-flop
A0000	00.03/E1	A counter first bit
A0001	00.03/G1	A counter second bit
A0002	00.03/J1	A counter third bit
ADBxx	00.12/D2--G4	
ADBxx-A	00.07/B3--D12	Address bus, bits 7 through 16
ADDRX	00.07/J2	
B100x	00.06/B1--B4	Input register bits, first word
B200x	00.06/H1--H4	Input register bits, second word
C0000	00.03/A4	Bit 1 of bit counter
C0001	00.03/C4	Bit 2 of bit counter
C0002	00.03/E4	Bit 3 of bit counter
CHK00	00.10/P2	Check register O.K.
CKTAA	00.12/K2	
CKTBA	00.08/P11	Transmitted data
CKTBB	00.12/K2	Received data
CKTCA	00.12/K2	Unused
CKTCB	00.12/K2	Unused
CKTCC	00.12/K2	Unused
CKTDB	00.12/K4	Transmit clock
CKTDD	00.12/K4	Receive clock
CKTXP	00.08/P5	Data set crosspatch
CLCHO	00.08/K11	Clear output check register
CLCHI	00.10/G11	Clear input check register
CLRB2-A	00.04/K2	Clear input register
CLRR2	00.01/P2	Clear transmit register
CLTBR	00.01/E6	Clear total transmit buffer
CMKXX	00.12/D4	Clear mask
DILxx	00.12/H2--H5	Data interrupt line to DMC
DALxx	00.12/H2--H5	Device address lines from DMC
DALRC	00.05/P11	Receive DAL from DMC
DALTN	00.07/P9	Transmitted DAL from DMC

**TABLE 5-1. (CONT)**  
**IMP MODEM MNEMONIC LIST**

Signal	LBD NO./Source	Definition
DATOT	00.08/P10	Data out
DATIN	00.04/E3	Data in
DCRMT	00.03/A7	Decrement SD counter
DLED C	00.04/P8	DLE detect, receiver
DLED T	00.01/M4	DLE detect, transmitter
DRLIN	00.07/P6	Data request line
ERLTN	00.01/J11	Transmit end of range
ERLXX	00.07/P5	End of range
ETXDT	00.04/N2	End of text detect
FFFFF	00.01/P4	Used for false DLE detection
FSTLD	00.01/P11	First load flip-flop
G0000+	00.01/F5	Bit counter at zero, transmit
G0000-	00.03/F5 }	
G0007	00.03/G3	Seventh bit indicator, transmit
GOBIT	00.01/H4	Enables transmit buffer strobe
GMABX	00.01/J2	Give me a bit
L0000	00.03/H9	A-counter zero, L00KX true
L00KX	00.05/C6	1 $\mu$ s delayed character detection
LD816+	00.02/P2	Enable second 8 bits of transmit buffer to S.R.
LD816-	00.02/P5	Enable first 8 bits of transmit buffer to S.R.
LDLDE	00.01/C10	
LDGP1	00.01/F8	Load group 1
LDGP2	00.01/H12	Load group 2
LDSTR	00.01/H5	Load strobe
LDSTX	00.01/C11	Load start-of-text character
LDSYN	00.01/C4	Load sync character
LDTBR	00.01/P10	Load total buffer register
LXPXX	00.01/N9	Line crosspatch
MOINT	00.01/H10	PI enable for transmit
MODOT	00.07/L3	Enables transmit
MODIN	00.07/L8	Enables receive
MODCP	00.07/B1	Modem command pulse
MINCP	00.04/J10	Modem input command pulse
MDRCL	00.05/C1	Same as receive clock
MDTCL	00.01/A1	Inverted transmit clock
MERRX	00.05/L5	Modem error flip-flop
MNINT	00.04/K12	Receive interrupt to PI
MPRST	00.07/L4	Modem reset pulse
MSGLO	00.04/B10	Coincidence of message mode and L0000
MSGSN	00.01/C7	Transmit mode, not sync or message mode
MSTCL	00.12/D5, D10	Master clear
MXPXX	00.01/M9	Modem crosspatch
NDXSD	00.05/P7	Index (step) SD counter
PIL00	00.12/D3, D8	Program interrupt line
PARCH	00.12/G4, G9	
PRCLR	00.07/P11	Generate SHFIN when not in X patch
PRCLT	00.07/K11	Generate GMABX when not in X patch
PREST	00.01/F9	Reset signal
PWRFL	00.12/D4, D10	Power failure signal
R200x	00.02/A12-N12	Transmit reg flip-flops
R2SHF	00.01/C3	Shift for false DLE detection
RCCLK+A	00.05/P9	Receive clock divided by 2
RCCLK-	00.05/D3	Receive controller clock
RDATA	00.04/B3	Receive data
READY+R	00.04/G7	Receive DIL to DMC
READY+T	00.01/J7	Transmit DIL to DMC
REQOT	00.01/P6	Request out
RESET	00.01/C5	Either PREST- or MSTCL-
RRLIN	00.07/P7	Reset ready line
RSERL	00.03/G12	Load "1" to transmit register bit

**TABLE 5-1. (CONT)**  
**IMP MODEM MNEMONIC LIST**

Signal	LBD No./Source	Definition
RTERL	00.03/D12	Resets ERLTN flip-flop
SC000	00.03/E10	Transmit mode counter bit 1
SC001	00.03/G10	Transmit mode counter bit 2
SC002	00.03/J10	Transmit mode counter bit 3
SCCC1	00.03/M9,J9	First check word (transmit)
SCCC2	00.03/M10,J6	Second check word (transmit)
SCCC3	00.03/M12, J6	Third check word (transmit)
SCDLE	00.03/M3, J5	DLE mode (transmit)
SCETX	00.03/M7, J6	End of text mode (transmit)
SCMSG	00.03/M6, J6	Message mode (transmit)
SCSTX	00.03/M4, J6	Start of text mode (transmit)
SCSYN	00.03/M2, J5	Sync mode
SD000	00.03/C6	Receive mode counter bit 1
SD001	00.03/E6	Receive mode counter bit 2
SD002	00.03/G6	Receive mode counter bit 3
SDCC1	00.03/P10, J4	First receive check word
SDCC2	00.03/P12, J4	Second receive check word
SDCC3	00.03/P1, J3	Third check word
SDCCT	00.08/P8	Enables third check word (transmit)
SDDLE	00.03/P6, J4	DLE mode (receive)
SDESC	00.03/P9, J4	Receive escape mode (receive)
SDMSG	00.03/P7, J4	Message mode (receive)
SDSCH	00.03/J3, P3	Search mode (receive)
SDSYN	00.03/P4, J4	Sync mode (receive)
SERLX	00.01/L11	Set at end of range — load group 2
SHCHK	00.09/N12	Inverted GMABX- to clock output check register
SHFIN+	00.05/G2	
SHFIN+A	00.05/M3 } SHFIN-	Shift input pulse
SHFB2	00.05/J2	
SHFB2	00.05/J3	Shifts 16 bit SR335
SMK01	00.12/F5, F10	SMACK 120
SMKXX	00.12/F5, F10	Set mask flip-flop
SNCC3	00.01/D11	Sync or CC3 transmit mode
SNREQ	00.01/J9	Sync req.
SPARE	00.12	Spare I/O pin
STBIN	00.04/E8	Strobe input
STERR	00.05/J4	Set error flip-flop
STXDT	00.04/N5	Start of text detect
SYNDT	00.04/N10	Sync detect
TNCLK	00.01/D2	Transmit clock
TRBxx	00.02/B2—N5	Transmit buffer 1—16 bits
VDC00-x	00.12/D5, G5	-6 volts I/O bus
VDC06-x	00.12/D5	-6 volts I/O bus
WANTS	00.05/P2	Coincidence with 2NDCH and MSGLO to generate DIL
WANTX	00.04/K10	Set by modem input command pulse
XPCLK	00.01/E3	Crosspatch clock

**TABLE 5-2.**  
**RTC, WDT, DISPLAY MNEMONIC LIST**

Signal	LBD No./Source	Definition
OCPLS+	01.02/D7	Output control pulse, inverted
OCPLS-	01.06/D4, D10	Output control pulse
OCPWD	01.02/B8, L2	OCP Watchdog timer
OTBxx	01.06/D2-G10	Output transfer bus, bits 1 through 16
INBxx	01.01/E10-P11	Input transfer bus, bits 1 through 16
ADBxx	01.06/D2-G10	Address bus, bits 7 through 16
ADDRX	01.01/F4	Address
ADOCP	01.01/G5	Address OCP
CLOCK	01.01/H3	Clock
CLOCK±A	01.01/A12	Clock
CNTxx	01.01/D10-D12	Count
DELAY	01.01/M2	DRLIN inhibit
DRLIN-	01.01/E7,F2	Data request line
DSLxx	01.03/C3-P8	Display shift register outputs
ENABL	01.01/D2	Clock enable
ENMVX	01.02/N5	Enable multivibrator
LDBFR	01.03/H12-M11	Load buffer
LGTxx	01.04/B2-M7	Lamp gates
PIL16	01.01/H6	Priority interrupt line 16
RRLIN	01.06/D4-D10	Reset ready line
RTCLK	01.01/M7	Real time clock
TNSEC	01.02/P3	Four second timer pulse
WD3PS	01.02/P11	Watchdog timer third countdown
WDADR	01.02/F3	Watchdog timer address
WDCLK	01.02/B11	Watchdog timer clock
WDIEN	01.02/L8	Watchdog interrupt enable
WDTIN	01.02/C5	Watchdog timer interrupt

**TABLE 5-3.**  
**IMP TO HOST MNEMONIC LIST**

Signal	LBD No./Source	Definition
OCPLS	02.03/H6 & H12	OCP from 516
OTBxx	02.03/H4 through L12	Lines from output bus
IMRDY	02.03/N2	I'm ready
INBxx	02.02/N1 through P10	Lines to input bus
ADBxx	02.03/H4 through L12	Lines from address bus
BTAVL	02.01/F7	Bit available
CTZRO	02.01/E10	Bit counter set to zero
CZPLS	02.01/B8	Generates SHIFT when CTZRO is false
DALIN+A	02.03/J2	DAL input-receive
DATAO	02.01/P10	Output data
DATAI	02.02/A9	Host data in
DELYA	02.02/E6	Initiates the 1 for padding
DELYB	02.02/H7	Enables RFNHB
DLAOS	02.03/B5	Delay A zero set
DRLIN	02.03/C10	Data ready line
ENABL	02.01/F12	Data enable
ENDHO	02.01/H2	End/host transmission
ENDRS	02.01/G4	End host transmission
ERLIN	02.02/G1	End-of-range line
F1xxx	02.02/E4	Flip-flop to add 1 to host word for padding
HOADD	02.01/C4	Host address
HOEOM	02.02/G4	Sets zeros into input register for padding
HOOPC	02.01/C2	Host OCP
HORDY	02.01/C5	Host ready (DILxx)
HIRDY	02.02/F9	Host input ready (DILyy)
HPLIN	02.03/C8	Host priority interrupt line
HSTAD	02.03/B3	Host address
HSTEN	02.02/J9	Host enable
HUPAD	02.02/B3	Host unpatch address
HXPAD	02.02/B3	Host crosspatch address
HXPCH	02.02/L10	Host crosspatch flip-flop
LIBIT	02.01/H10	Last IMP bit
LDBFR	02.01/B5	Load output buffer
LHBIT	02.02/A5	Last host bit
LSHFT	02.01/F9	Last shift
LSTWD	02.01/H3	Last word
NDOCP	02.01/G1	End output control pulse
NDXCT	02.01/B11	Output data shift count pulse
PILOT	02.01/E4	Transmit priority signal
PULSE	02.01/H5	Generated by RFNIB and used to generate SHIFT
RIRDY	02.02/C10	Reset receive interrupt
RFNIB	02.02/A10	Ready for next IMP bit
RFNHB	02.02/C2	Ready for next host bit
RRLIN	02.03/H6 & H12	Reset ready line
RSTIR	02.02/G9	Receive standard interrupt enable
RSTLW	02.01/D8	Reset last word flip-flop
SETH0	02.03/B2	Set host output
SETH1	02.03/B2	Set host input
SETND	02.03/B3	Set end of transmission
SHIFT	02.01/B8	Shift data out
SHACT	02.02/A11	Shift input shift register
SHDCP	02.03/F11	Set data counter
SRNHB	02.02/P11	Set ready for next host
STOCP	02.01/E2	Set output
STICP	02.02/A1	Set input
STIRD	02.02/M12	Set interrupt
STRDY	02.01/C12	Clear output shift register
TYIMB+A	02.01/H7	There's your IMP bit
TYHBX	02.02/A7	There's your host bit
TZERO	02.02/J11	Input bit counter @ zero
XMTOT	02.03/H8	Completes circuit in host to show IMP is ready
XMTXN		

**TABLE 5-4.**  
**MEMORY LOCKOUT AND NONHALT MNEMONIC LIST**

Signal	LBD No./Source	Definition
OPGNS	03.02/B11	Op group, negative sum
OPGWR	03.01/F7	Op group, read/write control
INCSC	03.01/M4	Increment shift counter if not 00 <sub>8</sub>
AZERO	03.01/P9	A-register equals zero
AZZZZ	03.02/L10	General control flip-flop
CLDTR	03.02/J5	Clear D-register to ONEs
CLETR	03.02/J2	Clear E-register to ONEs
CLFTL	03.02/J7	Clear F-register
CLRDR	03.01/P1	Clear D-register when master clock stops
DGONE	03.01/B10	D-register equals zero
DMCUP	03.02/L5	DMC up
DRFLP	03.02/E7	Device ready flip-flop
EICHL	03.02/F9	Enable ONE to shift counter bit 11
EICTS	03.02/J8	Enable ONE's to shift counter
EIDTS	03.02/J6	Enable input bus to D-register
EBETS	03.02/L1	Enable B-register to E-register
ECETS	03.02/L3	Enable shift counter to E-register (11-16)
EMCTL	03.02/L11	Enable M-register to shift counter (11-16)
ESDTS	03.02/L4	Enable adder sum to D-register
MEMCI	03.01/J12	Memory cycle initiate
PIL00	03.01/F3	Priority interrupt line
RDYFF	03.01/D3	Ready flip-flop
RPTT2	03.01/H7	Repeat TL2 timing level
RRCXX	03.01/B4, K5, M8	Read-regenerate cycle control to memory
RUNFF	03.01/M3	Run control flip-flop
SETA0	03.02/D9	Set A00FF control signal
SETAZ	03.02/H5	Set AZZZZ control signal
SLOSW	03.01/A4	Sector lockout switch
START	03.01/D4	Start PB switch release
WRINH	03.01/D9	Write inhibit

## SECTION VI LOGIC BLOCK DIAGRAMS

The logic block diagrams listed in Tables 7-1 through 7-4 are contained in this section.

**TABLE 6-1.  
IMP-MODEM LBD LIST**

<b>LBD No.</b>	<b>Title</b>	<b>Dwg No.</b>
00.01	Transmit Control — IMP to Modem	C70252920
00.02	Transmit Register — IMP-Modem	C70252921
00.03	IMP-Modem Counters	C70252922
00.04	Receive Controller — IMP-Modem (Sheet 1 of 2)	C70252923
00.05	Receive Controller — IMP-Modem (Sheet 2 of 2)	C70252924
00.06	Receive Input Register and Bus IMP-Modem	C70252925
00.07	Address Decoding and DRL Address 71-76 IMP-Modem	C70252926
00.08	Output Check Register IMP-Modem Interface	C70252927
00.09	Output Check Register IMP-Modem Interface	C70252928
00.10	Input Check Register IMP-Modem Interface	C70252929
00.11	Input Check Register IMP-Modem Interface	C70252930
00.12	IMP-Modem Connectors	C70252931
00.13	IMP-Modem PAC Layout	C70252932

**TABLE 6-2.  
RTC, WDT AND DISPLAY LBD LIST**

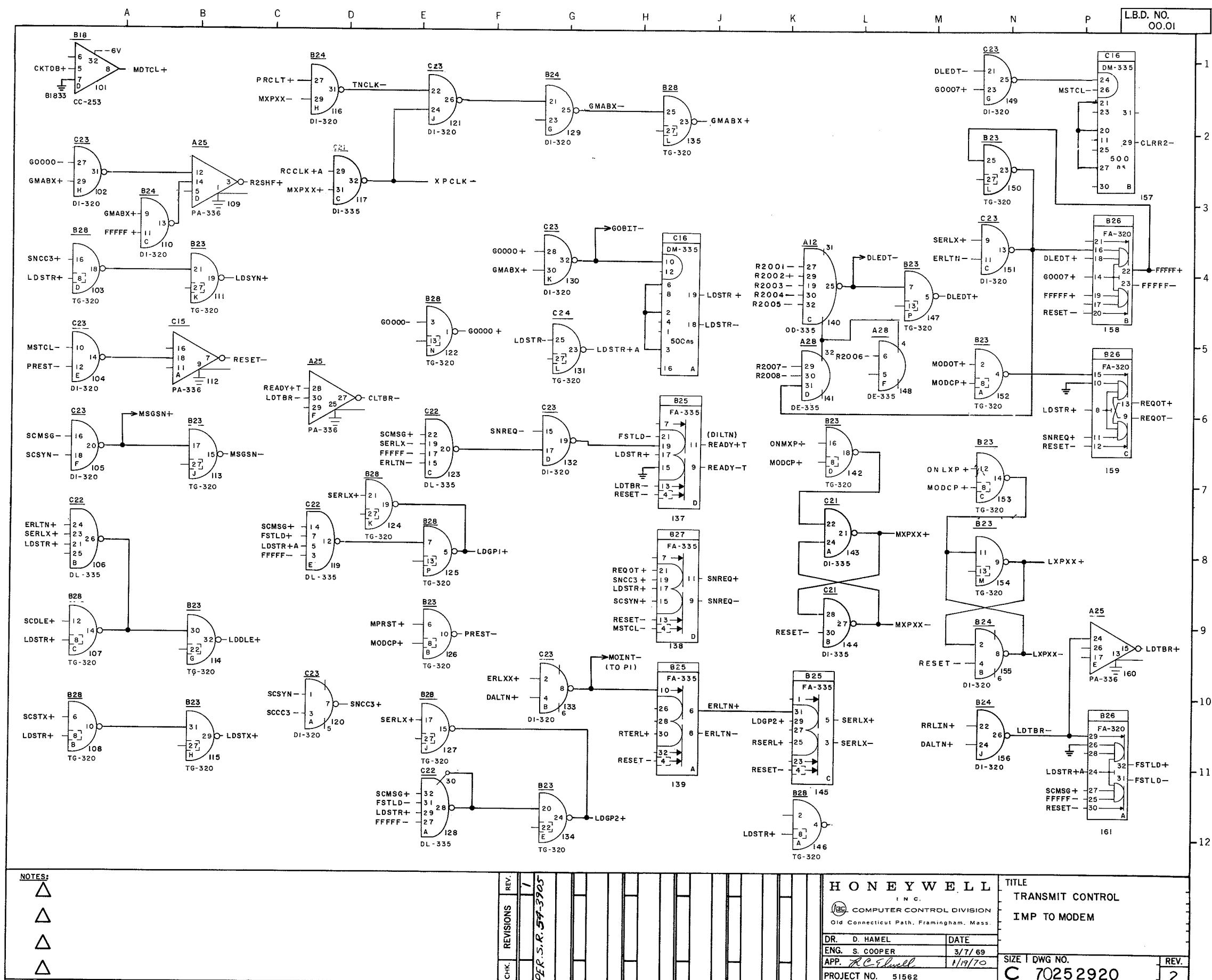
<b>LBD No.</b>	<b>Title</b>	<b>Dwg No.</b>
01.01	Real Time Clock Address 0040-1040 OCP Interrupt Address 41	C70252939
01.02	Watch Dog Timer and Display Control Logic Address 0026	C70252940
01.03	Display Register	C70252941
01.04	Display Lamp Drivers	C70252942
01.05	RTC, WDT and Display Logic PAC Layout	C70252943
01.06	Connectors	C70252944

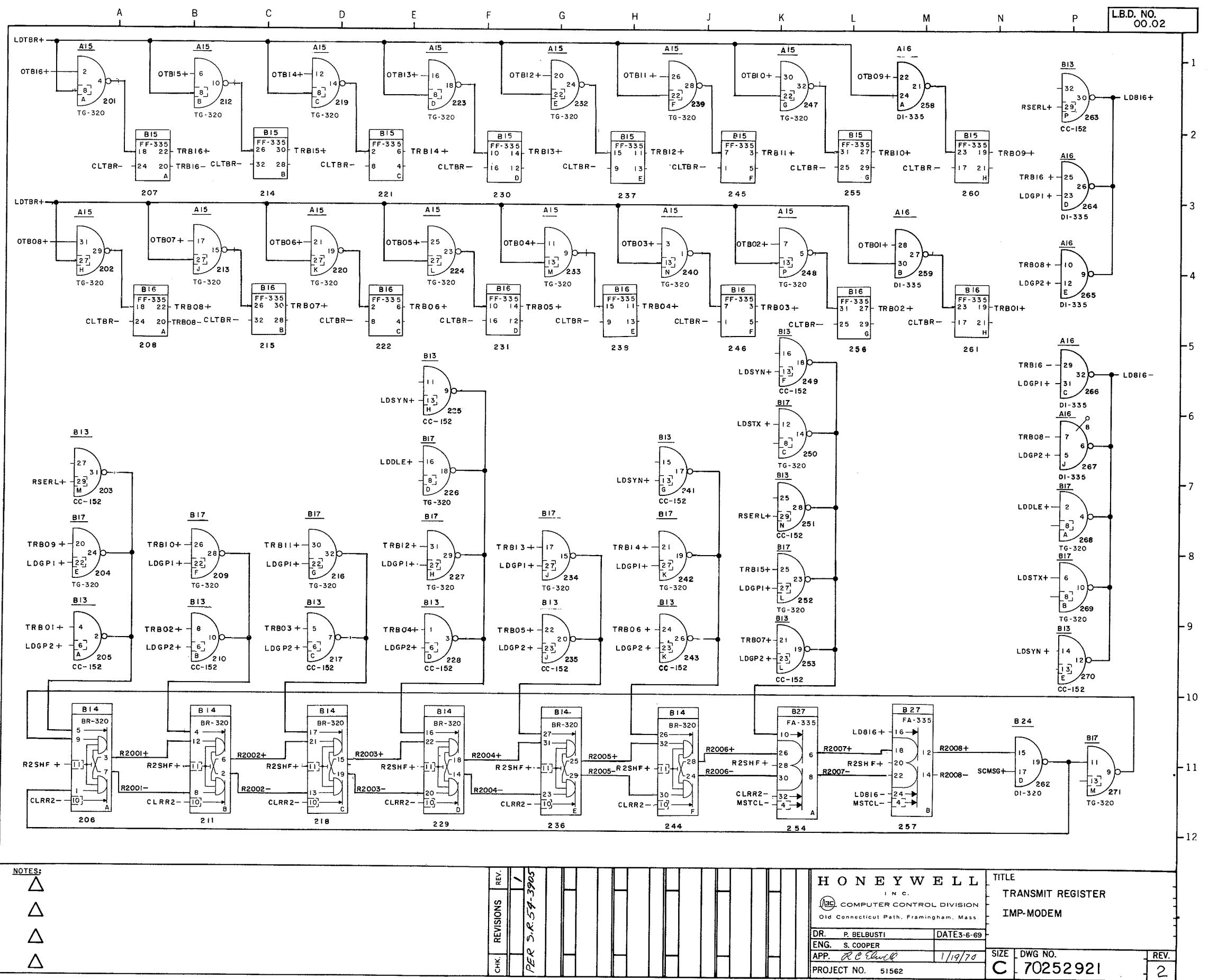
**TABLE 6-3.  
IMP-HQST LBD LIST**

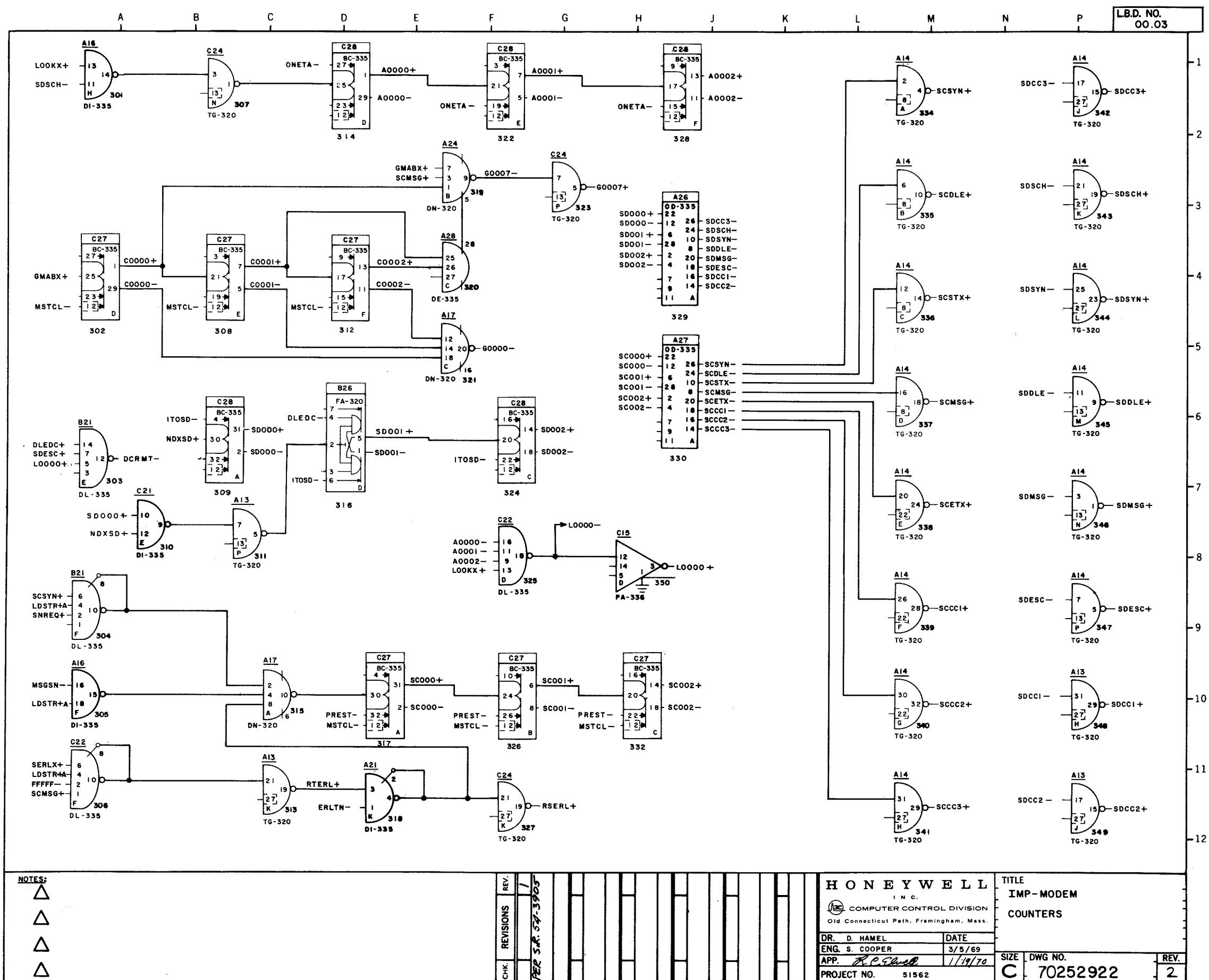
<b>LBD No.</b>	<b>Title</b>	<b>Dwg No.</b>
02.01	IMP-Host Output Control Logic and Buffer	C70252899
02.02	Host-IMP Input Control and Buffer	C70252900
02.03	Address Decoding PIL, DRL & Cabling IMP-Host	C70252901
02.04	IMP-Host PAC Layout	C70252902

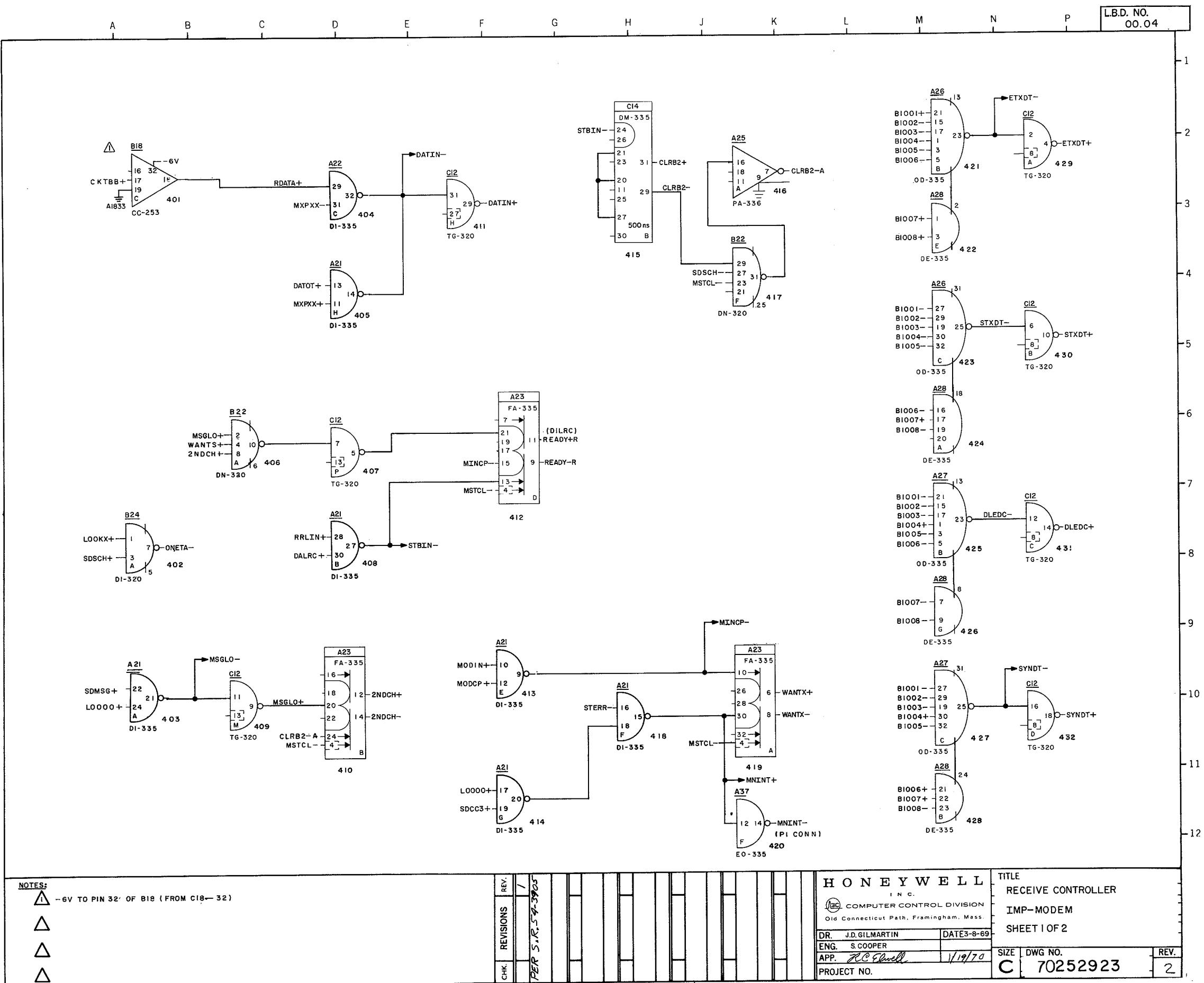
**TABLE 6-4.  
MEMORY LOCKOUT AND NONHALT LBD LIST**

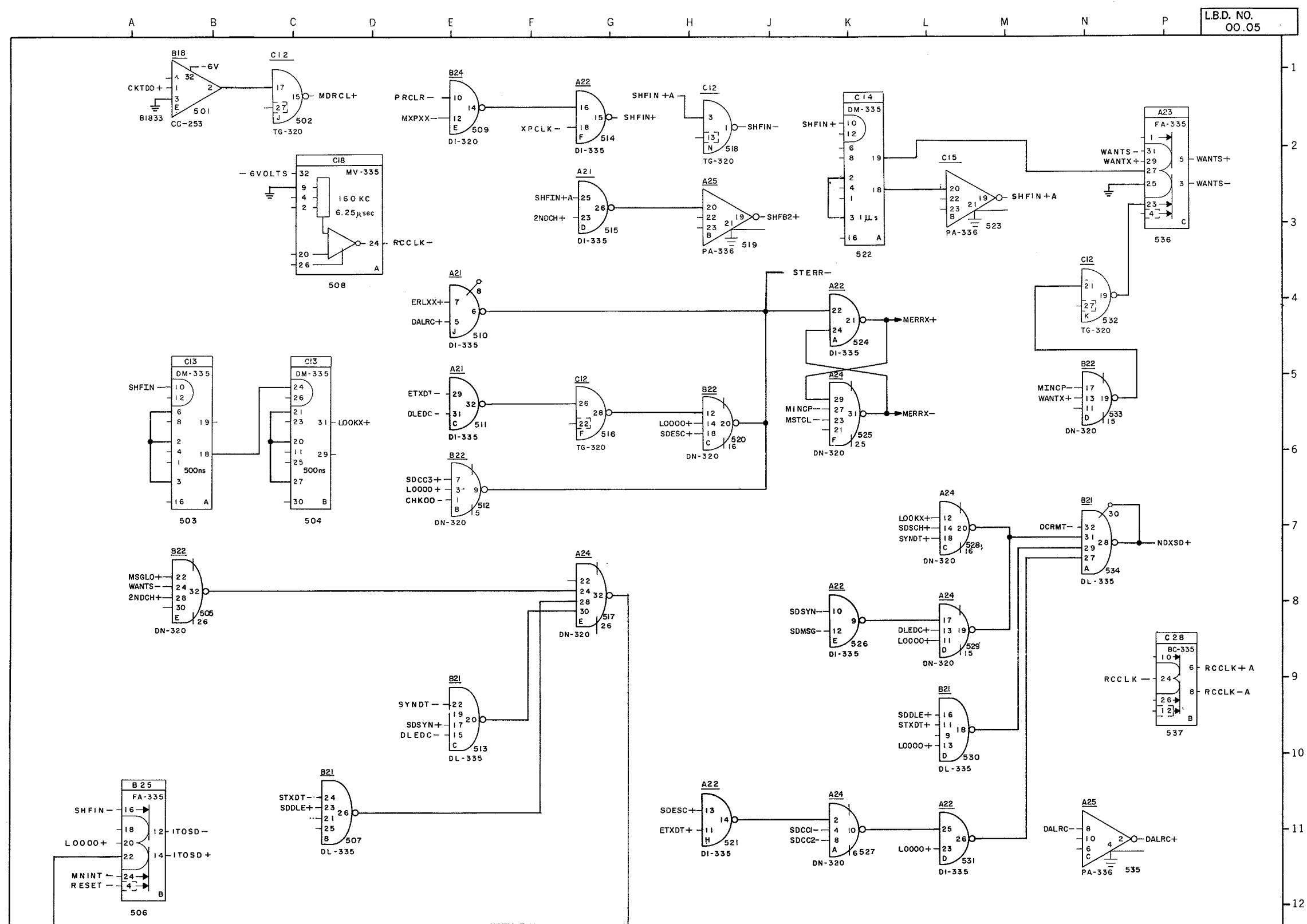
<b>LBD No.</b>	<b>Title</b>	<b>Dwg No.</b>
03.01	Memory Lockout	C70254130
03.02	Nonhalt Special	C70254084











**NOTES:**



	REVISIONS	REV.
	CHK.	

HONEYWELL

**I N C.**  
**JEC COMPUTER CONTROL DIVISION**

Old Connecticut Path, Framingham, Mass.

ENG.	S. COOPER	
APP.	R.C. Elwell	1/19/70

PROJECT NO. 51562

LE

## RECEIVE CONTROLLER

#### **TMP-MODEM**

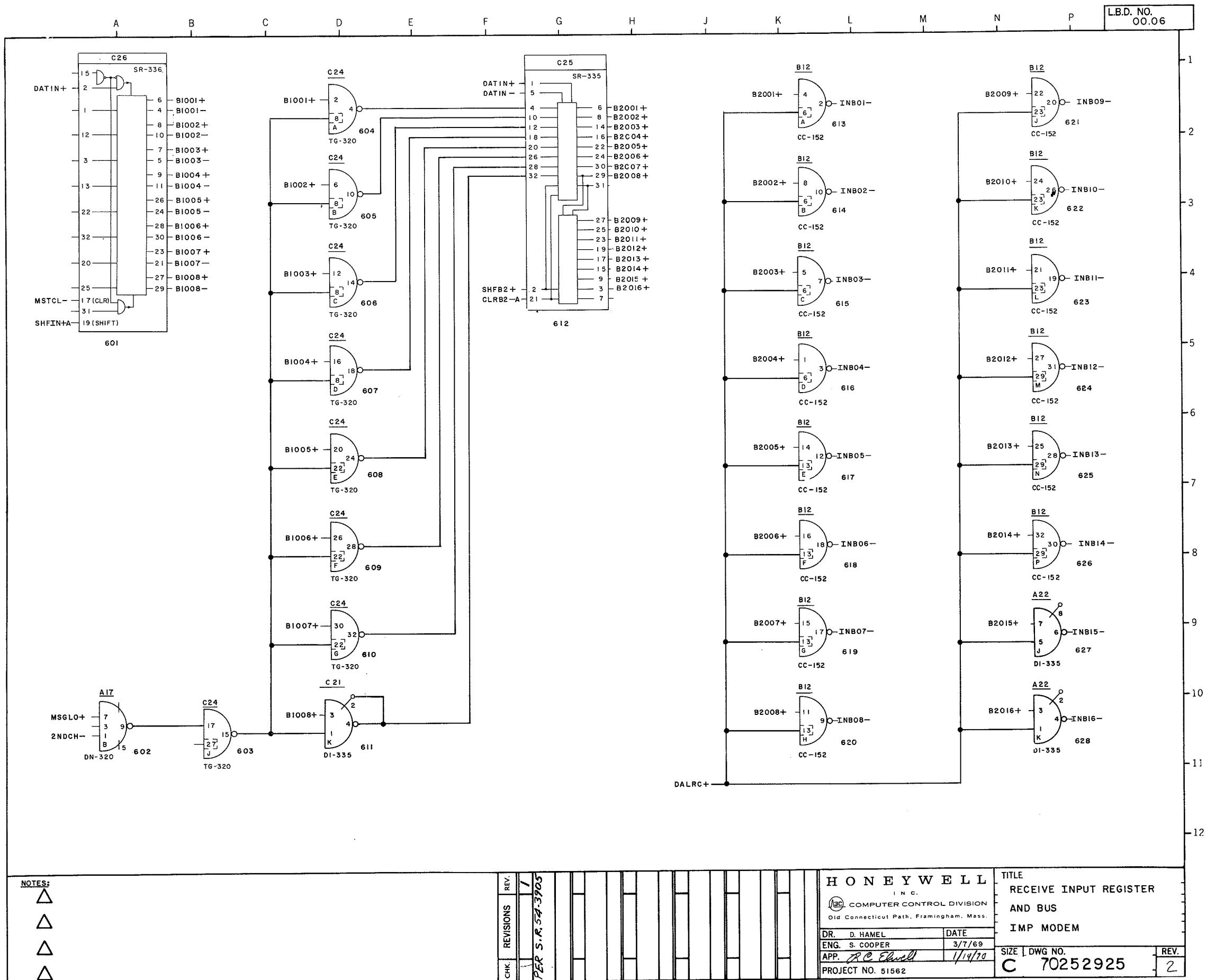
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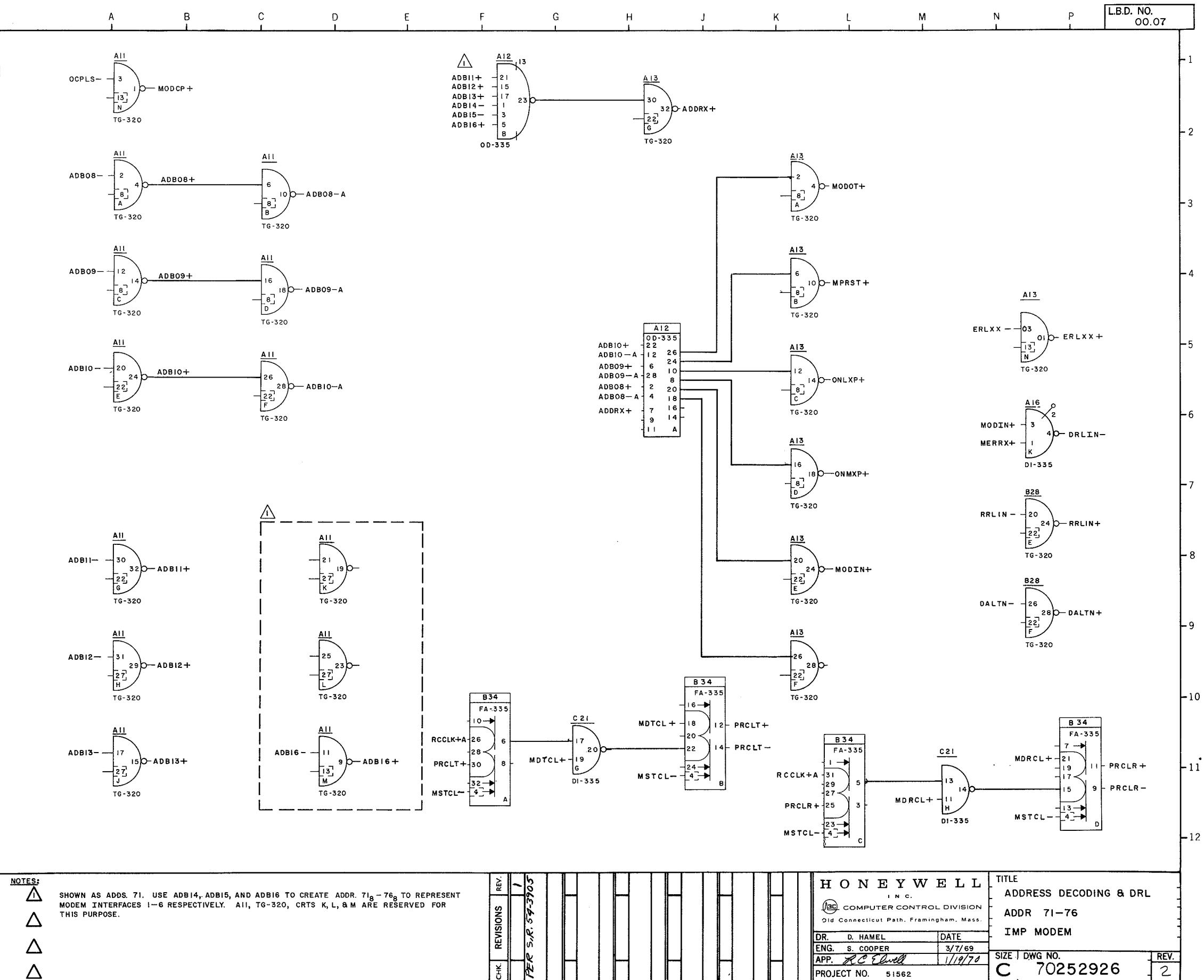
SHEET 2 OF 2

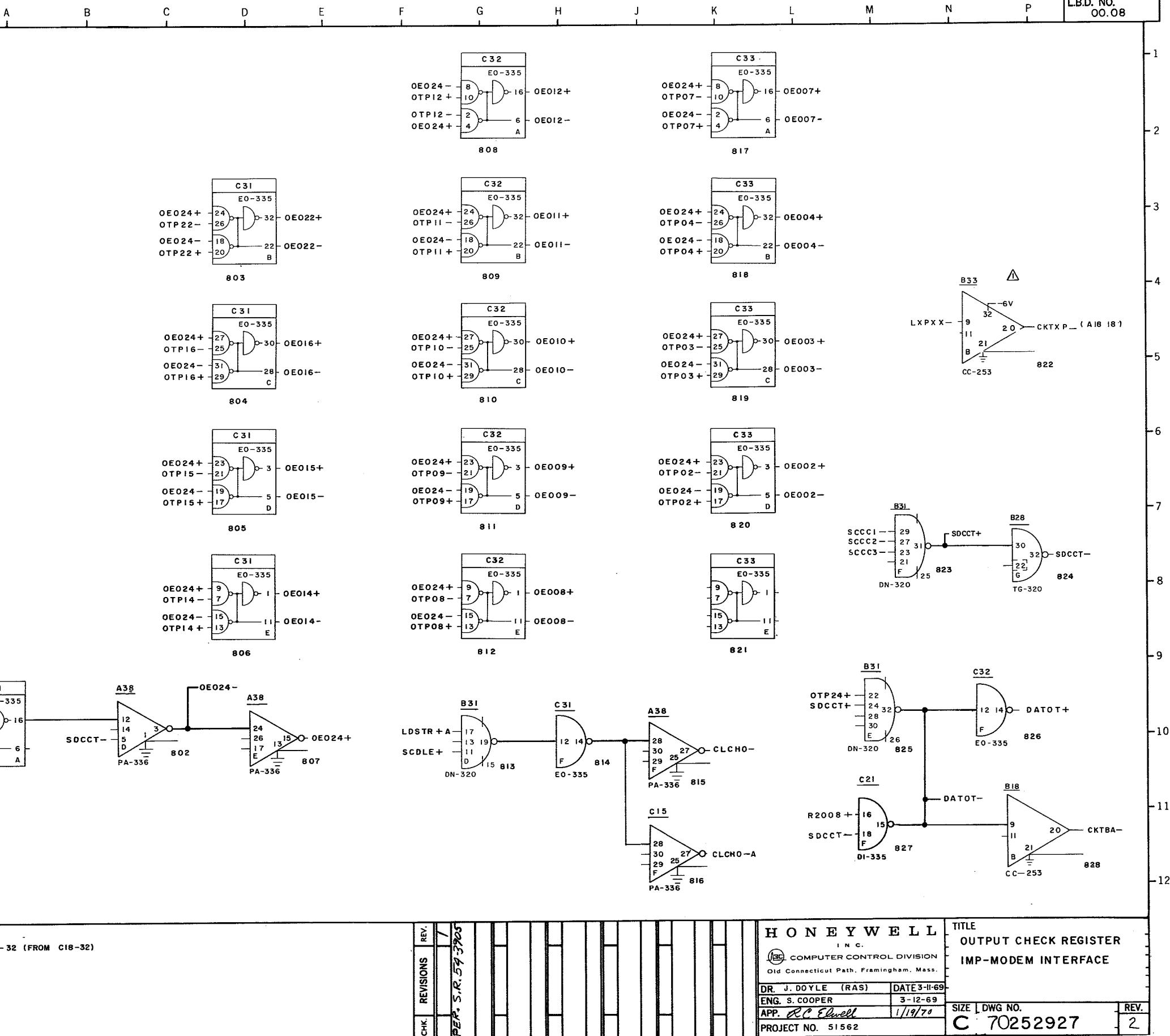
E | DWG NO.

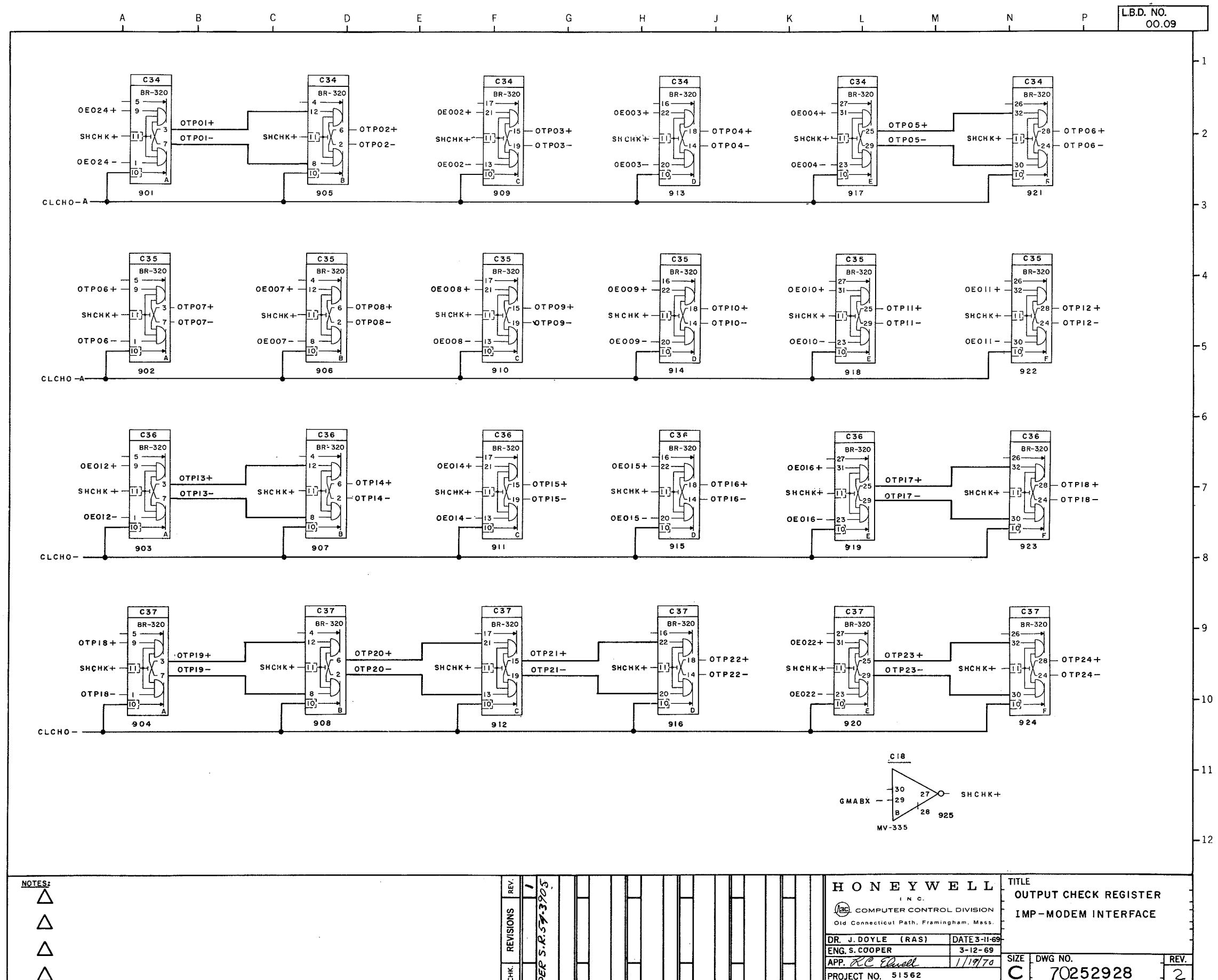
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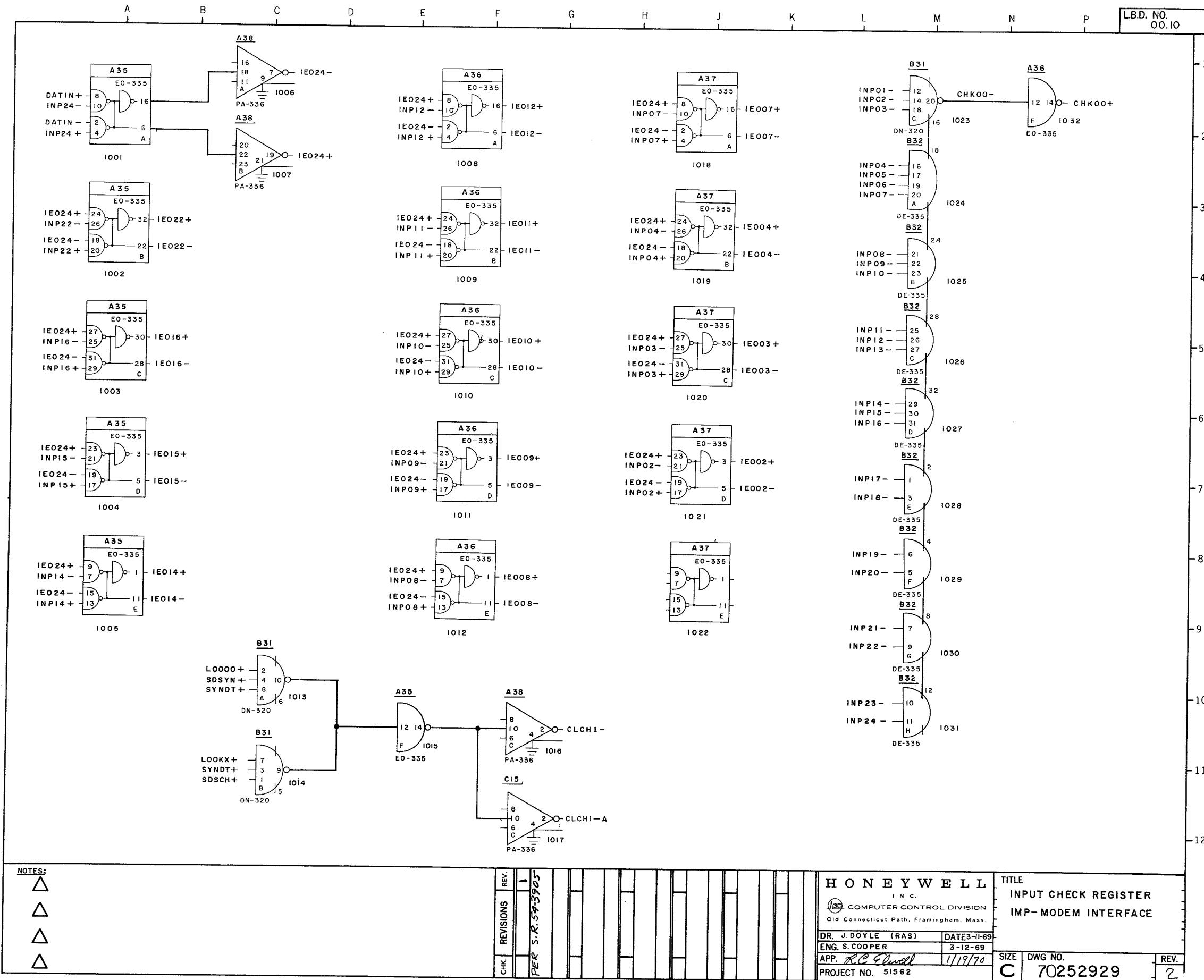
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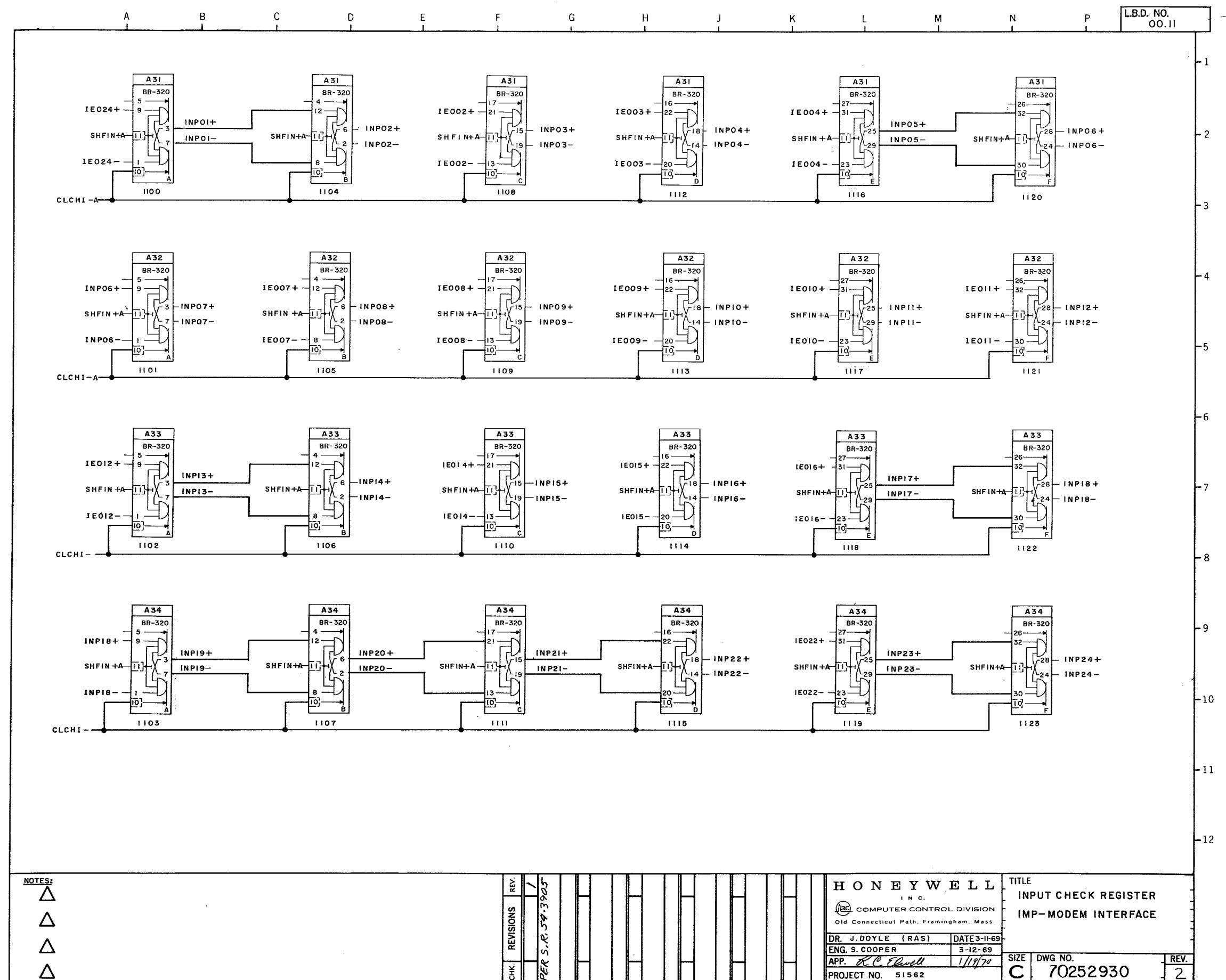
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00.06

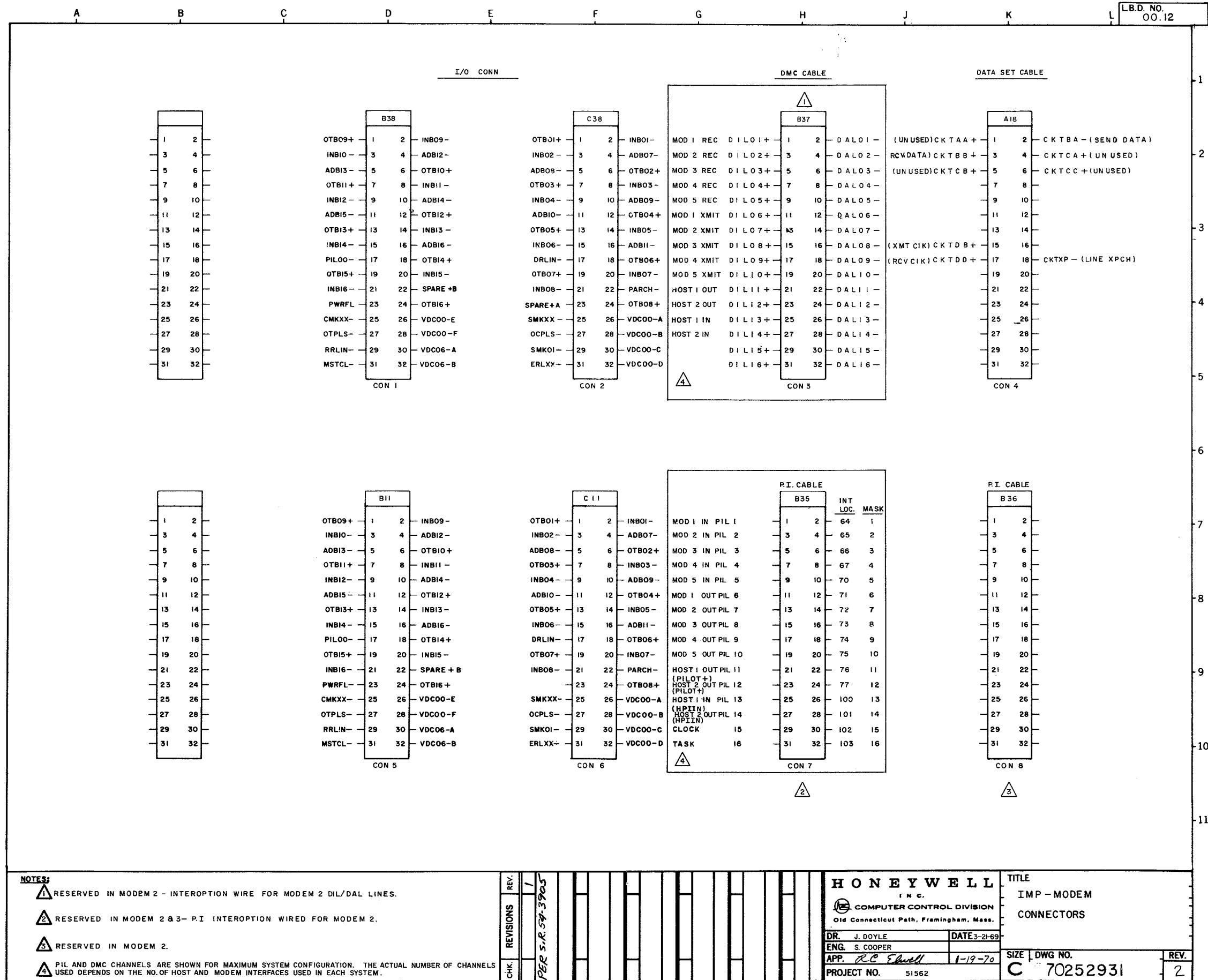


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00.08

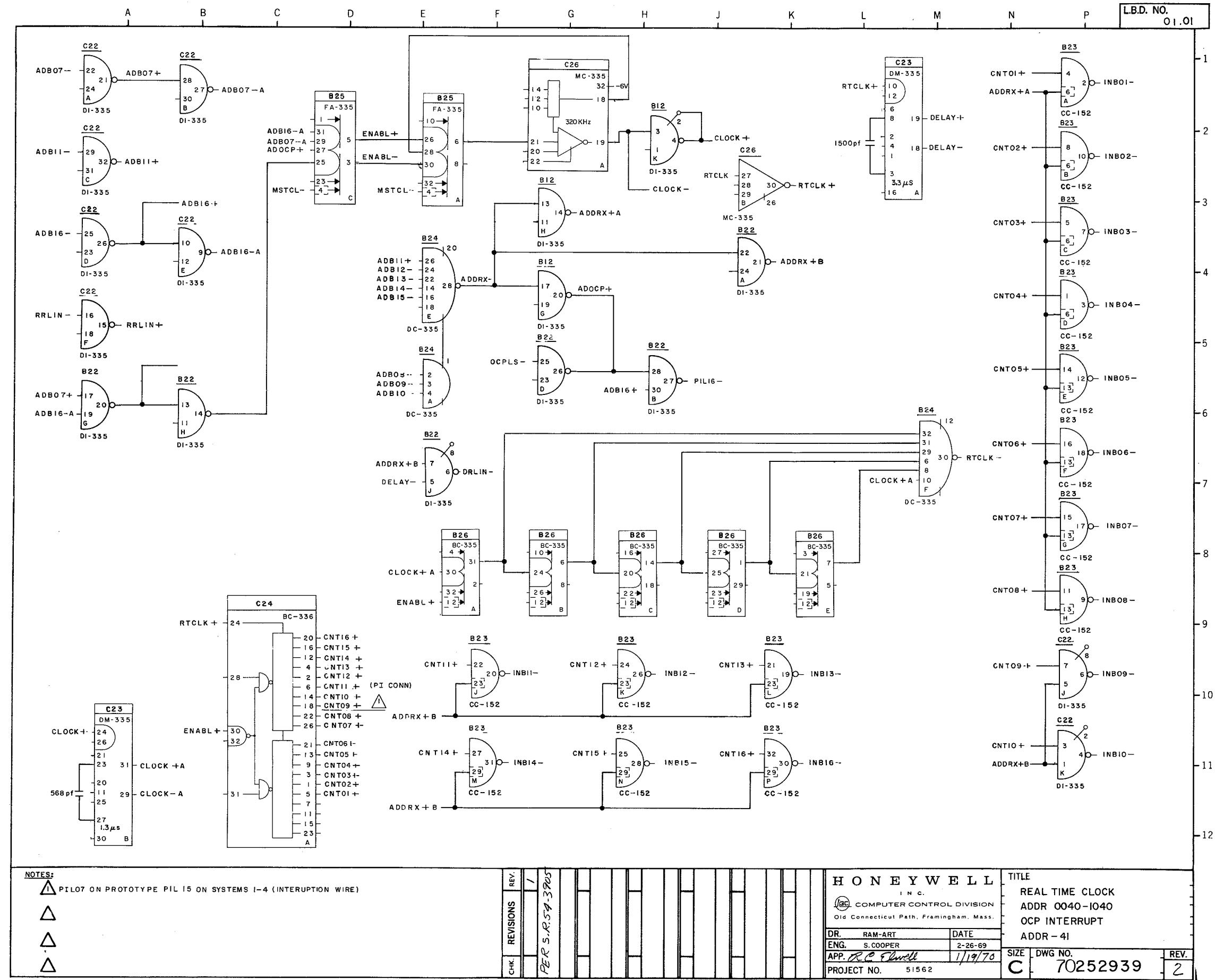


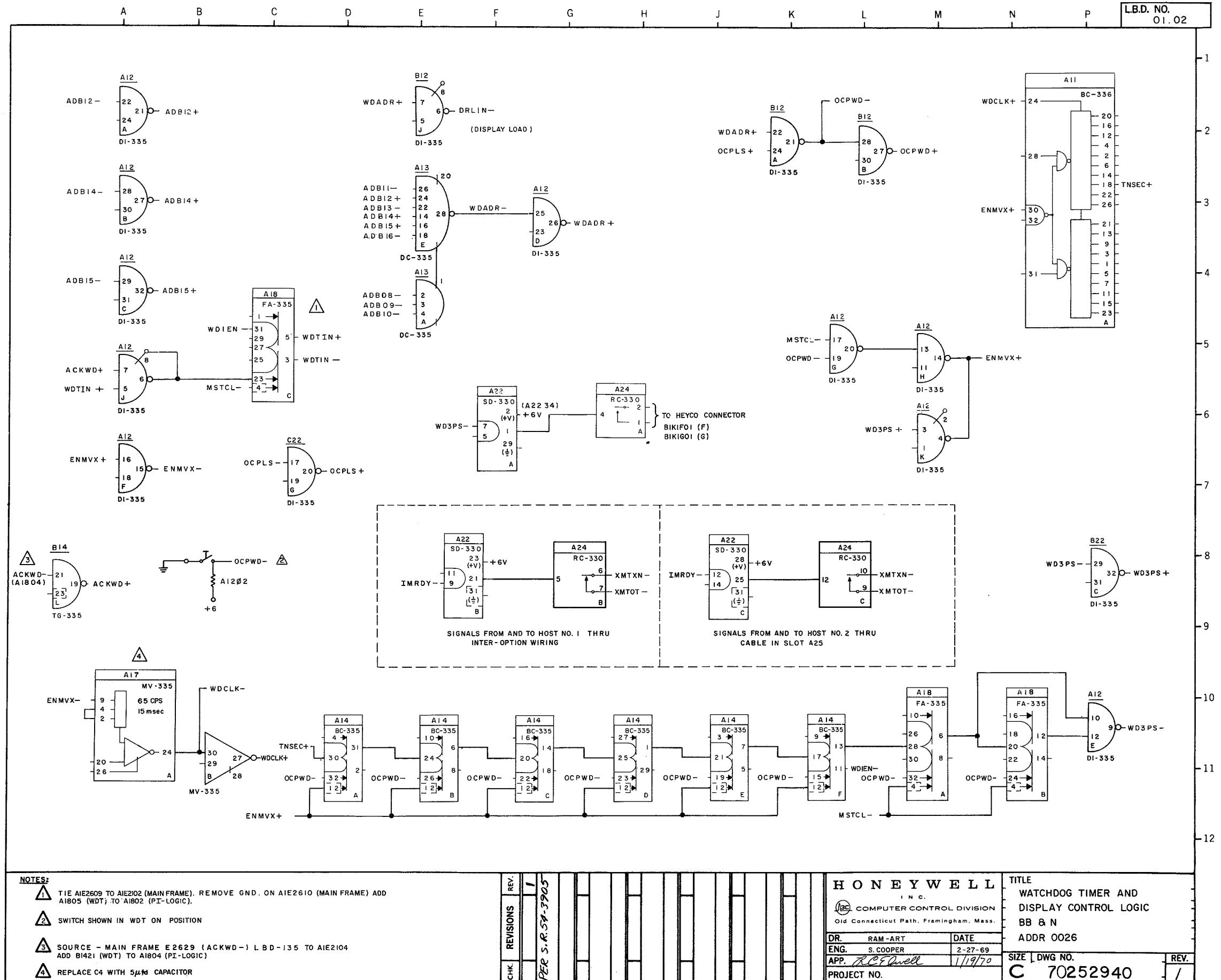


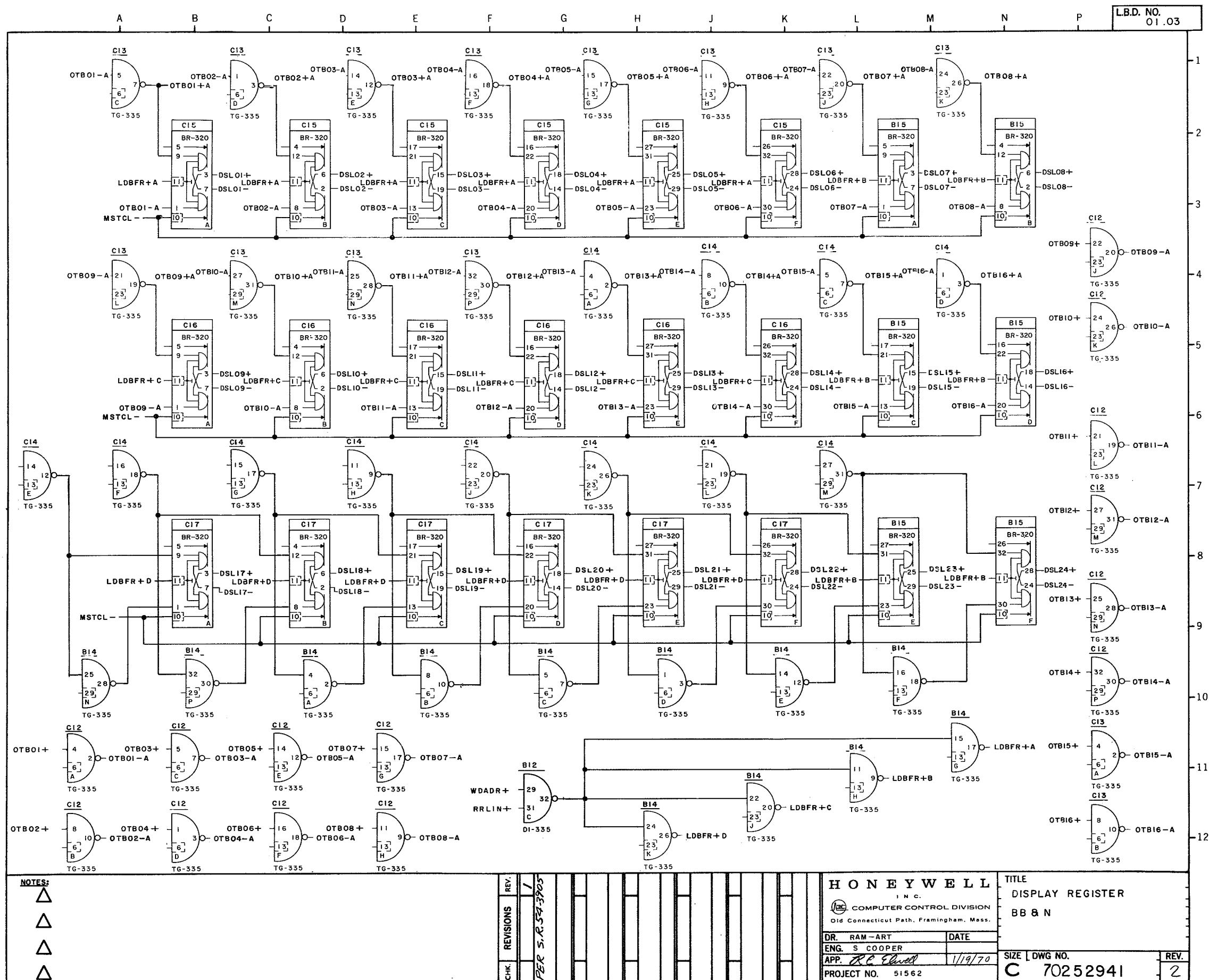




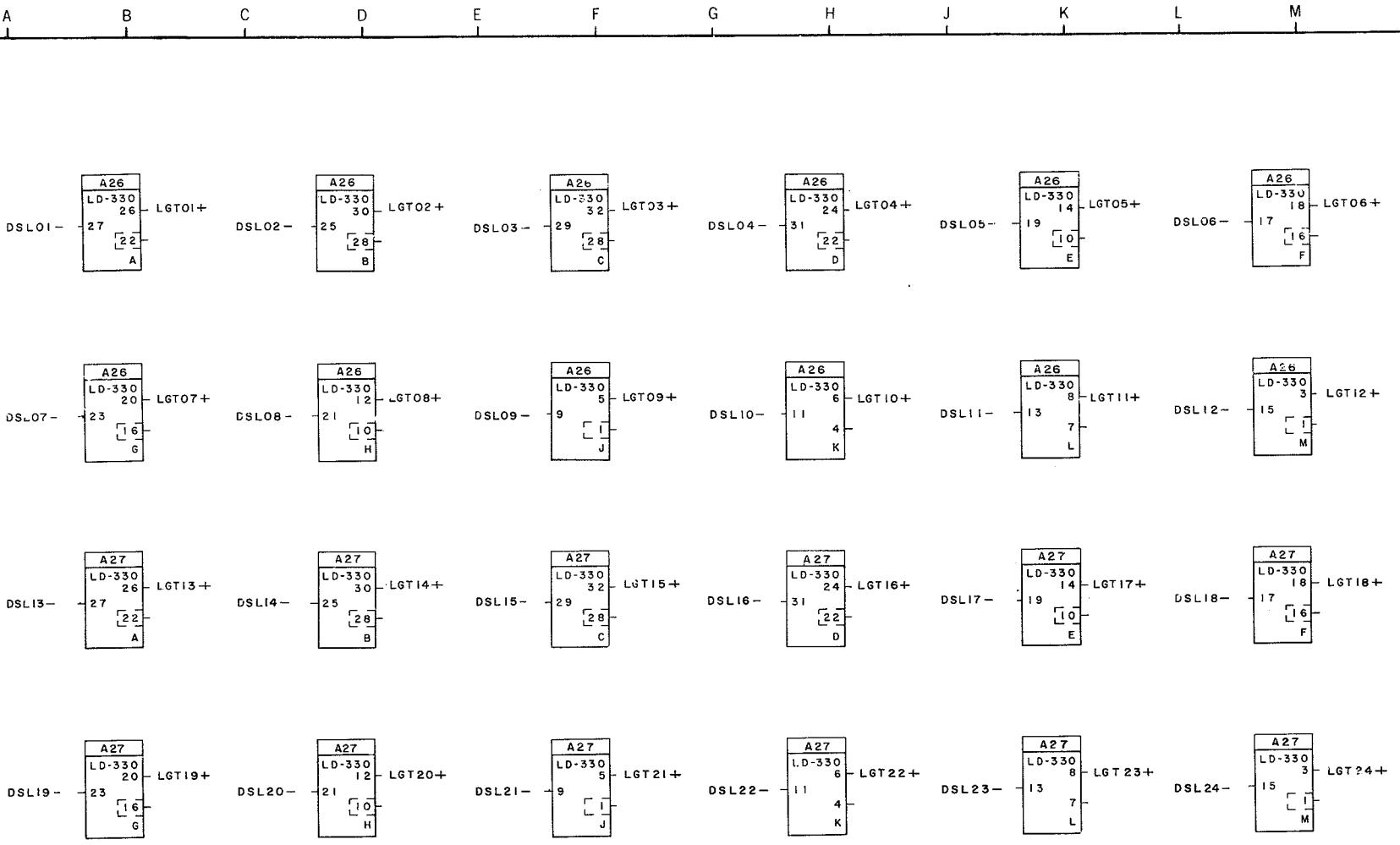






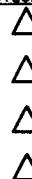


L.B.D. NO.  
C1.04



A28	
LGT01+	1 2 LGT02+
LGT03+	3 4 LGT04+
LGT05+	5 6 LGT06+
LGT07+	7 8 LGT08+
LGT09+	9 10 LGT10+
LGT11+	11 12 LGT12+
LGT13+	13 14 LGT14+
LGT15+	15 16 LGT16+
LGT17+	17 18 LGT18+
LGT19+	19 20 LGT20+
LGT21+	21 22 LGT22+
LGT23+	23 24 LGT24+
	25 26
	27 28
	29 30
	31 32

NOTES:



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PER S.R. 57-3905

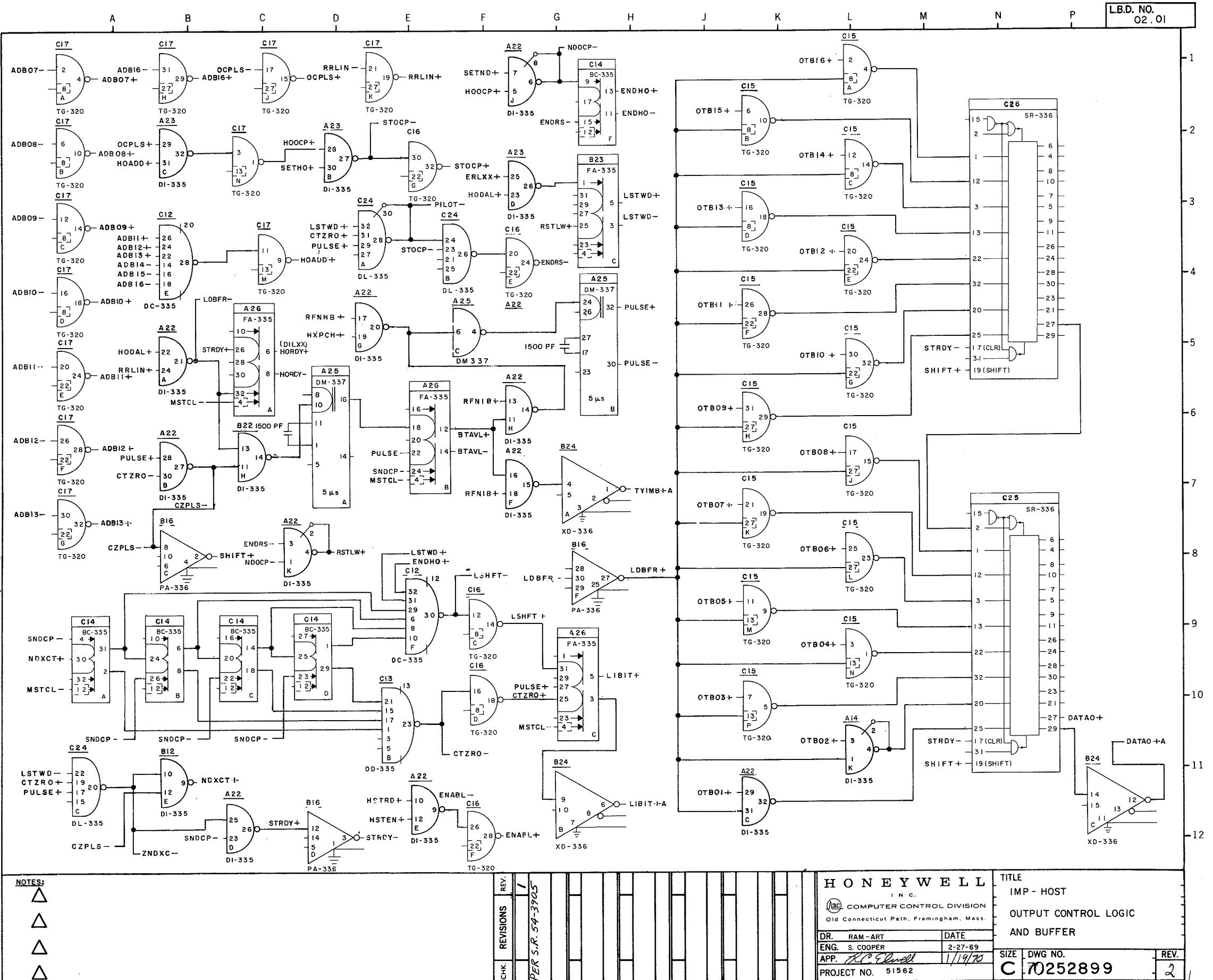
HONEYWELL  
IN C.  
COMPUTER CONTROL DIVISION  
Old Connecticut Path, Framingham, Mass.  
DR. RAM-ART DATE  
ENG. S COOPER  
APP. RC Flawell 1/19/70  
PROJECT NO. 51562

TITLE  
DISPLAY LAMP  
DRIVERS

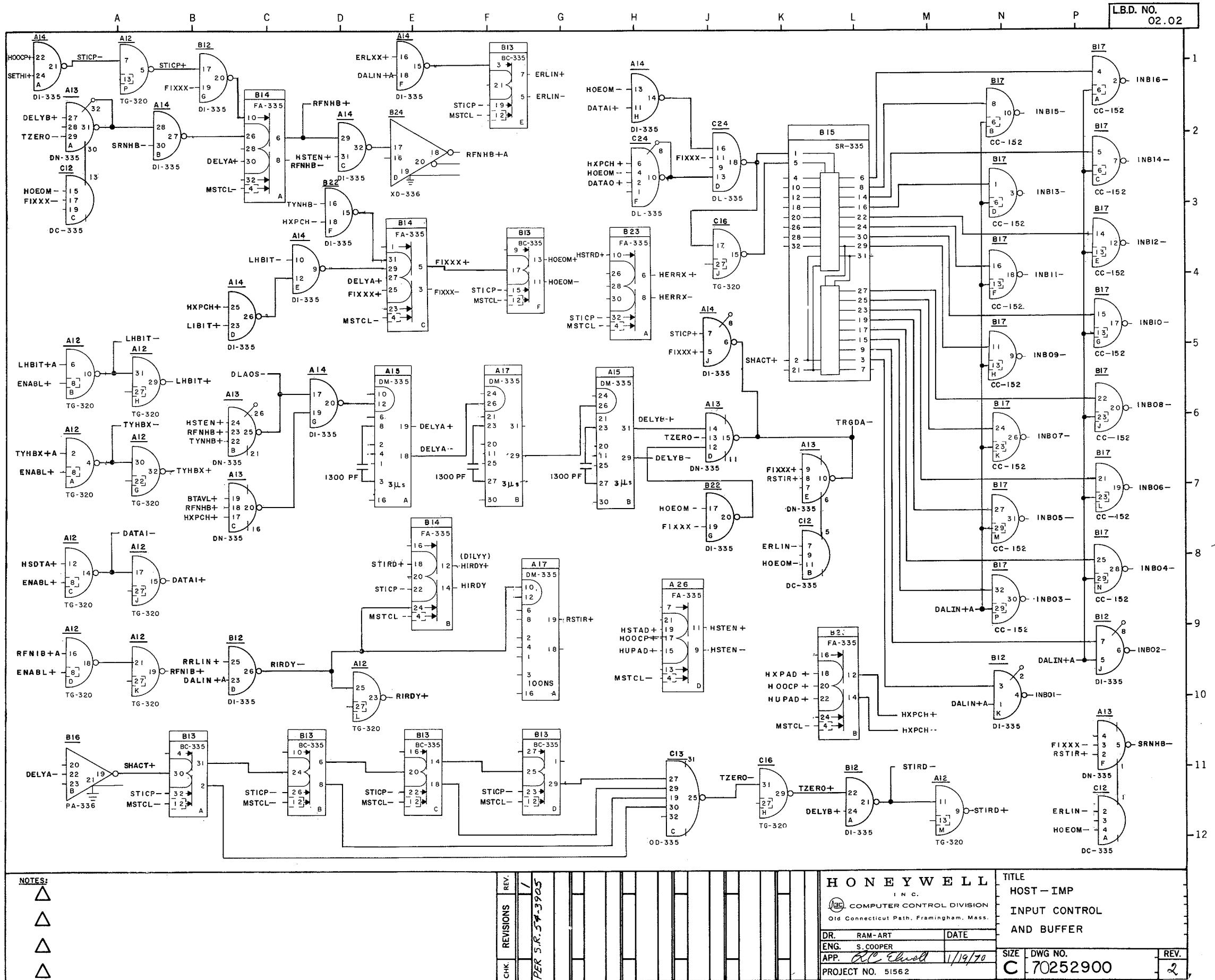
SIZE DWG NO. C 70252942 REV. 2

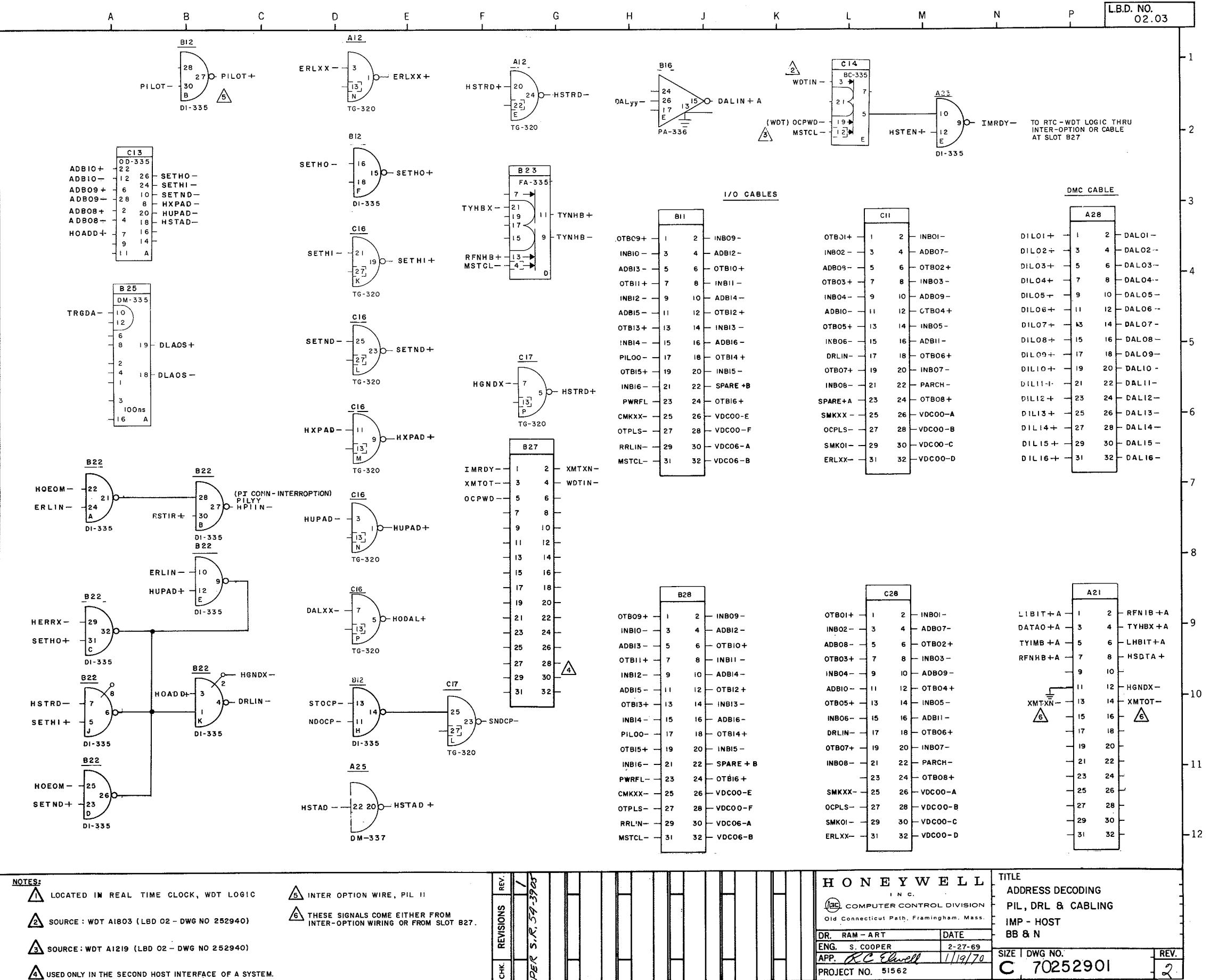


**NOTES:**  THIS SLOT USED ONLY ON SECOND HOST INTERFACE OF SYSTEM



L.B.D. NO.  
02.02





LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

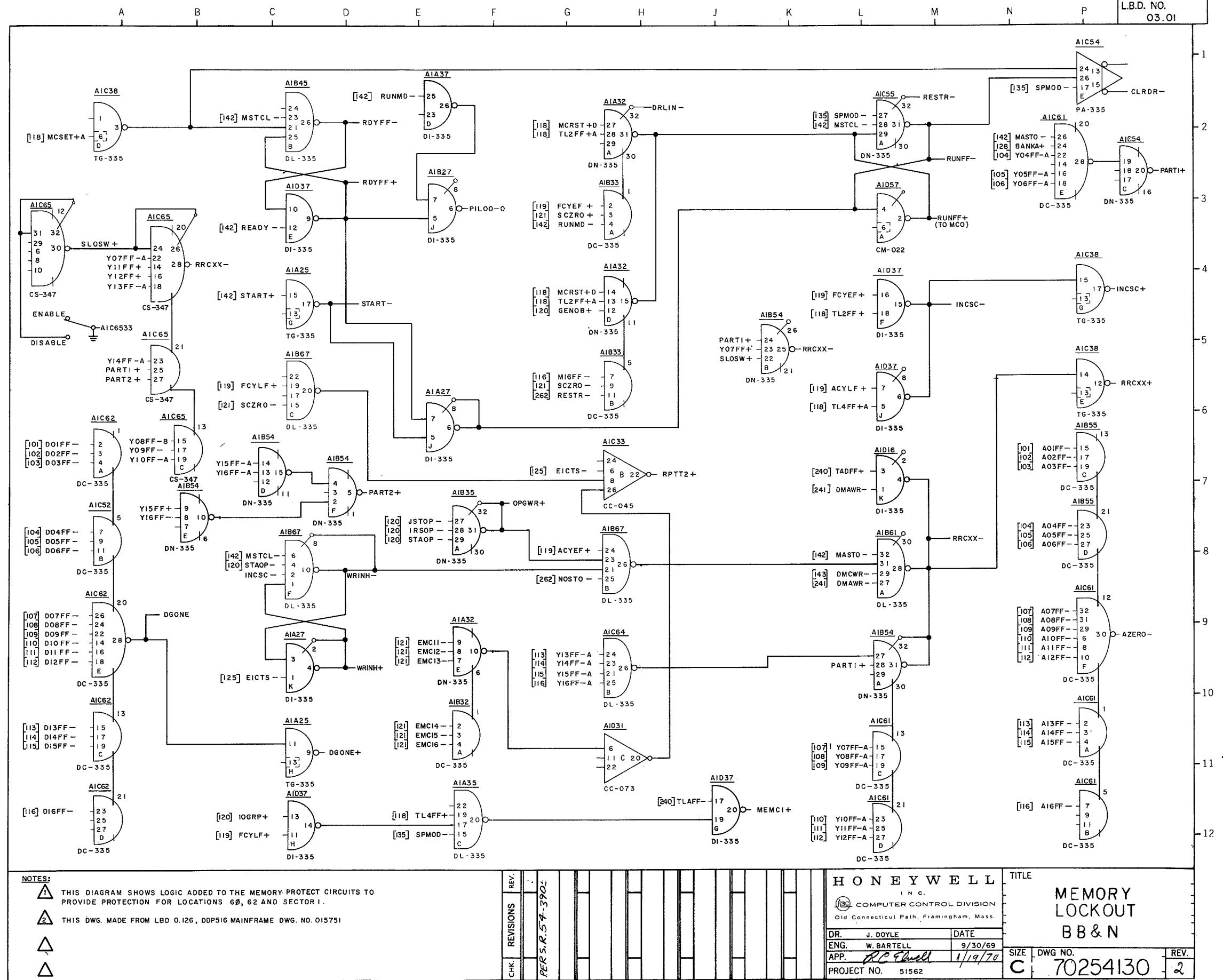
LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

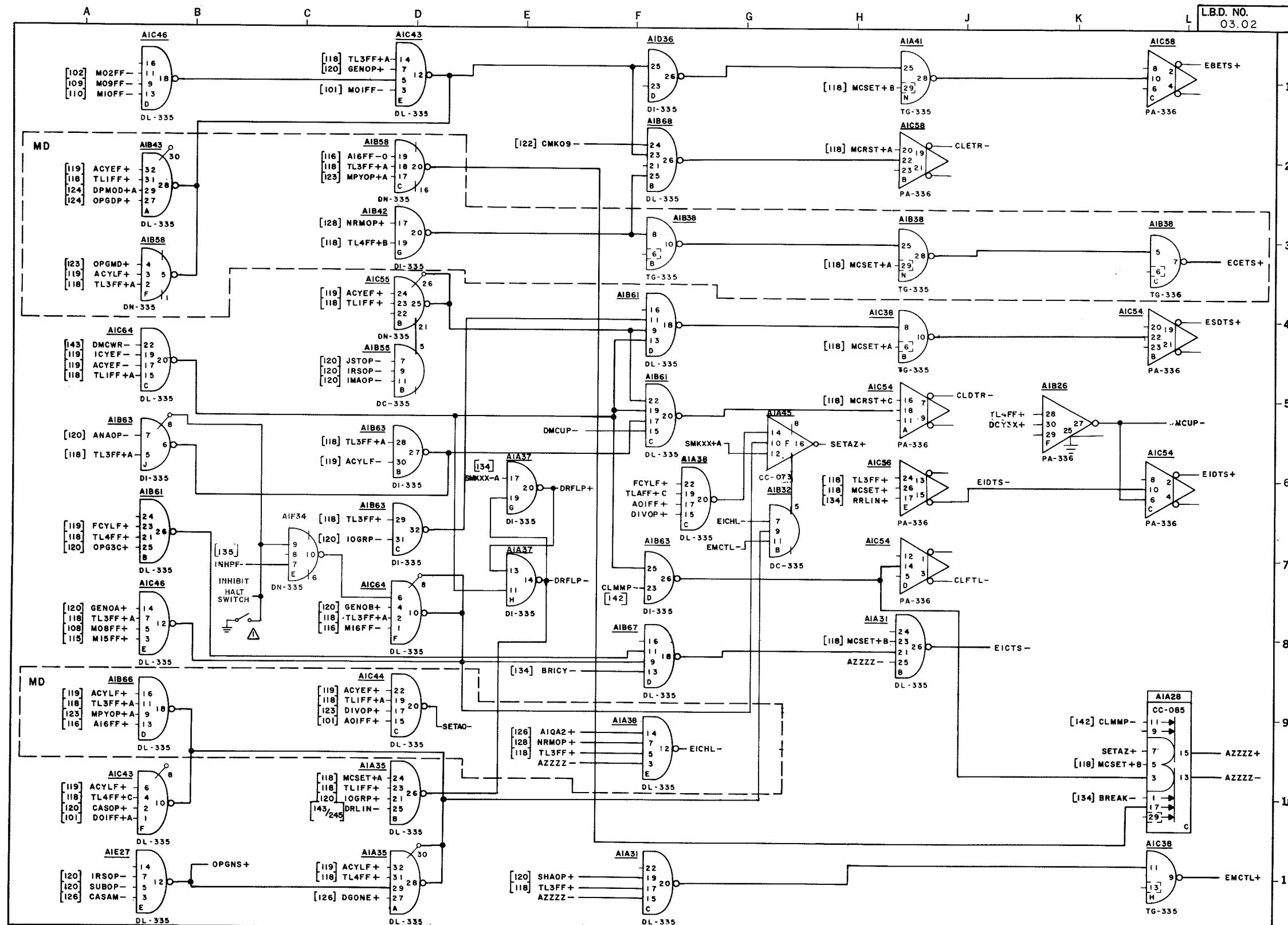
LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
5														
4														
3														
2														
1														

LOC	PAC A	B	C	D	E	F	G	H	J	K	L	M	N	P
8														
7														
6														
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3														
2														
1														

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NOTE : TAKEN FROM DWG. NO. 01575

**⚠ SWITCH SHOWN IN POSITION WHICH INHIBITS H  
INHPF - COMES FROM AIE2811**

REV.	/
REVISIONS	/

**HONEYWELL**  
I N C.  
 COMPUTER CONTROL DIVISION  
Old Connecticut Path, Framingham, Mass.

DR.		DATE
ENG.	S. COOPER	5-27-69
APP.	<i>R.C. Ewell</i>	1/19/70
PROJECT NO.		51562

TITLE  
NON HALT  
SPECIAL

E DWG NO. 70254084 REV. 2

**APPENDIX  
DESCRIPTION OF SPECIAL PACS**

This appendix contains circuit descriptions, schematic diagrams and parts lists for the special  $\mu$ -PACs that are in the IMP system.

CC-152  
CC-253  
CS-347

## TRANSFER GATE PAC, MODEL CC-152

The Transfer Gate PAC, Model CC-152 (Figure 1), contains 14 2-input NAND gates without collector resistors arranged in four independent groups. Two of the groups contain four NAND gates each with one input being common to the four gates. The other two groups contain three NAND gates each with one input being common to the three gates. All fourteen circuits provide a facility for connecting the NAND gates in parallel without decreasing the output drive capability.

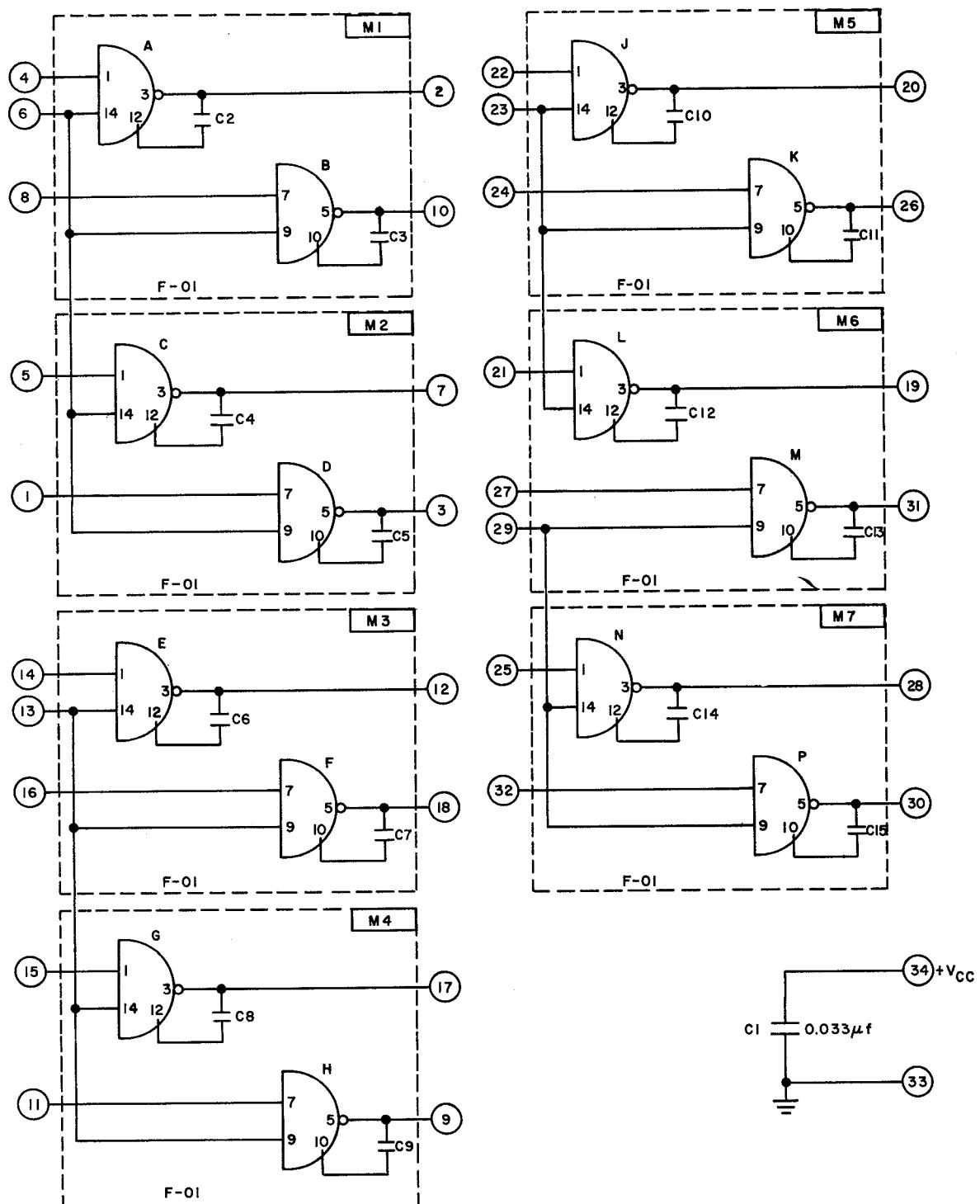
The Model CC-152 PAC can be used for the common transfer control of up to 14 data signals with the common input used as a control or strobe input. Turn-on rise time is controlled so as to have a guaranteed minimum of 50 ns with no load.

### Specifications

<i>Frequency of Operation</i>	<i>Circuit Delay</i>
Dc to 5 MHz (max)	120 ns (max) turn on 40 ns (max) turn off
<i>Input Loading</i>	<i>Current Requirements</i>
Individual inputs: 1 unit load each Common inputs: 1 unit load per gate	+6V: 95 mA
<i>Output Drive Capability</i>	<i>Power Dissipation</i>
8 unit loads	560 mW (max)

### ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: $0.033 \mu\text{F} \pm 20\%$ , 50 Vdc	930 313 016
C2-C15	CAPACITOR, FIXED, CERAMIC DIELECTRIC: $10 \text{ pF} \pm 10\%$ , 100 Vdc	930 173 204
M1-M7	MICROCIRCUIT: F-01 dual NAND gate integrated circuit	950 100 001



(1) - PIN NUMBER OF PAC

(2) - PIN NUMBER OF MICROCIRCUIT

M3 REFERENCE DESIGNATION OF MICROCIRCUIT

F-04 TYPE OF MICROCIRCUIT

3997

Figure 1. Transfer Gate PAC, Model CC-152, Schematic Diagram

## DATA SET ADAPTER PAC, MODEL CC-253

The Data Set Adapter PAC, Model CC-253 (Figure 1), contains one driver circuit and three identical receiver circuits which drive and terminate 50 feet of 95-ohm coaxial cable at speeds up to 1 MHz.

A positive  $\mu$ -PAC signal at the driver input will produce an output voltage more negative than -0.7V. A driver input signal at ground will produce an output voltage more positive than +1.0V.

A voltage more negative than -0.7V at the receiver input will produce an output at ground. A voltage more positive than +1.0V at the receiver input will produce a positive  $\mu$ -PAC signal at the output.

### Specifications

<i>Frequency of Operation</i>	<i>Circuit Delay</i>
DC to 1 MHz	Pin 20: 40 ns (max) Pins 18, 8 and 2: 60 ns (max)
<i>Input Loading</i>	<i>Current Requirements</i>
Pins 9, 11, 16, 6 and 4: 1 $\mu$ -PAC unit load each	+6V: 75 mA -6V: 50 mA
Pins 17, 5 and 1: Termination of 95 ohms coaxial cable each	<i>Total Power</i>
<i>Output Drive Capability</i>	700 mW
Pin 20: 50 feet of 95-ohm coaxial cable terminated by the characteristic impedance.	
Pins 18, 8 and 2: 8 $\mu$ -PAC unit loads each	

## ELECTRICAL PARTS LIST

Reference Designation	Description	CCD Part No.
C1, C2	CAPACITOR, PLASTIC DIELECTRIC: $0.033 \mu\text{F} \pm 20\%$ , 50 Vdc	70 930 313 016
CR1	DIODE: 1N276	70 943 023 001
CR2-CR4	DIODE: 1N914	70 943 083 001
M1	MICROCIRCUIT: F-02, NAND gate	70 950 100 002
Q1, Q2C, Q2D, Q2E	TRANSISTOR, SILICON, NPN: 2N3011	70 943 722 002
R1	RESISTOR, FIXED, COMPOSITION: 430 ohms $\pm 5\%$ , 1/4W	70 932 007 040
R2	RESISTOR, FIXED, COMPOSITION: 510 ohms $\pm 5\%$ , 1/4W	70 932 007 042
R3	RESISTOR, FIXED, COMPOSITION: 100 ohms $\pm 5\%$ , 1/4W	70 932 007 025
R4, R7	RESISTOR, FIXED, COMPOSITION: 12K $\pm 5\%$ , 1/4W	70 932 007 075
R5	RESISTOR, FIXED, COMPOSITION: 470 ohms $\pm 5\%$ , 1/4W	70 932 007 041
R6	RESISTOR, FIXED, COMPOSITION: 120 ohms $\pm 5\%$ , 1/4W	70 932 007 027
R8	RESISTOR, FIXED, COMPOSITION: 6.2K $\pm 5\%$ , 1/4W	70 932 007 068

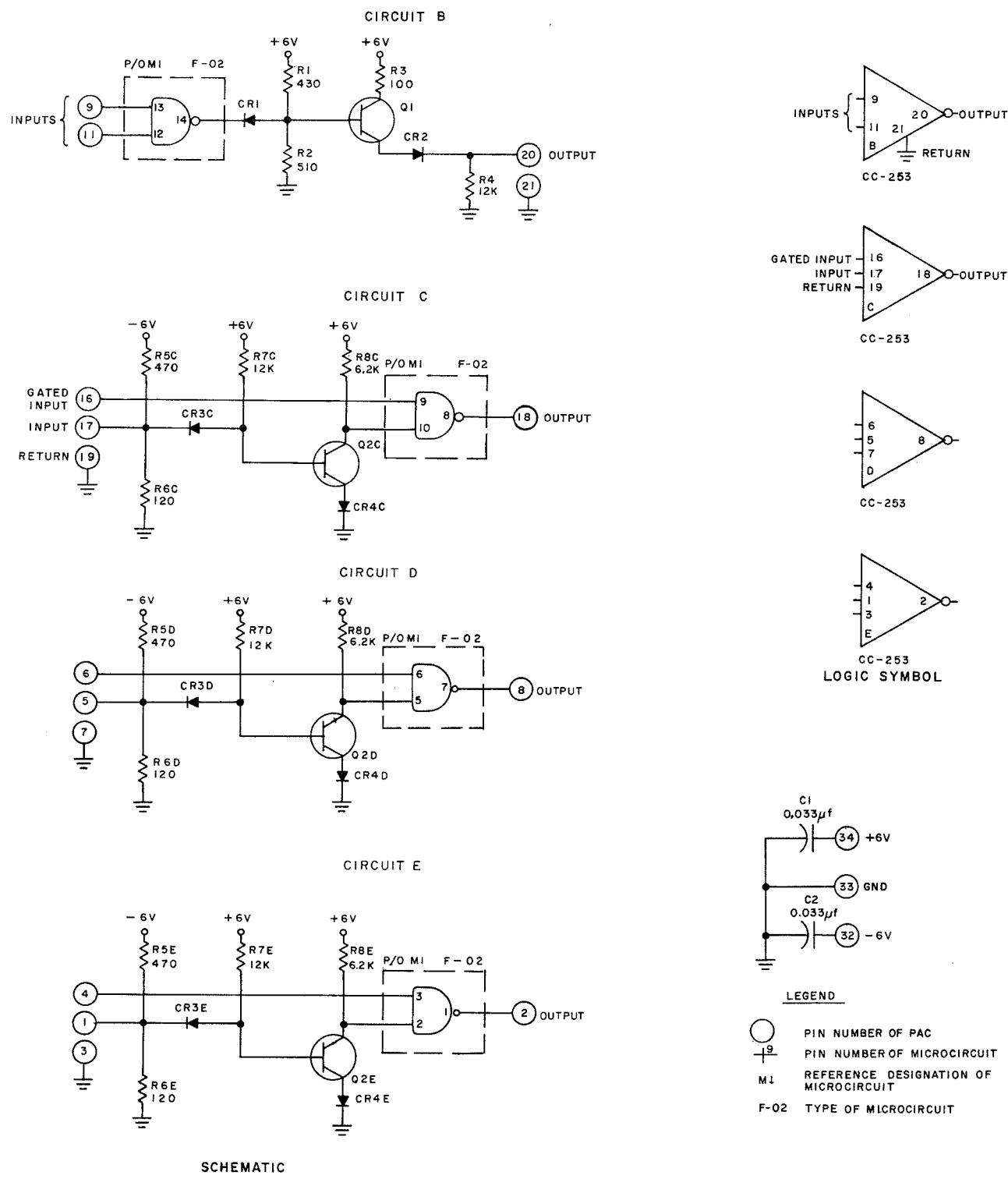


Figure 1. Model CC-253 Schematic Diagram and Logic Symbol

**MULTI-INPUT NAND PAC, MODEL CS-347**

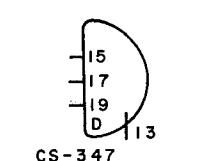
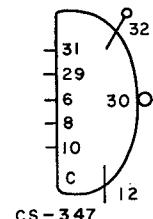
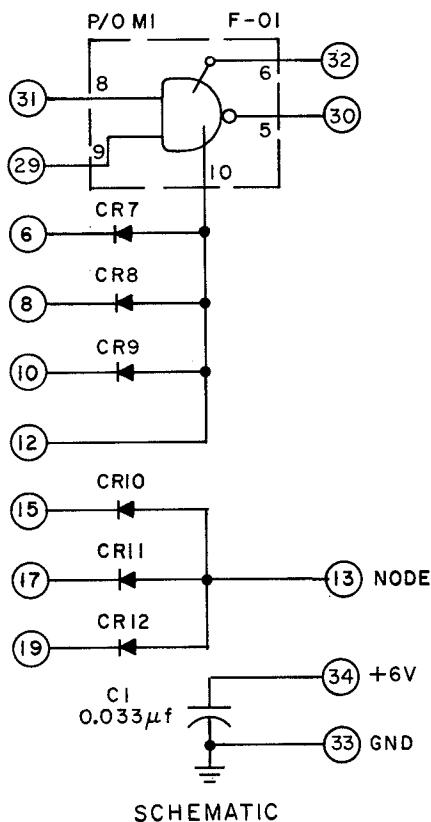
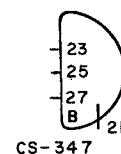
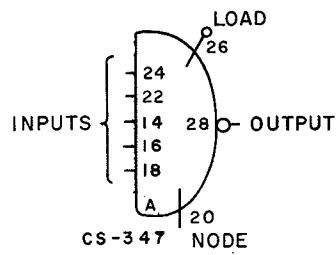
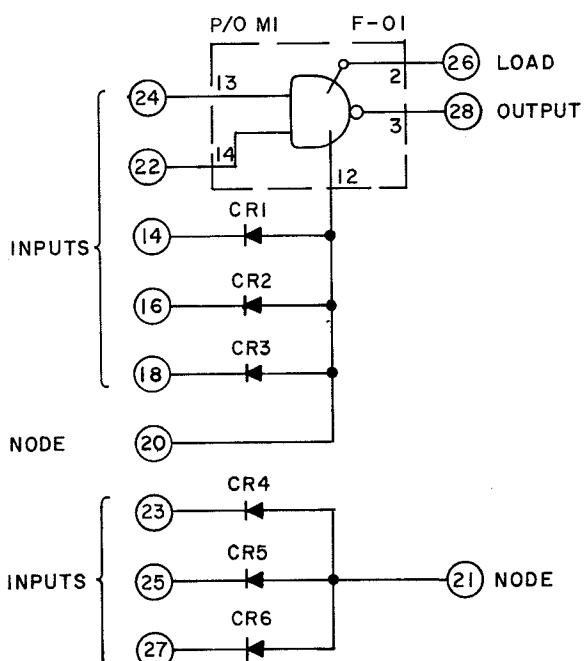
The Multi-Input NAND PAC, Model CS-347 (Figure 1), contains two 5-input NAND gates and two 3-diode clusters. Each gate contains a node, a collector output and a load resistor all connected to external pins. The number of inputs to each gate can be increased by connecting gate nodes to diode cluster nodes.

**Specifications**

<i>Frequency of Operation</i>	<i>Circuit Delay</i>
DC to 5 MHz	50 ns max
<i>Input Loading</i>	<i>Current Requirements</i>
1 $\mu$ -PAC unit load each	+6V: 25 mA
<i>Output Drive Capability</i>	<i>Total Power</i>
8 $\mu$ -PAC unit loads each	150 mV

**ELECTRICAL PARTS LIST**

Reference Designation	Description	CCD Part No.
C1	CAPACITOR, FIXED, PLASTIC DIELECTRIC: 0.033 $\mu$ F $\pm$ 20%, 50 Vdc	70 930 313 016
CR1-CR12	DIODE: 1N914	70 943 083 001
M1	MICROCIRCUIT: F-01, NAND gate	70 950 100 001



LOGIC SYMBOL

- LEGEND
- (6) PIN NUMBER OF PAC
  - (8) PIN NUMBER OF MICROCIRCUIT
  - M I REFERENCE DESIGNATION OF MICROCIRCUIT
  - F-01 TYPE OF MICROCIRCUIT

B6474

Figure 1. Model CS-347 Schematic Diagram and Logic Symbol