

Set II  
REPORT NO. 1877

# INTERFACE MESSAGE PROCESSOR

## Operating Manual

Developed for  
the Advanced Research Projects Agency  
by Bolt Beranek and Newman Inc.



Report No. 1877

Bolt Beranek and Newman Inc.

OPERATING MANUAL  
FOR INTERFACE MESSAGE PROCESSORS:  
516 IMP, 316 IMP, TIP

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Attn: Dr. L. G. Roberts

- Please put this manual in a conspicuous place near your IMP so that people from outside your group who need it can find it.

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\*Photographs on pp. 2, 3 and 84 by Hutchins Photography, Inc.,  
Belmont, Massachusetts; photograph on p. 4 by Ernest Vincent.

## INTRODUCTION

This manual contains all the information needed to operate and test the 516 Interface Message Processor (IMP), the 316 IMP, and the Terminal Interface Message Processor (TIP). It is imperative that no action be taken on any IMP or data lines without the approval of the Network Control Center (NCC). The NCC phone number is (617) 661-0100.

Since the manual describes procedures for three different devices, the operator must be sure that the procedures he uses are appropriate for his device. The devices are:

- The 516 IMP, ruggedized Honeywell DDP-516 (see Figure 1).
- The 316 IMP, Honeywell H316 (see Figure 2).
- The TIP, H316 with certain options, as described below (see Figure 3).

Procedures in this manual which apply to the 516 only or to the 316 only will be so indicated. Where procedures apply to both, no comment will be made.

Since the TIP incorporates a 316, references to the 316 IMP should be construed as applying equally to the basic main frame of the TIP. However, certain options exist for the TIP that are not in the 316 IMP. One of these is the Multi-Line Controller\*; also, the TIP has a greater core size in keeping with its more complex role of interacting with simple terminals.

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\* See: *User's Guide to the Terminal IMP*, BBN Report No. 2183, and *The BBN TIP*, BBN Report No. 2184.

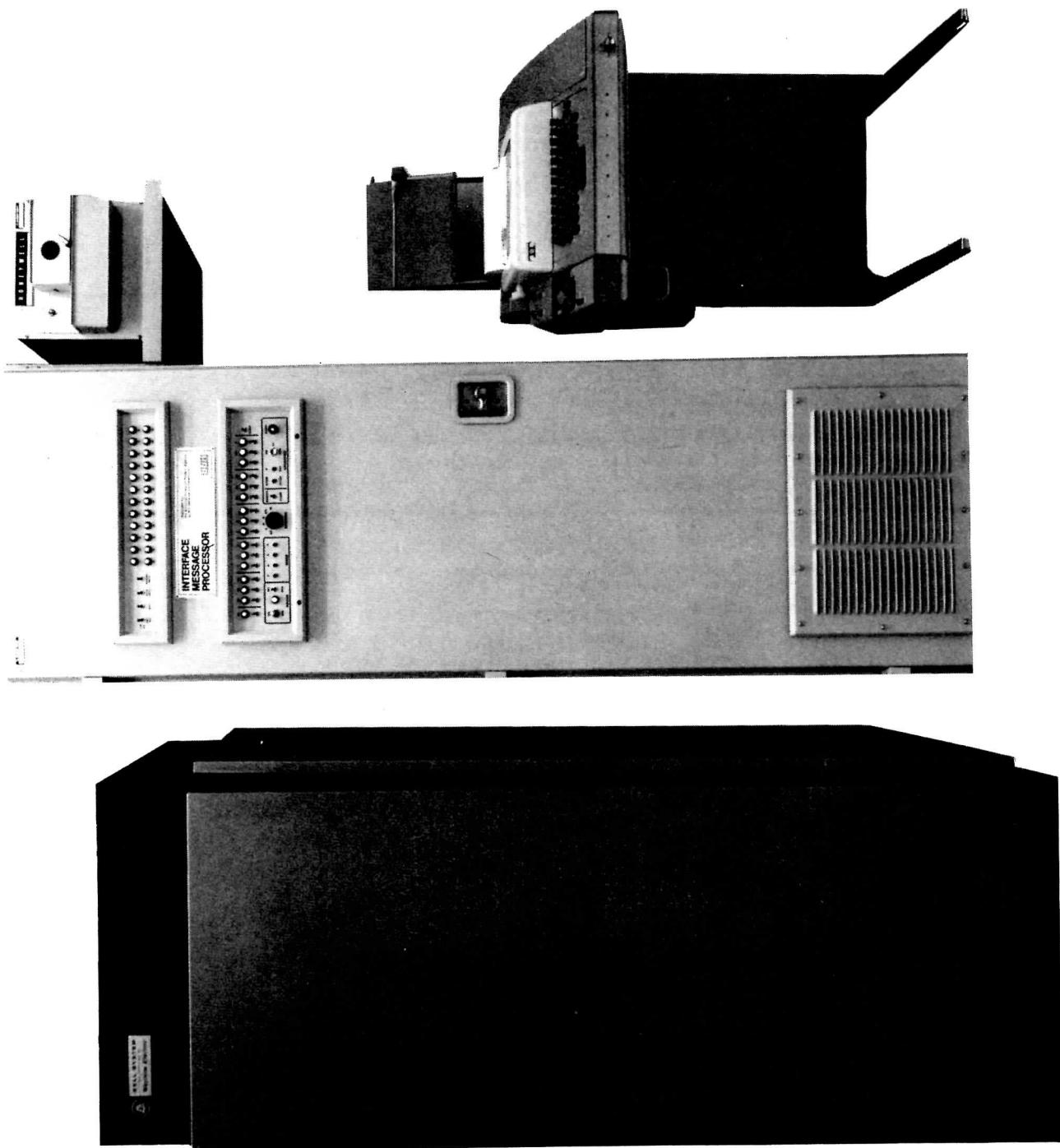


Figure 1. 516 IMP, Modem Cabinet, and IMP Teletype

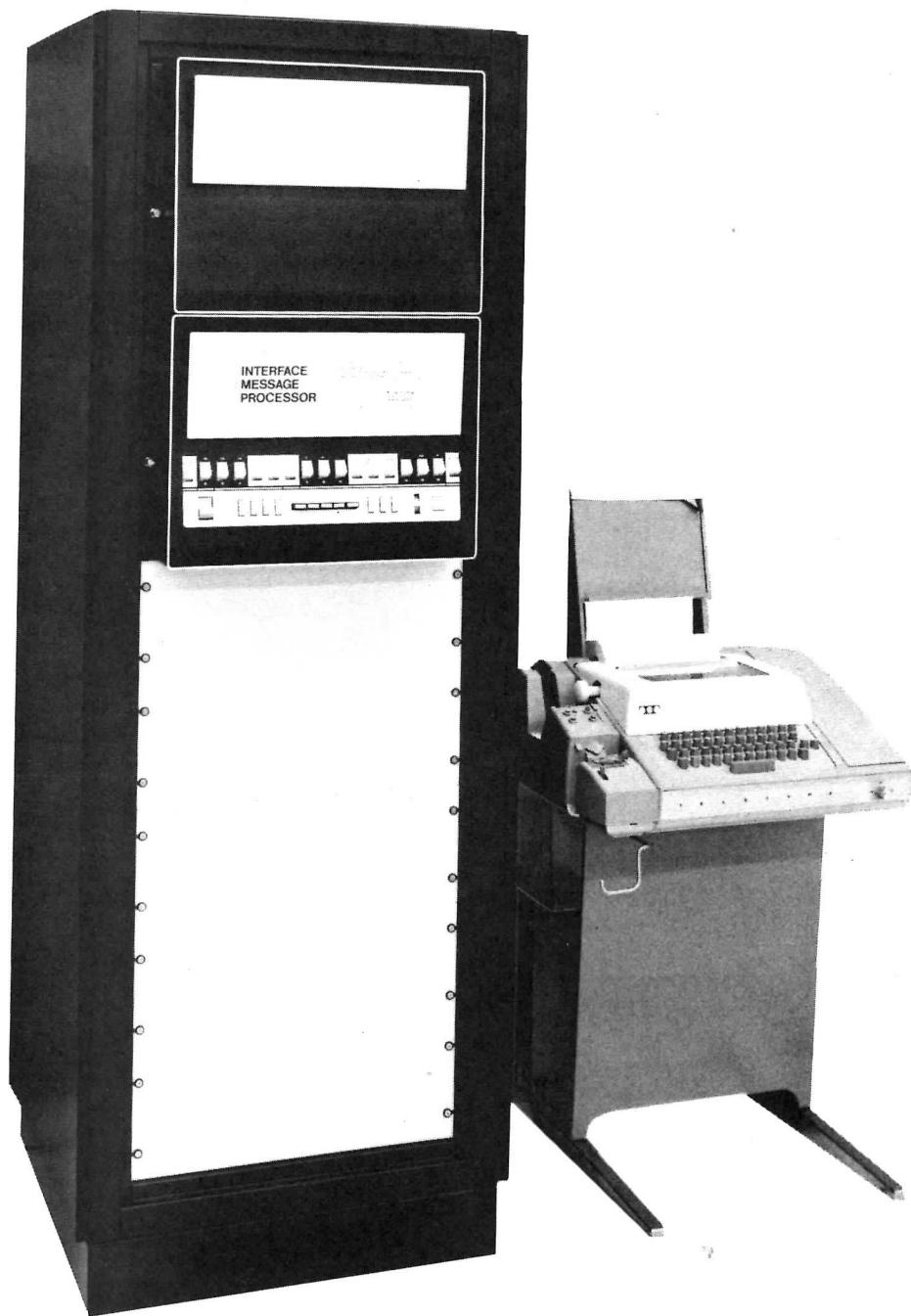


Figure 2. 316 IMP and IMP Teletype

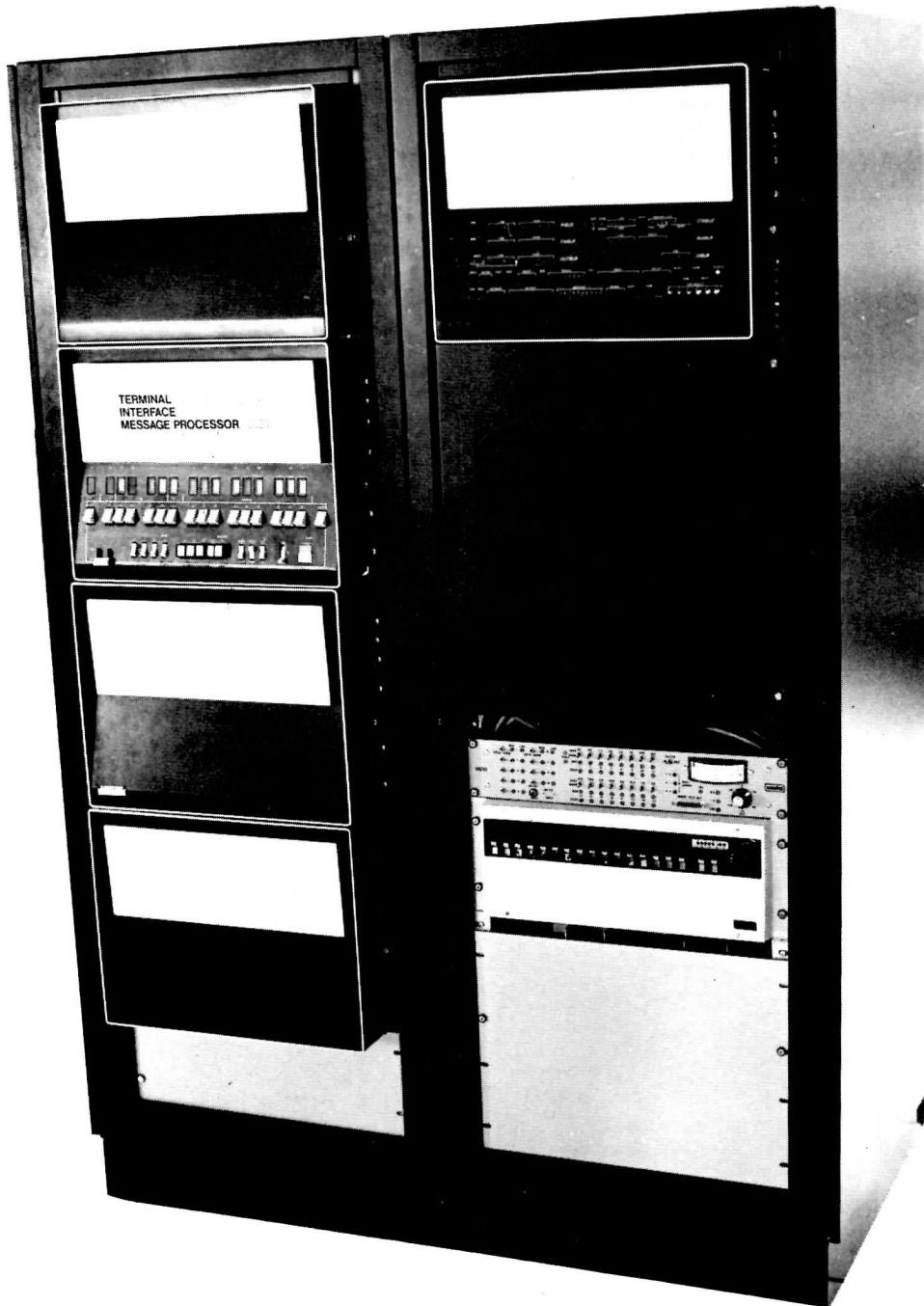


Figure 3. Terminal IMP

The Multi-Line Controller (MLC), which is an addition to the regular IMP function, is treated as somewhat of an external device (in this manual). While TIP operators may find this confusing, most TIP problems will require that the "IMP portion" of the TIP be verified as operable before continuing with the "terminal portion" of the problem. Operation of the magnetic tape transports connected to certain TIPs is described in the Honeywell documentation for that device.

A companion manual, *Specifications for the Interconnection of a Host and an IMP*, BBN Report No. 1822, includes information on the design and implementation of Host hardware and software message formats for both the TIP and the IMP. The procedure for connection of terminals to the TIP is detailed in the manual *Terminal Connection to the Terminal IMP*, BBN Report No. 2277.

## 1. OPERATING AN IMP/TIP

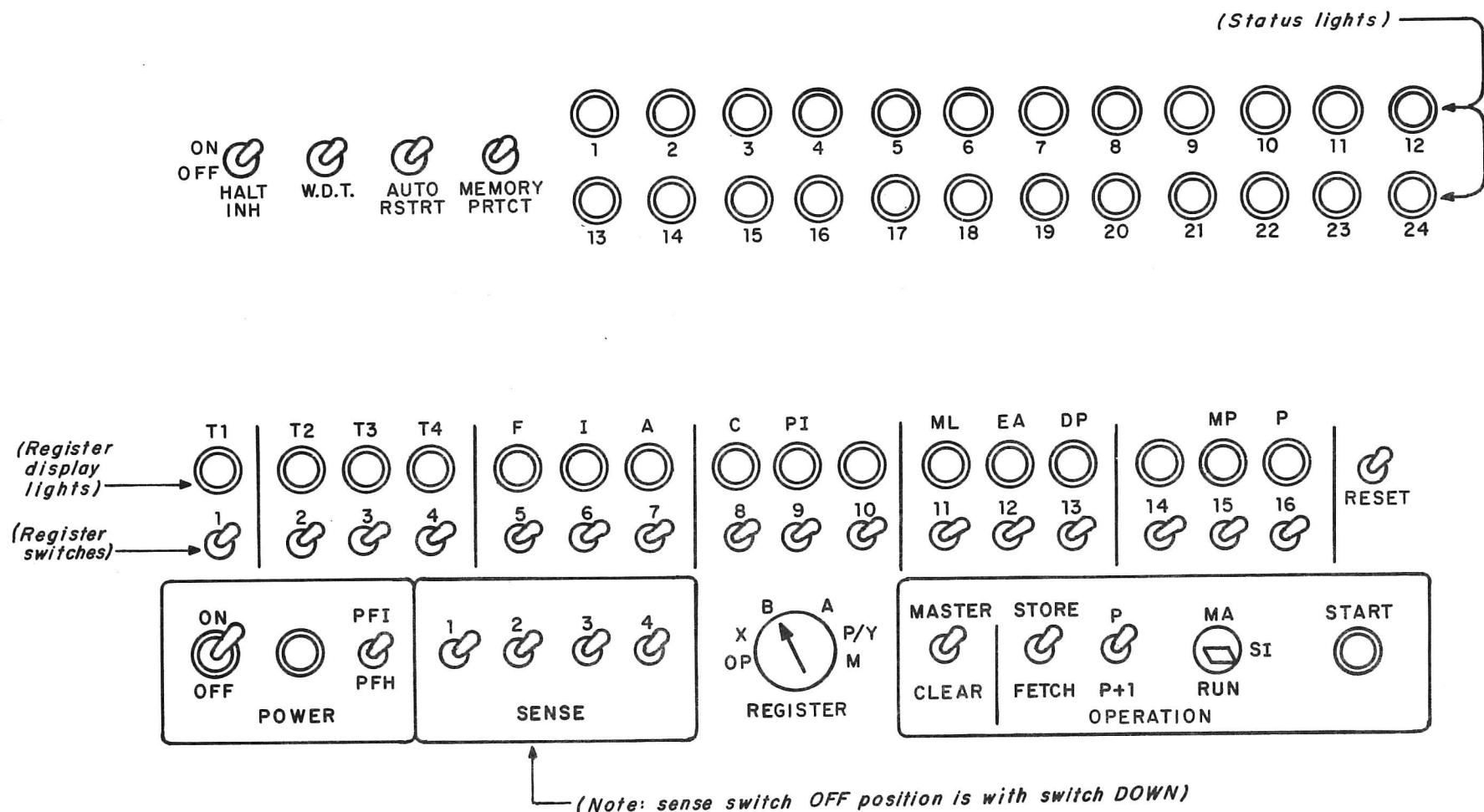
### 1.1 Control Panels

Figure 1-1 is a drawing of the 516 IMP control panel; Figure 1-2 shows the 316 IMP (or TIP) control panel. Table 1-1 describes the function of all control switches and indicators, and distinguishes between 316 and 516 machines. For further clarification see the Honeywell user's guide and programmer's reference manual.

### 1.2 Powering UP and DOWN

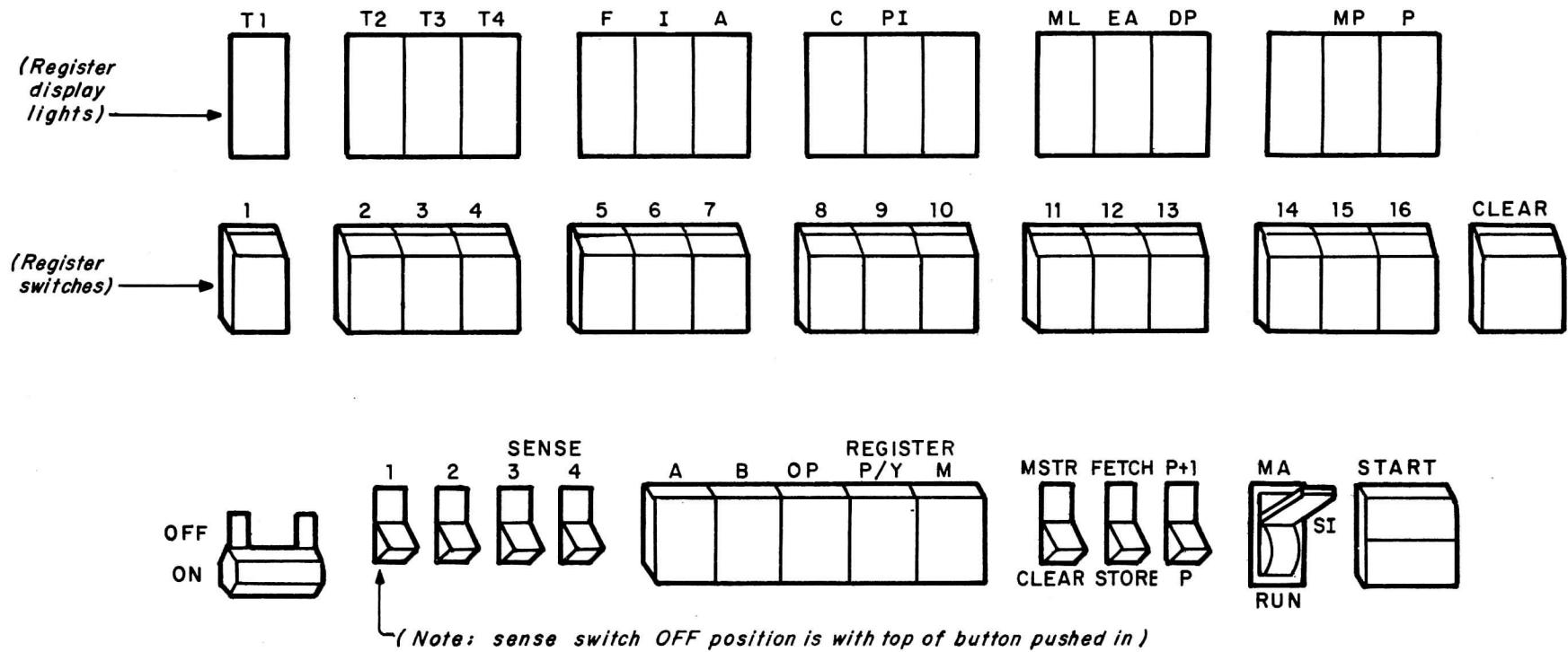
To power UP, throw the POWER ON/OFF switch on the control panel to the ON position and release. The power indicator light should go on. On a 516 machine, if this light does not go on, open the door and make sure that the MAIN POWER SWITCH is ON (see Figure 4-2), push the WATCHDOG TIMER RESET button (see Figure 4-2) and then power UP as above. On a 316, the light will come on only after several seconds and the control panel will be operable only after about 20 seconds.

To power DOWN, put the MA/SI/RUN switch to SI. If the START light remains lit, push the MASTER CLEAR switch. Throw the POWER ON/OFF switch to the OFF position and release.



## 516 IMP CONTROL PANEL

Figure 1-1



### 316 IMP OR TIP CONTROL PANEL

Figure 1-2

TABLE 1-1

## SWITCHES AND INDICATORS

<u>Designation</u>	<u>Type</u>	<u>Function</u>
REGISTER DISPLAY	lights	When the REGISTER selector switch is in position for the particular register, displays the contents (bits 1-16) of the X, A, B, P/Y, and M registers in the CPU. On 316 the X register is not displayed.
REGISTER LOAD (1 through 16)	2-position momentary toggle switches	When the REGISTER selector switch is in the OP position, displays the status of the key control flip-flops as listed below the indicators.
RESET (CLEAR on 316)	2-position momentary toggle switch	Pressing down on any switch loads a 1 bit into the indicated position of the register designated by the REGISTER selector switch. If a 1 bit is in the bit position, no action will result. Loading in a 1 bit lights the indicator displaying the respective bit.
POWER ON-OFF	3-position momentary toggle switch;	These switches perform no function in the OP or X positions of the REGISTER selector switch.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
	2-position on 316	is applied, the power light goes on. Pressing the switch toward the OFF position removes the primary power and the light goes off. On the 316, the light goes on several seconds after the power switch is thrown ON.
POWER INDICATOR	light	This light is on when power is on.
PFI/PFH (516 only — 316 has non-defeatable PFI)	2-position maintained toggle switch	<p>1) PFI (Power Failure Interrupt) When the switch is in the up position and a power failure occurs, the memory content is protected and the computer executes a user-incorporated interrupt routine to save the contents of the various registers.</p> <p>2) PFH (Power Failure Halt) When the switch is in the down position and the power fails, the contents of the memory are protected; however, the contents of the hardware registers are not protected and auto restart is disabled.</p>
SENSE (1-4)	2-position maintained toggle switch	These switches are sampled by user programs to determine their status and, when operated with corresponding skip instructions in the computer repertoire, enable the operator to initiate a skip instruction to select and/or alter the course of a program during its execution.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
MASTER CLEAR	2-position momentary toggle switch	Pressing down initiates a master clear, placing the computer in a standard cleared state in which registers A, B, M, P, and Y are cleared; the clock is stopped, and all timing registers are set to the condition that would exist following the execution of a HALT (HLT) instruction. The operation of this control has no effect on memory or the X register. Pressing also clears all interfaces.
STORE/FETCH	2-position maintained toggle switch	When the computer is in the memory access (MA) mode, selected by the MA/SI/RUN switch, this switch determines whether information will be stored into memory or read from memory.
P/P+1	2-position maintained toggle switch	In the FETCH position, this switch permits the readout and display of an addressed memory word location. In the STORE position, the switch enables the insertion of data into an addressed memory word location. If the MA/SI/RUN switch is in SI or RUN mode, the STORE/FETCH switch is disabled.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
MA/SI/RUN	3-position maintained toggle switch	<p>addresses by causing the previous address to be incremented by one. If the MA/SI/RUN switch is in the SI or RUN mode, the P/P+1 switch is disabled.</p> <p>This switch, when used with the START pushbutton, enables the operator to select the operating mode of the computer. The modes selected by each switch position are as follows:</p> <ul style="list-style-type: none"> <li>1) MA selects the memory access mode operation determined by the STORE/FETCH switch position. The START pushbutton is then pressed to execute the memory access operation.</li> <li>2) SI selects the single instruction mode, to permit the step-by-step execution of a program. The START pushbutton is pressed to initiate each step-by-step operation.</li> <li>3) RUN selects the normal computer operating mode during which the performance of a program may be stopped either by the execution of a HALT (HLT) instruction or by the positioning of the mode selector switch to either of the other two positions. The START pushbutton is depressed to initiate the RUN mode of operation.</li> </ul>

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
START	Pushbutton/ light	This switch implements the step-by-step reading or insertion of data into consecutive memory locations when in the memory access mode, and the step-by-step instruction of programs when in the single instruction mode. It also initiates program operation when in the run mode. The light on indicates a run condition (bottom half of START button on 316--the top half is the POWER INDICATOR).
REGISTER SELECTOR	6-position rotary selector switch	When in the M, X*, B, or A position, the switch causes the contents of the corresponding main-frame registers to be displayed on the sixteen indicators (1 through 16).
	5-position pushbutton bank on 316	In the P/Y position, the switch causes the contents of the Y register to be displayed on the sixteen indicators (1 through 16).  If the computer is in the MA mode, the main frame Y and P registers contain the same data. If the computer is in the SI mode, the P register contains a binary count of one more than the Y register. In either case, only the Y register content is displayed.

\* 516 only; to examine the X register for a 316, fetch location Ø.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
HALT INH (516 only)	2-position maintained toggle switch	In the OP position, the switch causes display of the states of the key control flip-flops, whose designation is listed under the 16 indicators. (Refer to Display Operational Data Procedure in the Honeywell Programmers' Reference Manual.)
W.D.T. (516 only)	2-position maintained toggle switch	When this switch is down, the IMP will halt when a HLT instruction is executed. When this switch is up, HLT is treated as a NOP instruction except in the case of a power failure. When a power fail has been sensed, the halt inhibit feature is overridden and a HLT instruction will be executed when encountered.
AUTO RESTART (516 only — 316 has non- defeatable auto restart)	2-position maintained toggle switch	When the W.D.T. (WatchDog Timer) switch is down, the WatchDog Timer feature is disabled. When this switch is up, the feature is enabled - i.e., a running program executes a special OCP at least every two minutes to prevent the W.D.T. interrupt. A second W.D.T. interrupt will be generated after 6 min. and a third after 10 min. If the OCP is not given within 12 min., the machine is automatically powered off.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
MEMORY PROTECT (516 only)	2-position maintained toggle switch	Automatic program restart will occur if the proper power fail program was executed.
STATUS LIGHTS (1-24) (516 only)	lights	When the switch is down and power comes back after a power failure, the machine can be restarted by pushing POWER ON and START, assuming again that PFI is selected and the interrupt program runs.
MAIN POWER (516 only)	2-position maintained toggle switch	When this switch is up, memory locations 60, 62 and 1000-1777 cannot be changed. When the switch is down, these locations can be changed.
WATCHDOG TIMER RESET (516 only)	pushbutton	STATUS LIGHTS 1-16 are programmable; STATUS LIGHTS 17-24 are currently inoperative.
		Located inside the computer on the power distribution unit (see Fig. 4-2), this switch controls all power to the IMP. It is usually not necessary to throw this switch down, except to test the auto-restart logic or to work on the machine.
		Located inside the computer on the power distribution unit (see Fig. 4-2), this button must be pushed to reenable machine operation if the WatchDog Timer has gone through the last phase of its powerdown cycle or to turn on power to the IMP if power does not come on when the POWER ON switch is pushed.

TABLE 1-1 cont'd.

<u>Designation</u>	<u>Type</u>	<u>Function</u>
PAPER TAPE READER POWER	2-position maintained toggle switch	Located on the front left of the high speed paper tape reader, this switch should be down (i.e., the reader off) except when a paper tape is being loaded.
TELETYPE POWER	3-position rotary selector switch	Located on the right front of the Teletype, this switch should be in the LINE position when the Teletype is in use and in the OFF position when the Teletype is not in use.
TELETYPE PAPER TAPE PUNCH CONTROLS	pushbutton	These are located on top of the Teletype punch; the OFF button should normally remain depressed.
TELETYPE PAPER TAPE READER CONTROL	lever	The lever on the Teletype reader should normally remain in either the STOP or FREE position. Pushing the lever to the START position turns on the reader.

### 1.3 Starting a Program

- Put the MA/SI/RUN switch to SI and push MASTER CLEAR.
- Select P register (P/Y on the REGISTER selector switch).
- Put the octal starting address in the P register, using the REGISTER LOAD switches. This address should be correctly displayed in the register display lights. If an error is made while inserting the address, push the RESET switch (located to the right of the lights) and try again.
- Put MA/SI/RUN switch to RUN.
- Push START button. The button should light up.

### 1.4 Loading a Paper Tape

Paper tapes are loaded using the high speed paper tape reader where available, or otherwise the Teletype paper tape reader. On the 516 machine, put W.D.T., MEMORY PROTECT, and HALT INH switches down. Refer to the proper section below, High Speed or Teletype.

#### *Procedure for High Speed Tape Readers:*

- Turn tape reader power switch on.
- Put the MA/SI/RUN switch to SI and push MASTER CLEAR.
- Put the paper tape in the reader tape holder. The 3-hole side of the tape goes toward the reader.
- Thread the paper tape through the reader and flip the lever from right to left with a satisfying clunk. Inspect to be sure tape guide is positioned properly and not pinching tape.
- Start the IMP at location 1 - i.e., octal address 1.
- To confirm that a paper tape is loading correctly while

the load is in progress, select the A register, which should be rapidly changing, or the X register (516 only) which should be counting.

- If the paper tape stops reading before the end, a checksum error occurred - try again.
- If the tape pulls out of the reader, the tape may have been mispositioned in the reader or the reader lever may have been closed incorrectly - try to read the tape in again. If it fails again, verify the bootstrap loader.
- Using the procedure described in Section 1.5, check locations 1-17 and correct any discrepancies. Be sure to use the bootstrap loader for high speed reader - see Table 1-2. Now repeat the loading procedure.
- If the tape stops exactly at the end, the load is successful, and the machine will either halt or start executing the program.
- Turn the READER POWER switch off.

*Procedure for Teletype Paper Tape Readers:*

- Turn the Teletype power switch to LINE.
- The reader assembly sits on the left front of the Model 33 Teletype. Push the small lever on the upper right-hand side of the reader unit to the right to release the plastic shroud that will later clamp over the paper tape. The shroud should pop up.
- Orient the paper tape so that the beginning of the tape points toward the operator and the 3-hole side is on the left side of the tape roll.

TABLE 1-2 BOOTSTRAP LOADER (KEY-IN)

<u>Octal Address</u>	<u>High Speed Reader Contents (octal)</u>	<u>Teletype Reader Contents (octal)</u>
1	010057	010057
2	030001	030004
3	131001	131004
4	002003	002003
5	101040	101040
6	002003	002003
7	010000	010000
10	131001	131004
11	002010	002010
12	041470	041470
13	130001	130004
14	002013	002013
15	110000	110000
16	240000	240000
17	100040	100040

Note: The two types of bootstrap loaders differ only in locations 2, 3, 10, 13

- Place the tape between the reader unit and the shroud, carefully fitting the tape over the protruding toothed wheel and between the tape guides.
- Carefully push the shroud down until the little right-hand-side lever clicks and locks the shroud in place over the tape. If the toothed wheel is not properly aligned with the tape holes, this will be difficult and the tape may be damaged.
- Put the MA/SI/RUN switch to SI and push MASTER CLEAR.
- Start the IMP at location 1 — i.e., octal address 1. Push the lever on the left-hand side of the reader (START-STOP-FREE) toward the START position. The tape should begin to move.
- To confirm that a paper tape is loading correctly while the load is in progress, select the X register (516 only), which should be counting, or the A register, which should be changing.
- If the paper tape stops in the reader before the end, or if the run light goes out and/or the A register stops changing, then a checksum error occurred. Put the reader lever into the FREE position and pull the tape back to the beginning. Restart the procedure as before.
- If the tape pulls out of the reader or the A register stops changing, verify the bootstrap loader. Using the procedure described in Section 1.5, check locations 1-17 and correct any discrepancies. Be sure to use the bootstrap loader for Teletype reader - see Table 1-2. Now repeat the loading procedure.

- If the tape stops exactly at the end, the load is successful, and the machine will either halt or start executing the program.
- Turn the Teletype power switch to OFF.

### 1.5 Inspecting or Changing a Memory Location

To inspect a memory location:

- Put the MA/SI/RUN switch to MA.
- Put the P/P+1 switch to P.
- Put the STORE/FETCH switch to FETCH.
- Select P/Y with the REGISTER selector switch.
- Put the address to be inspected in P using the REGISTER LOAD switches.
- Select M using REGISTER selector switch.
- Push the START button once.

M now contains the contents of the desired location. To inspect successive locations, operate as instructed above, except put P/P+1 switch to P+1 and push START repeatedly.

To change the contents of a memory location:

- Put the MA/SI/RUN switch to MA.
- Put the P/P+1 switch to P.
- Put the STORE/FETCH switch to STORE.
- Select P/Y with the REGISTER selector switch.
- Put the address to be changed in P using the REGISTER LOAD switches.
- Select M.
- Push RESET.
- Put the new contents in M using the REGISTER LOAD switches.
- Push START once.

The location has now been changed. To change succeeding locations, put the P/P+1 switch to P+1 and repeatedly set up M and push START.

### 1.6 Operating a Modem

It is not normally necessary for an IMP user to be concerned with operation of a modem. Occasionally, however, it is useful for testing purposes to be able to crosspatch a modem in various ways. These steps should only be undertaken at the request and under the supervision of the Network Control Center. This is essential to maintaining network integrity. Otherwise, the modems should not be disturbed.

The modem control panel is shown in Figure 1-3. The position of a modem in a site-to-site configuration is shown in Figure 1-4.

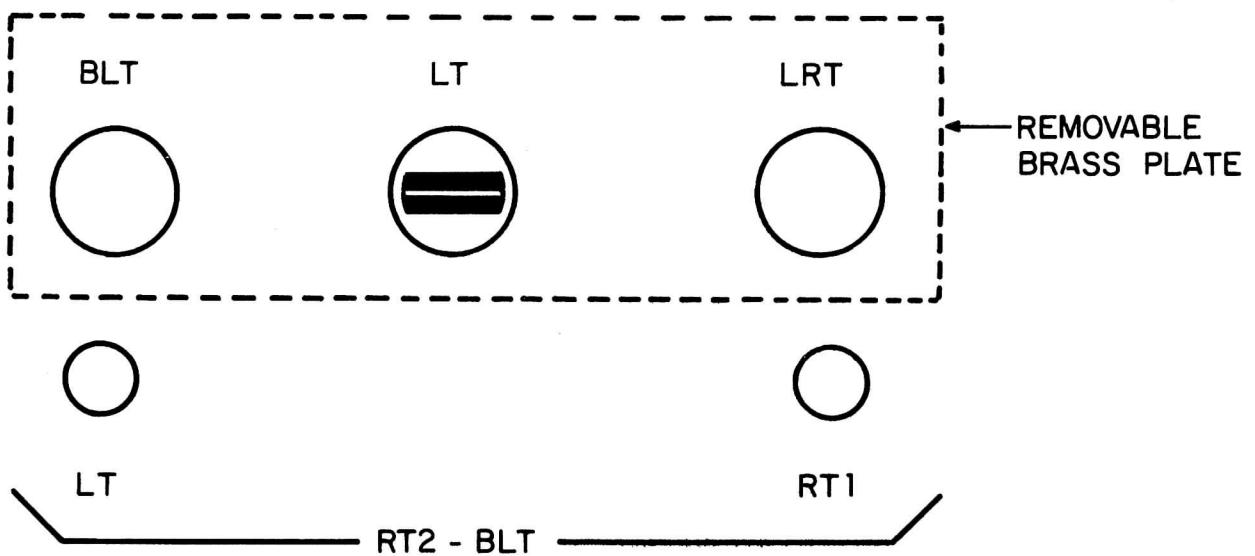


Figure 1-3. Modem Control Panel

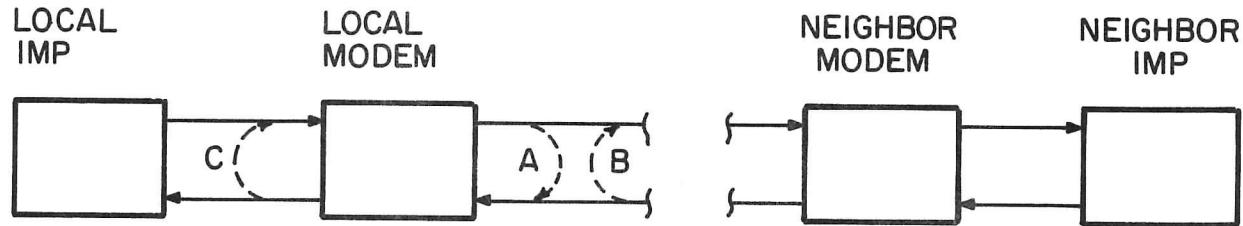


Figure 1-4. Modem Data Paths

To crosspatch the modem so that data follows path A (LT mode—loop test), put the LT switch to its vertical position. To unpatch, return it to the horizontal.

To crosspatch so that the data follows path B (RT1 mode—remote line test), push the LRT button for 10 seconds. You will hear a click. Release the button and light RT1 will come on. To crosspatch so that the data follows path C (RT2 mode—remote data set test), push the LRT button again for 10 seconds. You will hear another click. Release the button and the LT light will also come on. To return to the normal mode, push the LRT button a third time for 10 seconds.

To test the indicator lights, push the BLT button. Both lights should light.

### 1.7 The Multi-Line Controller (MLC) Console

Figure 1-5 is a picture of the MLC console, to be found immediately below the 316 operating console on the Terminal IMP. The MLC console displays the status and contents of the various MLC internal registers and is primarily used for debugging and maintenance. A list of the important lights and their significance to MLC operation is given in Table 1-3.

The panel as shown is divided into two sections. The upper half is associated with the central logic which is common to all MLC lines and interfaces in the computer. The lower half displays the status of an individual MLC line. The line to be displayed is selected by entering the line number into the LINE SELECT switches. The setting of these switches only concerns the display and in no way affects the internal functioning of the MLC.

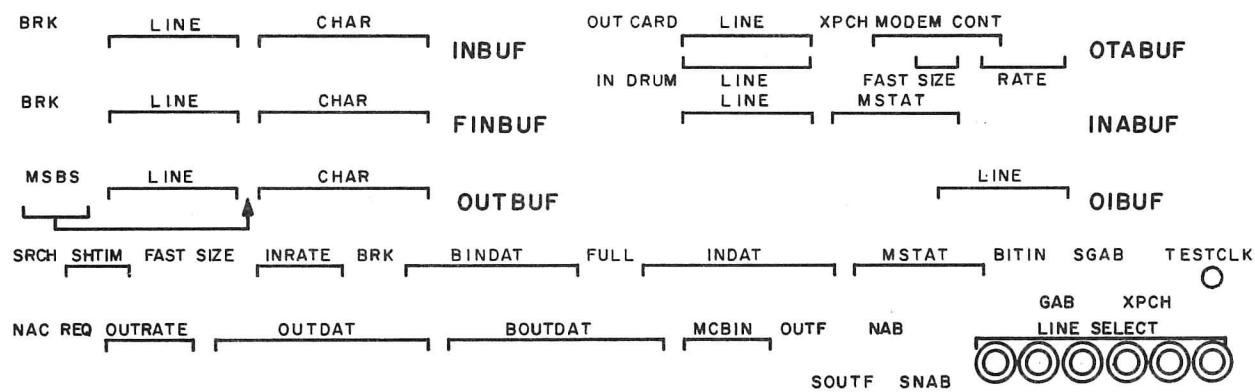


Figure 1-5. MLC Console

TABLE 1-3 MLC CONSOLE INDICATORS

<u>Field Name</u>	<u>Subfield</u>	<u>Bits</u>	<u>Function</u>
<u>Common Logic Information</u>			
INBUF		15	Character information waiting for input to the computer
	BRK	1	Indicates if line is sending break
	LINE	6	MLC line number
	CHAR	8	Character of data
FINBUF		15	Character information waiting for input via the fast channel to the computer
	BRK	1	Same as INBUF
	LINE	6	
	CHAR	8	
OUTBUF		16	Character information just output from computer to MLC
	MSBS	2	Most significant two bits of 10-bit output character
	LINE	6	Same as INBUF
	CHAR	8	
OTABUF		16	MLC control words output from computer by OTA instruction
	OUT/IN	1	Determines whether parameters are for input or output section of MLC
	CARD/DRUM	1	Determines whether parameters are for the LIU card or the pseudo-drum
if CARD is set	LINE	6	MLC line number
	XPCH	1	LIU crosspatch test enabled
	MODEM CONT	4	Control bits to data set through LIU card
if CARD is not set (DRUM)	FAST	1	Input routed through fast channel
	SIZE	2	Character size
	RATE	4	Baud rate

TABLE 1-3 cont'd.

<u>Field Name</u>	<u>Subfield</u>	<u>Bits</u>	<u>Function</u>
INABUF	LINE	12	Status information from MLC to computer
	MSTAT	6	MLC line number
		6	Status from data set via LIU card
OIBUF	LINE	6	MLC line number to be input on out/in channel
<u>Line Specific Information</u>			
(line number selected by LINE SELECT switches)			
FAST		1	Input to be routed through fast channel
SIZE		2	Character size
INRATE		4	Baud rate for input to MLC
BRK		1	Input line is breaking
BINDAT		8	Buffered input data
INDAT		8	Input data shift register
MSTAT		6	Status from data set on LIU card
XPCH		1	Crosspatch test enabled on LIU card
TESTCLK	switch		Serves as synchronous clock when LIU is crosspatched
OUTRATE		4	Baud rate for output from MLC
OUTDAT		10	Output data shift register

TABLE 1-3 cont'd.

<u>Field Name</u>	<u>Subfield</u>	<u>Bits</u>	<u>Function</u>
BOUTDAT		10	Buffered output data
MCBIN		4	Control information to data set on LIU card

Note: Those fields not listed above are for maintenance purposes only.

For further details consult TIP Manual, BBN Report No. 2184.

## 2. TEST PROGRAMS

### 2.1 Honeywell Test Programs for the Standard DDP-516/H316

The following programs are discussed in this section:

High Speed Reader Test	(RPT-2)
Teletype Test	(TWT-1)
Power Fail Test	(PFT-3)
Central Processor Test	(CCT-4)
Memory Test	(CMT-4)

These standard Honeywell programs test the mainframe and the I/O devices. Full documentation is available in the individual Honeywell Verification and Test Program listings. The instructions given below include a description of proper machine operation under these programs; any other operation implies a machine failure. Generally, a failure is indicated by an unusual or unexpected halt.

Please note that the Network Control Center must always be contacted before any non-network program is run in the IMP.

#### 2.1.1 High Speed Reader Test (RPT-2)

- After the program has been loaded, insert the reader test loop into the reader and start the program at  $1000_8$ .
- In response to the Teletype request for "MODE?", type RVD  $\text{CR}$  (carriage return). For "PASS COUNT?", type the desired number of passes, decimal from 1 to 100.
- In case of data error, the reader will halt at the bad character and the Teletype will print "IS XXX SB YYY" to indicate the bad character. Type C to continue or R to reset followed by a carriage return.

- In case of logic error, the Teletype will print an error number and halt. Refer to the Honeywell listing for further information.
- If there are no errors, the test loop will pass through the reader the proper number of times and the Teletype will indicate completion of the test.

### 2.1.2 Teletype Test (TWT-1)

- Start at  $1000_8$  with A register bit 3 set for a 316 and bit 5 set for a 516.
- First, interface functions are tested; the Teletype will print "AA" and ask that "X-OFF" be typed.
- Now the program tests the printer. After the machine halts, press START. The Teletype will print 70 lines containing all characters, rotated by one per line, then one line each of every character.
- Next, the keyboard is tested. The program echoes the string typed on the keyboard terminated by a carriage return.
- Operation of the answer-back drum is tested by program activation. The test checks for the correct number of characters.
- The printer should print nothing during the null character test.
- Follow printer instructions for the punch/reader test. After the punch test, the machine will halt allowing the tape to be loaded in the reader. Put the reader switch in the STOP position. Any halt indicates an error.
- Any particular test can be chosen by starting at  $1000_8$  with A register bit 3 or 5 set for the appropriate machine type and the test routine number bits in 14 to 16. The machine will halt at the end of the test after requesting a new A register setting. Test numbers are as follows:

<u>Test Number</u>	<u>Test</u>
1	Function
2	Printer
3	Keyboard
4	Answer Back
5	Null Character
6	Punch and Reader

### 2.1.3 Power Fail Test (PFT-3)

Tests for the 516 machine will consist of two parts, one for the power fail interrupt and the other for the power fail halt. Whenever a mode selection is made for the program (see below), the 516 PFI/PFH switch should be in the corresponding position (I=PFI, H=PFH). The auto restart should be turned on.

The 316 machine has only the power fail interrupt capability, so only that mode is meaningful.

- Start at  $1000_8$ . On the 516 machine, HALT INHIBIT should be in the off position.
- The program will automatically determine the computer type and the memory size.
- Next, the program asks for "MODE". Type either "I" (for the PFI test) or "H" (for the PFH test).
- Now, turn off machine power either by turning off the circuit breaker or by pulling the power plug.
- Turn power on. For the PFH test, start the 516 at location  $\emptyset$ . For the PFI test, both the 516 and 316 machine should start shortly after power returns (within 20 seconds).
- If the particular mode of test was successfully completed, a "test complete" message will be printed, showing pass count and mode.

- If an error condition exists it will be typed. A computer halt will always follow each error report. Hitting "START" will continue with the printing of further failures (if any) and/or successes. Generally, after each halt associated with an error there is information of use contained in the "A" register. See the detailed listing for its significance.
- Try repeating the test at least once.
- On the 516 machine, set the PFI/PFH switch to PFH and repeat the test for the other mode. Restart at  $1000_8$ .

#### 2.1.4 Central Processor Test (CCT-4)

- Start at  $110_8$ ; HALT INHIBIT on the 516 should be off.
- Test the SENSE switches (SS) by doing the following:
  - \* SS1 on.
  - \* Press START. Bit 1 light should come on in the A register.
  - SS1 off.
  - \* Press START. Bit 1 light should go off.
  - \* Repeat this test for SS2, SS3, and SS4; the respective lights for bits 2, 3, and 4 should go on and off as for SS1.
- After SS4 has been reset, press START. The program will exercise the CPU hardware completely every minute (approximately). Allow several passes, and, if possible, run the test for several hours. A halt indicates an error condition; see detailed Honeywell listing.
- Setting SS1 will cause the program not to relocate to higher sectors but halt after each pass through the first five sectors.

### 2.1.5 Memory Test (CMT-4)

The program starts at  $1000_8$ . On the 516 machine, MEMORY PROTECT should be initially turned off. Later, it can be checked for operability.

If no SENSE SWITCHES are set, locations  $1760$  (octal) through  $XX777$  (where XX is the highest sector in core) are tested and following each pass the program will print the pass count and the locations tested (LO through HIGH).

#### *SENSE Switch Controls*

- 1) SS1: At the end of an ongoing pass the Teletype prints "LO"; to this the operator responds by typing a low (octal) limit value followed by a carriage return. If this limit is improper (such as overlapping the CMT-4 program) the value will not be accepted and a new request for "LO" will be issued. Once an acceptable "LO" has been entered, the program asks for "HIGH" and a suitable high limit should be entered followed by a carriage return. Again, unacceptable values are rejected. If SS1 is not set, the program will test all available core.

If SS1 is left on until the end of the first pass with the newly selected limits, the program will ask for new limits, so be sure to turn off SS1 if repeated operation between the limits entered is to continue. To change the limits, raise SS1 again or restart at  $1000_8$  with all SENSE switches off.

- 2) SS2: If reset, the program will relocate itself after each pass to allow repeated testing of all available core. If SS2 is set, the program remains at its present location at the end of any given pass.
- 3) SS3: When this switch is set, single errors are not printed as they occur; instead they are printed only when 10 errors accumulate.
- 4) SS4: When set, the error buffer which is storing the errors (see SS3) is immediately dumped.

- The program prints out the following for each pass:

PSXXX (pass)	LLLLLL (low limit)	HHHHHH (high limit)	ERYYY (error count)
-----------------	-----------------------	------------------------	------------------------

- Error messages are printed in the following format:

L XXXXXX (location)	SB YYYYYY (correct contents)	IS ZZZZZZ (contents)	PTXX (pattern type) (see Honeywell listing)
------------------------	---------------------------------	-------------------------	---

- After having verified that a 516 type machine passes the Memory Test satisfactorily, the MEMORY PROTECT switch should be put UP and the program restarted from 1000 with SS2 reset. After the first pass, set SS2 to cause a repeating test of lower core. If MEMORY PROTECT is working properly, error messages will be generated for octal locations 60, 62, 1000 - 1777. Putting the MEMORY PROTECT switch down while this is going on should terminate the error indications.

## 2.2 BBN Test Programs

### 2.2.1 NIMPTS (IMP Test Program)

The BBN NIMPTS program is divided into two parts. First are one-time tests of certain special features of the 316 and 516 IMP. Tested on the 516 machine are the status lights, halt inhibit, WatchDog Timer, power fail interrupt, auto restart, real time clock rate, memory protect, and hard-wired IMP number. Tested on the 316 machine are the clock and hard-wired IMP number, since the others do not exist. The MLC option is not tested here (see TIPTST). The main body of the program tests the IMP/Host and IMP/modem interfaces, the real time clock, and the program-forced interrupt, for extended periods.

After completion of the one-time tests, the program initializes all DMC (Direct Multiplex Control -- high speed memory data transfer mode) pointers and interrupt locations, starts the hardware to be tested, and then enters its main loop. The program determines the machine type and sets up certain timing conditions accordingly. As the program is executing the instructions of the main (background) loop, it tests the real time clock to see that the clock is generating interrupts frequently enough. A program-forced interrupt (rather than a jump instruction) closes the loop, and control returns to the beginning of the background loop.

When interrupts occur, the interrupt service routines signify the activity by setting flags. Service routines associated with the data transfer also reset DMC pointers and compare the data received with that transmitted. After enough time has elapsed to permit the occurrence of all interrupts, the background loop checks and resets the interrupt flags.

As messages are passed across the Host-IMP boundary, each message is rounded off to an integral number of Host or IMP words. Details of the padding are given in BBN Report No. 1822, *Specifications for the Interconnection of a Host and an IMP*. This program incorporates a feature that tests whether or not both the Host and IMP are padding properly.

If Sense Switch 1 (SS1) is set while NIMPTS is running, the occurrence of an error will halt the machine, and the error type will be displayed in the B register. However, if this switch is not set, the program will record the total number of errors in the B register, and keep a separate count of certain types of errors. If SS4 is set at the same time as SS1, then not only will the machine halt upon occurrence of the error, but the receive buffer will contain the actual data received, so that any bit or word in error may be located. Not setting this switch (SS4) will put the exclusive-or of the data in the receive and transmit buffers into the receive buffer on the SS1 halt, and thus will alter the receive buffer data.

The program will also save the number of the device interface making the error and the error type, together with the relative time of the error, in locations  $2000_8$  through  $6777_8$  of memory. The resulting table consists of pairs of registers such as :

$2000$	Device/Interface (making error), Error type No.
$2001$	Value of RLTM (elapsed time clock - a relative indication of event chronology)
$2002$	.....

If this table becomes full, only error count totals will be maintained.

The following sections summarize the operation of NIMPTS. Complete operating instructions may be obtained by contacting the Network Control Center at BBN. The NCC should always be consulted before a non-network program is run in the IMP, and the NCC staff will always be willing to assist in any testing phase.

*One-Time Tests*

(All Sense Switches off; 516 Memory Protect off, Halt Inhibit off, WatchDog Timer (W.D.T.) off, Auto Restart off; A and B register configurations entered--see Table 2-1.)

After the NIMPTS program has been loaded, the P/Y register should be set to contain  $7000_8$  and the program started from there. The one-time tests will be as follows:

- 1) 516: The machine should halt immediately with STATUS LIGHTS 1-16 on. The program cannot be restarted by pressing START until HALT INH is turned on. Doing so and toggling SS2 causes the program to enter a loop in which the changing REAL TIME CLOCK is displayed in the STATUS LIGHTS if Sense Switch 1 is off, or if SS1 is on, the octal IMP number is displayed.

The WatchDog Timer is tested next by turning on the W.D.T. switch and toggling SS3. Note the time on a convenient room clock, and observe the counting of interrupts in the B register at 2, 6 and 10 minutes after the start of the test. Error halts indicate that these interrupts are occurring too soon, or that they are too many in number; see Table 2-2. After the third interrupt raise HALT INHIBIT and switch PFI/PFH to PFI.

TABLE 2-1

BIT SETTINGS OF A AND B REGISTERS PRIOR TO STARTING  
 AT  $7000_8$  OR  $10,000_8$  (MAIN PROGRAM)

A REGISTER — CROSSPATCH CONFIGURATION, TYPE OF DATA

<u>Bit</u>	<u>Significance (xpatch = crosspatch)</u>			
1	Do not xpatch modem 1 interface			
2	xpatch modem 1			
3	Do not xpatch modem 2 interface			
4	xpatch modem 2			
5	Do not xpatch modem 3 interface			
6	xpatch modem 3			
7	Do not xpatch modem 4 interface			
8	xpatch modem 4			
9	Do not xpatch Host 3 interface			
$10$	Do not xpatch Host 2 interface			
11	Do not xpatch Host 1 interface			
<u>Bits</u>	14	15	16	
	$\emptyset$	$\emptyset$	$\emptyset$	Do not change data (old buffers reused)
	$\emptyset$	$\emptyset$	1	All zeroes
	$\emptyset$	1	$\emptyset$	All ones
	$\emptyset$	1	1	125252
	1	$\emptyset$	$\emptyset$	52525
	1	$\emptyset$	1	Random data - piece of program
	1	1	$\emptyset$	Use old data
	1	1	1	Use old data

TABLE 2-1 cont'd.

B REGISTER — DEVICES TO BE TESTED

<u>Bit</u>	<u>Significance</u>
1	Test modem 1
2	Test modem 2
3	Test modem 3
4	Test modem 4
5	Test Host 3
6	Test Host 2
7	Test Host 1

SENSE SWITCH USAGE — MAIN LOOP

- 1 Halt on error - type displayed in B register
- 2 Ignore Host - hung errors
- 3 Ignore modem line errors
- 4 Do not clear receive buffers after compare

TABLE 2-2 LIST OF ERROR HALTS IN 516 ONE-TIME TESTS (NIMPTS 46)

<u>Location (octal)</u>	<u>Cause</u>
7012	Load Status Lights failure.
7013	Normal halt for Halt Inhibit test.
7022	Read IMP Number failure.
7027	Load Status Lights failure.
7051	No W.D.T. interrupt after specified time.
7056	Load Status Lights failure.
7062	W.D.T. interrupt too soon.
7066	W.D.T. interrupt too many times (four).
7120	Halt Inhibit failed during a Power Down situation. Thus, Halt Inhibit was not overridden.
7132	Power Failure Interrupt failed.
7136	W.D.T. Power Down came too late.
7141	W.D.T. Power Down came too soon.
7154	Real-Time Clock is slow or Mainframe is too fast.
7157	Real-Time Clock is fast or Mainframe is too slow.
7256	Memory test failed.*
7323	Memory test failed.*

\* The address of the word failing the MEMORY PROTECT TEST can be determined as follows (for a halt at 7256):

$$\text{ADDR} = C \text{ (Loc. 7275)} + C \text{ (Loc. } \emptyset\text{)}$$

(bits 3-16) (index register contents)

For a Halt at 7323 use 7331 instead of 7275 to find address.

The following features are now tested: WatchDog Power Down, Power Fail Interrupt, Halt Inhibit Inhibit, Auto-Restart. Twelve minutes from the start of the WatchDog Timer Test, the IMP should power down. If the STATUS LIGHTS start flashing, the power down is late. Once the machine powers down, raising the POWER ON switch should have no effect. Now, turn off W.D.T. and HALT INHIBIT, and turn on AUTO RESTART. Open the IMP door and push the RESET button on the POWER DISTRIBUTION UNIT. The IMP should power up and self-start within one minute.

If the machine comes on and appears to halt immediately (RUN LIGHT off), then the override of HALT INHIBIT during a "power failure" is not being accomplished properly (HALT INHIBIT inhibit). If this occurs, set the P/Y register to two more than its present contents and restart the machine to continue with the other tests; see Table 2-2.

The Real-Time Clock rate is now tested. Error halts indicate that the clock is too slow or too fast; see Table 2-2. When the P/Y lights stabilize, turn off MEMORY PROTECT and briefly raise SS3. Error halts now indicate failures in the memory or the MEMORY PROTECT logic. Otherwise, the program now enters its main loop.

- 2) 316: With SS1 turned on, the IMP NUMBER should be displayed in the A register; with SS1 off the changing REAL TIME CLOCK is displayed in A. Toggling SS3 on and off briefly causes the program to enter its main loop.

A halt at 7022 indicates that the Read IMP Number command failed.

*Tests in the Main Loop*

If A and B register settings were not entered prior to the one-time tests, halt the machine and select a crosspatch configuration in the A and B registers (see Table 2-1) and start at P/Y =  $10000_8$ . The main loop is essentially a timing loop that is interrupted by the selected devices. Each time the program passes through the main loop, it increments a pass count and checks the real-time clock to see that it has not changed by an unreasonable amount. After checking the clock, the program returns to the beginning of the main loop via the program-generated forced interrupt. When the program has looped 177777 times (more than 1.5 seconds), it checks all interrupt flags for the occurrence of interrupts from all devices under test. It then sets the flags and resumes execution of the loop. Displayed in the STATUS LIGHTS (on 516 only) will be the real-time clock contents at the time of its interrupt. This will cause the lights to appear to be counting.

While the program is running in the main loop, asynchronous interrupts occur. If any of these interrupts occur from devices not under test, the unwanted interrupts will be processed by appropriate error routines. Legitimate interrupts are processed by routines whose addresses were deposited in their respective interrupt locations during initialization. When the program enters an interrupt location, flags are set to denote the occurrence of that particular interrupt. If the hardware is operating properly the only active interrupt lines should be those servicing the Host and modem interfaces (to receive and transmit data) and the program-forced and power-fail interrupts.

If a modem interface is being tested, data in the transmit buffer area are passed out through the IMP-modem interface and received through a modem-IMP interface. The two interfaces may either be directly crosspatched or be looped on the line side of the modem. After the transfer to the input buffer has been completed, NIMPTS resets the DMC pointers in preparation for the next data transfer. Received data are compared with the data in the transmit buffer area, and unless SS<sup>4</sup> is set, the receive buffer is cleared. If the data aren't identical, the program will generate an error message. Because the contents of the transmit buffer are known and do not change after they are set up, the test program can also detect when the received checksum is not revealing data errors. Data errors are, then, of two kinds, either undetected by the checksum hardware or detected and denoted by a checksum error in addition to the data error. The error that must be avoided is that of bad data being mistaken for good because of a checksum hardware failure.

In principle, the test program handles the data transfer process identically for the Host/IMP interaction as for the modem/IMP interaction, but one must also consider the effect of padding Host or IMP words. Data passed across the Host/IMP boundary require padding that should be supplied by both the Host and IMP hardware as described in BBN Report #1822. If the unpadded contents of the transmit buffer in the data source are known, one can calculate the padding that should be supplied by both the Host and the IMP hardware. Appending the calculated amount of necessary padding to the contents of the transmit buffer enables a direct comparison with the data of the receive buffer.

NIMPTS has the capability to allow either the Host or the IMP to act as the data source; thus, both IMP and Host padding hardware can be tested from either side of the Host/IMP boundary. However, only the IMP side padding test will be performed under control of the BBN test program. This test takes the data from the transmit buffer in the IMP (i.e., the Host transmit buffer) and sends them through the IMP-Host interface; incoming data come through the Host-IMP interface where IMP padding is added to the Host input buffer. These interfaces may be tested by cross-patching or by passing data through the Host.

If the data are being passed through a Host\*, the operator must set a location in the padding routine to contain the (octal) number of bits in a Host word; otherwise, the program assumes crosspatching. The program calculates the padding added by Host and IMP and adjusts the buffer pointers; the Host-in interrupt routine processes the data. A rigorous test of the IMP/Host bit-passing capability can be accomplished by halting the Host while data are being transferred through it. To avoid registering an error while the Host is hanging, set SS2 to leave the Host-in and -out flags untested. The program assumes that the Host will return to the IMP information identical to that which was received, plus Host padding.

To perform the Host side padding test, the operator must start the IMP at a specified location. Doing so will initialize various locations and pointers, and the IMP will do an out to the Host for every in performed. The IMP will hold the received data in the same buffer area from which data are returned to the Host. The Host must be programmed to allow proper processing of the data.

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\* for procedural assistance please contact BBN

While the program is processing interrupts as they occur, errors may arise from various sources. These errors are processed either directly by the main error routine, or indirectly through an intermediate error routine. Error routines are entered through a jump and store location (JST) command that allows returning to the original point in the program. When entered directly from the main program, the main error routine selects the location stored at its beginning, places this location on the error return list found in locations 2000 to 6777, and then increments the overall error count. When the main error routine is entered indirectly through an individual error subroutine, the corresponding individual error count is incremented and the location that caused a JST to the individual error subroutine is recorded on the error return list. To halt when an error occurs, set SS1.

*Explanation of Error Types in the Main Loop*

In the introduction to NIMPTS an error list starting at location 2000<sub>8</sub> was described. That list occurs in two formats:

List Type 1: Even location (e.g., 2000) — contents 0XYY, where X represents bits 8-10 and signifies the channel number (see Table 2-3). YY represents the error type in bits 11-16; see Table 2-4.

Odd location — contains the value of real time in arbitrary units of time. This location is the one just after the channel/error type location.

List Type 2: Even location — contents 00YY; Y represents the error type only (see Table 2-4). Bits 11-16 only.

Odd location — real time as above.

TABLE 2-3

NIMPTS Device Numbers

Channel #	1	Modem 1
	2	Modem 2
	3	Modem 3
	4	Modem 4
	5	Host 3
	6	Host 2
	7	Host 1

TABLE 2-4

## ERROR LIST FOR MAIN LOOP

<u>Error No.</u>	<u>List Type</u>	<u>Explanation</u>
Ø0	2	<u>Real-Time Clock-Increment Error.</u> The routine called by the RTC interrupt found that the interrupt either came too soon or too late. Not quite the same as type No. 4.
Ø1	1	<u>No Receive Interrupt.</u> The receive section of the device under test has not interrupted during the current timeout period.
Ø2	2	<u>No Transmit Interrupt.</u> The transmit section of the device under test has not interrupted during the current timeout period.
Ø3	2	<u>No RTC Interrupt.</u> The clock has not interrupted during the current timeout period.
Ø4	2	<u>Real-Time Clock Increment Wrong.</u> The RTC changed by an unreasonable amount between two successive passes through the loop.
Ø5	2	<u>Task Interrupt Failed.</u> The program forced interrupt instruction failed and the ENB instruction following the return point was destroyed.
Ø6	2	<u>Task Interrupt Failed.</u> The program forced interrupt instruction failed, but the ENB instruction was not destroyed.
Ø7	1	<u>Transmit DMC Error.</u> Transmit buffer pointers did not meet.
Ø8	1	<u>Transmit DMC Error.</u> Transmit buffer pointers crossed.

TABLE 2-4 cont'd.

<u>Error No.</u>	<u>List Type</u>	<u>Explanation</u>
11	1	<u>Receive DMC Error.</u> The receive buffer was shorter than expected.
12	1	<u>Receive DMC Error.</u> The receive buffer was longer than expected.
13	1	<u>Modem Checksum Error.</u> The checksum hardware has detected a difference in the checksum generated by an interface for receive and transmit. A data error indication should normally accompany this.
14	1	<u>Undetected Data Error.</u> Data errors are occurring without checksum errors, indicating that the error was not detected by the checksum.
15	1	<u>Data Error.</u> The program detects interface errors by exclusive-oring the receive and transmit buffers.
16	2	<u>Unwanted Interrupt.</u> An unused interrupt line has signalled an interrupt.
17	1	<u>Unwanted Receive Interrupt.</u> A Host or modem not under test has generated an interrupt.
20	1	<u>Unwanted Transmit Interrupt.</u> See Unwanted Receive Interrupt.

Another list that may be of convenience when several types of errors occur is that starting at location  $500_8$ . The number of occurrences of error type N is found at location  $500$  plus N. Thus, at location  $510$ , we can find the number of occurrences of a type 10 error. The error numbers are octal. The "Error List for Main Loop" relates the error number to the list type (i.e., the list format type for the error table starting at  $2000_8$ ) and a meaning is supplied for that type of error.

### 2.2.2 TIPTST (Terminal IMP Test Program)

The BBN TIPTST program is concerned with testing the functions of the Multi-Line Controller (MLC) and the connections between the MLC and the CPU of the TIP. TIPTST, like NIMPTS, has two parts. The first consists of the one-time tests which individually test several of the features of the MLC to facilitate debugging. The main body of the program exercises the majority of the MLC logic by inputting and outputting characters through the various lines.

In the main loop, the user may set several parameters to define the test environment. Each of the lines may be placed in a crosspatch made such that characters output on that line are routed for output on other lines. In this manner, characters may be passed "around" the MLC, utilizing any selected combination of lines. Error-checking facilities log and display any discrepancies that may occur. Parameters may be changed at any time to help localize difficulties. Default options exist for all parameters which can be used for a general test.

#### *One-Time Tests*

This section tests the MLC clock rate, the clock and output completion interrupts, the character rate and size mechanisms,

the break bits, the DMC and INA/OTA logic, and the console lights. After the program is loaded (see Section 1.4), the computer should be started at 2000. The machine should then halt at 7000. Set the console LINE SELECT switches to 77 (all up) and compare the status of the lights to Figure 2-1. All lights indicated with a '+' should be on and all with a '-' should be off. Press START and the machine should halt at 7002. Set LINE SELECT to 00 (all switches down) and again compare the lights with Figure 2-1. Now all '-' lights should be on and '+' lights off. In both cases ignore the status of all lights indicated with an 'x'. Pressing START resumes the remainder of the one-time tests. Upon successful completion of the one-time tests, the main section of the program (described below) is entered.

Any halts other than those mentioned above are errors. The halt locations and the associated errors are given below:

- 7000 - normal halt — see above
- 7002 - normal halt — see above
- 7004 - no clock interrupts
- 7005 - no output completion interrupts
- 7006 - MLC clock slow or 316 fast
- 7007 - MLC clock fast or 316 slow
- 7010 - data errors in size test
- 7011 - INBUF break bit not being set
- 7012 - FINBUF break bit not being set
- 7013 - MLC character rate fast
- 7014 - MLC character rate slow
- 7015 - Flush error

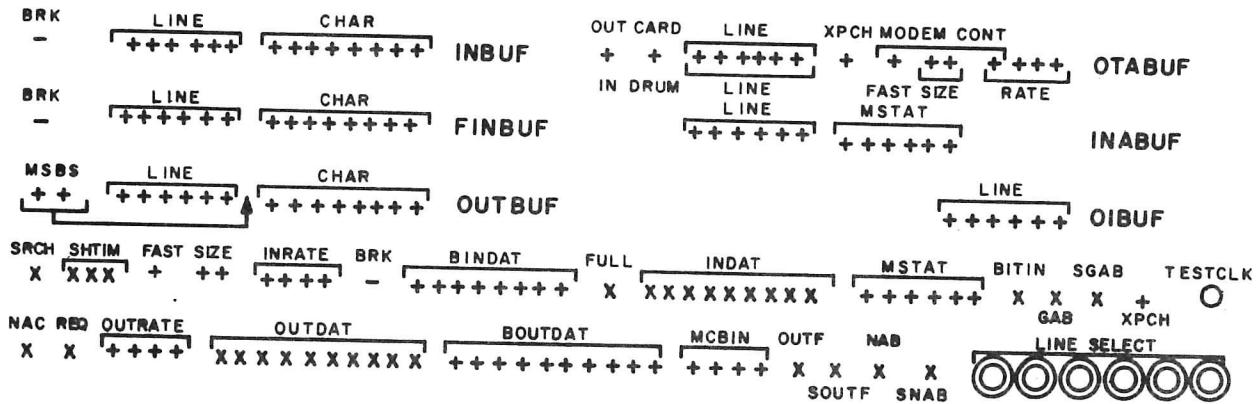


Figure 2-1. MLC Console Lights

*Main Loop*

This portion of the program may either be entered automatically upon completion of the one-time tests or directly by start-in at location 3000. An asterisk will be printed on the Teletype indicating that dialog mode has been entered. In this mode the user may set up or modify any of the parameters by entering commands on the Teletype. As each command is accepted, an asterisk prompt will be echoed. Commands may be aborted by typing a rubout. All numbers are entered as two-digit octal numbers. A list of the commands which may be used follows:

- |                                |   |
|--------------------------------|---|
| An <sub>1</sub> n <sub>2</sub> | If n <sub>2</sub> is 01, makes line n <sub>1</sub> a character generator--the character in that line's buffer will be continually output. An n <sub>2</sub> of 00 turns off that line's generator.  |
| C                              | Clears all goto's (see G).  |
| D                              | Jumps to DDT (DDT command R returns to the program).  |
| Fn <sub>1</sub> n <sub>2</sub> | Sets the FAST bit of line n <sub>1</sub> to n <sub>2</sub> ; n <sub>2</sub> must be 00 or 01.   |
| Gn <sub>1</sub> n <sub>2</sub> | Specifies a goto: any input arriving on line n <sub>1</sub> is routed to line n <sub>2</sub> for output. Every line which is desired to be set up must be the first argument in a G command. An n <sub>2</sub> of 80 clears line n <sub>1</sub> --it will not be set up and no data will pass through it, regardless of other commands. |
| Hn <sub>1</sub>                | Sets up each line as an individual echoer with rate n <sub>1</sub> .  |

L Resets all crosspatches to on, turns off all character generators, and sets character size and rate to 8 and 110 respectively.

P Proceed: causes a general reset and then all specified lines are set up to the latest parameters.  
Dialog mode is exited and the main loop is entered.

Q Causes a printout of the number of errors accumulated followed by the errors themselves. For each error, the first two numbers are the two words of the elapsed time (in 3 msec increments) that the error occurred. The high order bit of the first number printed denotes the error type and the content of the remaining numbers as follows:

Type Ø: Data Error

character checked against  
actual input character

Type 1: Overflow

character which caused the line buffer to overflow

Printout may be halted with Sense Switch 2. If no errors have been logged, the bell is rung.

R<sub>n<sub>1</sub></sub>n<sub>2</sub>

Sets the character rate of line n<sub>1</sub> to n<sub>2</sub>.

<u>Rate (baud)</u>	<u>n<sub>2</sub></u>
75	Ø1
11Ø	Ø2
134.5	Ø3
15Ø	Ø4
3ØØ	Ø5
6ØØ	Ø6
12ØØ	Ø7
18ØØ	1Ø
24ØØ	11
48ØØ	12
96ØØ	13
192ØØ	14
synchronous	17

S<sub>n<sub>1</sub></sub>n<sub>2</sub>

Sets the character size of line n<sub>1</sub> to n<sub>2</sub>.

<u>Size (bits)</u>	<u>n<sub>2</sub></u>
5	ØØ
6	Ø1
7	Ø2
8	Ø3

T<sub>n<sub>1</sub></sub>n<sub>2</sub>

Specifies that the low order 4 bits of n<sub>2</sub> be sent out on the modem control lines of line n<sub>1</sub>.

X<sub>n<sub>1</sub></sub>n<sub>2</sub>

Sets the crosspatch bit of line n<sub>1</sub> to n<sub>2</sub>. n<sub>2</sub> must be either ØØ or Ø1. If crosspatch is set, all characters output on that line will be input. External input will be ignored. The crosspatch bit also enables the TSTCLK button if the line is set to synchronous rate.

Z        Resets the clock and clears all errors.

The correct error count is displayed in the B register.

When the user has finished entering commands, he executes a P command to begin testing. He may reenter dialog mode at any time by depressing Sense Switch 1.

#### *General Tests*

A general test may be entered by utilizing the defaulted conditions loaded with the program. All 64 lines will be tested and the appropriate terminals may be connected to any line to observe the test stream. The terminal type is specified by the program start address as follows:

3000 - normal start

3001 - ASCII Teletype 110 baud

3002 - correspondence IBM 2741 134.5 baud

3003 - BCD IBM 2741 134.5 baud

While conducting a general test, errors will be logged as usual. The user may toggle Sense Switch 1 to enter dialog mode.

### 3. THE OPERATIONAL IMP PROGRAM

#### 3.1 Loading, Normal Operation and Halting

The IMP/TIP should be taken down or reloaded only with the approval of the Network Control Center. The NCC staff will gladly assist in the event of user difficulties.

##### 3.1.1 Loading and Normal Operation

The IMP memory can be in one of three states of preparedness for running the operational IMP system program (IMPSYS). The procedures below describe each method of bringing the IMP (or TIP) up on the network.

The most prepared state exists when the IMP program has previously been loaded in some manner and now waits, intact, in memory, to be turned on. In this case, set all the switches according to Table 3-1 and start the IMP at 2000<sub>8</sub>.

After a few seconds, the STATUS LIGHTS (516) or B register (316) should stabilize to a reasonable pattern (see Table 3-2). The P/Y register should stabilize at about 3000 with higher order bits flashing about every 1/2 second.

The next most prepared state exists when the operational network IMP program has previously been loaded but may or may not be intact. If the reload portion of the program is intact it is possible to get a new copy of the system from a neighboring IMP. To do so, set all the switches according to Table 3-1 and start the IMP at 1003<sub>8</sub>.

The reload program trying to get a fresh copy of the system program appears to be cycling in the lower half of the P register

TABLE 3-1  
NORMAL SETTINGS OF SWITCHES FOR  
RUNNING OPERATIONAL SYSTEM

(see Figures 1-1, 1-2 for 516, 316 respectively)

SS 1-4 (all machines)	all off
PFI/PFH switch (516 only)	up (PFI position)
AUTO RESTART switch (516 only)	up (on)
WDT switch (516 only)	down (off)
MEMORY PROTECT switch (516 only)	down (off)
HALT INH (516 only)	down (off)

TABLE 3-2  
FUNCTIONS OF STATUS LIGHTS (516) OR B REGISTER (316)

<u>Status Light</u>	<u>All Lights Normally Off</u>
1	lit indicates modem channel 1 dead
2	lit indicates modem channel 2 dead
3	lit indicates modem channel 3 dead
4	lit indicates modem channel 4 dead
5	Host 1 dead
6	Host 2 dead
7	Host 3 dead
8	Host 4 dead
9	unused
10	unused
11	unused
12	unused
13	unused
14	unused
15	unused
16	blinks if any modem is looped
17 - 24	unused

every 5 seconds. If it succeeds, the normal IMP system flashing will be noticed (every 1/2 second in the P register upper half).

If reload from  $1003_8$  fails to bring the IMP back up on the network in a few minutes, assume that the reload program in the IMP is not intact. It will then be necessary to restore it by loading in a paper tape called IMPLOD\*. Follow the tape loading procedure in Section 1.4 to load in IMPLOD. Then, start the IMP again at  $1003_8$ . After the machine stabilizes running the operational program, set switches according to Table 3-1. To verify that the system is up, turn on the Teletype and type 1/. The Teletype should respond by typing  $10057$ .

### 3.1.2 Halting

To take a properly running IMP down gracefully, put SS3 on and take the 516 HALT INH switch down. After about thirty seconds, the system will halt. Do not forget to put these switches back to their normal setting before restarting the system.

*The next two sections (3.2 and 3.3) describe the operation of many special IMP features. Users who are concerned with the IMP merely as a communications device may skip these sections.*

*The sections in no way refer to the Terminal IMP System program, TIPSY.*

---

\* On a 516, memory protect must be off (down) to load the IMPLOD tape into core.

### 3.2 Operating the IMP Background Programs

When operating IMP Background Programs from the IMP Teletype, one may compose and transmit messages to Hosts and other IMPs, print messages from other sites, and inspect and change core on the local IMP or a remote IMP. This section describes how to operate these features. BBN Report No. 1822 discusses the message formats for communicating with the Background Programs.

#### 3.2.1 Printing Messages on the IMP Teletype

Receiving and printing messages requires little operator intervention -- messages simply type out on the IMP Teletype. The only special operator intervention that may be required is that of typing an extra line feed to advance the paper after a message has been received. This procedure is necessary only when the person transmitting the message has forgotten to include a line feed in the message.

Messages are printed in one of two forms. If the octal-print bit ( $10000_8$  bit) has been set in the first leader word of the message, the receiving IMP will print the octal representations of both leader words and the octal representation of all of the body of the message, one word per line. The IMPs know nothing of marking conventions and treat all marking as data. If the octal print bit has not been set in the message leader, the IMP will not print the leader and will interpret the body of the message as successive 8-bit ASCII characters (see Appendix B), which will be printed literally (e.g. separate carriage returns and line feeds) on the Teletype.

### 3.2.2 Sending Messages from the IMP Teletype

There are two methods of composing messages from the IMP Teletype. The Teletype program (TTY) normally transmits each character typed on the Teletype as a separate message with a standard leader. This leader normally specifies the destination as the DDT program at the local IMP. One can change the leader to specify any other destination by using the crosspatch debug command, C, and can reset it to the nominal value by typing SHIFT-CONTROL-P. Thus, if nC is typed on an IMP Teletype, all characters subsequently typed on the Teletype (with the exception of those bracketed by semicolons - see below) are sent to destination n as one-character messages. If n has the form 4Øijj, the one-character messages will be sent to Host i at site jj. If n has the form ØØijj, the messages will be sent to IMP Background Program i at site jj. To have the characters typed out on the destination IMP Teletype, set i to Ø so that the leader will read ØØØjj.

TTY treats *all* text strings that are bracketed by semicolons (even when the Teletype is crosspatched) as special messages, and uses a different leader (established by the leader debug command, "L") for them. Occasionally, it will be desirable to construct a FROM-TTY message containing a bit sequence that is difficult to enter as ASCII text - e.g., an octal number or a semicolon character. Whenever a colon is typed in a FROM-TTY (semicolon format) message, the characters entered up to the next carriage return are interpreted as a 16-bit octal number.

Examples of the use of the semicolon feature follow. The user types 3,4ØØL. This sets up a leader for subsequent semi-colon-bracketed messages. The octal number preceding the comma

is the first leader word. The octal number after the comma is the second leader word. Thus, the above leader indicates that semicolon messages are to go to site 3 on link 1.\* The user types

```
;HI CR LF  
; CR LF
```

to send characters "H", "I", CR (carriage return), and LF (line feed) in a message having the above leader.

If the user types

```
40002,0L
```

he sets up a semicolon message leader to the IMP Teletype at destination 2 over link Ø. If the user then types

```
;:1      each line terminated by a  
:12  
:4      carriage return,  
;  
;
```

he sends a three word message with the preset leader.

To send a semicolon message to a Host, one must set the first leader word, by using the L command, to the form ijj, meaning to Host i at site jj. For transmission to an IMP Background Program, the first leader word should have the form

---

\* N.B. The link number is in the left 8 bits of the second leader word.

40ijj\* -- in particular, the first leader word of a message to the IMP Teletype at site jj should have the form 400jj.

In the two previous examples, the user is actually setting up message leader words that have many other meaningful bits. The reader is referred to BBN Report No. 1822 for the meaning of these other bits.

Since ; and : have special uses in the system, one should avoid typing these characters in other contexts. If you type a semicolon by mistake, you should type another to correct the error. To correct a colon mistake, you should type a carriage return. Note that semicolon messages must be enclosed in semicolons to prevent the text from being interpreted as commands to the system DDT. Note also that the terminating semicolon must be typed within 15 seconds of the first, or the IMP's "Host" logic will "time out" and discard the entire message.

### 3.2.3 Inspecting and Changing IMP Core - The IMP DDT Program

The IMP DDT program (not to be confused with the Honeywell DEBUG test tape) is primarily a tool for debugging the IMP operational program. For instance, DDT allows core to be inspected while the system is running. We have already discussed two DDT commands, L and C, but the program's primary use is to inspect IMP memory. To inspect a particular memory location, type <octal memory location> / . The system will

\*This is the *normal* use of the FOR IMP bit; the C command sets up a leader with the FOR IMP bit sense reversed for operational convenience.

respond with the octal contents of the memory locations on the IMP Teletype. We have already seen an example of this when we type l/ to see if the system is running. We now see that 10057 is the contents of location 1, which is said to be open -- i.e., can be changed. Once a location has been examined, you may type ↑ to examine the previous location and type ↓ to examine the next location. In both these cases, the contents of the new location will be displayed, the location that was open will be closed, and the newly displayed location will be opened. Typing ¶ at any time during this procedure merely closes the open location (if any) and causes a carriage return and a line feed to be printed. This is a good way to get back to the left margin.

The octal memory location preceding the / above could actually have been an arithmetic expression involving addition and subtraction. Thus, typing

300+20-4/

displays the contents of location 314<sub>8</sub>. (Spaces can be substituted for plusses.)

In the DDT program, a period may be used in address computations as above. In such cases the period has the value of the last opened location. Thus typing\*

l/ 10057 ¶  
.+100/

displays the contents of location 101<sub>8</sub>. This method is most often used to reexamine the contents of a location that has just closed by mistake, e.g., ./.

---

\* Underlined characters represent user input.

The back arrow has the value of the last number typed by DDT. Thus, typing

123/456 ←+2 #

adds two to the contents of location 123.

Typing RUBOUT at any time causes DDT to discard everything typed to it since the last time it typed to the user. The system responds to RUBOUT by typing a sharp sign (#). An alternate method for correcting a typing error is to type a series of zeros and then the correct data. For example, since only the low-order 16 bits of any expression are meaningful, 123000004 is equivalent to 4.

Any time a location is open, the contents of that location may be changed by typing the new contents (an expression possibly containing symbols with special values) and then closing the location. Thus, if the user types

100/ 123 456 ↵

the contents of location 100 are changed from 123 to 456 and location 101 is opened.

The rest of the DDT commands are single letter commands preceded by an appropriate number of arguments, which are separated by commas - e.g., the L and C commands. The arguments can be arithmetic expressions.

al,a2W                  Print the contents of locations al through a2.

al,a2L                  Set up a leader for semicolon messages with leader words al and a2.

alC	Set up a leader for character from Teletype messages with the first leader word al, "exclusive-ored" with $40000_8$ and the second leader word $\emptyset$ .
TC	Crosspatches to the IMP TTY which was last (is) crosspatched to this DDT.
T=	IMP TTY which last crosspatched to this DDT.
al,a2,a3Z	Store al in locations a2 through a3.
al,a2,a3,a4E	Print location and contents of locations between a3 and a4 that are the same as a2 in the bit positions indicated by ones in al.
al,a2,a3,a4N	Print location and contents of locations between a3 and a4 that are not the same as a2 in the bit position indicated by ones in al.
al,a2H	Same as L.
al,a2,a3S	Load X register with al, A register with a2 and start machine at a3.
Q	A mode switch which turns off DDT output (but not DDT input). Each time Q is typed, the mode is reversed.

If any of the arguments to the above commands, excluding the S command, are omitted - e.g. ,a2,,a4E - any previous values for those arguments will be employed. For the S command, the previous value of only the P register is available.

To stop an executing command (e.g., W), hold down the break key for a few seconds.

DDT cannot do potentially destructive things with SS4 off. Thus, to have the S, Q, and Z, and word change functions work, SS4 must be turned on. Normally this switch should be off and the status of this switch is monitored and sent to the Network

Control Center. Any time a command cannot be executed because of the position of SS4, DDT types a sharp sign (#). Consult the NCC before turning on SS4.

### 3.2.4 Two Debugging Aids

Occasionally it is useful to see the *exact bits a Host sends to an IMP* or to see the *leaders of messages arriving at the IMP*. Both of these are possible using mechanisms available with a call to the Network Control Center. See Section 3.6 in BBN Report No. 1822, *Specifications for the Interconnection of a Host and an IMP*.

## 3.3 Special Procedures for Network Measurement and Control Centers

Both the Network Measurement Center (NMC) and the Network Control Center (NCC) will need to send messages to IMP parameter change programs. The NMC will usually send these messages from the Host, while the NCC usually sends them from the IMP Teletype.

To send messages to a parameter change, SS2 on the source IMP must be on. If a message is sent to a parameter change with SS2 down, a destination-dead message will be returned to the Host or IMP Teletype. SS2 should be on only at the NMC or the NCC and should be on only when parameter change messages are being sent frequently. The status of SS2 is monitored and reported to the NCC.

Following is a list of IMP parameters that may be changed by parameter-change messages.

TABLE 3-3  
IMP PARAMETERS

<u>Parameter # (octal)</u>	<u>Parameter Name</u>
Ø	trace on flag
1	snapshot on flag
2	cumulative statistics on flag
3	message generator on flag
4	unassigned
5	reserved - used by IMP system internally
6	unassigned
7	trace leader - word 2
1Ø	snapshot leader - word 2
11	cumulative statistics leader - word 2
12	message generator leader - word 2
13	unassigned
14	reserved
15	trace leader - word 1
16	snapshot leader - word 1
17	cumulative statistics leader - word 1
2Ø	message generator leader - word 1
21	unassigned
22	reserved
23	autotrace frequency
24	snapshot frequency
25	cumulative statistics frequency

TABLE 3-3 cont'd.

<u>Parameter # (octal)</u>	<u>Parameter Name</u>
26	message generator frequency
27	unassigned
30	reserved
31	message generator length
32 - 37	unassigned

The following, if typed at an IMP Teletype, will send a parameter change message.

```
40205,6000L      turn cumulative stat on
;:2
:1
:17               leader word 1
:2
:11               leader word 2
:4000
;
```

The first line sets up a leader for a from-TTY message for parameter-change, fake Host number two, at site five, and over link  $1^4_8$ . Since parameter change expects pairs of words specifying a parameter number and a value for that parameter, this message will turn on the cumulative statistics program at IMP 5, which will send these statistics to Host zero at site 2 on link  $10_8$ . Within one message, the order of setting up parameters is unimportant.

When an IMP is restarted, its parameters are all reset to zero.

#### 4. PHYSICAL DETAILS

##### 4.1 Cabling (For Reference Purposes Only)

Connection of the IMP control and data signals to and from the modems, the Host Special Interface, the high-speed paper tape reader, and the Teletype are made via cables from each of the devices to the IMP. The 516 cables all enter on the rear connector panel. The 316 has no connectors, and cables mate with the regular drawer slots.

Figure 4-1 shows the 516 rear connector panel; Appendix A describes the pin assignments for the Host and modem connectors. The 316 has paddle connectors which are referenced in the Honeywell logic block diagrams (LBDs).

Terminal IMP users should refer to the specifications for terminal connection to the Terminal IMP (BBN Report No. 2277) for a description of the cabling involved when connecting a terminal to the TIP.

Be sure the AC line cords for the IMP, the paper tape reader and the Teletype are plugged in.

##### 4.2 System Hardware Layout

Figure 4-2 illustrates the location of the major assemblies and their reference designations in the 516 machine.

Table 4-1 and Figure 4-3 show the location of the major functions in the 516 IMP.

Figures 4-4 and 4-8 show the scheme for locating an individual  $\mu$ -pac and for finding its associated pin connections in

the logic block diagrams (LBDs) provided with the system.

Figure 4-5 shows the location of the major assemblies in the Terminal IMP and the 316 IMP.

Figure 4-6 and Table 4-2 illustrate the location of the major functions of the 316 IMP and TIP. Figure 4-7 accompanied by Figure 4-8 show location of individual  $\mu$ -pacs and their associated pin connections. Figures 4-9 through 4-11 show layout and pin designations for the MLC common logic drawer and the LIU rack in the Terminal IMP.

On the 316 machine no connection of 24 VDC power control is made to the Teletype or the high speed reader.

#### 4.3 The Multi-Line Controller Power Supply Panel

The MLC power supply panel (see Figure 4-12) is located on the rear of the power supply assembly. The toggle switch controls the main AC power and lights the neon lamp. The main AC line fuse is contained in the indicating holder. The DC fuses, located immediately to the right, can be accessed by raising the hinged panel. The failure of any DC fuse will cause an alarm to sound; immediately unplug the machine upon hearing this. This will stop the alarm as well as prevent possible damage.

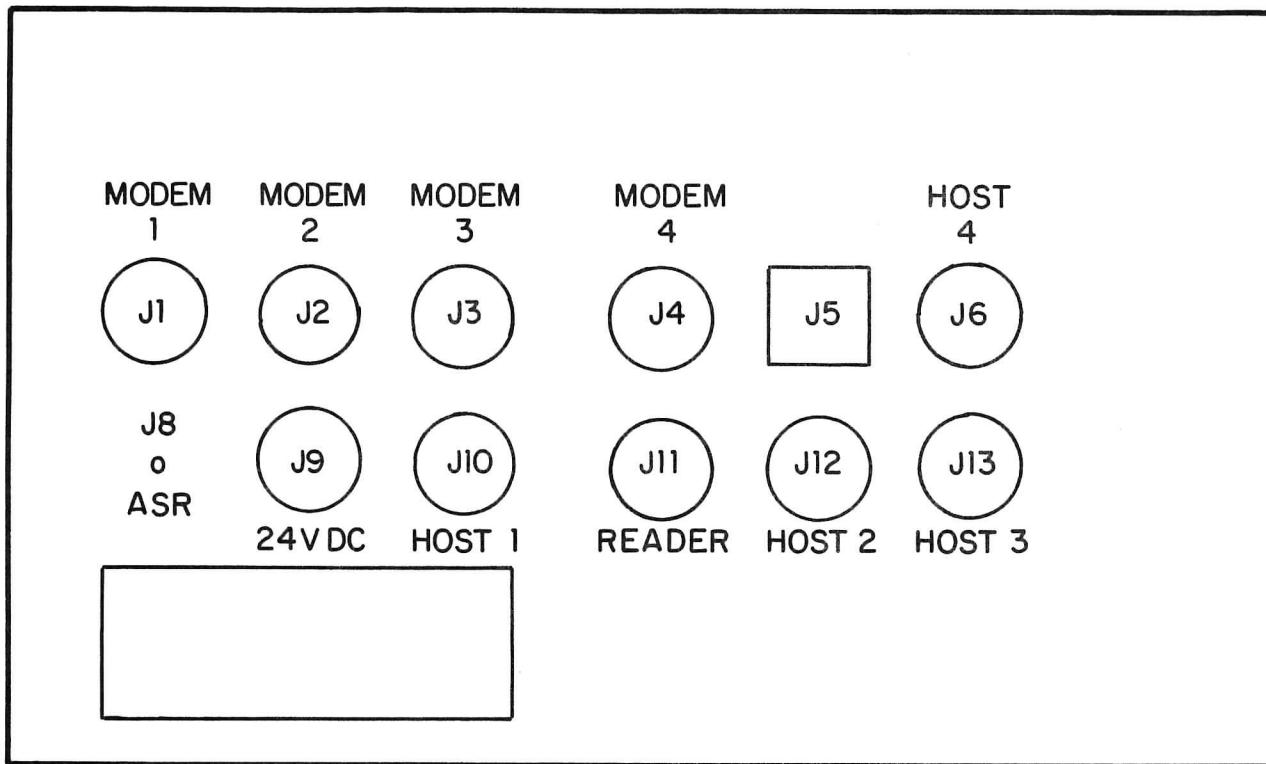


Figure 4-1. 516 Rear Connector Panel

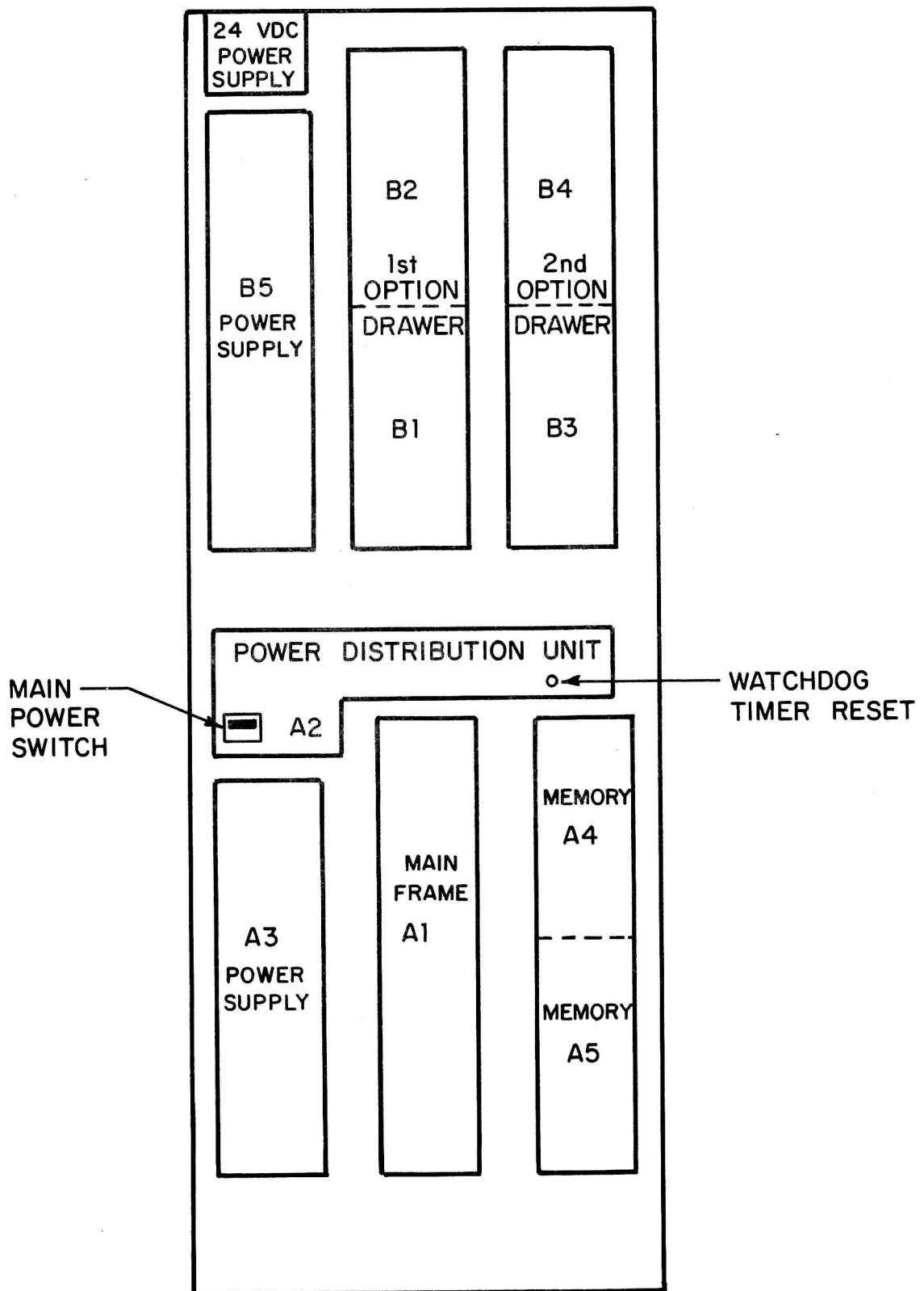
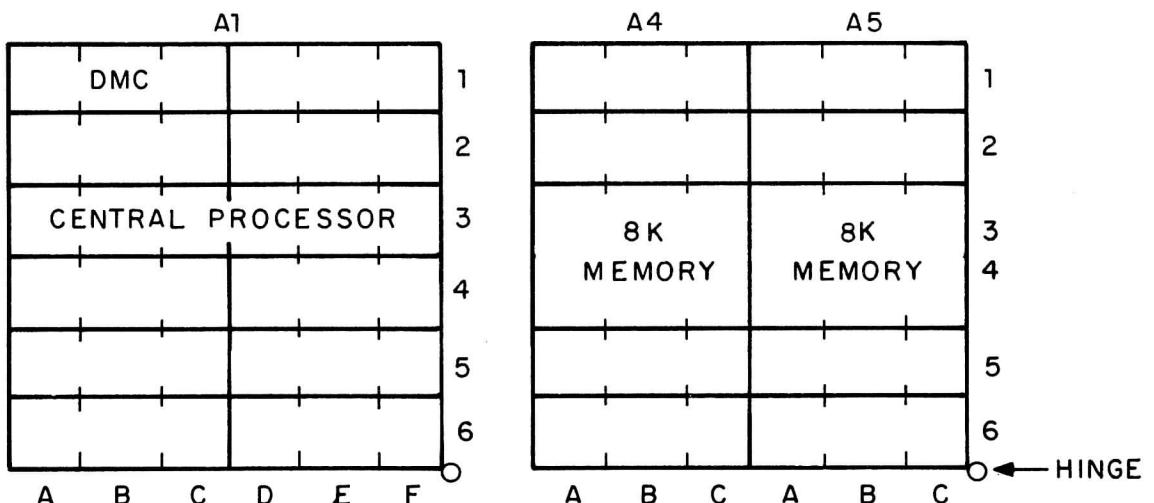
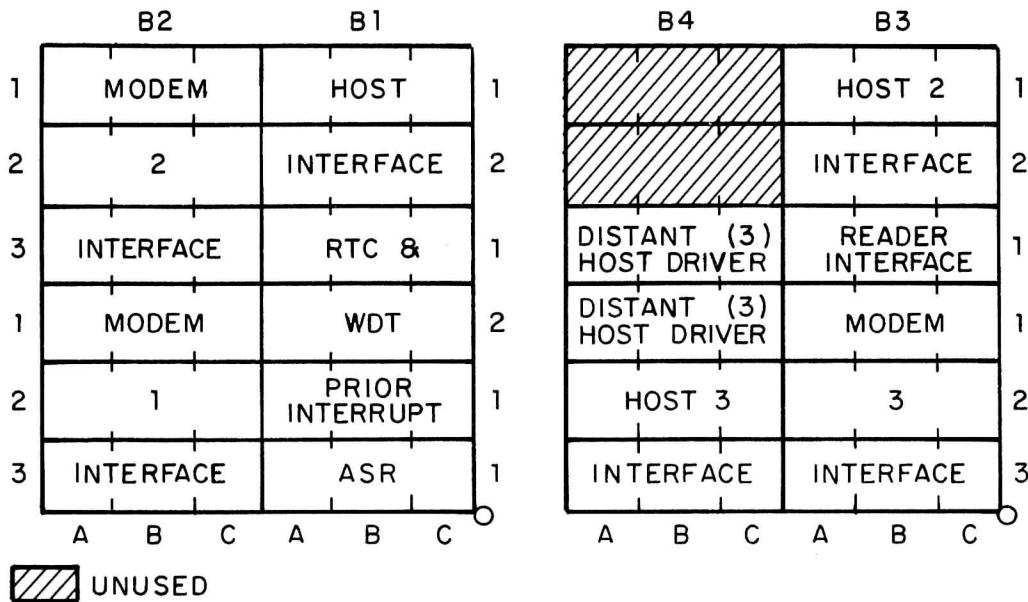


Figure 4-2. Location of Major Assemblies in 516 IMP

TABLE 4-1  
LOCATION OF MAJOR HARDWARE FUNCTIONS  
(516 Only)

<u>Function</u>	<u>Location</u>
ASR	B1
Auto Restart	Rear of control panel
Central Processor	A1
DMC	A1
Host 1 Interface	B1
Host 2 Interface*	B3
Host 3 Interface*	B4
Host 4 Interface*	B4
Memory (8K)	A4
Memory Expansion (4K)	A5
Modem 1 Interface	B2
Modem 2 Interface	B2
Modem 3 Interface	B3
Modem 4 Interface*	B4
Priority Interrupt	B1
Paper Tape Reader**	B3
Real Time Clock	B1
WatchDog Timer	B1
Distant Host Drivers*	B4

\* depending on specific configuration  
 \*\* optional



NOTE: ASSEMBLIES VIEWED FROM  $\mu$  PAC SIDE, HINGE IS TO THE RIGHT

Figure 4-3. Typical 516 Drawer Configuration  
(see Table 4-1)

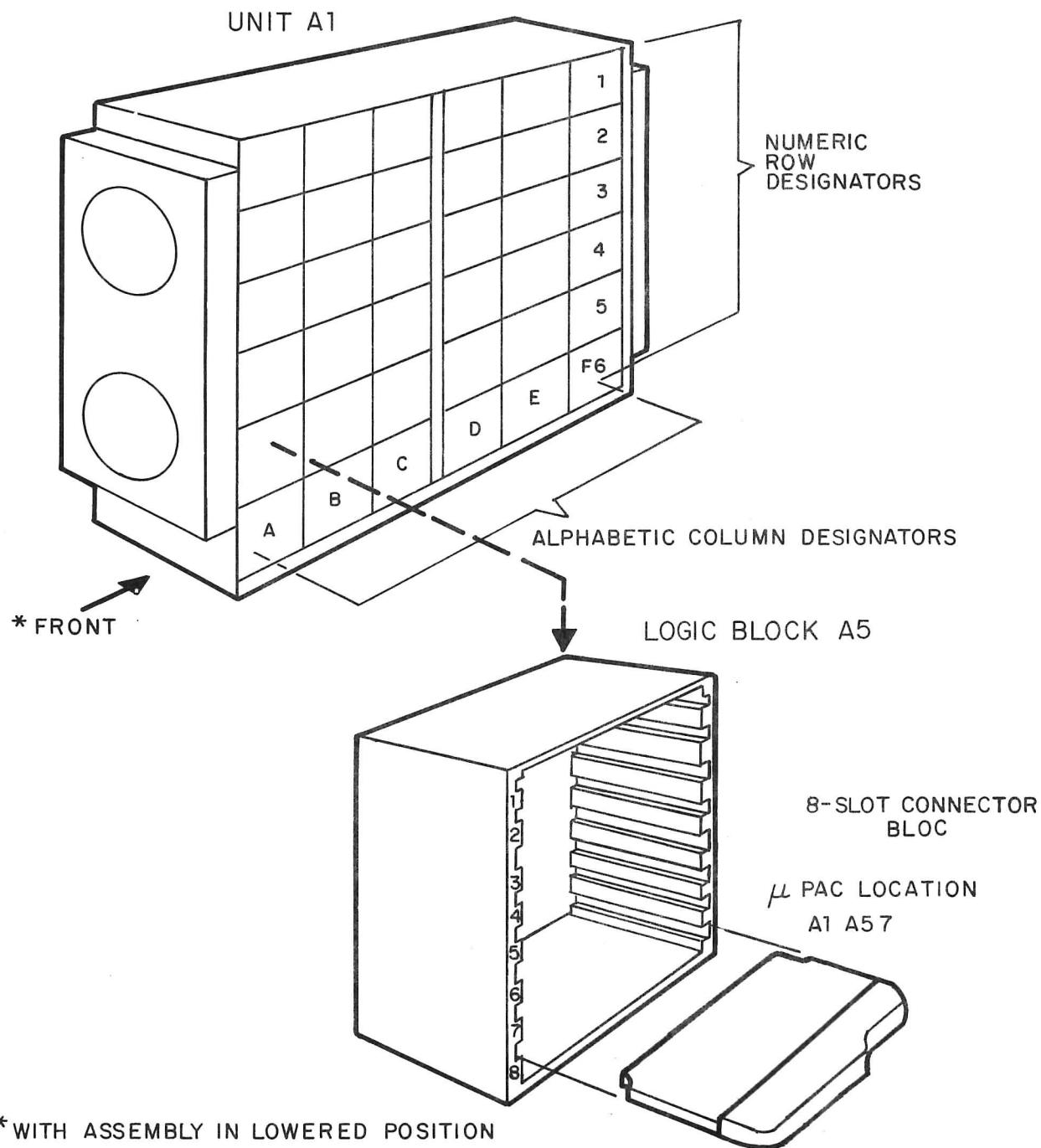
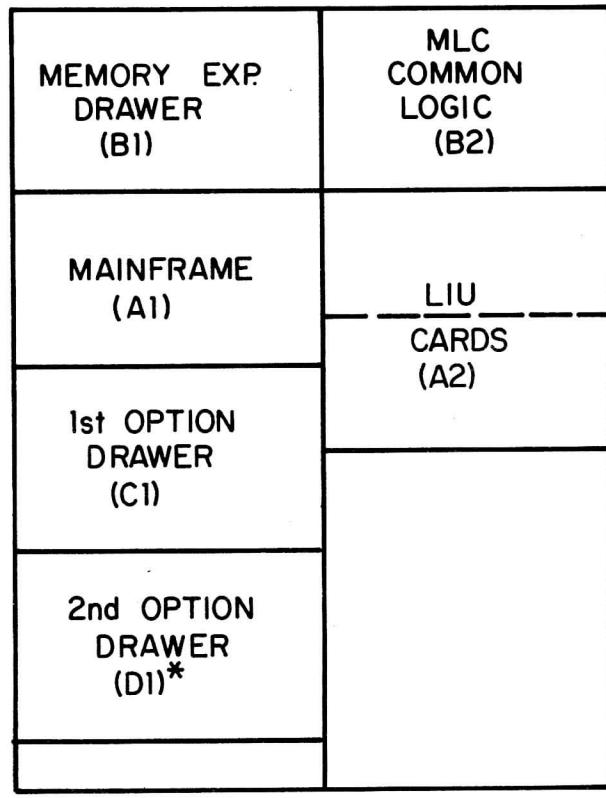
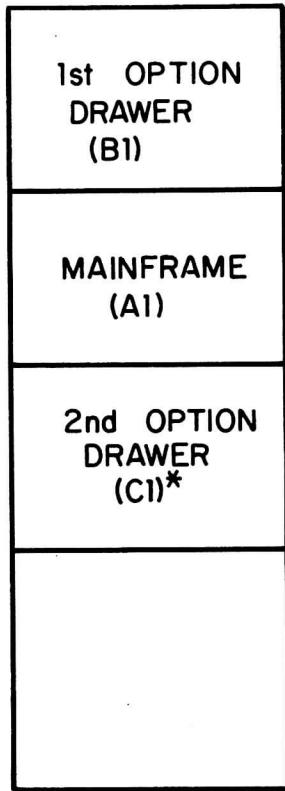


Figure 4-4. Tilt-out Assembly, Logic Bloc Row and Column Designators for Central Processor Unit A1 (516 Only) (see Figure 4-8).



\*OPTIONAL

Figure 4-5. Location of Major Assemblies in 316 IMP and TIP

TABLE 4-2  
LOCATION OF MAJOR HARDWARE FUNCTIONS  
(316 IMP and TIP)

<u>Function</u>	<u>Location</u>	
	<u>316 IMP</u>	<u>316 TIP</u>
Auto Restart		Behind Control Panel
Central Processor	A1	A1
DMC	A1	A1
Host Interface	B1	C1
Memory (16K)	A1	A1
Memory Expansion (12K)	—	B1
Modem 1 Interface	B1	C1
Modem 2 Interface	B1	C1
Priority Interrupt	A1	A1
I/O Bus Extender *	A1	A1
Real Time Clock	B1	C1
Multi-Line Controller	—	B2
LIU Cards	—	A2
Magnetic Tape Controller	—	D1

\*Optional

	B1	B4
SPACER		6
SPACER	MODEM #1	5
SPACER		4
HOST		3
	MODEM #2	2
RTC		1

G F E ↑ C B A  
D

	B1	B4
EXT. ADD.	SPACER	6
4K MEMORY	SPACER	5
4K MEMORY	SPACER	4
4K MEMORY	SPACER	3
SPACER	SPACER	2
RESISTOR	SPACER	1

G F E ↑ C B A  
D

	A1	A4
4K MEMORY		6
4K MEMORY	HSDMC	5
4K MEMORY		4
4K MEMORY	20 CENTRAL PROCESSOR LOGIC	A
IOBCU		
PRI/INT	1	

G F E ↑ C B A  
D

316 IMP

	A1	A4
4K MEMORY		6
4K MEMORY	HSDMC	5
4K MEMORY		4
4K MEMORY	20 CENTRAL PROCESSOR LOGIC	A
IOBCU		
PRI/INT	1	

G F E ↑ C B A  
D

NOTE: ASSEMBLIES VIEWED FROM  $\mu$ -PAC SIDE:  
FRONT IS TO THE RIGHT.  
LOCATION DESIGNATION OF INDIVIDUAL  
SLOTS AND PINS IS SIMILAR TO 516.

Figure 4-6. Location of Major Functions in 316 IMP and TIP.

	C1	C4
SPACER		6
SPACER	MODEM #1	5
SPACER		4
HOST		3
	MODEM #2	2
RTC		1

G F E ↑ C B A  
D

316 TIP

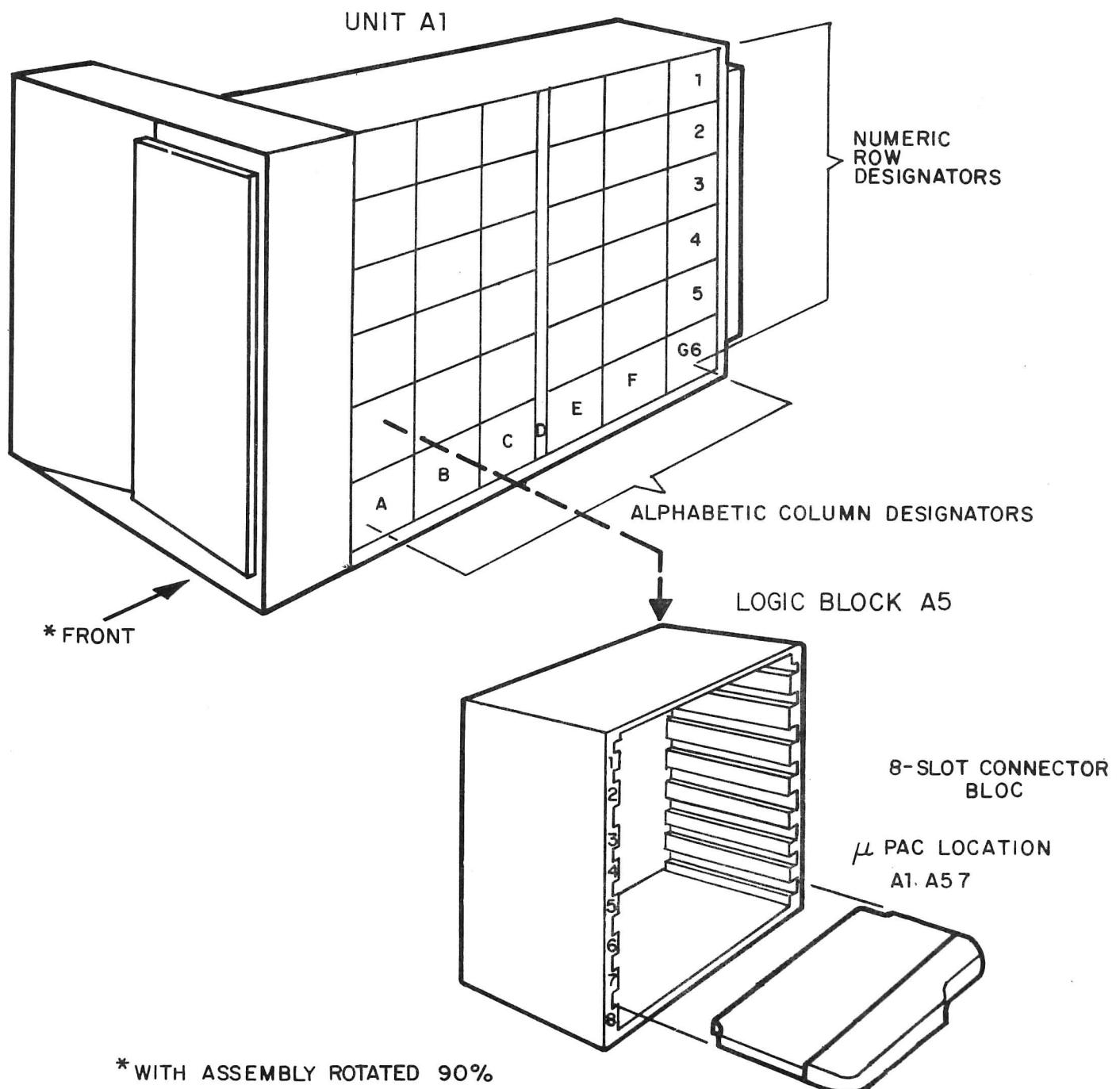
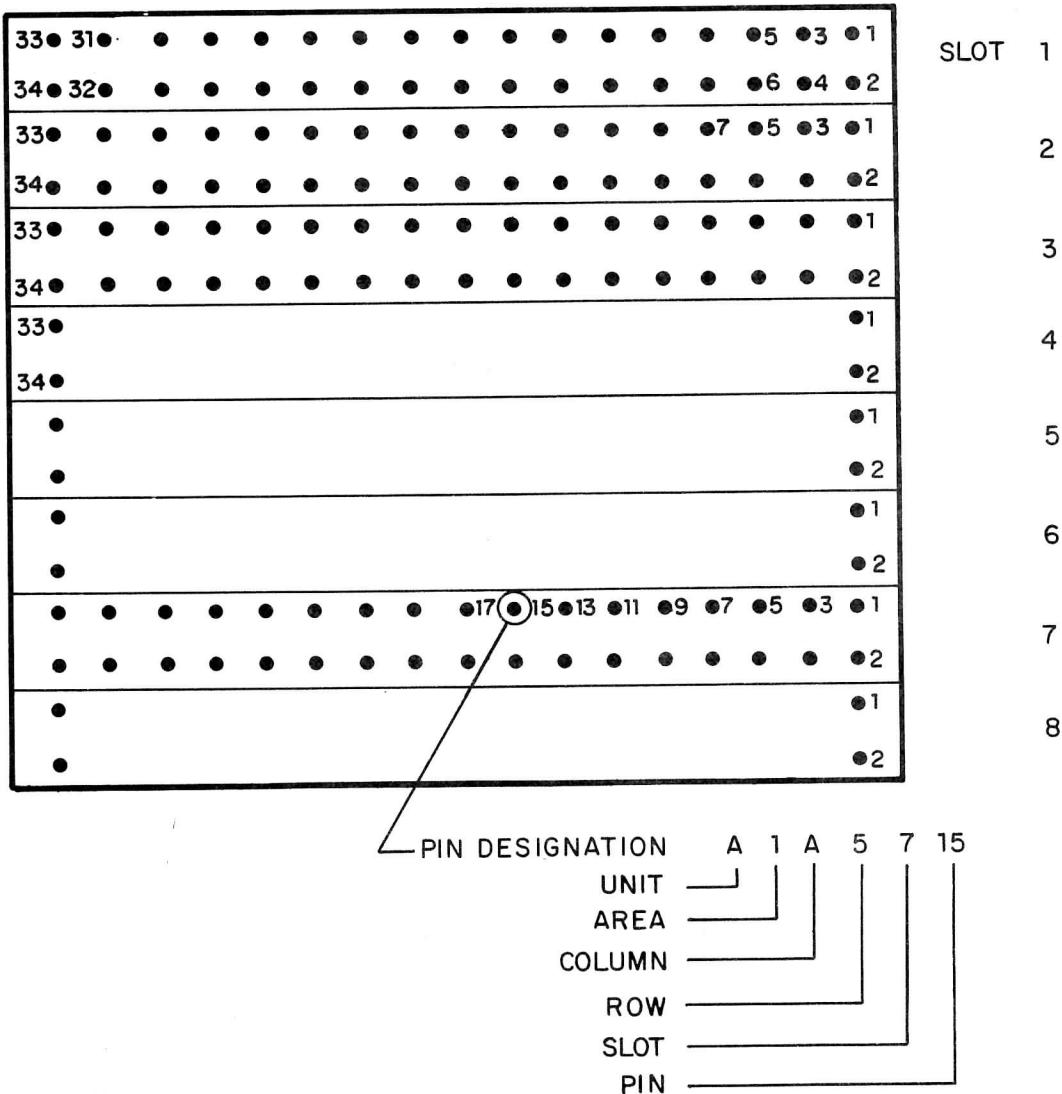
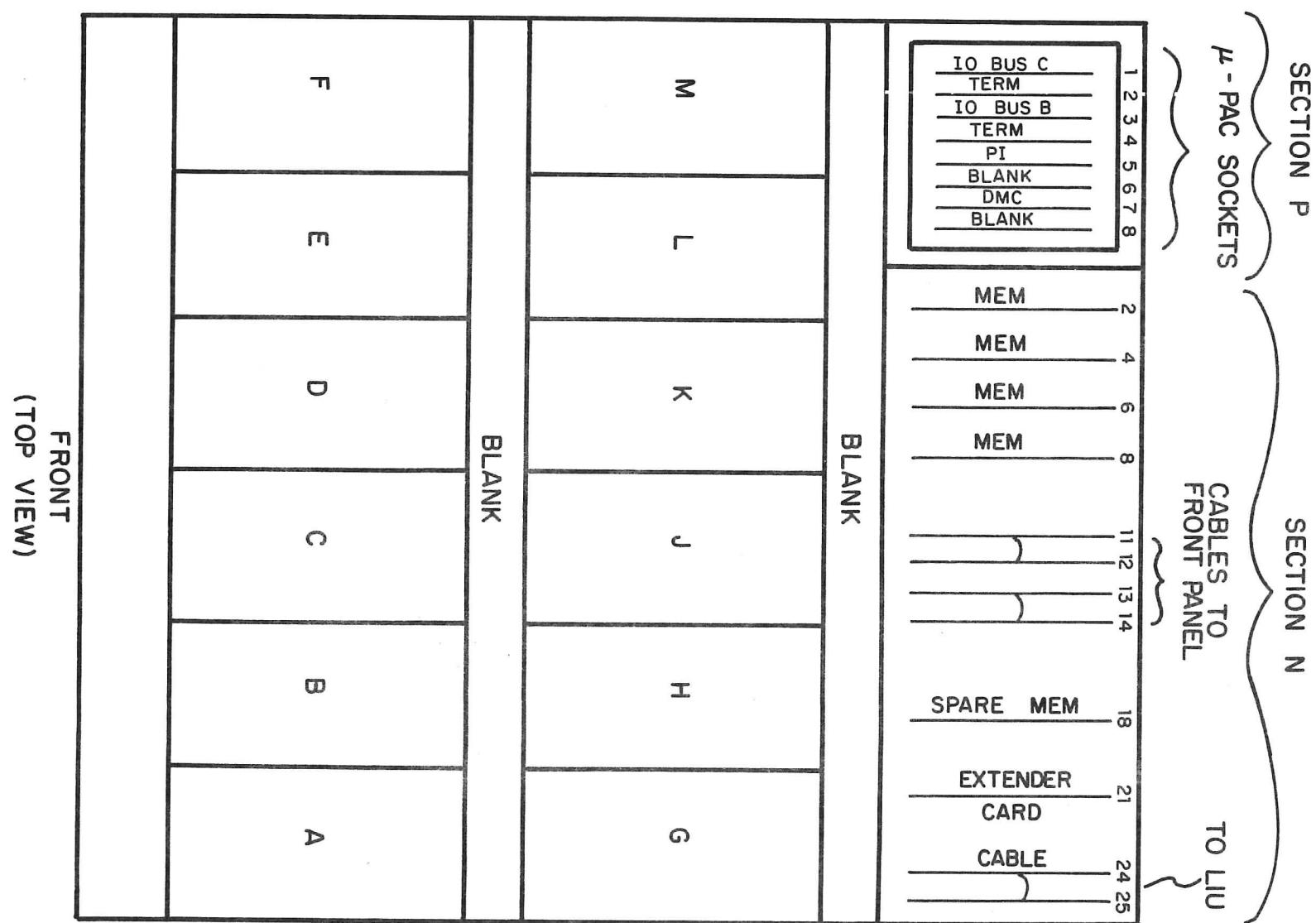


Figure 4-7. 316 Drawer Assembly, Logic Bloc Row and Column Designators for Central Processor Unit A1 (see Figure 4-8).

## CONNECTOR BLOC A1A5

Figure 4-8 Wiring Side of the 8-Slot Connector Bloc  
Shown in Figures 4-4 and 4-7



FRONT  
(TOP VIEW)

Figure 4-9. MLC Common Logic Drawer (C) - Expanded View

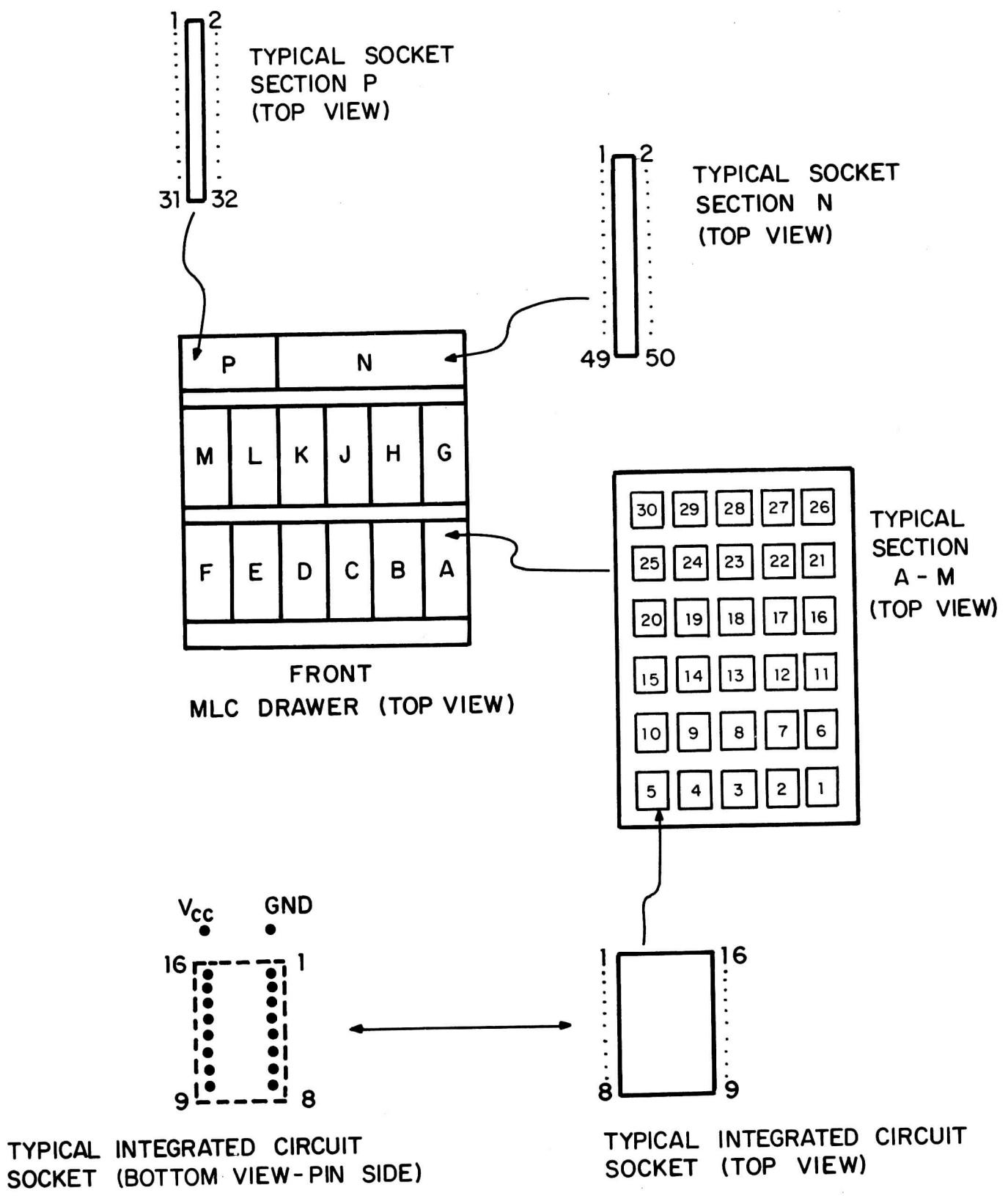
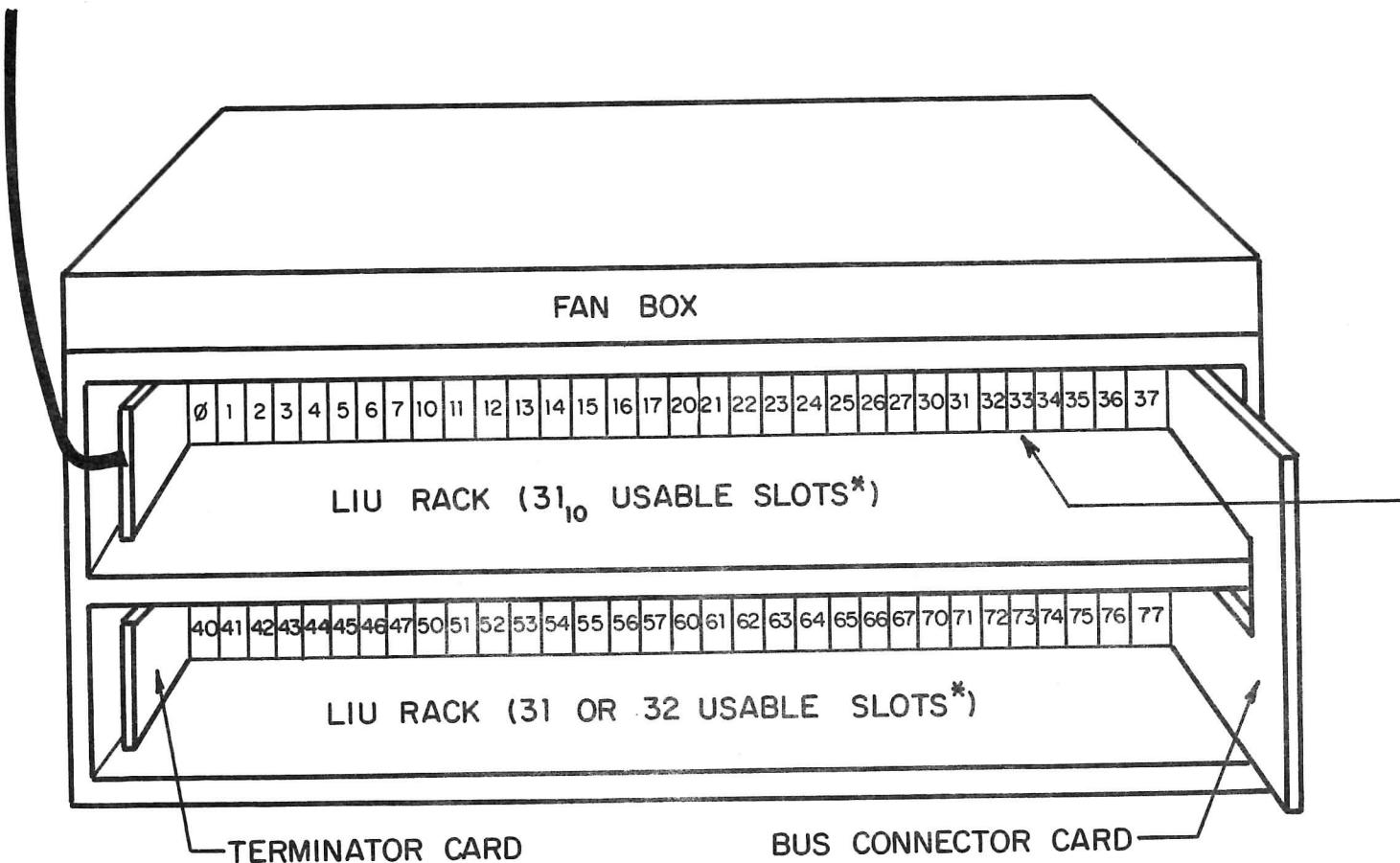
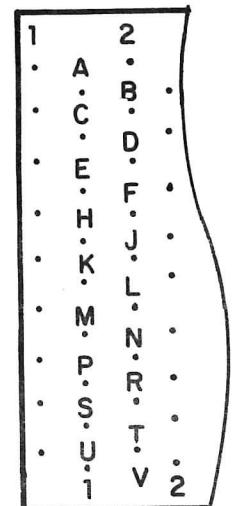


Figure 4-10. MLC Common Logic Drawer (C) - Pin Designations

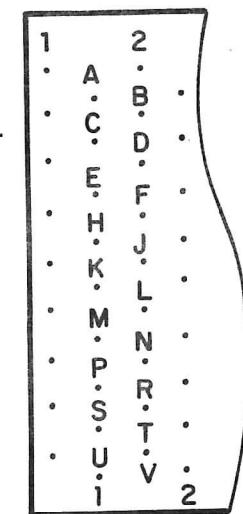
CABLE TO MLC  
DRAWER (N24, 25)



\*LIU SLOTS NUMBERED IN OCTAL 0-77. SLOT 0 IS NEVER USED,  
SLOT 77 IS UNUSED IN SYSTEMS WITH MAG TAPE OPTION.



"A"  
SECTION  
36 PINS



"B"  
SECTION  
36 PINS

33  
TYPICAL  
SOCKET

Figure 4-11. MLC Line Interface Units Rack

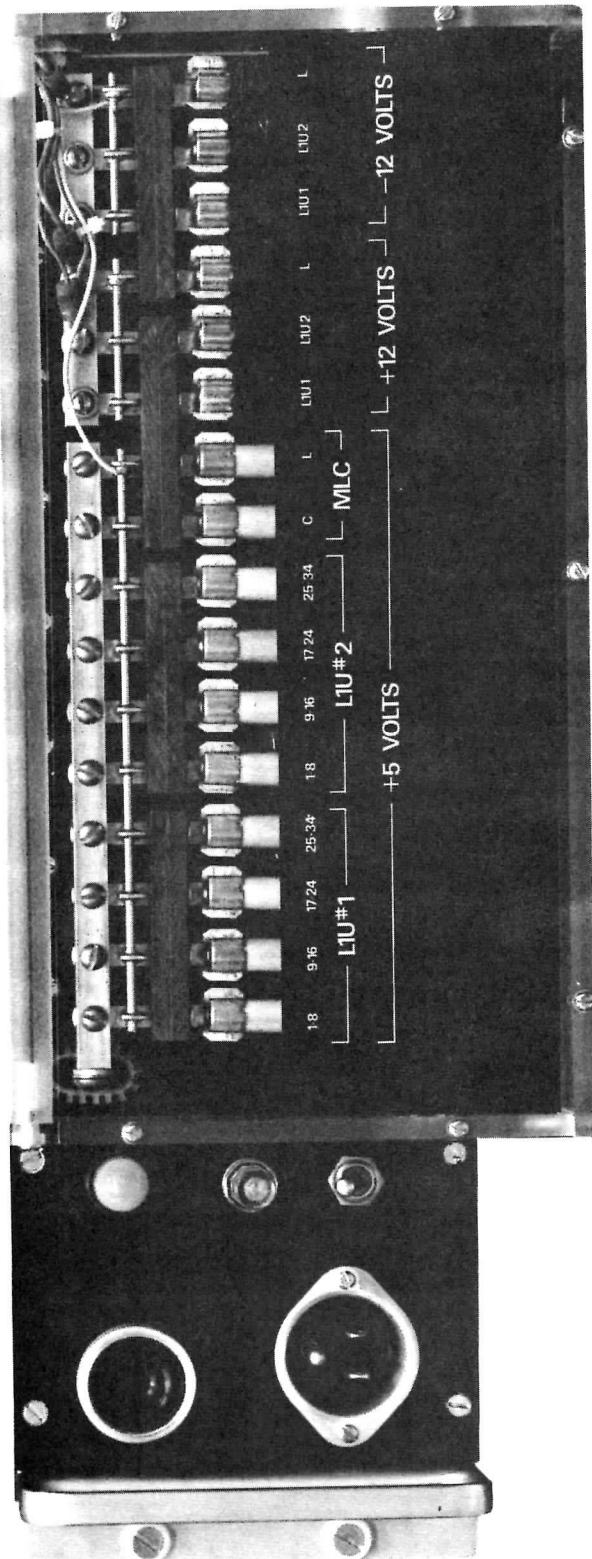


Figure 4-12. MLC Power Supply Panel

## APPENDIX A

## Connector Pin Assignments

Modem Burndy to Amphenol (516) and μ-pac (316)

<u>Modem</u>		<u>516</u> <u>Amphenol</u>	<u>316</u> <u>μ-pac</u>
A	Unused		
B	Unused		
C	Unused		
D	Unused		
E	CKTBA-(send data)	3	2
F	Unused		
G	CKTXP-(line cross-patch)	35	18
H	Unused		
I	Unused		
J	CKTDB+(xmit clock)	29	15
K	CKTBB+(rcv data)	5	3
L	CKTDD+(rcv clock)	33	17
M	Unused		

516: The shield for each signal is connected to the adjacent higher even-numbered Amphenol pin. Burndy pins are coaxial.

316: The ground for each signal is connected to μ-pac pin 33. Burndy pins are coaxial.

Amphenol to RG-174/U for Local Host (516 Only)

1	LIBIT+A	last IMP bit
2	Shield	
3	RFNIB+A	ready for next IMP bit
4	Shield	
5	DATAO+A	data: IMP to Host
6	Shield	
7	TYHBX+A	there's your Host bit
8	Shield	
9	TYIBX+A	there's your IMP bit
10	Shield	
11	LHBIT+A	last Host bit
12	Shield	
13	RFNHB+A	ready for next Host bit
14	Shield	
15	HSDTA+	data: Host to IMP
16	Shield	
17	Unused	
18	Unused	
19	Unused	
20	Unused	
21	Ground	Host ready test
22	Shield	
23	HGNDX-	Host master ready
24	Shield	
25	XMTXN-	IMP ready test
26	Shield	
27	XMTOT-	IMP master ready
28	Shield	

All other Amphenol pins unused; RG-174/U tagged with Amphenol pin numbers.

μ-pac to Twisted Pair for Local Host (316 Only)

1	LIBIT+A	last IMP bit
2	RFNIB+A	ready for next IMP bit
3	DATAO+A	data: IMP to Host
4	TYHBX+A	there's your Host bit
5	TYIBX+A	there's your IMP bit
6	LHBIT+A	last Host bit
7	RFNHB+A	ready for next Host bit
8	HSDTA+	data: Host to IMP
9	Unused	
10	Unused	
11	Ground	Host ready test
12	HGNDX-	Host master ready
13	XMTXN-	IMP ready test
14	XMTOT-	IMP master ready

μ-pac pins 15-32 unused; twisted pairs tagged with μ-pac pin numbers; the signal (colored) wire of each pair is connected to the above μ-pac pins; the ground (black) wire of each pair is connected to μ-pac pin 33.

μ-pac to Amphenol

1	1
2	3
3	5
4	7
5	9
6	11
7	13
8	15
9	17
10	19
11	21
12	23
13	25
14	27
15	29
16	31
17	33
18	35
19	37
20	39
21	41
22	43
23	45
24	47
25	49
26	51
27	53
28	55
29	57
30	59
31	61
32	63

All black wires from even-numbered Amphenol pins to μ-pac pin 33.

Amphenol Connector for Distant Host

1	LIBIT+C	
2	LIBIT-C	last IMP bit
3	DATAO+C	
4	DATAO-C	data: IMP to Host
5	TYIMB+C	
6	TYIMB-C	there's your IMP bit
7	RFNHB+C	
8	RFNHB-C	ready for next Host bit
9	SPARE+A	
10	SPARE-A	spare
11	IMPGN-	
12	HGNDX-	Host ready test Host master ready
13	XMTXN-	
14	XMTOT-	IMP ready test IMP master ready
15	SPARE+B	
16	SPARE-B	spare
17	RFNIB+C	
18	RFNIB-C	ready for next IMP bit
19	TYHB+C	
20	TYHB-C	there's your Host bit
21	LHBIT+C	
22	LHBIT-C	last Host bit
23	HSDTA+C	
24	HSDTA-C	data: Host to IMP
25	Unused	
26	Unused	
27	Unused	
28	Unused	
29	Unused	
30	Unused	
31	Ground	Host ground

μ-pac to Amphenol (Distant Host)

B18	7	1
	8	2
	9	3
	10	4
	11	5
	12	6
	13	7
	14	8
B16	7	9
	8	10
	9	11
	10	12
	11	13
	12	14
	13	15
	14	16
B14	7	17
	8	18
	9	19
	10	20
	11	21
	12	22
	13	23
	14	24

Cable outer shield connected to Amphenol shell.

All μ-pac pin 33 connected to Amphenol pin 31.

All other μ-pac and Amphenol pins unused.

Report No. 1877

Bolt Beranek and Newman Inc.

APPENDIX B

ASCII Codes

ASCII CODES

ASCII			
OCT	HEX	MNEMONIC	SYMBOL
2ØØ	8Ø	NUL	↑Ø
2Ø1	81	SOH	↑A
2Ø2	82	STX	↑B
2Ø3	83	ETX	↑C
2Ø4	84	EOT	↑D
2Ø5	85	ENQ	↑E
2Ø6	86	ACK	↑F
2Ø7	87	BEL	↑G
21Ø	88	BS	↑H
211	89	HT	↑I
212	8A	LF	↑J
213	8B	VT	↑K
214	8C	FF	↑L
215	8D	CR	↑M
216	8E	SO	↑N
217	8F	SI	↑O
22Ø	9Ø	DLE	↑P
221	91	DC1	↑Q
222	92	DC2	↑R
223	93	DC3	↑S
224	94	DC4	↑T
225	95	NAK	↑U
226	96	SYN	↑V
227	97	ETB	↑W
23Ø	98	CAN	↑X
231	99	EM	↑Y
232	9A	SUB	↑Z

ASCII		MNEMONIC	SYMBOL
OCT	HEX		
233	9B	ESC	↑[
234	9C	FS	↑\
235	9D	GS	↑]
236	9E	RS	↑↑
237	9F	US	↑←
24Ø	AØ	SP	Space
241	A1		!
242	A2		"
243	A3		#
244	A4		\$
245	A5		%
246	A6		&
247	A7		,
25Ø	A8		(
251	A9		)
252	AA		*
253	AB		+
254	AC		,
255	AD		-
256	AE		.
257	AF		/
26Ø	BØ		Ø
261	B1		1
262	B2		2
263	B3		3
264	B4		4
265	B5		5
266	B6		6
267	B7		7
27Ø	B8		8

ASCII		MNEMONIC	SYMBOL
OCT	HEX		
271	B9		9
272	BA		:
273	BB		;
274	BC		<
275	BD		=
276	BE		>
277	BF		?
3ØØ	CØ		@
3Ø1	C1		A
3Ø2	C2		B
3Ø3	C3		C
3Ø4	C4		D
3Ø5	C5		E
3Ø6	C6		F
3Ø7	C7		G
31Ø	C8		H
311	C9		I
312	CA		J
313	CB		K
314	CC		L
315	CD		M
316	CE		N
317	CF		O
32Ø	DØ		P
321	D1		Q
322	D2		R
323	D3		S
324	D4		T
325	D5		U
326	D6		V
327	D7		W

ASCII		MNEMONIC	S Y M B O L
OCT	HEX		
33Ø	D8		X
331	D9		Y
332	DA		Z
333	DB		[
334	DC		\
335	DD		]
336	DE		⌚ (↑)
337	DF		-
34Ø	EØ		~
341	E1		a
342	E2		b
343	E3		c
344	E4		d
345	E5		e
346	E6		f
347	E7		g
35Ø	E8		h
351	E9		i
352	EA		j
353	EB		k
354	EC		l
355	ED		m
356	EE		n
357	EF		o
36Ø	FØ		p
361	F1		q
362	F2		r
363	F3		s
364	F4		t
365	F5		u

ASCII		MNEMONIC	SYMBOL
OCT	HEX		
366	F6		v
367	F7		w
370	F8		x
371	F9		y
372	FA		z
373	FB		{
374	FC		
375	FD		}
376	FE		~
377	FF	DEL	RUBOUT

---

The IMP uses 8-bit ASCII with the left-most bit set to one.

↑ = control

↑@ = shift control - P

## APPENDIX C

## List of Tapes

Paper Tape Library

System Tapes:	IMPLOD*
Honeywell Test Programs:	RPT-2 TWT-1 PFT-3 CCT-4 CMT-4 Reader Test Loop
BBN Test Programs:	NIMPTS* TIPTST* (Terminal IMPs only)

\* Versions are updated from time to time. Consult relevant memos for current version numbers. If in doubt, consult the NCC.

## APPENDIX D

### What To Do If Something Goes Wrong

The Network Control Center (NCC) should be called at (617) 661-0100 before any decision concerning the IMP or the phone lines is made. The NCC does all liaison with computer field service; similarly it handles all line problems. The NCC is manned 24 hours a day, seven days a week.

#### *Terminal IMPs Only:*

There is a warning tone alarm on the back of the TIP that will sound in the event that any fuse in the DC circuitry blows. The TIP should be unplugged immediately if this is heard, and the NCC should be contacted.