

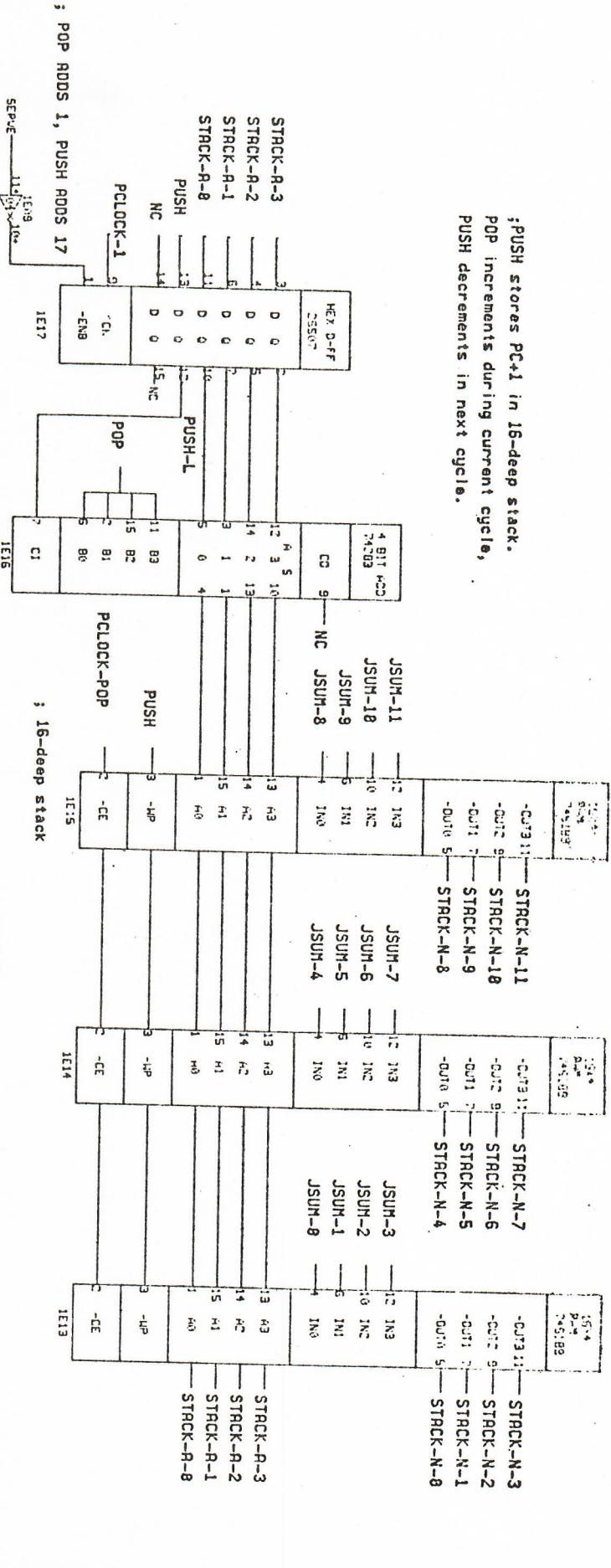
;1A12 VECTOR SCOPE
;TAPE RECORDER

TH0: BUS INPUT CHANNELS?
;CH ADDRESS ;CH DATA OUT

;BUFFERED
BUS OUTPUTS

;DEBUGGING POINTS
;CONTROLS

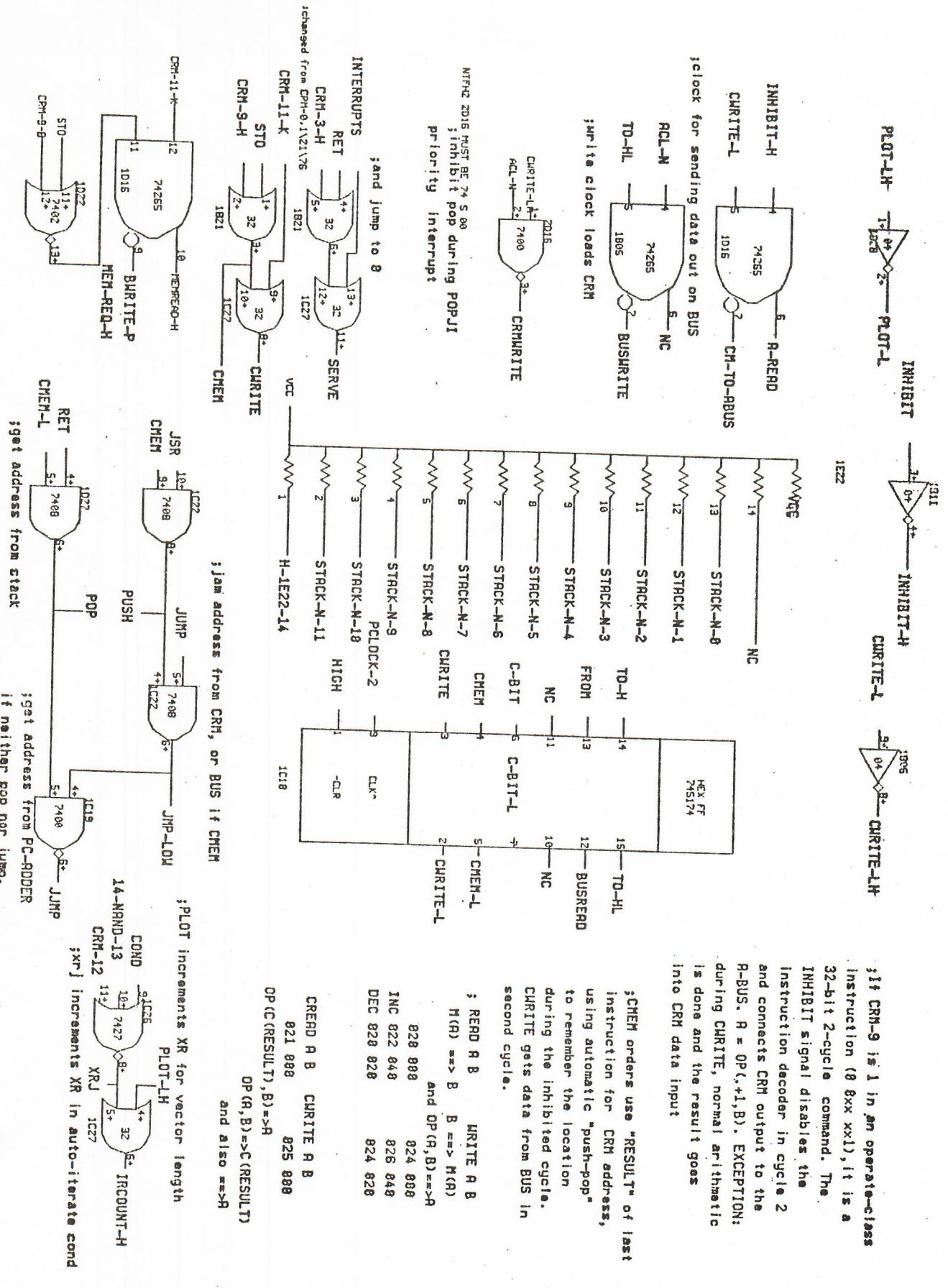
NC	1A11-3	V12-PLUS	CRM-8	JE1-19	QD1-9	NOLOCK-OUT	JE1-10	CLEAR
EIA-OUT	1A11-6	V12-MINUS	CRM-1	JE1-20	QD1-10	READ-27	JE1-10	
EIA-IN	1A11-3	BRIGHT	CRM-2	JE1-20	QD1-10	WRITE-27	JE1-10	
HIGH-EIA	1A11-3	X-SCOPE	CRM-3	JE1-20	QD1-10	FROM-18	JE1-10	CLEAR-PC
HIGH-EIA	1A11-3	V12-PLUS	CRM-4	JE1-20	QD1-10	FROM-11	JE1-10	HIGH
HIGH-EIA	1A11-3	V12-MINUS	CRM-5	JE1-20	QD1-10	CRM-POP	JE1-10	NC
GND	1A11-3	Y-SCOPE	CRM-6	JE1-20	QD1-10	CRM-SU	JE1-10	NC
HIGH-EIA	1A11-3	NC	CRM-7	JE1-20	QD1-10	CRM-R	JE1-10	SC-CRM
NC	1A11-3	NC	CRM-8	JE1-20	QD1-10	PUSH	JE1-10	SC-SWITCH
NC	1A11-3	NC	CRM-9	JE1-20	QD1-10	RET	JE1-10	STEP-HIGH
CLEAR-PC	1A11-3	NC	CRM-10	JE1-20	QD1-10	RRA-8	JE1-10	STEP-LOW
CLEAR	1A11-3	NC	CRM-11	JE1-20	QD1-10	RRA-1	JE1-10	RATE-A
NC	1A11-3	T-CLO-IN	CRM-12	JE1-20	QD1-10	RRA-2	JE1-10	RATE-B
NC	1A11-3	TAPE-IN	CRM-13	JE1-20	QD1-10	INT-0	JE1-10	RATE-C
NC	1A11-3	T-CLO-OUT	CRM-14	JE1-20	QD1-10	INT-1	JE1-10	RATE-D
NC	1A11-3	TAPE-OUT	CRM-15	JE1-20	QD1-10	INT-2	JE1-10	HIGH-4
NC	1A11-3	NC	CRM-16	JE1-20	QD1-10	INT-3	JE1-10	NC
60-HZ-CLOCK	1A11-3	CRM-17	CRM-18	JE1-20	QD1-10	INT-4	JE1-10	INS-68000 QD1-10
POWER-ON	1A11-3	MR-8	MEM-9	JE1-20	QD1-10	INT-5	JE1-10	NC
BATT-5-N	1A11-3	MR-1	MEM-1	JE1-20	QD1-10	VCC	JE1-10	
BATT-5-N	1A11-3	MR-2	MEM-2	JE1-20	QD1-10	V12-MINUS	JE1-10	BUSWRITE
BATT-5-N	1A11-3	MR-3	MEM-3	JE1-20	QD1-10	V12-PLUS	JE1-10	BUSREAD
BATT-5	1A11-3	MR-4	MEM-4	JE1-20	QD1-10	KB-PARITY	JE1-10	BB-8
BATT-5	1A11-3	MR-5	MEM-5	JE1-20	QD1-10	KB-STROBE	JE1-10	BB-1
TIMER	1A11-3	MR-6	MEM-6	JE1-20	QD1-10	KB-8	JE1-10	BB-2
PWR-DN	1A11-3	MR-7	MEM-7	JE1-20	QD1-10	KB-DENB-H	JE1-10	BB-3
NC	1A11-3	MR-8	MEM-8	JE1-20	QD1-10	KB-1	JE1-10	BB-4
BATT-12	1A11-3	MR-9	MEM-9	JE1-20	QD1-10	KB-SH-H	JE1-10	BB-5
BATT-12	1A11-3	MR-10	MEM-10	JE1-20	QD1-10	KB-2	JE1-10	BB-6
BATT-12	1A11-3	MR-11	MEM-11	JE1-20	QD1-10	KB-CTRL	JE1-10	NC
BATT-12-N	1A11-3	MR-12	MEM-12	JE1-20	QD1-10	KB-3	JE1-10	NC
BATT-12-N	1A11-3	MR-13	MEM-13	JE1-20	QD1-10	KB-4	JE1-10	NC
NC	1A11-3	MR-14	MEM-14	JE1-20	QD1-10	KB-5	JE1-10	NC
V12-MINUS	1A11-3	MR-15	MEM-15	JE1-20	QD1-10	KB-RESET	JE1-10	NC
V12-MINUS	1A11-3	NC	DM-14	JE1-20	QD1-10	KB-6	JE1-10	NC
NC	1A11-3	NC	DM-15	JE1-20	QD1-10	KB-7	JE1-10	NC
;	MAIN MEMORY ADDRESS, MEMORY DATA OUT	;	MEMORY DATA IN	;	KEYBOARD	;	KEYBOARD	;
;	POWER CONNECTOR	;	;	;	;	;	;	;



;SERVE forces STACK-N to 111 111 111 111 for interrupt servicing; i.e., to address 8

;JBUS is tri-state PC-address bus. POP attaches stack. JMP-LDI attaches crm for jumps. CMEI attaches BUS for crm-loading. Default is JSUM (page 9).

STACK TO PC GATE

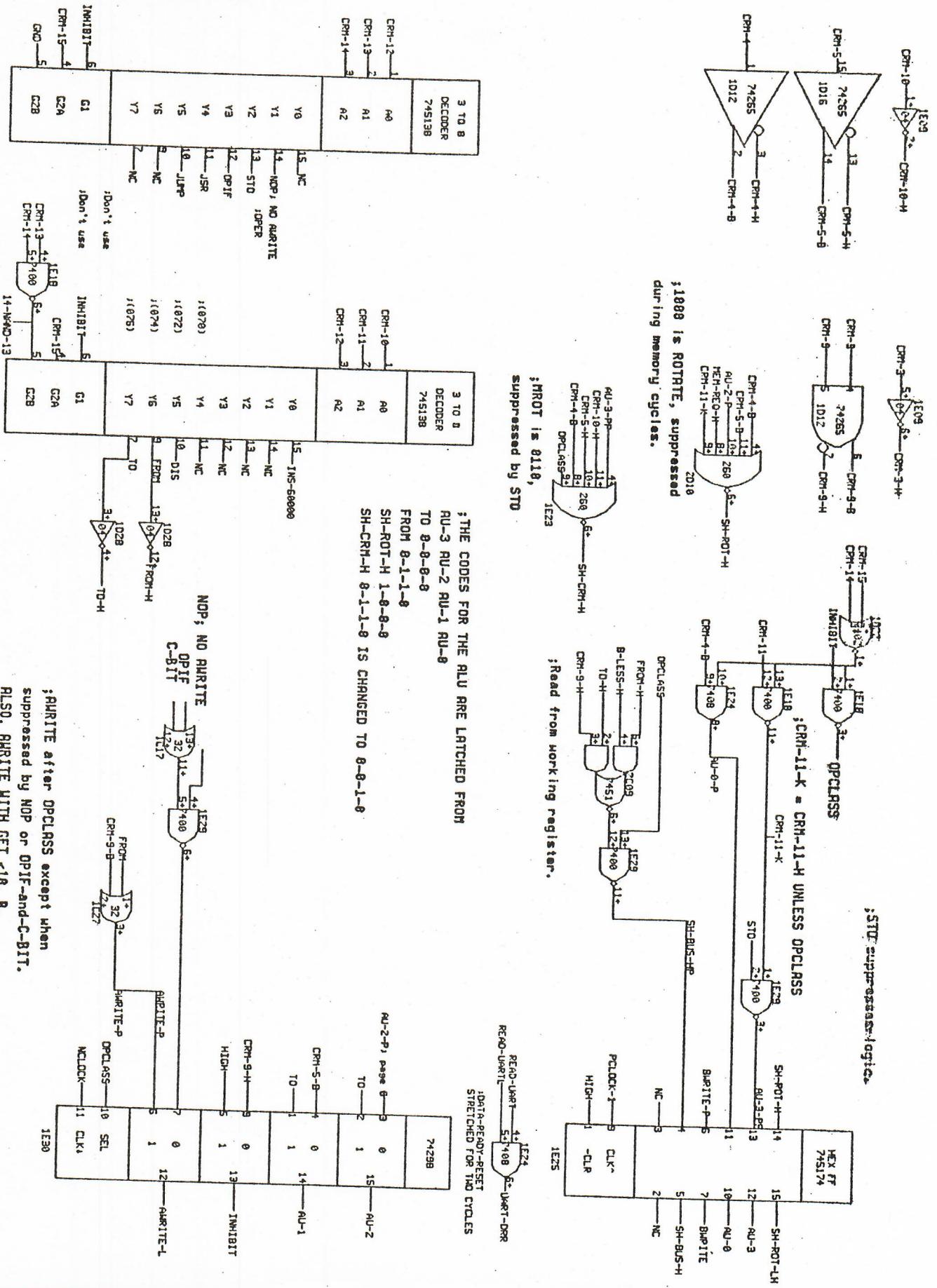


JUMP CONTROL

MILKY WAY

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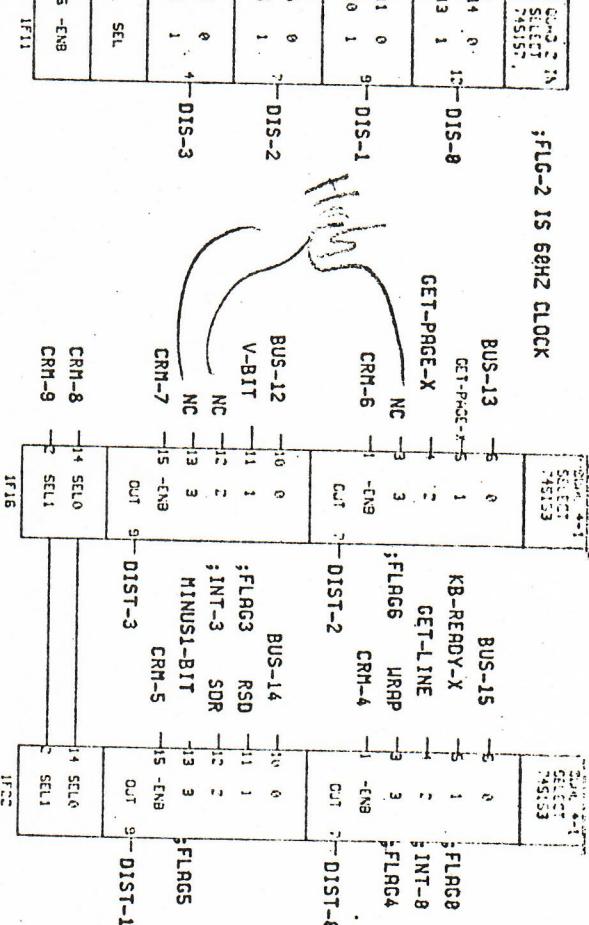
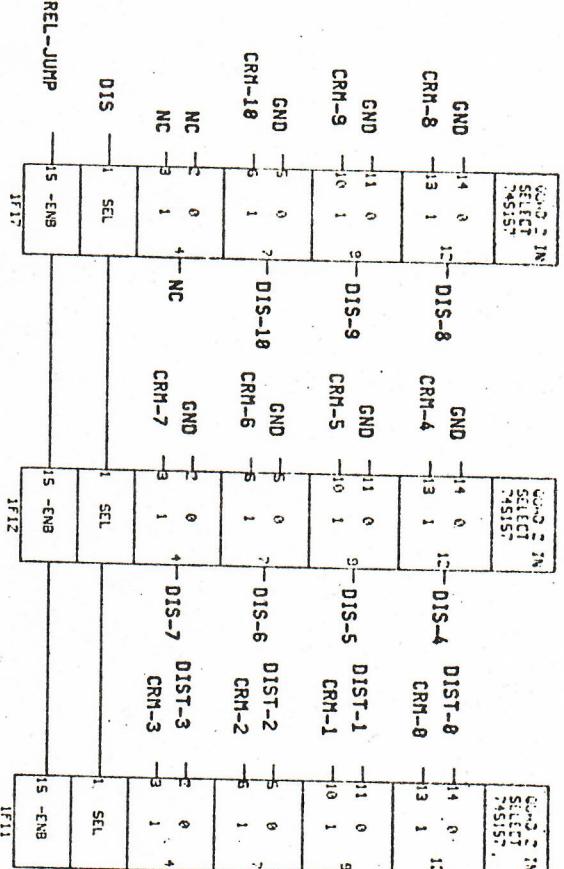


INSTRUCTION DECODER

MIGEY 366

110

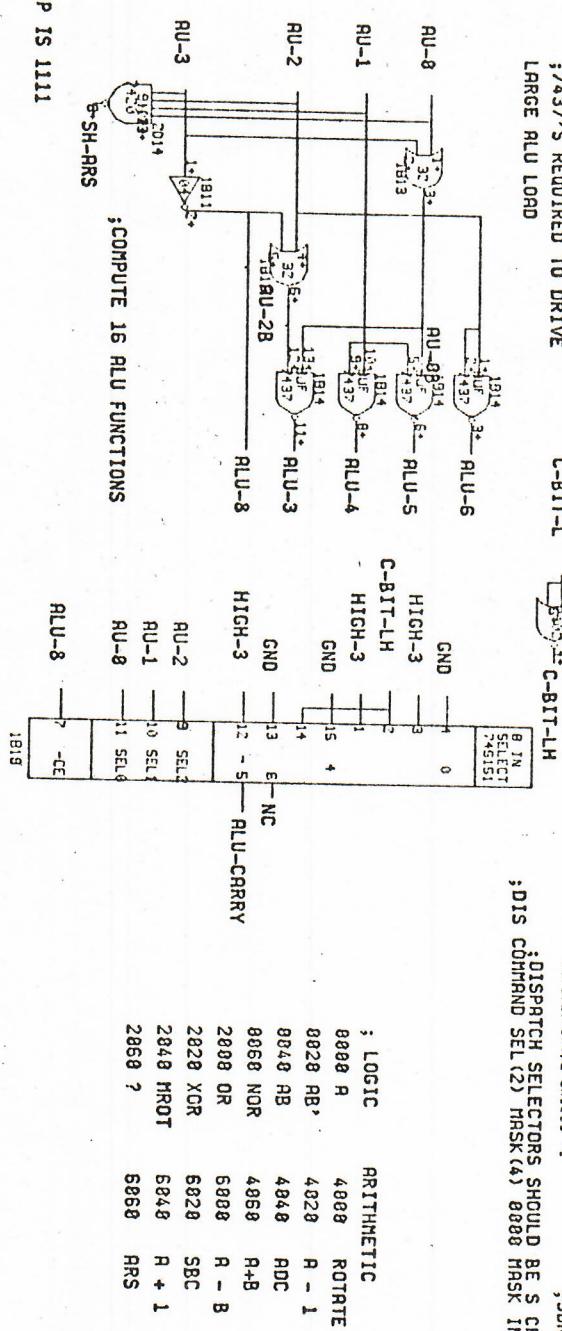
卷之三



:MINUSI-BIT is low if BUS=1????

;SDR is UART-data-in-ready

;DIS COMMAND SEL(2) MASK(4) 8000 MASK INVERTED CHIPS



; OP IS 111

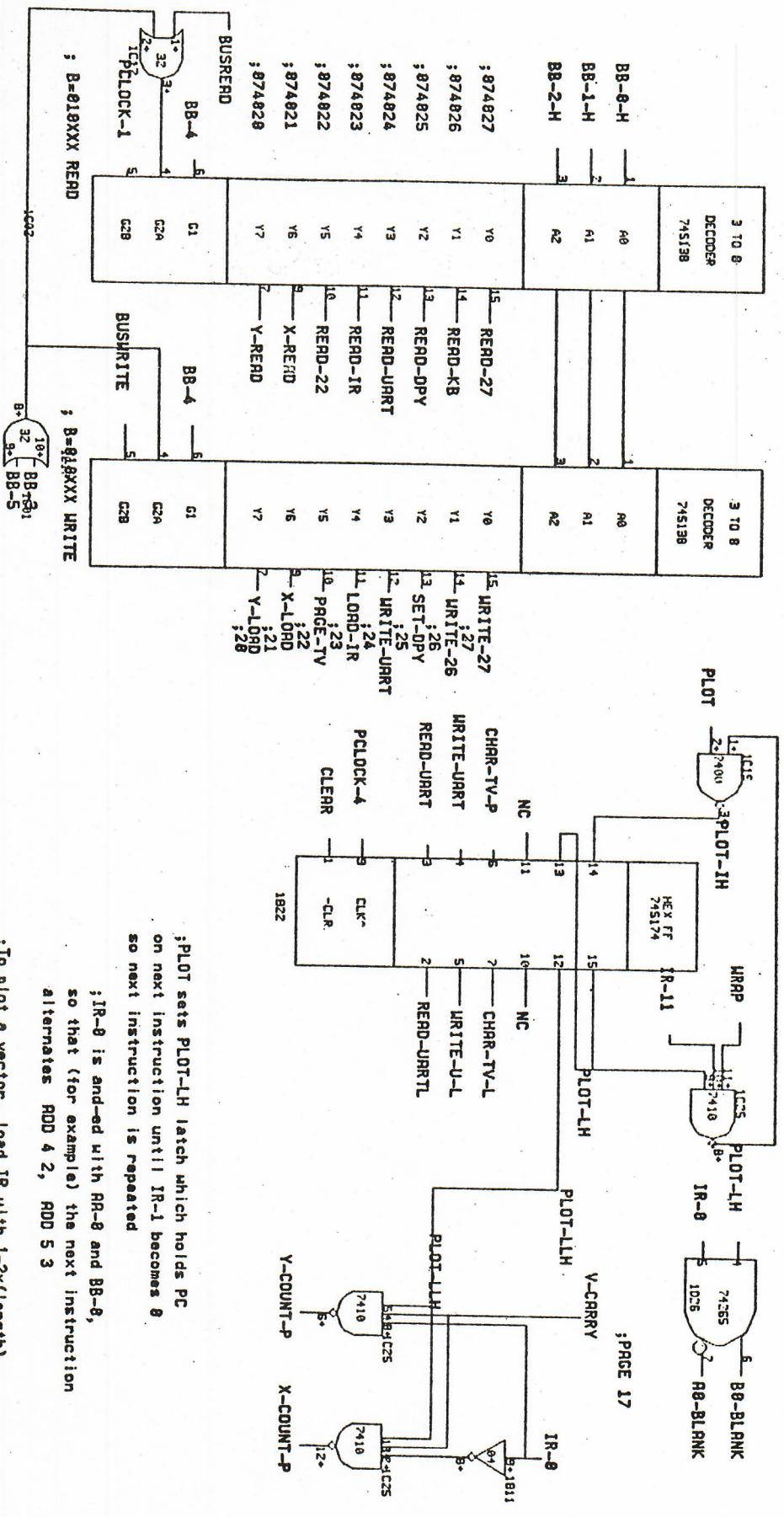
;pin 6 inverts, diagram wrong!

ALU FUNCTION

DISPATCH

AA=APP=7E 22:00

MICHIGAN



;NOTE: WRITE-UART is latched to
stretch 220ns pulse

;NOTE: WRITETIME is latched to
stretch 228ns pulse ;NOTE BUSWRITE is an 88 ns pulse

- ;PLOT sets PLOT-LH latch which holds PC on next instruction until IR-1 becomes 0 so next instruction is repeated
- ;IR-0 is added with RR-0 and BB-0 so that (for example) the next instruction alternates ADD 4 2, ADD 5 3
- ;To plot a vector, load IR with 1-2x(lenn). When an ADD operation, the X or Y counter by IR-0 is incremented or decremented according to the sign of the B-addend.

; to plot a vector, load IR with 1-2x(length).
When an ADD overflows, the X or Y counter selected
by IR-0 is incremented or decremented
according to the sign of the R-contents

;PLOT sets PLOT-LH latch which holds PC
on next instruction until IR-1 becomes 0
so next instruction is repeated

;IR-0 is and-ed with RR-0 and BB-0,
so that (for example) the next instruction
alternates ADD 4 2, ADD 5 3

;To plot a vector, load IR with $1-2x(\text{length})$.
When an ADD overflows, the X or Y counter selected
by IR-0 is incremented or decremented
according to the sign of the B-addend.

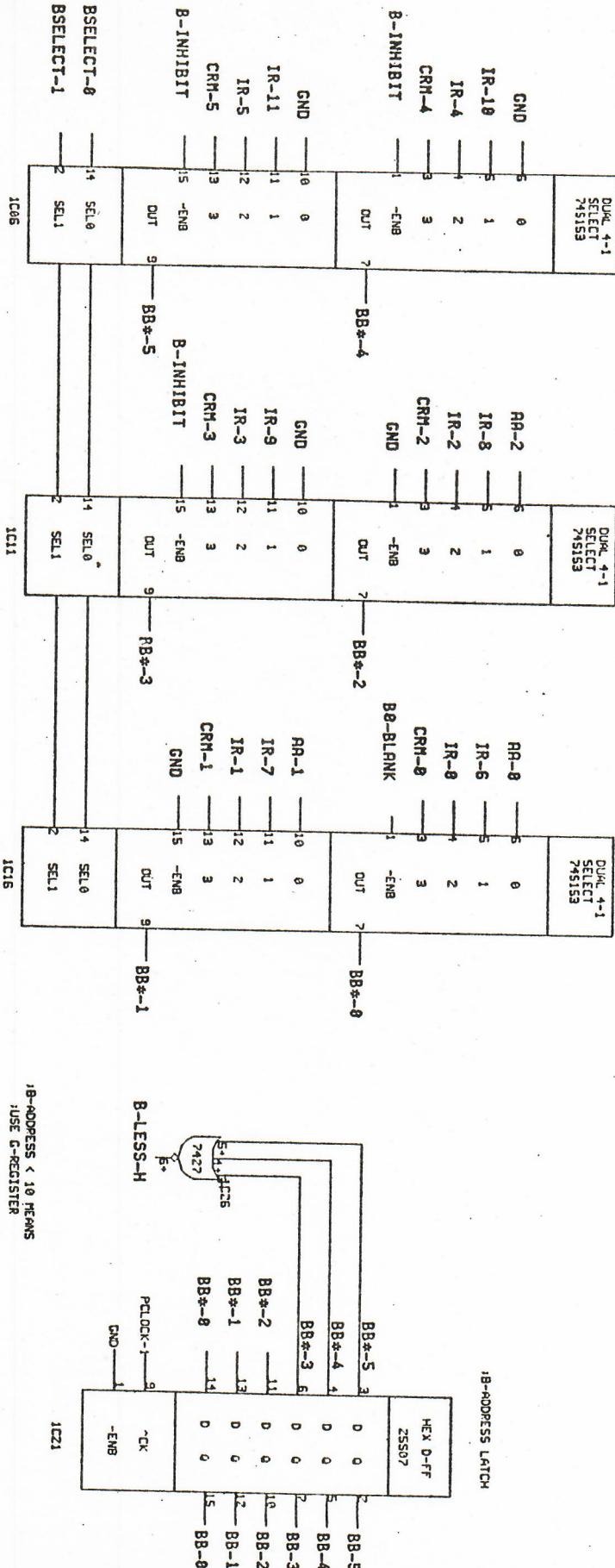
;PLOT sets PLOT-LH latch which holds PC
on next instruction until IR-1 becomes 0
so next instruction is repeated

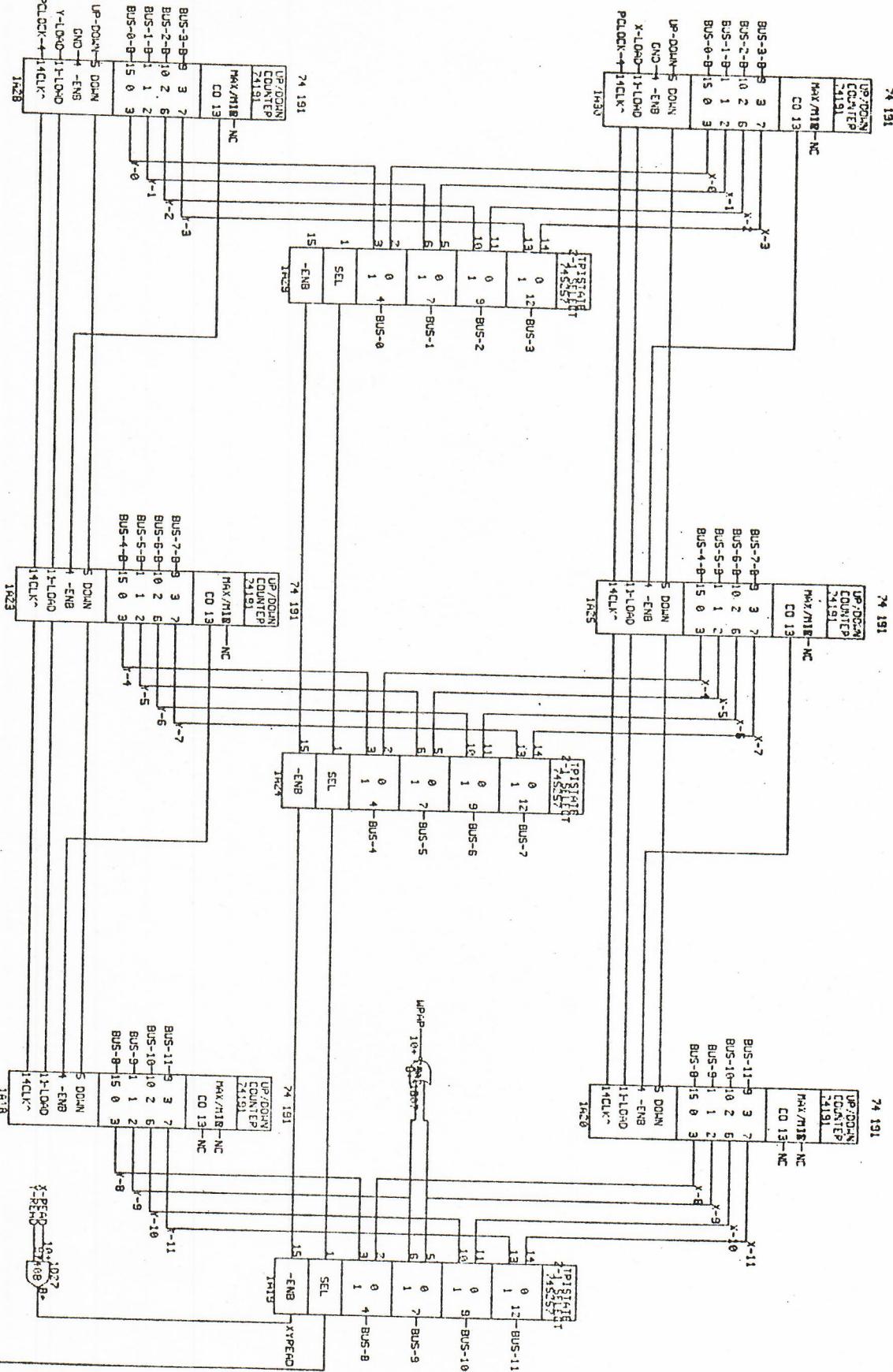
;IR-0 is and-ed with RR-0 and BB-0,
so that (for example) the next instruction
alternates ADD 4 2, ADD 5 3

;To plot a vector, load IR with $1-2x(\text{length})$.
When an ADD overflows, the X or Y counter selected
by IR-0 is incremented or decremented
according to the sign of the B-addend.

:USE 74 LS 153

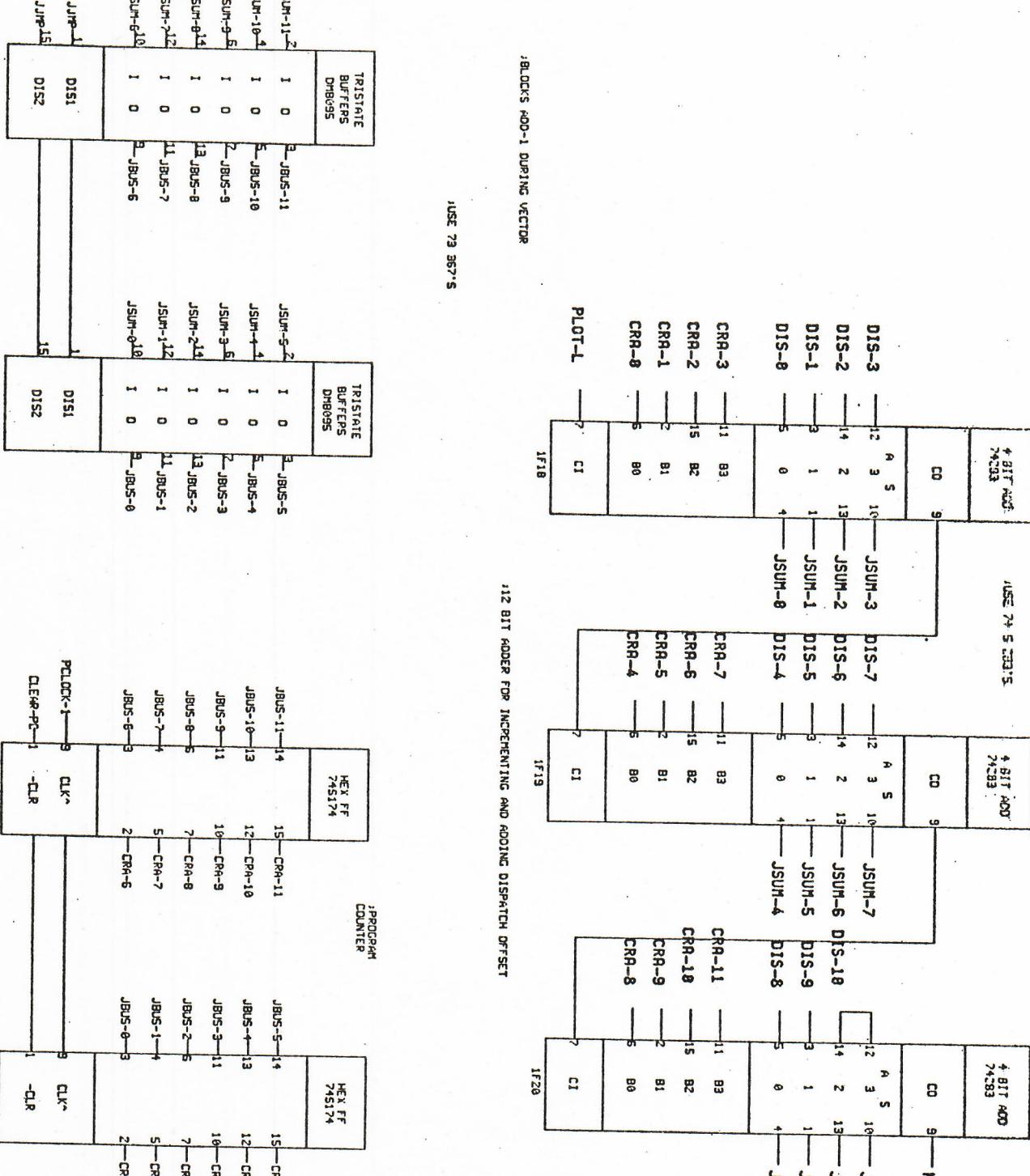
:BB-BLANK used in vector generation





VECTOR-GENERATOR OUTPUT REGISTERS

;BUFFER - DRIVEN FROM 74LS133



BLOCKS ADD-1 DURING VECTOR

5.95 € 357.5

11

F15

PC ADDER

MINSKY 2500

31-IAN-76.02:1E

MUNICH

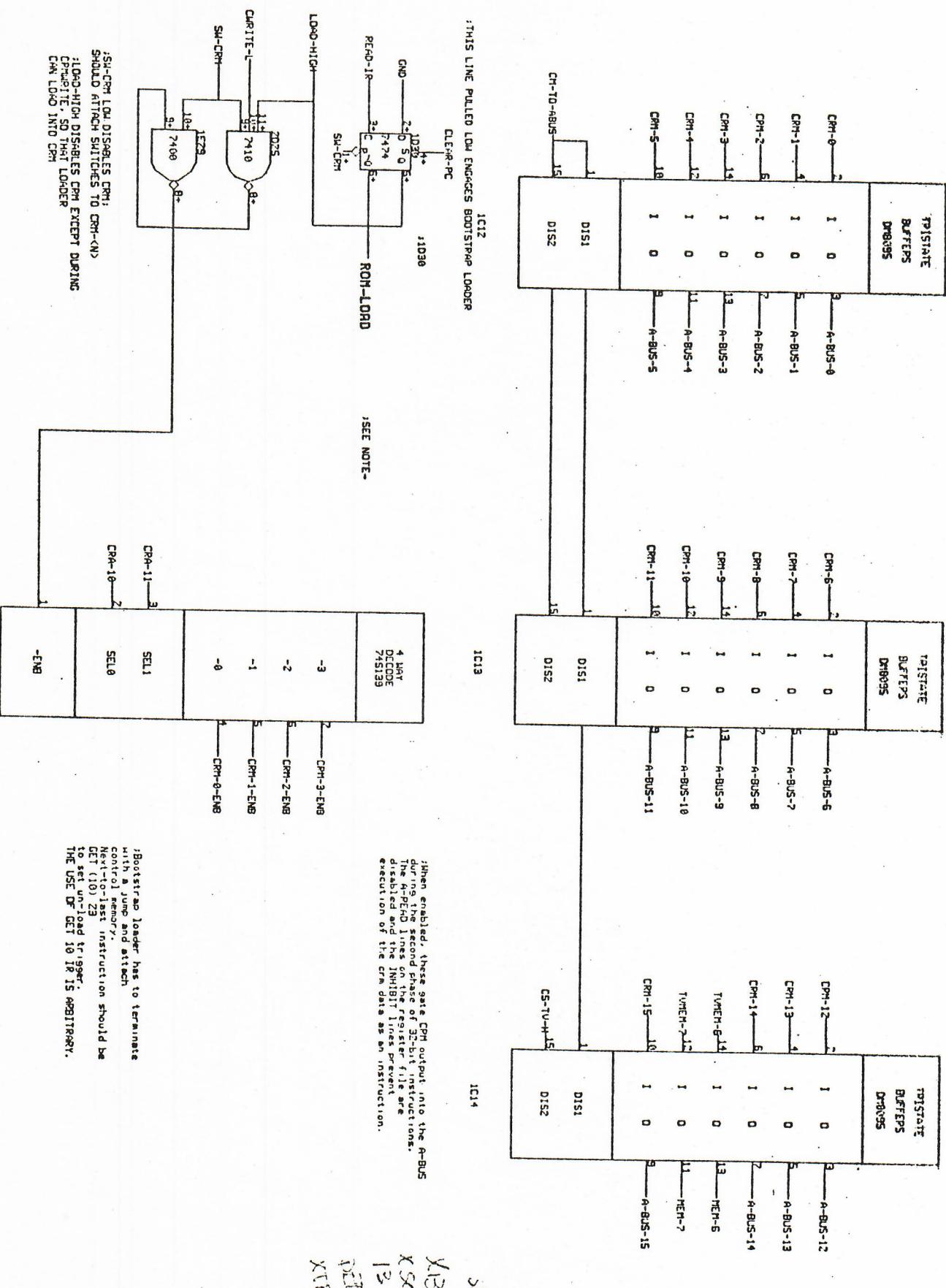
CONTROL MEMORY GATES

2500 MINSKY

01-APR-76 12:51

HQM: NTFH10

1018

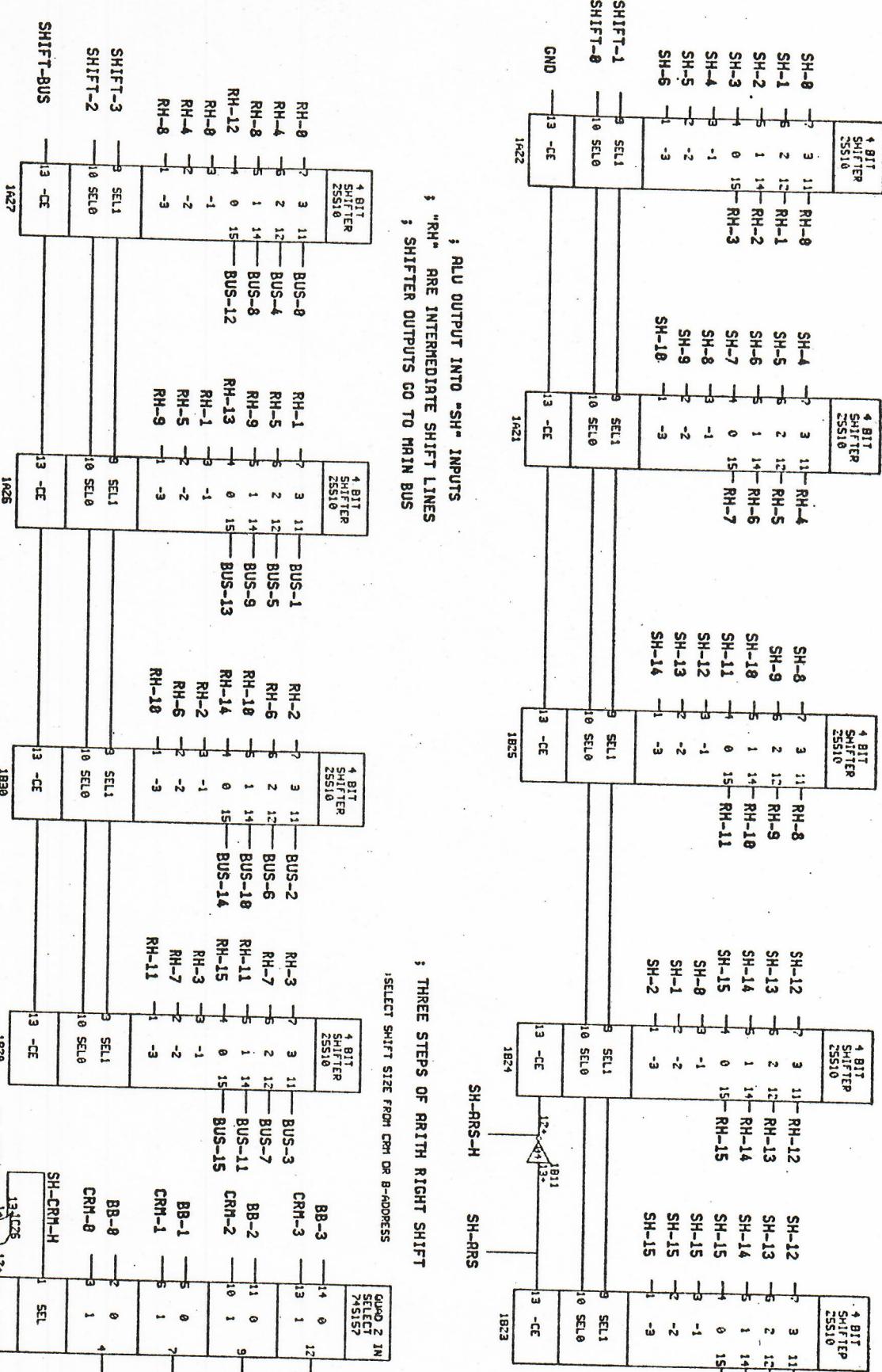


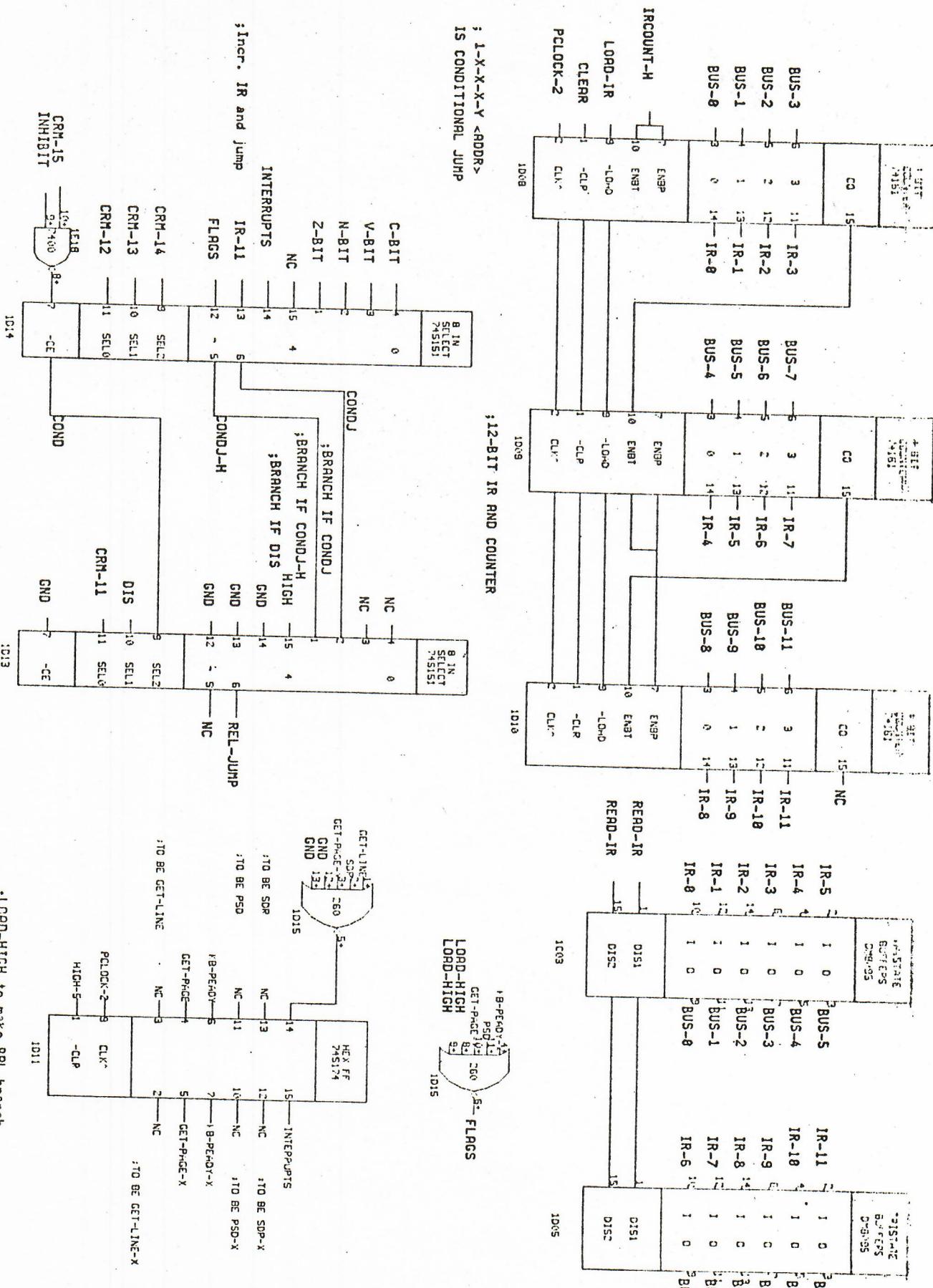
SHIFT ROTATE

MINSKY 2500

-26- EEP-7C 11·EA

卷之二





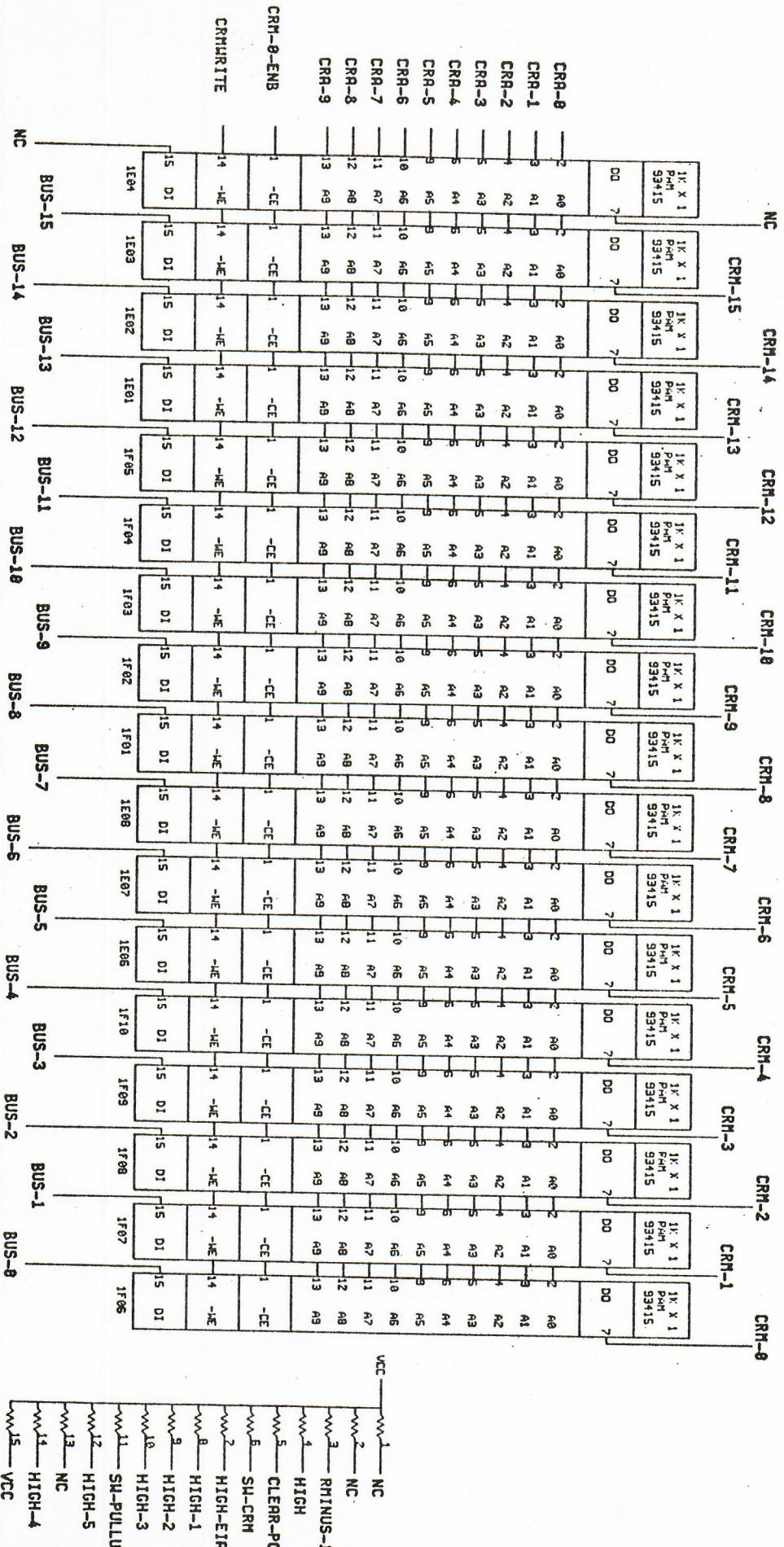
;LCD-HIGH to make BPL branch during ROM-1000

CONDITIONAL SELECT

INSTRUCTION REGISTER

卷一百一十一

;CRM-18 IS EXTRA BIT FOR PARITY OR WHATEVER



PARITY IN

; USE 93425 TRI-STATE RAMS

100

CONTROL MEMORY

PULL-UPS

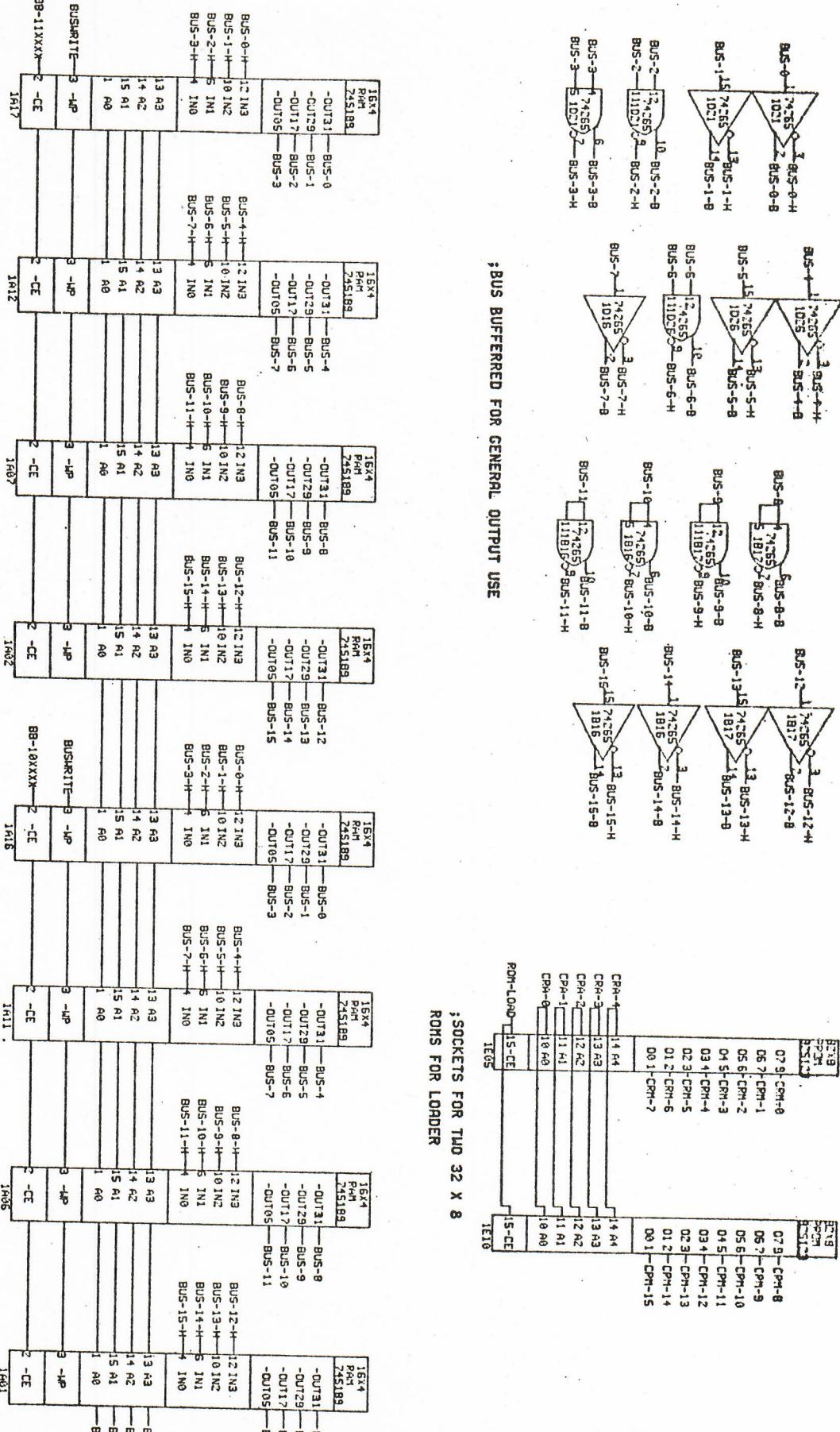
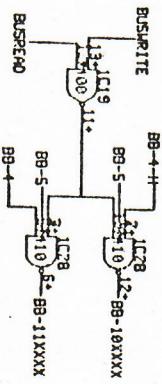
31-MAR-76 19:13

HOM. · HINTERZ

SCRATCHPAD REGISTERS

29-FEB-76 13:25

HQM: NTFH14

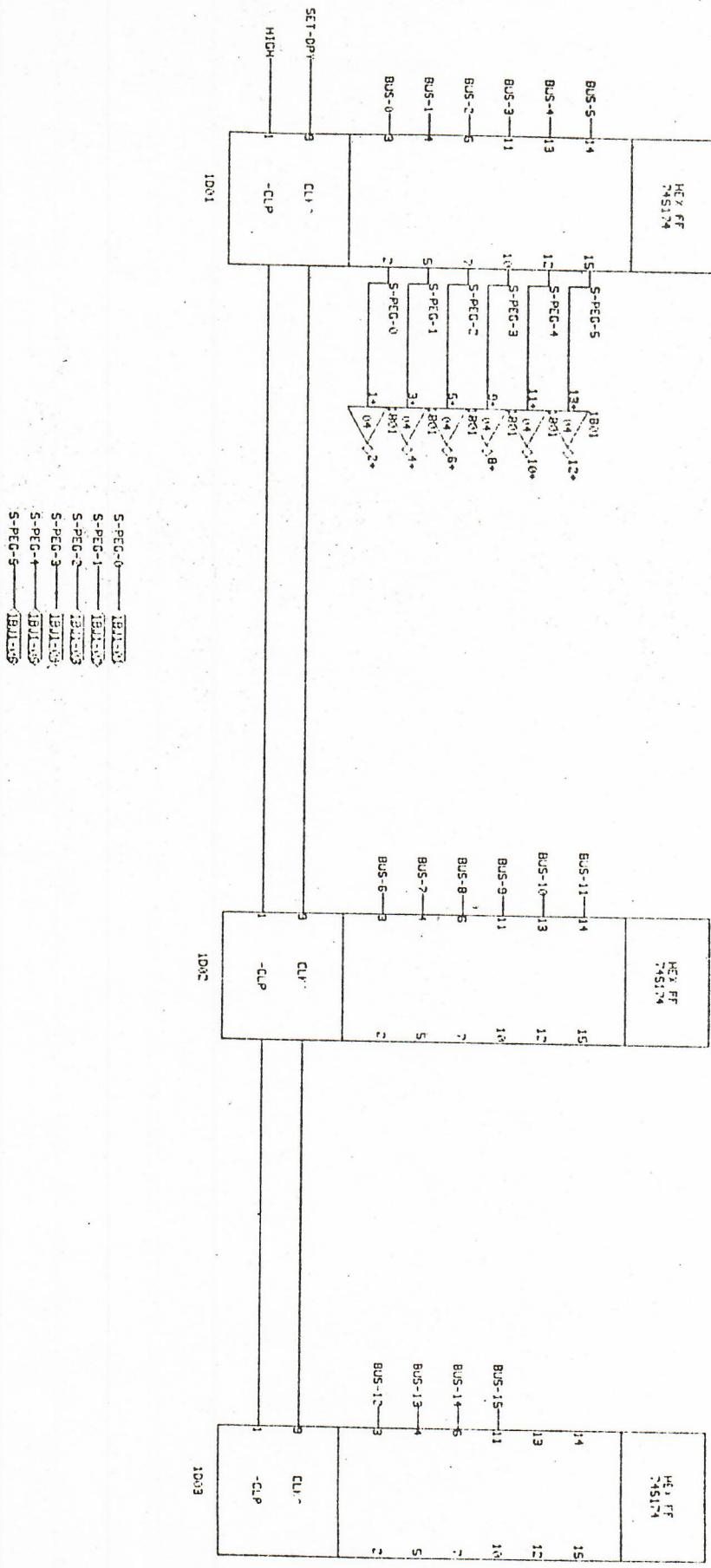


NOTES

TFH ORDER CODE

04-APR-76 16:56

HQH; NTFH15

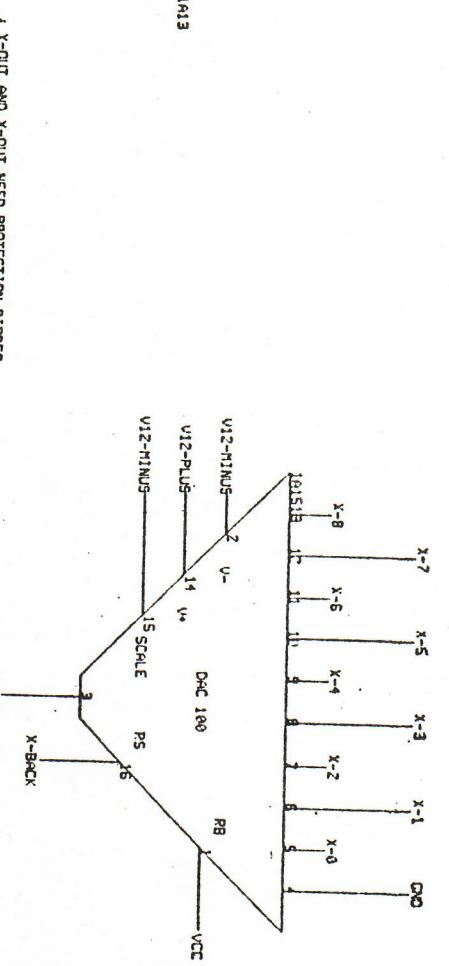
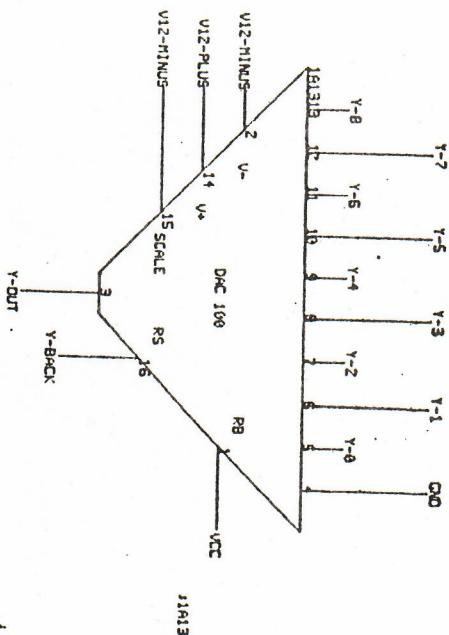
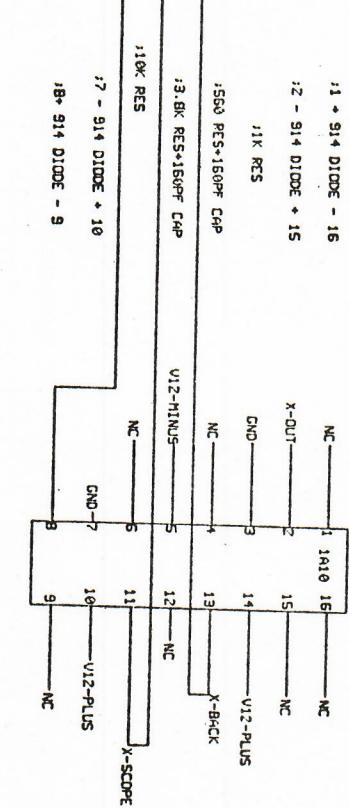
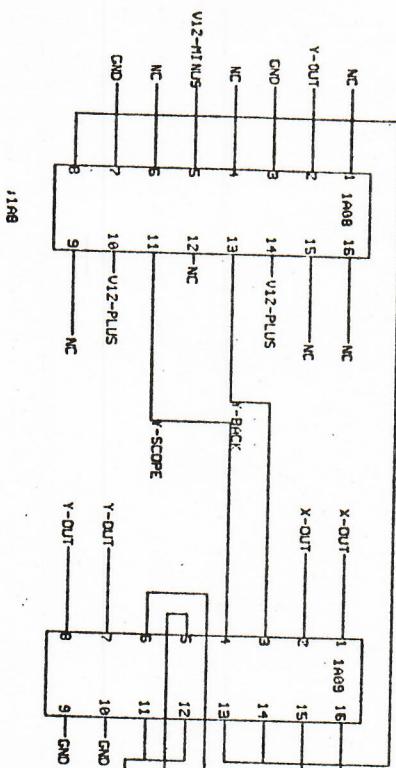


VECTOR DACS

MINSKY 2500

03-APR-76

17:35 HQM: NTFH16



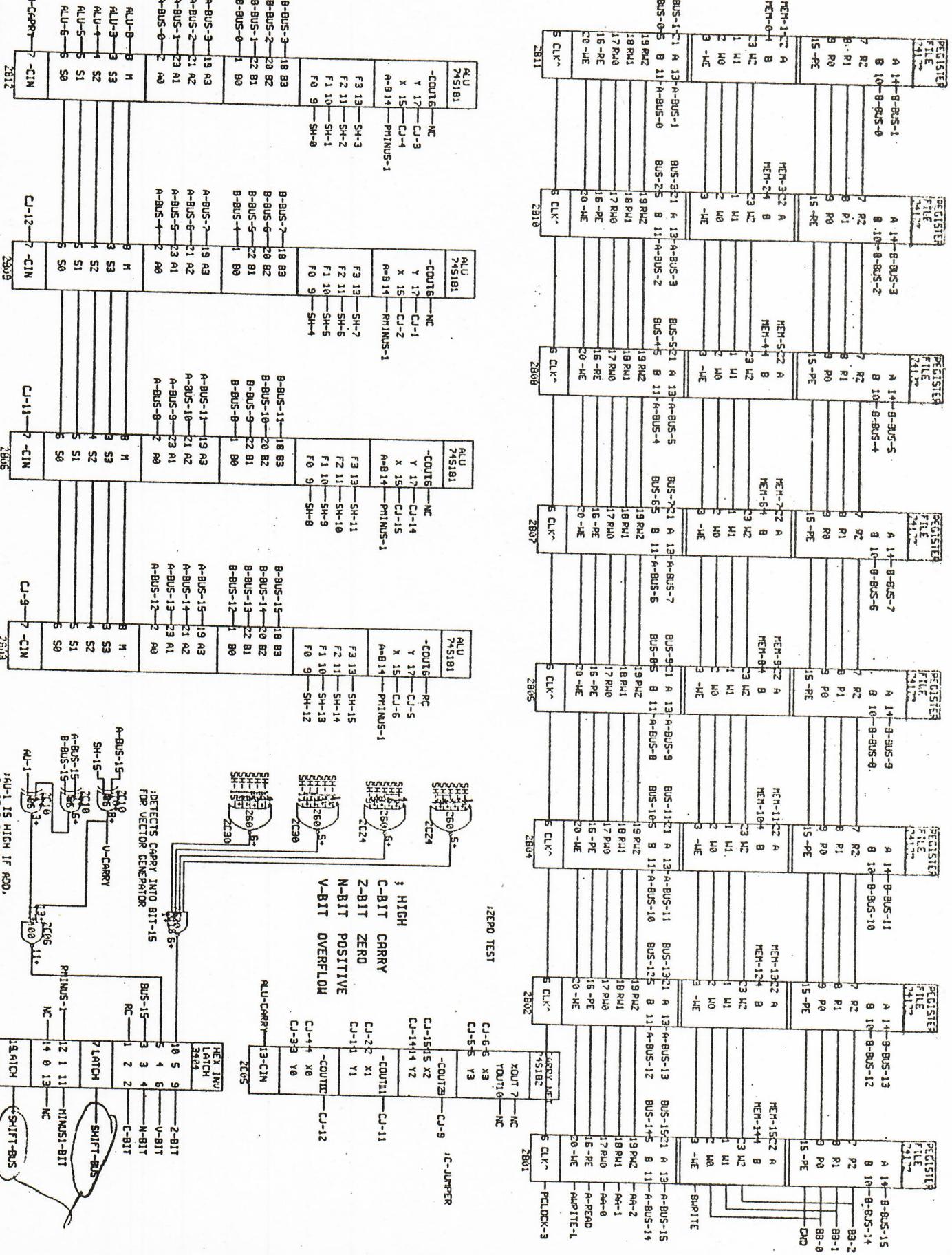
; THIS IS A 72247 OP-AMP

;1A09

; Y-DUT AND X-DUT NEED PROTECTION DIODES

; PINS 4 AND 10 EACH HAVE 470MF CAP TO GND
; PUT NEAR VECTOR GENERATOR

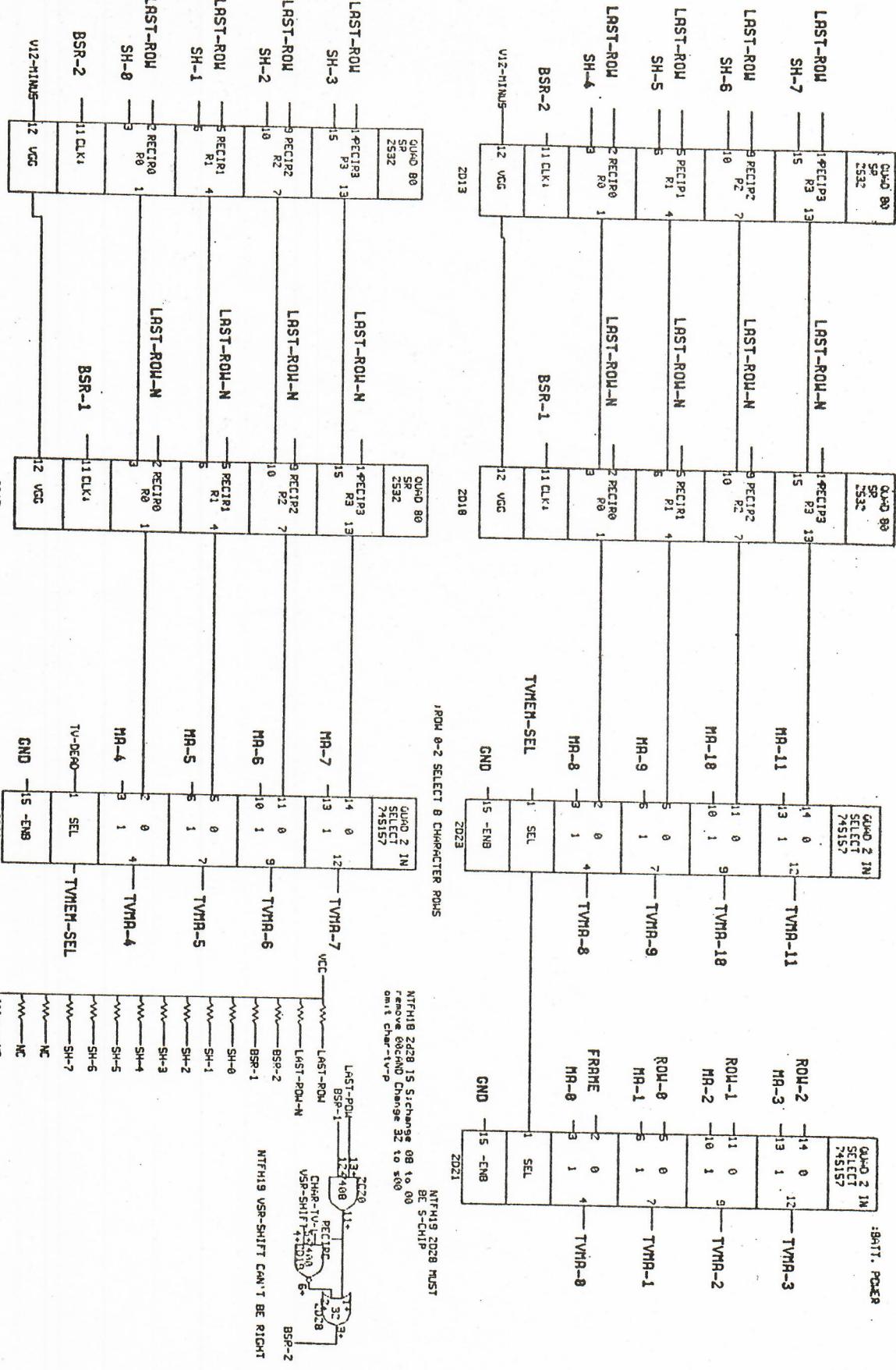
;1A10



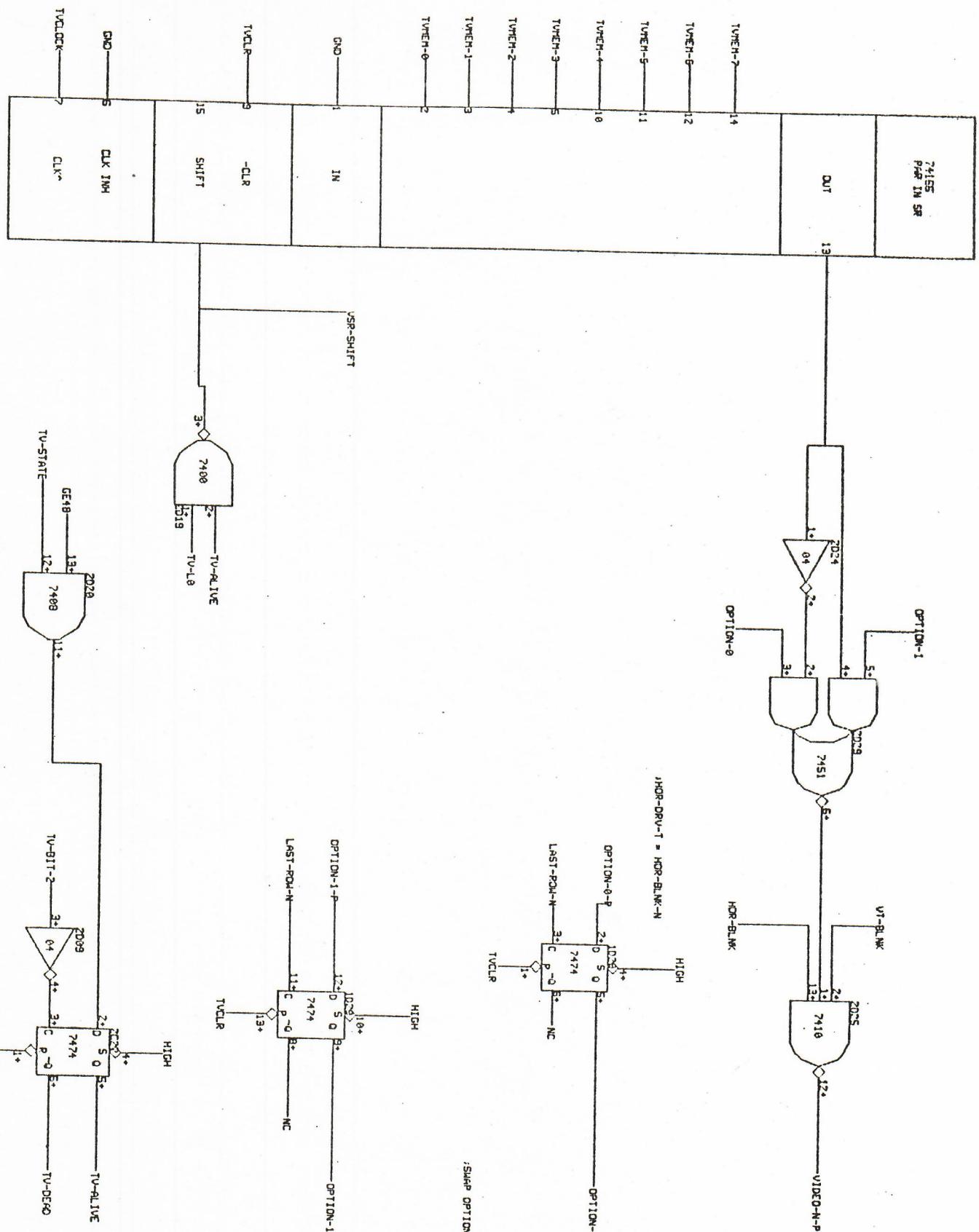
MINSKY 2500

29-FEB-76 13.29

HUM. NETHL.



RECYCLE TEXT-LINE THIS BY 02/23 L29220 2023 MUST BE LS 157 CHIPS

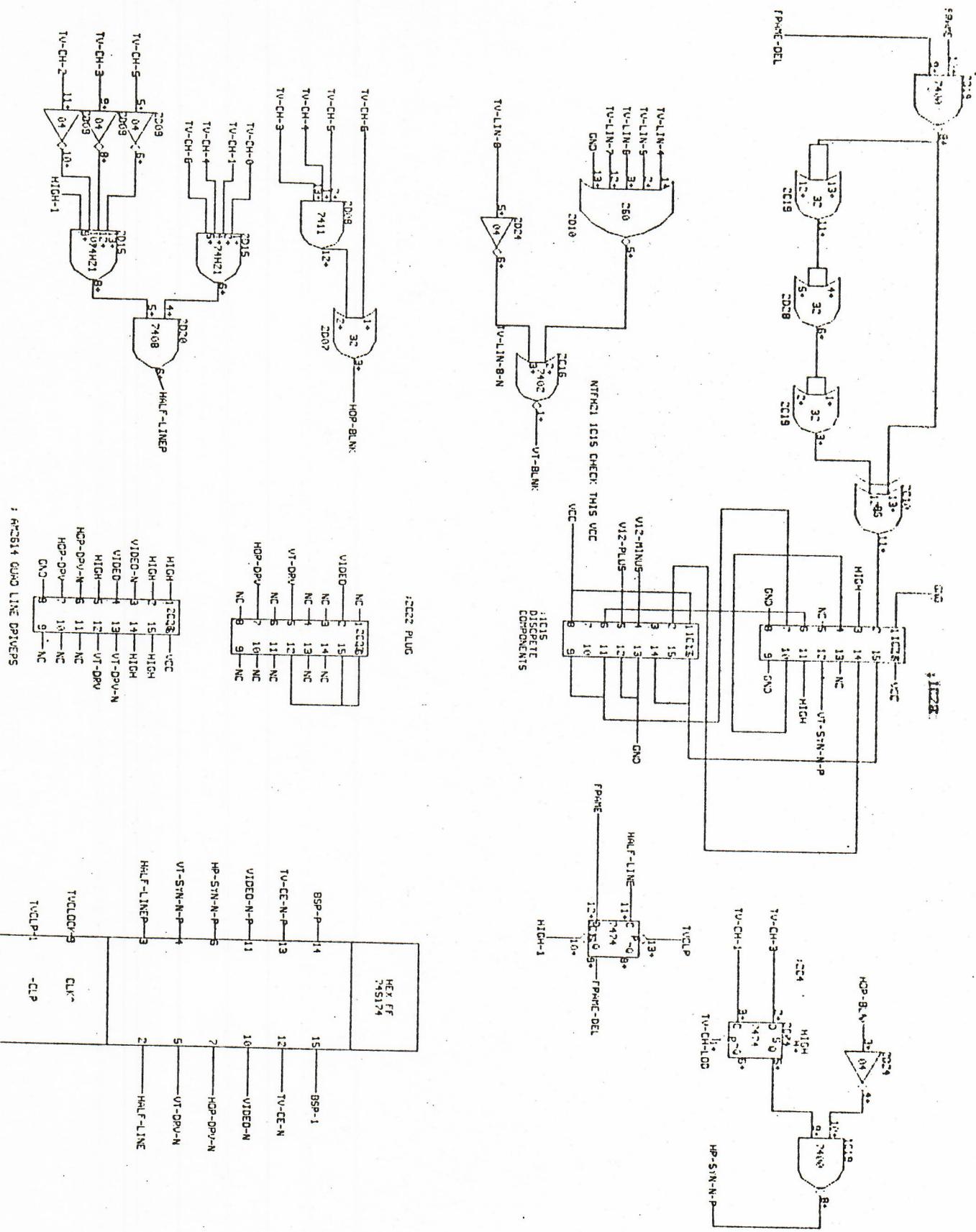


TV SIGNALS

INCLUDING DRIVERS

Q3=APP=76 1E:09

HOM. MITTE



LINE BUFFERS

ADDRESS MILITARY

G1-ABB-ZC 33: 18

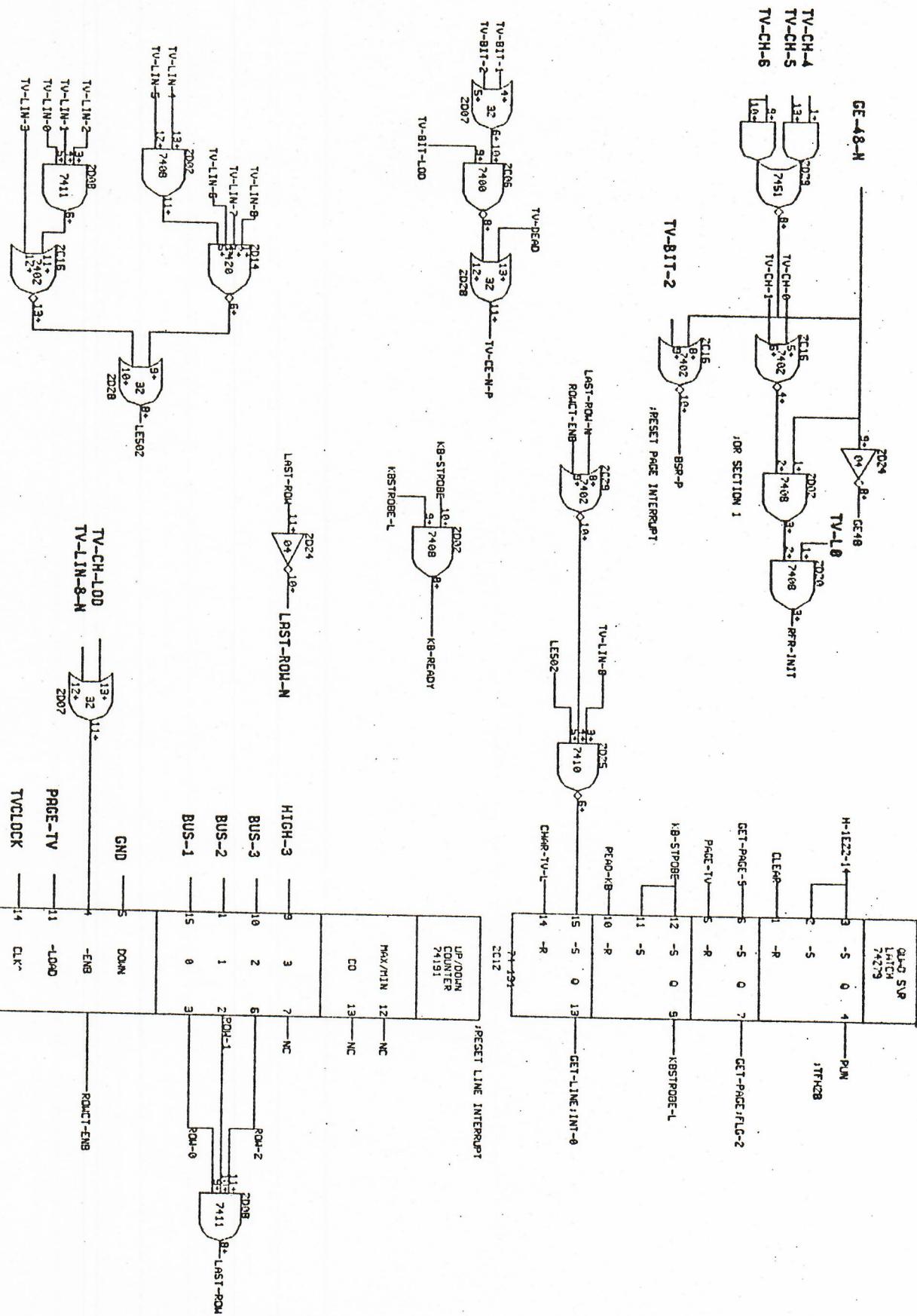
161

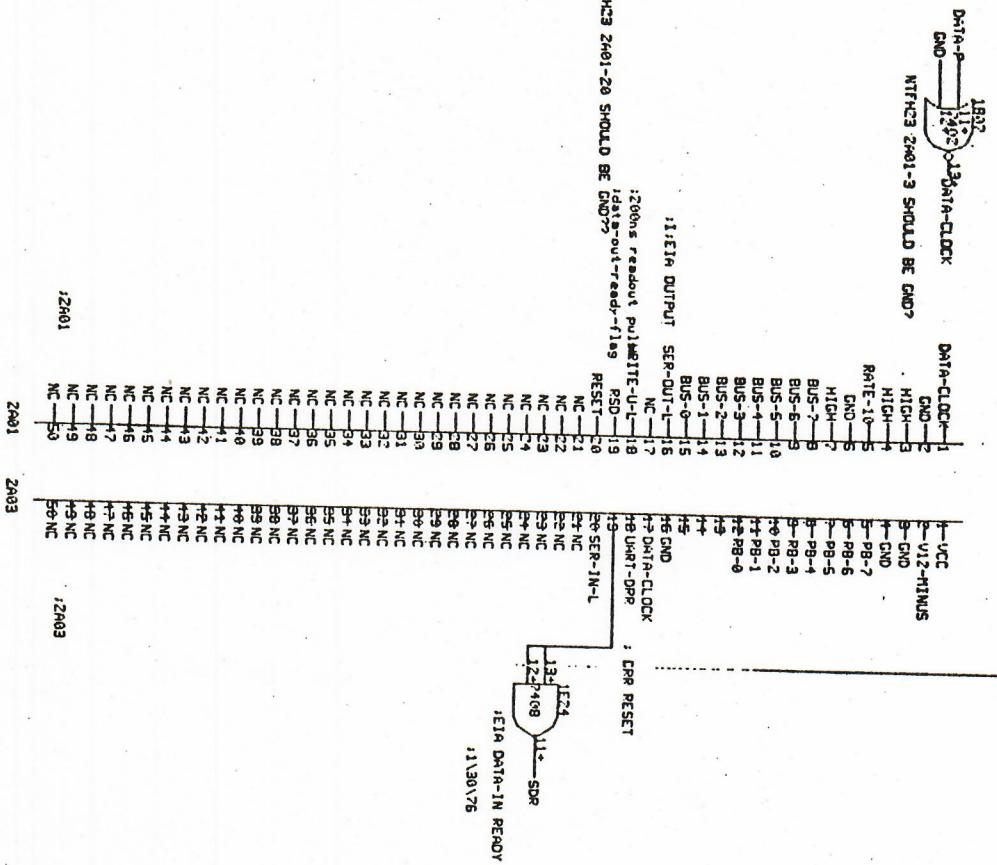
TV SIGNALS

INCLUDING DRIVERS

02-APR-76 11:23

NUM. 1175



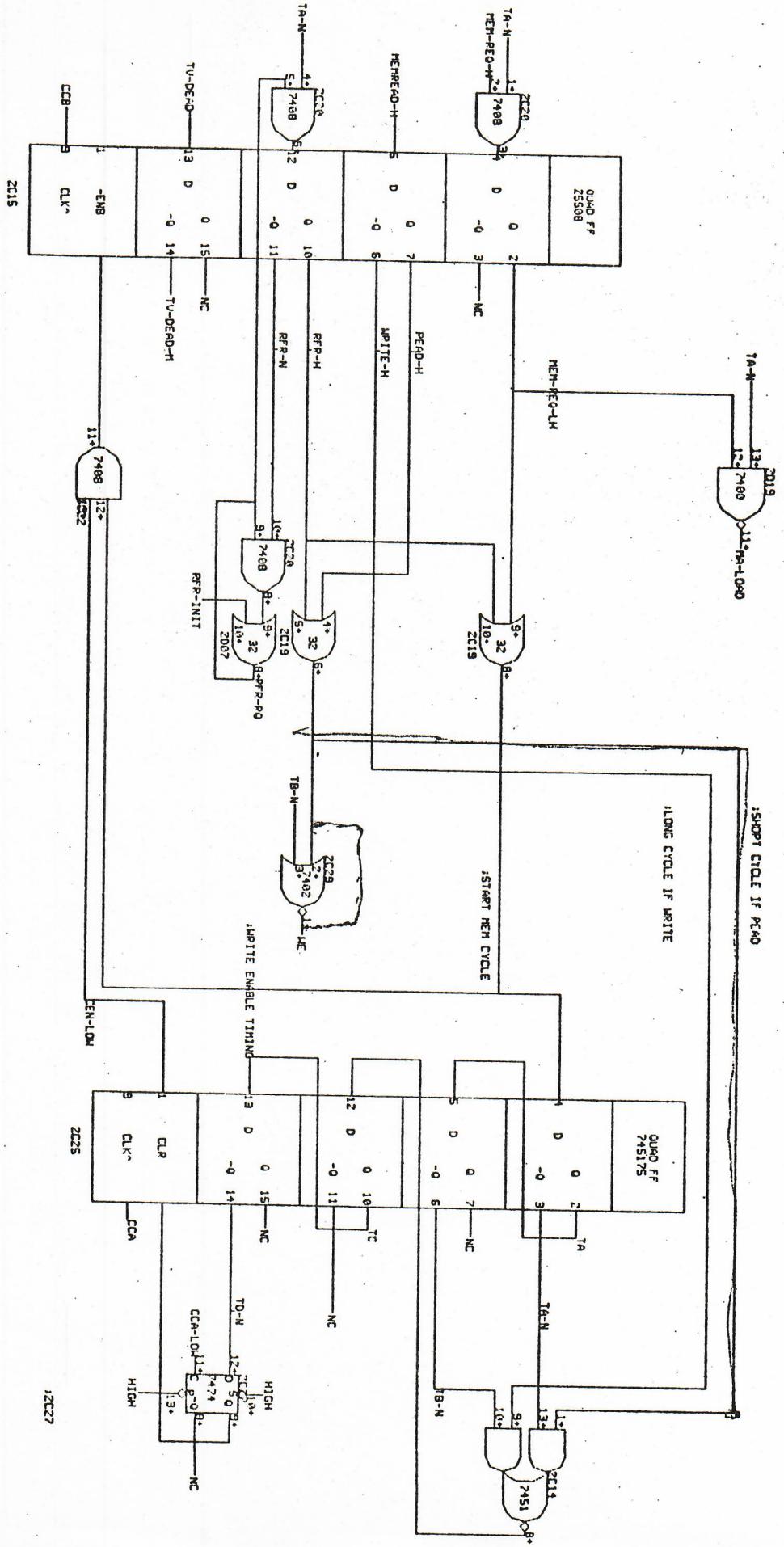


UART

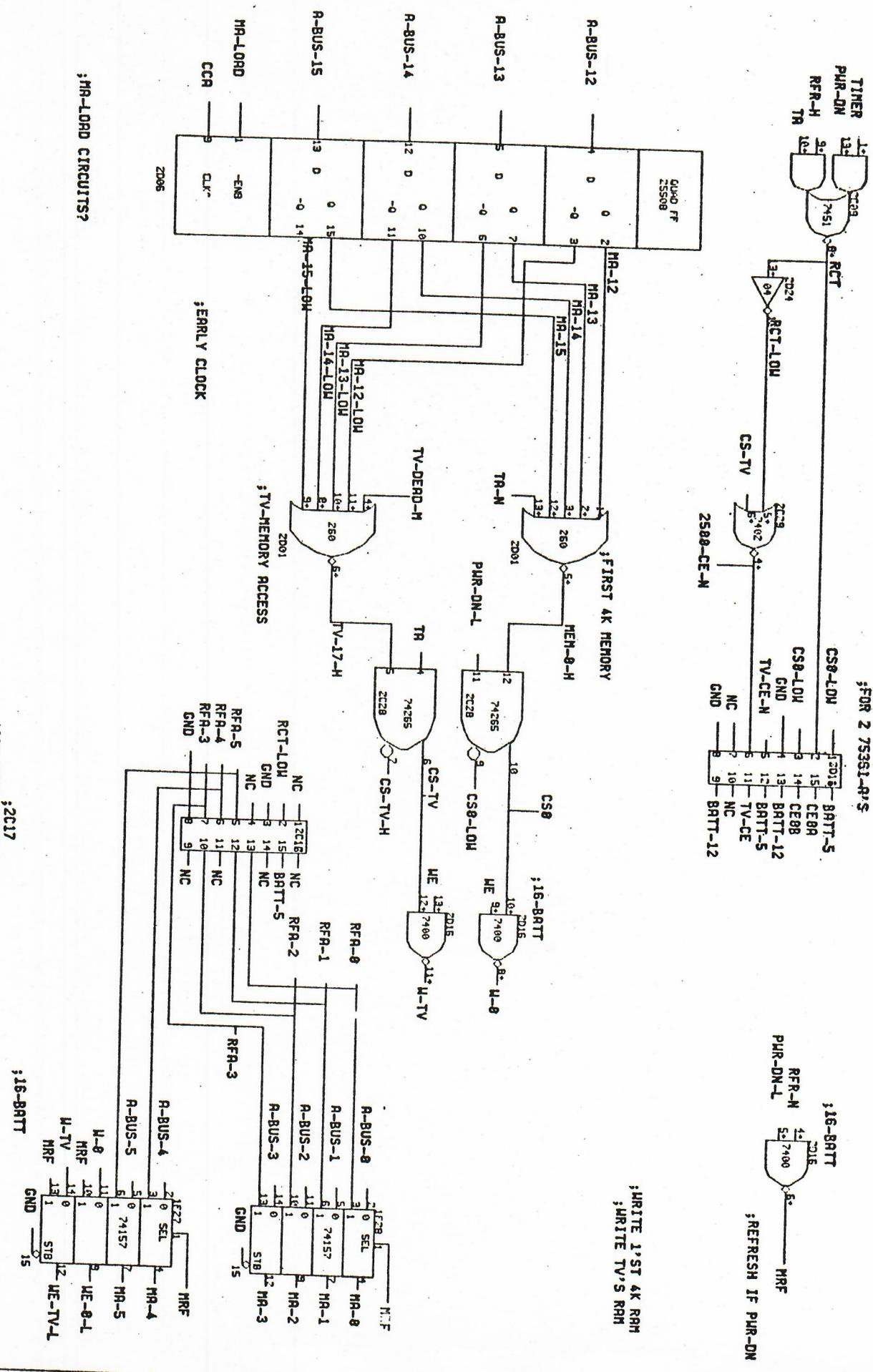
UNIVERSAL SECTION

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三



DISABLE UNTIL MEM-DONE



MEMORY ADDRESS REGISTER

250

29-FEB-76 14:32

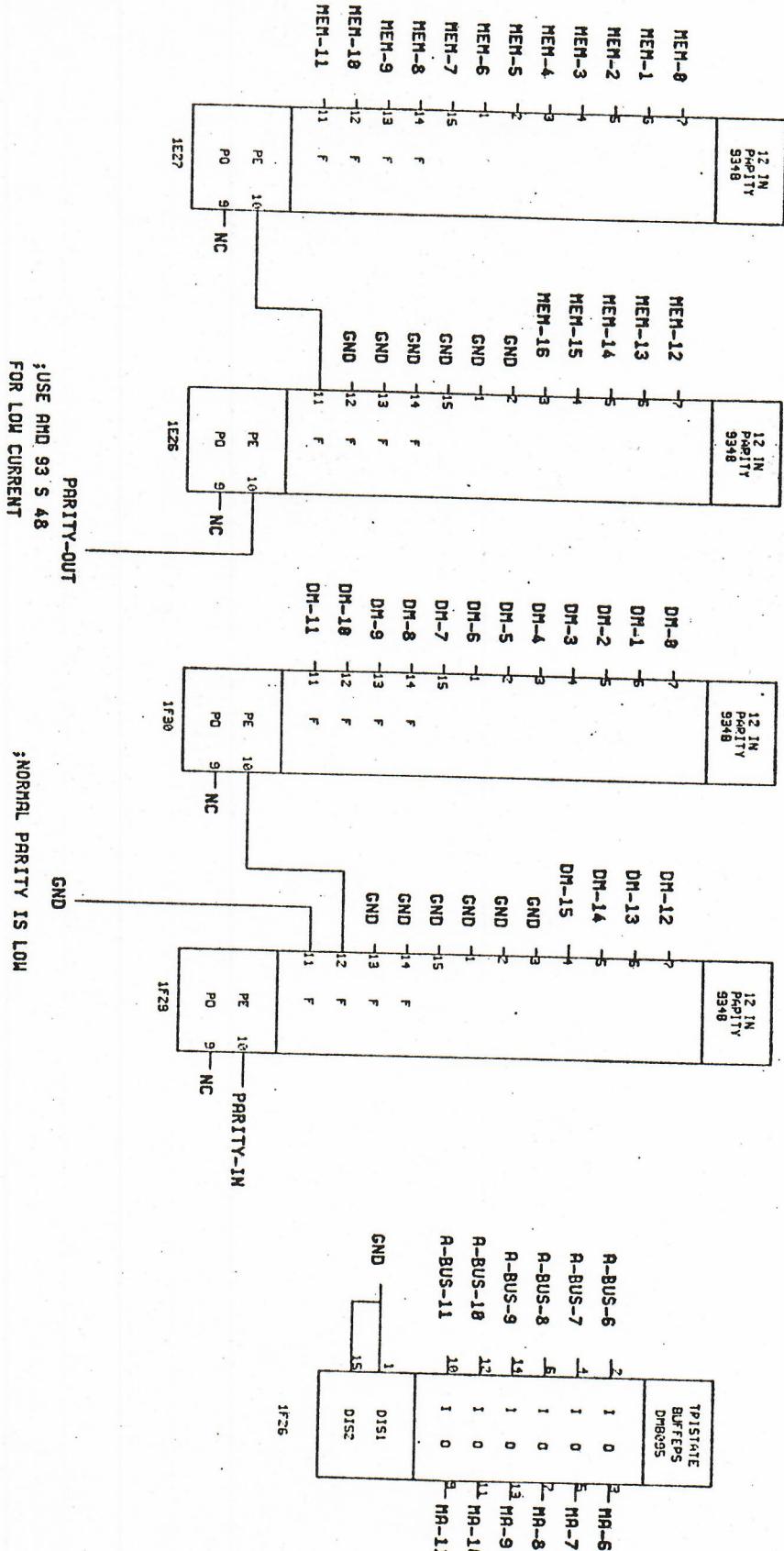
HEM: NTEHNS

PARITY CHECK

MEMORY 2500

29-FEB-76 14:33

HQM: NTFH26

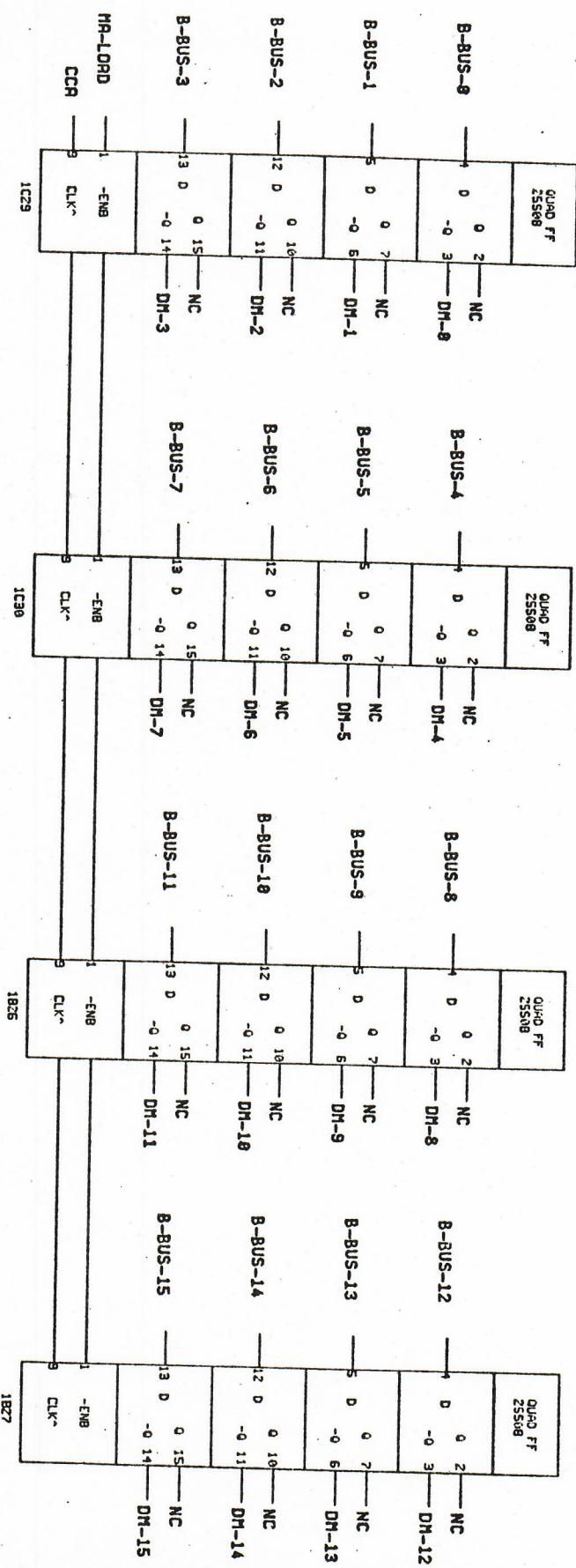


MEMORY DATA REGISTER

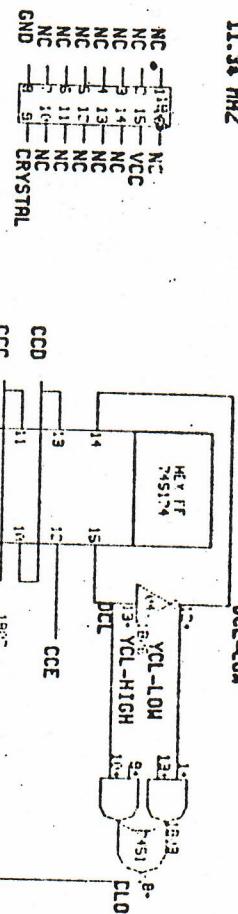
۲۵۰

28-FEB-76 1A 2F

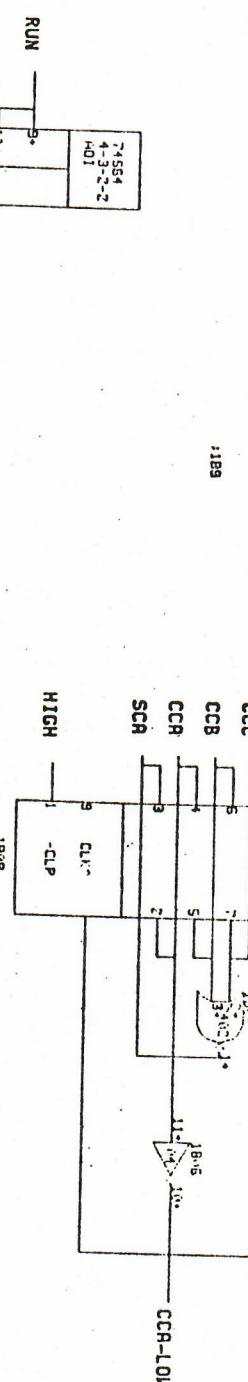
二二



CRYSTAL
11.34 MHz

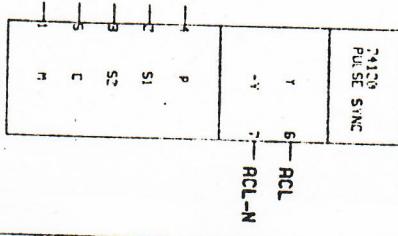


;FREQUENCY
DOUBLER
;CCE IS EARLY CLOCK



;ST=RUN\\\$INGLE-STEP

;ACL = MAIN
PROCESSOR CLOCK



74554
4-3-2-2
KD1

~~SECRET//NOFORN FOR NMH ACCESS~~

MEN-REQ-H TR - 8° - STC-LOW

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TR — 11
READ-H — 12
TD-N — 13

1B16

CRYSTAL
YCL-L04

Pclock-1

STEP-1 ON

	1815
PULSE SYNC	1810

C
SOC

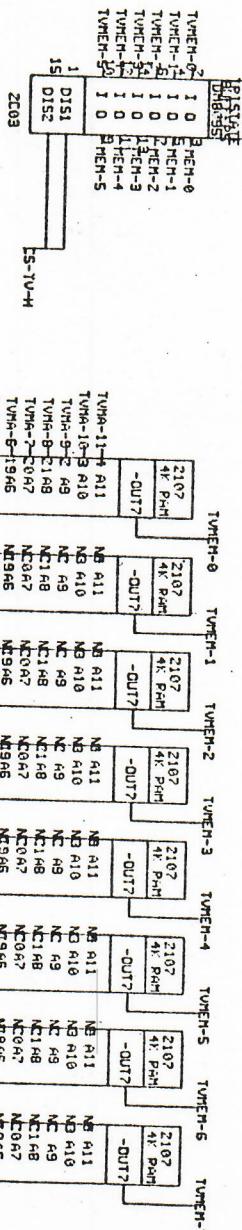
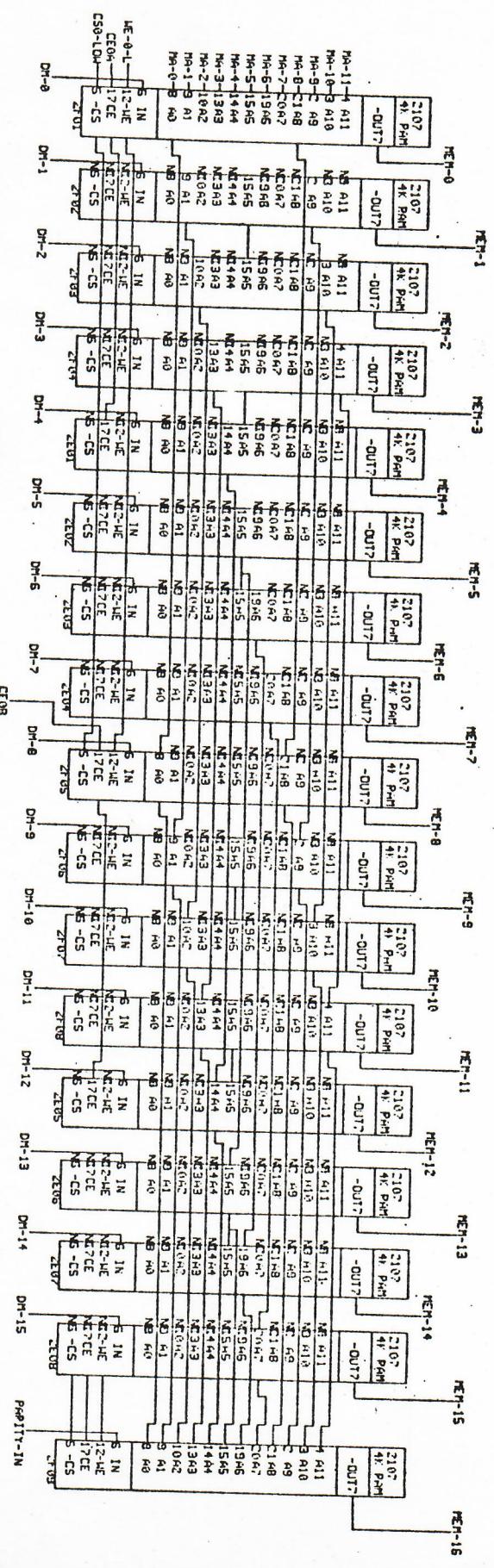
CLOCK CONTROL

2588

DA-APP-76 22: E

1111

;FIRST 4K OF MAIN MEMORY on main board



BE SURE WIRELIST DOESN'T CONNECT 1-8-11 ON MEMORY CHIPS
other two gates on
IC14 (TUM-10)
CONNECT
ZEL3-1 2EJ1-3 (BATT-5-N)
ZEL5-1 2EJ1-4
ZEL3-8 2EJ1-11 (BATT-12)
ZEL5-8 2EJ1-12
ZEL3-11 2EJ1-05 (BATT-5)
ZEL5-11 2EJ1-05 (BATT-5)

;4K BY 8-BIT FONT MEMORY

use signetics 2804's