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CE 3101
Lab 10
5/20/18

CE 3101 Lab Experiment 10

Abstract

Often in the consumer electronics industry, its necessary to make decisions based on really small (or large) signals. When such a case arises, it can be difficult or damaging for the central processing unit or microcontroller to operate using these signals. For that reason, signal conditioning circuits are often designed when both range signals to an appropriate range and protect the microcontroller from damaging voltages. To construct such a circuit, as we have done in previous laboratory experiments, op-amps are used with particular resistor configurations which allow the signal to be ranged appropriately. Sometimes however, the impedances from the signal sources are not appropriate for proper configuration. To solve this, a unity gain buffer is often used to buffer the input signal from the circuit operating off its voltage. Using this in series with the ranging circuit provides and ideal, ranged source to the microcontroller. Even this, however, may not be appropriate for proper functionality. For extremely small signals, noise from external sources may corrupt the input signal. To prevent this, bandgap filters can be constructed using a series of high and low pass butterworth op-amp filters. These filters are designed similarly to the ranging circuit but use RC configurations to produce cutoff frequencies. Placed in series with the buffer and the ranging circuit, a microcontroller can then be fed a buffered, ranged, and filtered signal for ideal operation.

The purpose of this lab was to explore such a configuration. In previous labs, the construction of the buffer and ranging filters had been explored with great success. In this lab however, the filtering capabilities would be added. In doing this, a circuit was constructed which would range a [-200:200] mV signal to a [-4000:4000] mV range while buffering the input and filtering out signals larger than 15 kHz and smaller than 100 Hz. The circuit was first designed and then simulated using the PSPICE circuit simulation software. Upon proper verification of the design, the circuit was implemented on a breadboard and then measured using the analog discovery's network analysis function. The results indicated proper design, with minor error most likely a result of rounding capacitance and resistor values. The design and results of this experiment can be observed in the following section.

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Experiment

The design of the signal conditioning circuit required the following:

Input: [-200:200] mV -> Output: [-4000:4000] mV

Lower cutoff frequency: 100 Hz

Upper cutoff frequency: 15 kHz

Buffered input

The first step taken in design of this circuit was determining the RC configuration to use for the highpass filter step. To do this, a capacitance of 1 µF was chosen due to its commonality and ability to work with resistors in the kΩ range. Next, resistance values were calculated using the following methodology:

$$R = \frac{1}{2\pi(100Hz)(1\mu F)} = 1591.55\Omega$$

$$R_2 = (0.707)(1591.55\Omega) = 1125.23\Omega \rightarrow 1100\Omega$$

$$R_2 = (1.414)(1591.55\Omega) = 2250.45\Omega \rightarrow 2200\Omega$$

$$C = 1\mu F$$

The second step in the design of the signal conditioning circuit was determining the RC configuration for the lowpass section of the circuit. Similarly, to the design of the highpass filter, a common resistance value was chosen that would work with capacitors of a reasonable capacitance. For this, a resistance of 1000 Ω was chosen. The capacitors to use in combination with the resistors were then calculated to be:

$$C = \frac{1}{2\pi(15kHz)(1000\Omega)} = 1.06*10^{-8}F$$

$$C_2 = (1.414)(1.06*10^{-8}F) = 15nF$$

$$C_2 = (0.707)(1.06*10^{-8}F) = 7.5nF$$

$$R = 1000\Omega$$

The combination of those RC configurations would allow all signal outside of the range between 100 – 15000 Hz to be filtered out. Next, the amplification resistor configuration was needed. This would involve scaling a [-200:200] mV signal to [-4000:4000] mV. This was a process done similarly in previous labs, and involved the following calculations:

$$m = \frac{(4000+4000)mV}{(200+200)mV} = 20$$

$$V_o = 20V_s + b \rightarrow 4000 = 20(200) + b \rightarrow b = 0$$

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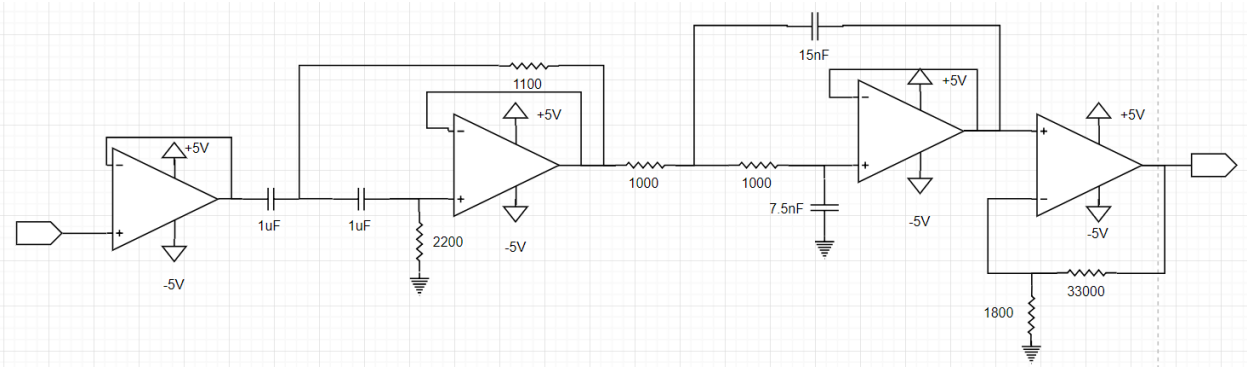
Since the amplifier was being implemented using a non-inverting configuration, it meant the resistor ratio for amplification was related to m in the following way:

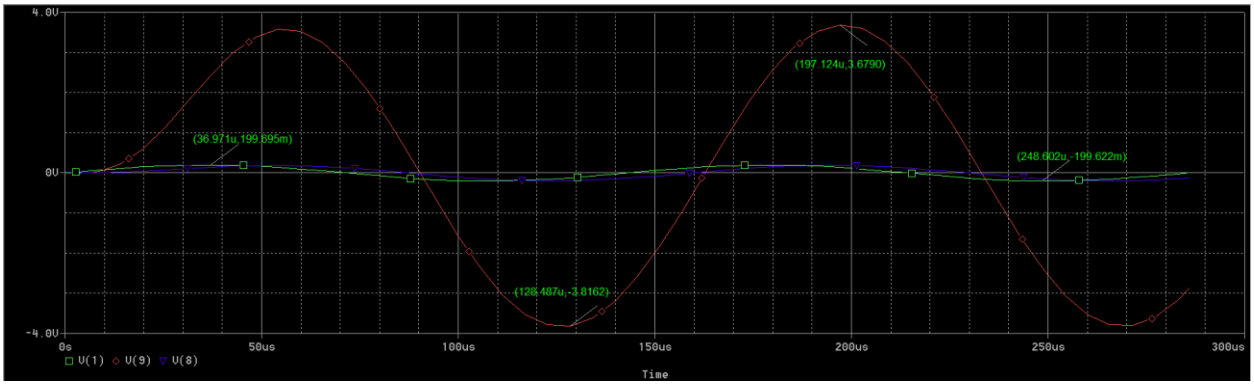
$$[\frac{R_1}{R_2}+1]=m \rightarrow \frac{R_1}{R_2}=19$$

Choosing resistors available as standard resistors as specified by International Electrotechnical Commission standard IEC 60063:2015, R1 was chosen to be 33 kΩ, and R2 was chosen to be 1.8 kΩ. This yielded a resistor value of 18.33 – not perfect, but close. Such a ratio would be expected to yield an error of 3.5%, within the acceptable error range of 5%.

Combining all these circuits in series yielded the desired signal circuit conditioning design. Such a design schematic looked as follows:

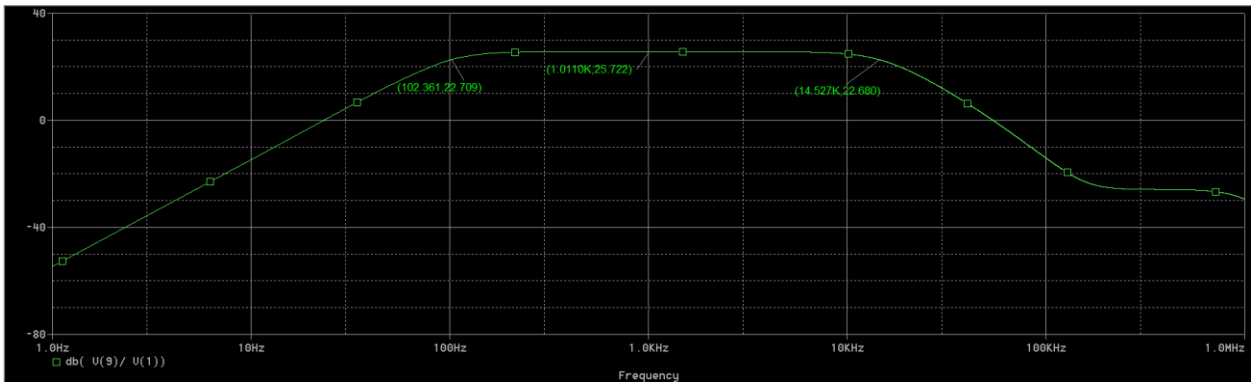


After design of the circuit, it was tested using PSPICE software for verification. First, a time domain analysis was done to verify the amplification design. This resulted in the following waveform output.



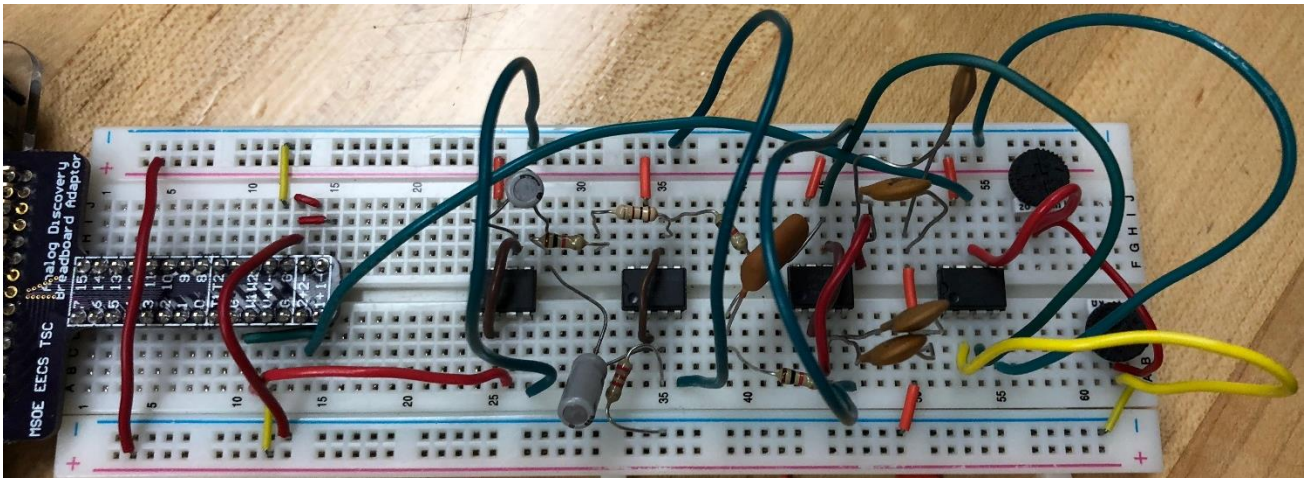
As can be seen from the waveform, a [-200:200] mV input signal was ranged to [-3862:3679] mV. As expected, the input wave was not perfectly amplified to [-4000:4000] mV, which is due to the rounding involved when choosing proper resistors for amplification. Due to this, an error of 6.3% was being observed when observing the peak to peak differences. This is slightly larger than expected, but the

error introduced is being observed at both the maximum and minimum voltages, so it makes sense. This simulation seemed to verify the design amplification. Next, the frequency domain behavior was simulated using the AC sweep feature of PSPICE. This resulted in the following waveform.



For the frequency domain, it was expected that the gain in dB would be 26, with a lower cutoff frequency of 100 Hz and an upper cutoff frequency of 15 kHz. The simulation of this seemed to verify the design, with a lower cutoff frequency near 102 Hz, and an upper cutoff frequency near 14.5 kHz. Additionally, the gain can be observed to be close to 26 dB, at 25.7 dB. With both the amplification and filtering capabilities of the signal conditioning circuit verified, it was time to implement the circuit using physical hardware.

When constructing the actual circuit, a 7.5 nF capacitor was not available for use. To handle this, 4 2nF capacitors were placed in parallel to approximate this capacitance. This would yield a capacitance of 8 nF, so it was expected that the low cuff off frequency would deviate slightly from the desired frequency. In addition, since 33 kΩ and 1.8 kΩ resistors were not readily available either, a 20 kΩ and 10 kΩ potentiometer were used to rather than resistors. This allowed the amplification to be fine tuned so it would be as close as possible to the desired output envelope. When the circuit was built, the analog discovery kit was used to generate the input waveform and provide 5 and -5 V power supplies. Construction of the circuit yielded the following.



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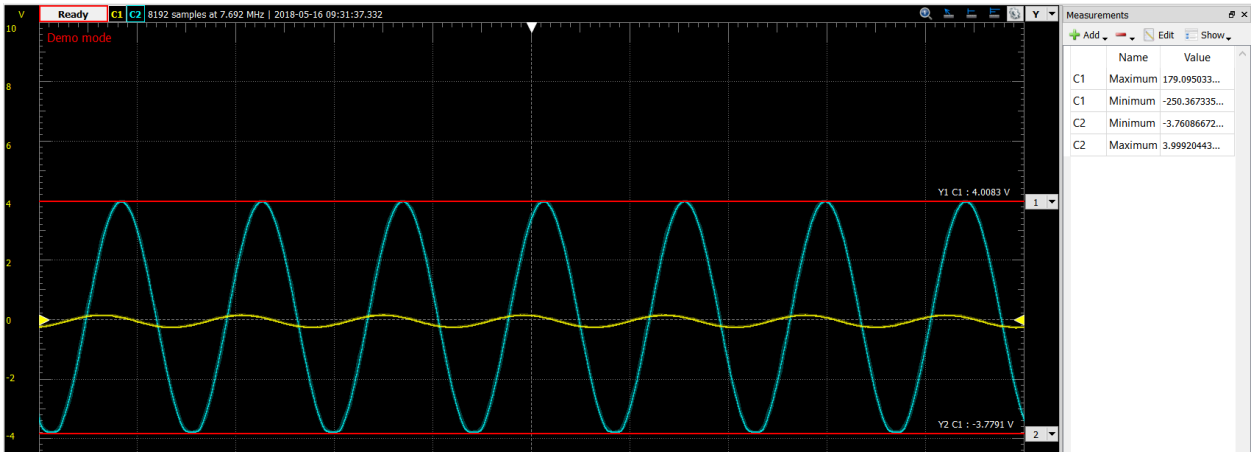
First, a time domain analysis was performed using the oscilloscope feature of waveforms. This yielded the following.



The time domain analysis yielded very good results – the maximum output voltage was almost exactly 4V, and the minimum voltage was close to the desired value. This yielded an error of 3.0% error – even better than the simulated results. This may seem abnormal that the actual results could have been better than the simulated results, but this makes sense in this situation because of the use of potentiometers. The potentiometers allowed the amplification to be fine tuned so that it would result in a maximum amplitude as close as possible to the desired value. It should be noted that the output voltage is out of phase with the input voltage (shown in yellow). This is expected behavior though and should not be treated as error. Since the filters are built using capacitors, its expected that the output voltage should lag the input voltage. Other than this, the shape of the output voltage was maintained from the input voltage. In summary, the oscilloscope view was able to verify proper amplification, with less error than simulated.

Next, an AC sweep was performed to verify and analyze the frequency response of the signal conditioning circuit. It was expected that input voltages below 100 Hz would be filtered out, and frequencies above 15 kHz would be filtered out. The AC sweep yielded the following.

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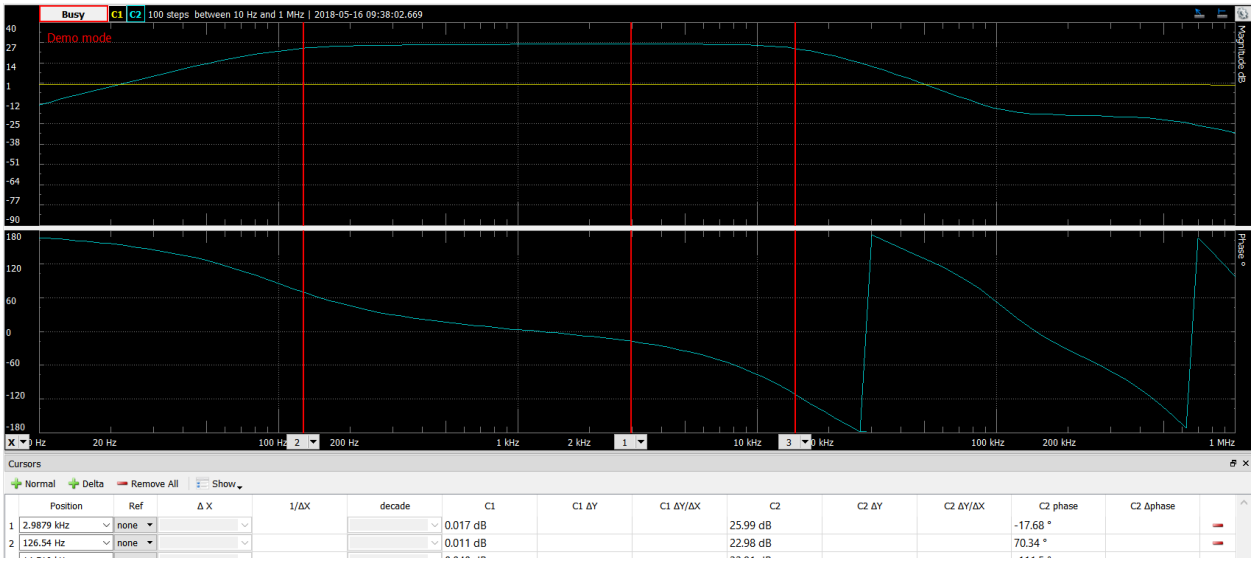

According to the AC sweep, the lower cutoff frequency occurred near 126 Hz, and the upper cutoff frequency occurred near 14.5 kHz. This behavior strongly mirrored what was observed in the simulation; in fact, the upper cutoff frequency agreed spot on with the simulation. As expected however, the lower cutoff frequency was slightly farther off, and this was a result of the design choice made when implementing the circuit. Rather than using a 7.5 nF capacitor, 4 capacitors were used to achieve 8 nF, so error was expected. The AC sweep observed a gain of 25.99 dB however, which was even better than the results of the simulation. The expected value was 26 dB, differing by only .01 dB. The results of this AC sweep validated correct design of the filtering capabilities of the signal conditioning circuit.

Conclusion

The purpose of this laboratory experiment was to design a signal conditioning circuit capable of ranging a [-200:200] mV signal to [-4000:4000] mV, while filtering out frequencies lower than 100 Hz and higher than 15 kHz, while also buffering the input voltage from the output voltage. The results of the laboratory exercise were very successful, and as a result, very instrumental in further and extending the theory taught in class. While lecture provided a very thorough explanation of this type of circuit, designing, building, simulating, and measuring the circuit helped fortify understanding of this topic. Building such a circuit in lab introduces aspects of design and decision making that aren't' necessarily necessary when designing on paper – such as making resistance and capacitance substitutions and approximations. Because of the value and rich fortification of theory (in addition to proper results), this laboratory experiment can be concluded to be a success.