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Lab 6
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CE 3101 Lab Experiment 6

Abstract

In the digital electronic industry, inverter circuits make up the base unit for almost all logic chips. The first inverting circuit was designed using a resistor and a BJT, and it was called an RTL inverter. This design has several disadvantages to it, such as power consumption, size, cost, and its voltage characteristics. Following this initial design, several others followed, further advancing the technologies. These were DTL circuits, TTL circuits, PMOS circuits, and eventually CMOS circuits. As the technology advanced, the size, power, and cost of the circuits were reduced, while their voltage characteristics improved. Eventually, this technology was integrated into chips, allowing for easy implementation of circuits. As manufacturers built their own brand of chips, they established “families” of chips, all designed with similar voltage characteristics so that they could be used together to build more advanced logic circuits. When integrated chips are from different families are used together, it's important that their voltage characteristics are inspected so that a designer is sure that they will work together. A chip family with a VOH lower than the required high input voltage for a different chip family would cause input voltages to be falsely interpreted as logic-0.

The purpose of this laboratory experiment was to explore 4 inverting chips from different chip families and analyze their voltage characteristics. To do this, chips were wired using a breadboard, and an analog discovery board was used to power, input, and read voltage levels for the chip. The 4 chips used for experiment were the CD4096, 74LS04, 74HC04, and 74HCT04 chips. These chips were tested using a 1 KHz, 5 V ramp function as an input for reading VOH, VIL, VM, VOL, and VIH. To test the time voltage time characteristics of the chips, a 1 KHz, 5 V square wave was used. The resulting findings of the experiment can be found in the following sections of this report.

Mitchell Larson
CE 3101
Lab 6
4/21/18

Experiment

The following circuit was used for testing all the inverter chips in this experiment. Different load resistance and capacitance was used for the chips and is noted in their analysis sections.

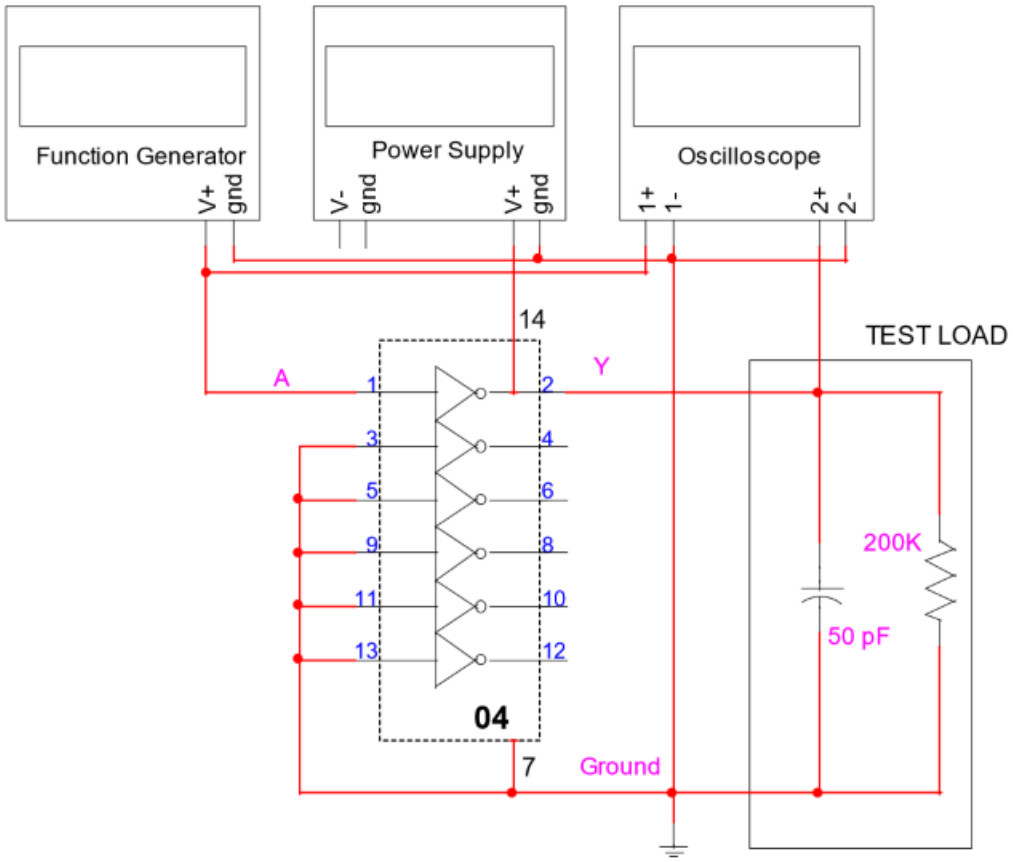
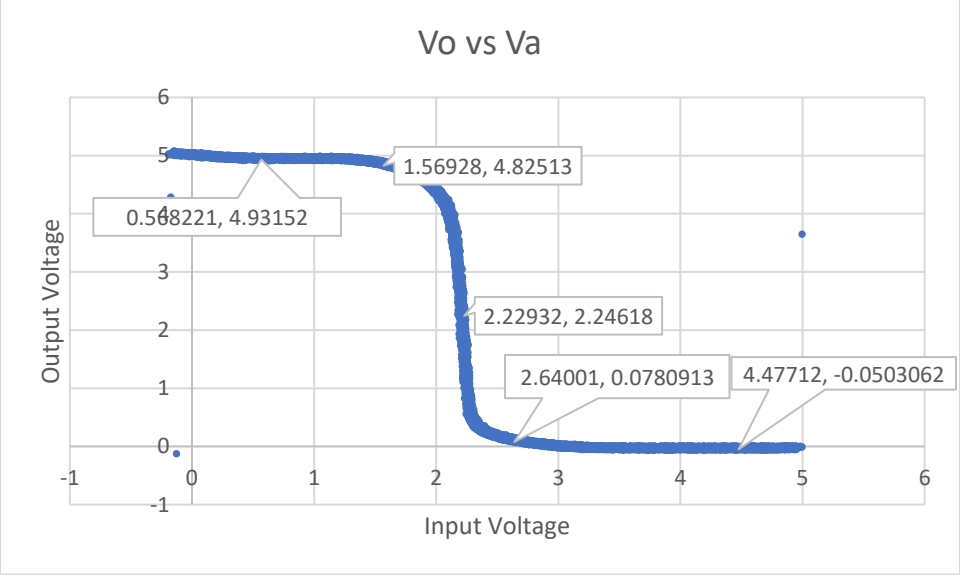


Figure 3: The Unit Under Test

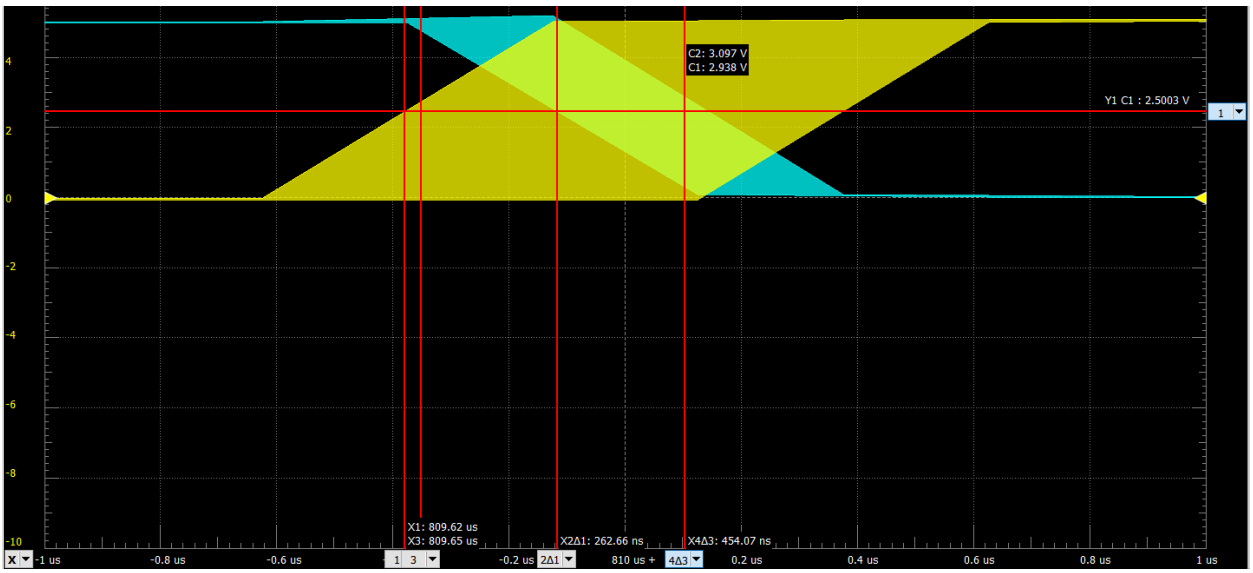
Mitchell Larson
CE 3101
Lab 6
4/21/18

CD4069

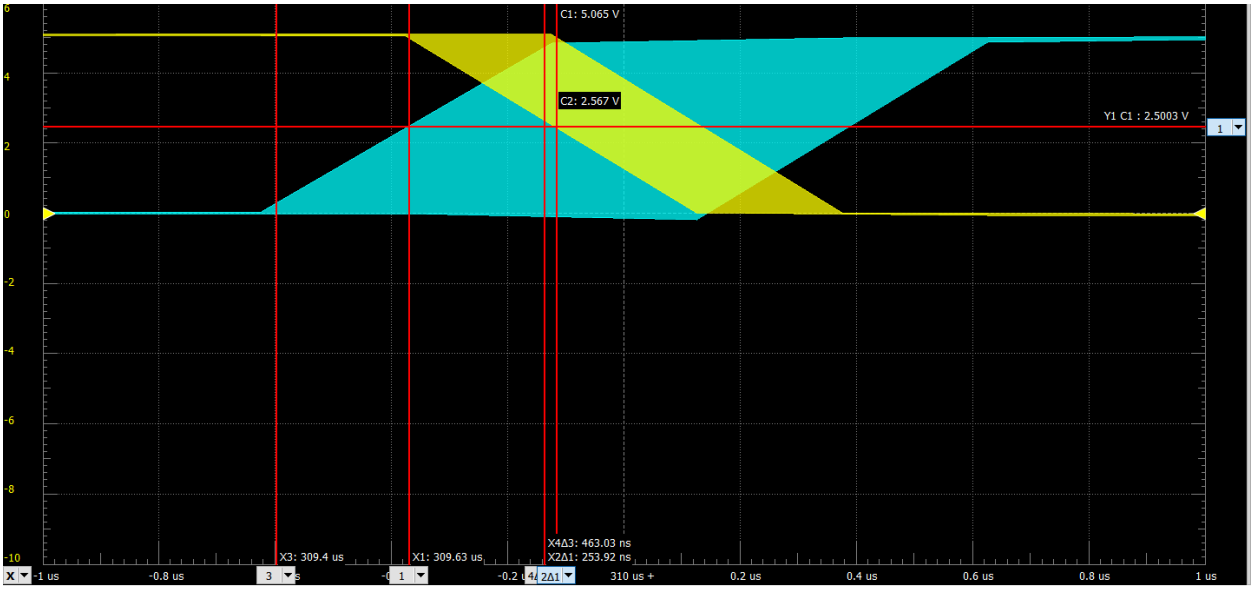
The following plot is data taken from the analog discovery kit and plotted in Excel for its extra analytical functionality. It shows a plot of output voltage against input voltage. The load resistance used for this circuit was 200 KΩ, and the load capacitance was 50 pF.



When the input voltage was changed to a square wave, the input and output voltages were observed to have the following propagation characteristics in the time domain.



Mitchell Larson
CE 3101
Lab 6
4/21/18



From the following plots shown above, the key voltage and propagation delay values could be extracted. While they couldn't be extracted as their exact values, best estimations were derived from the available data.

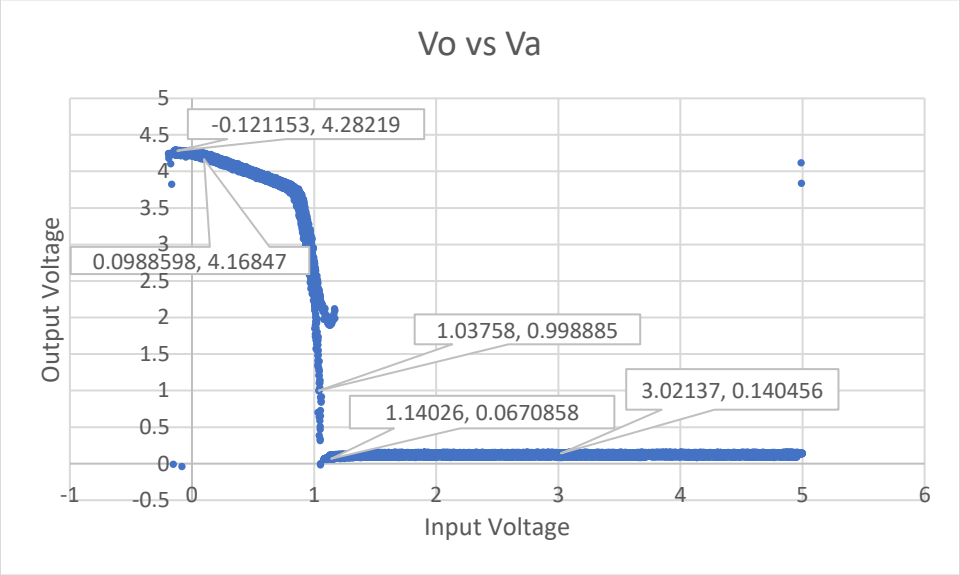
VOH:	4.93 V	VIL:	1.6 V
VIH:	2.6 V	VOL:	-0.05 V
NMH:	4.93 V – 2.6 V = 2.33 V	NML:	1.6 V - -0.05 V = 1.65 V
TPHL:	263 nS	TPLH:	234 nS
Tr:	463 nS	Tf:	454 nS

The CD4069 inverter chips exhibited a very smooth voltage-voltage curve, as shown in the plot above. The transition region that occurs is relatively small, and occurs close to the 2.5V input range, which is preferred behavior, as it increases the high and low noise margin. These characteristics would make it easier to interface with different types of chips, as a large range of input voltages would be acceptable for logic-0 and logic-1, with a relativily narrow range of input voltages that would result in undefined logic output. Additionally, the output low voltage was extremely close to 0V, which would are ideal characteristics, helping reduce power consumption and ensure proper logic levels when used as an input for other logic chips. Interesting to note however, is the 0.7V difference between output high voltage and Vdd. This suggests that power is being dissipated when a logic-0 is input into the inverting chip. The timing characteristics of this integrated chip appear to be similar to the timing characteristics of the 74LS04 and 74HC04 chip, but are significantly higher than the 74HCT04 chip.

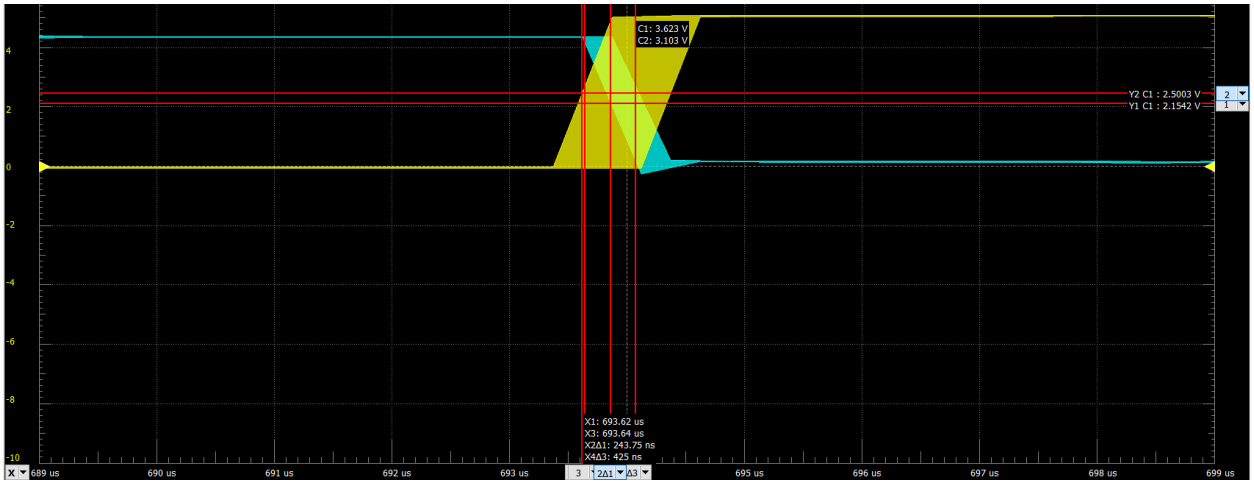
Mitchell Larson
CE 3101
Lab 6
4/21/18

74LS04

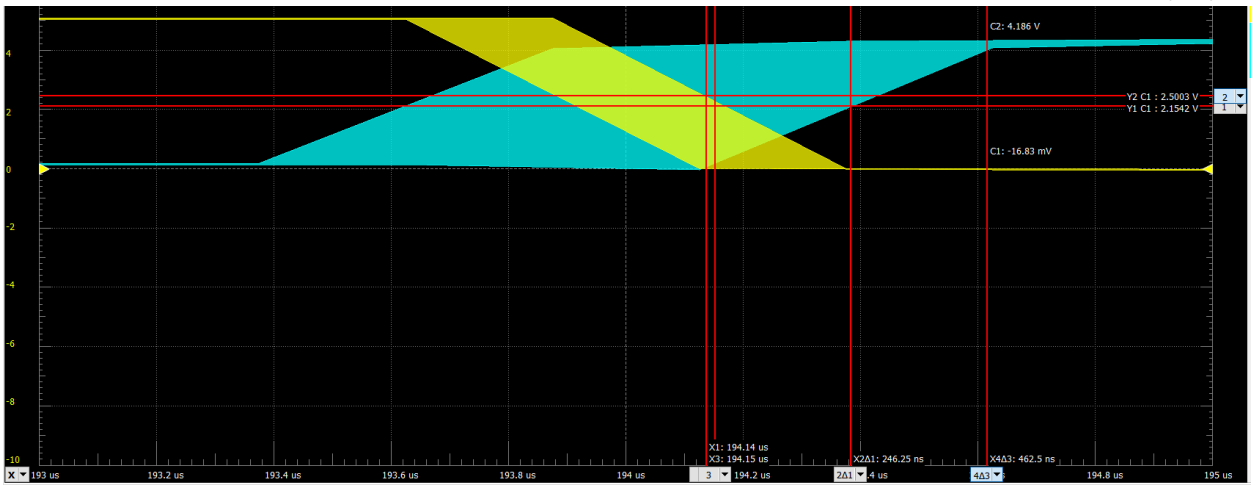
The following plot is data taken from the analog discovery kit and plotted in Excel for its extra analytical functionality. It shows a plot of output voltage against input voltage. The load resistance used for this circuit was 0 Ω, and the load capacitance was 15 pF.



When the input voltage was changed to a square wave, the input and output voltages were observed to have the following propagation characteristics in the time domain.



Mitchell Larson
CE 3101
Lab 6
4/21/18



From the following plots shown above, the key voltage and propagation delay values could be extracted. While they couldn't be extracted as their exact values, best estimations were derived from the available data.

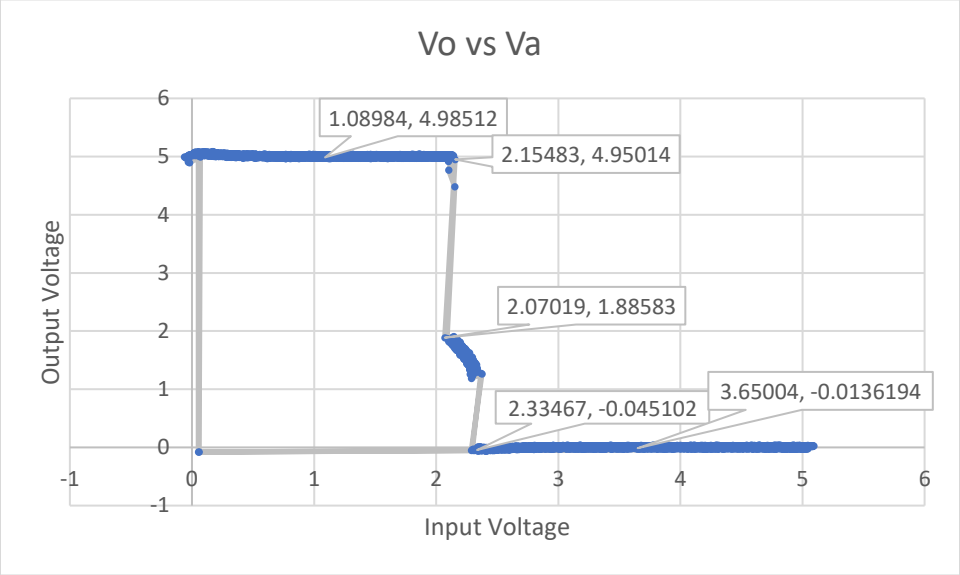
VOH:	4.28 V	VIL:	0.99 V
VIH:	1.14 V	VOL:	0.14 V
NMH:	4.28 V – 1.14 V = 3.14 V	NML:	0.99 V – 0.14 V = 0.85 V
TPHL:	244 nS	TPLH:	246 nS
Tr:	463 nS	Tf:	425 nS

The voltage-voltage plot displayed for the 74LS04 chips revealed a curve very different from the CD4096 chip. Rather than making a quick, smooth transition from output high voltage to output low voltage, it makes a very sharp and steep change. More important however, is the very small VIL and NML values. As portrayed by these values, and by visual inspection of the plot, the input range for a input producing a logic-1 output is very small; any input wishing to produce a logic-1 output would be required to be under 0.99 V, a very small number. With a VOL of 0.14V, this only leaves 0.85V for noise levels. For other inverter chips, this may be even worse, and may prevent proper functionality. Similar to the CD4096 chip, this chip has a roughly 0.7V drop between Vdd and VOH, indicating that power is consumed by the chip when producing a logic-1 output. Due to the sharp transition between output high and output low, this chip might be preferred over the CD4096 chip (or others), but its low noise margin, and with its transition occurring near 1V, it may cause developers to use a different inverter chip. The timing statistics for this chip appeared to be very similar to timing characteristics seen in the CD4096 and 74HC04 chip.

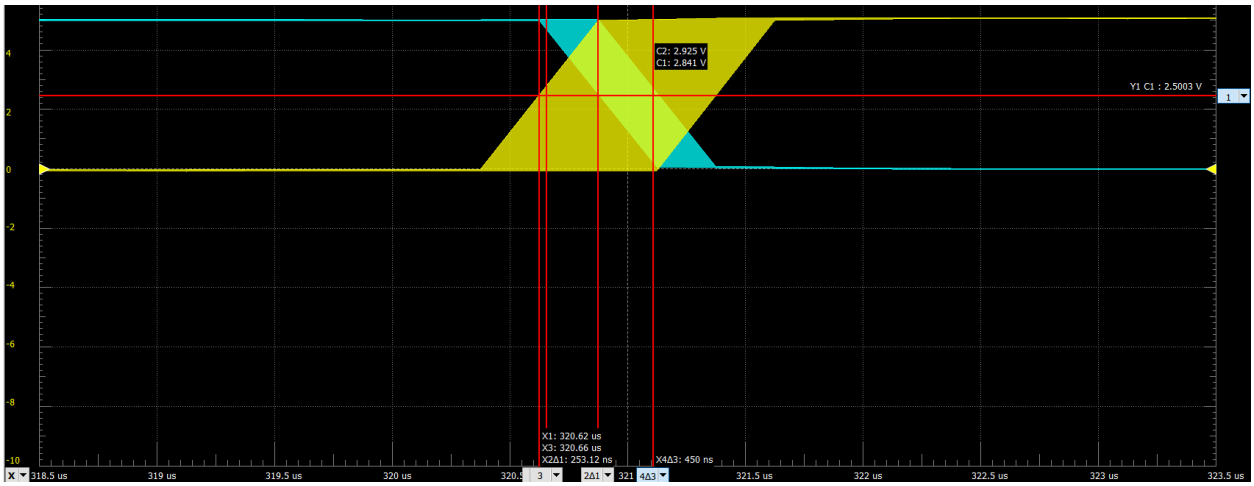
Mitchell Larson
CE 3101
Lab 6
4/21/18

74HC04

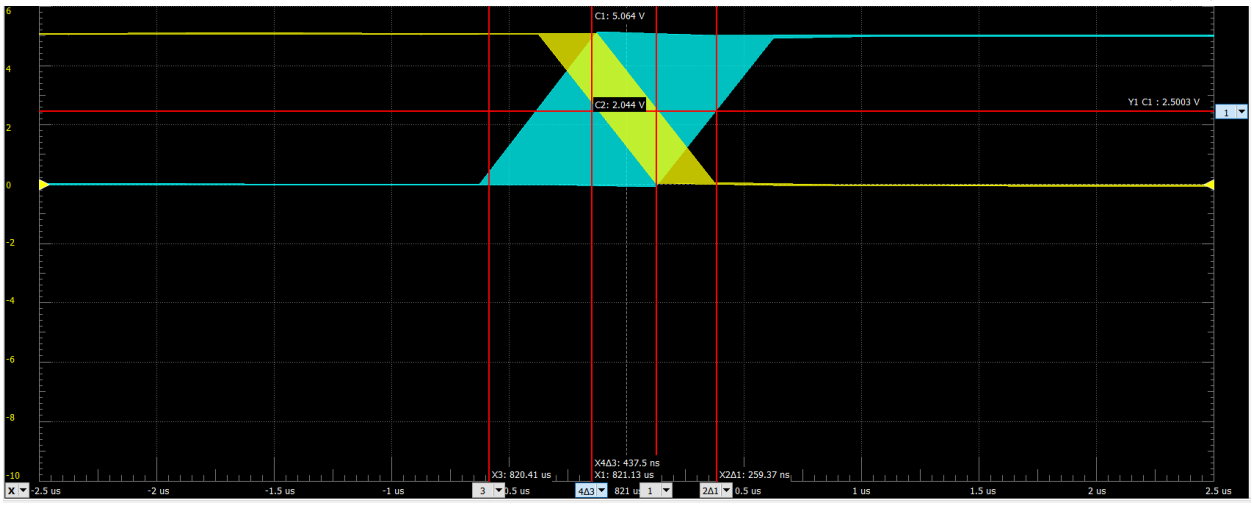
The following plot is data taken from the analog discovery kit and plotted in Excel for its extra analytical functionality. It shows a plot of output voltage against input voltage. The load resistance used for this circuit was 0 Ω, and the load capacitance was 50 pF.



When the input voltage was changed to a square wave, the input and output voltages were observed to have the following propagation characteristics in the time domain.



Mitchell Larson
CE 3101
Lab 6
4/21/18



From the following plots shown above, the key voltage and propagation delay values could be extracted. While they couldn't be extracted as their exact values, best estimations were derived from the available data.

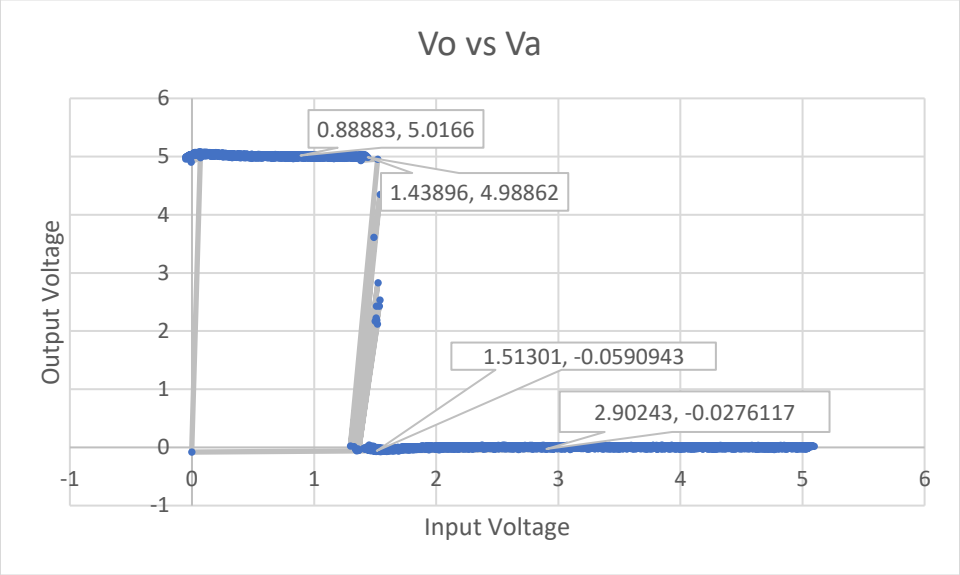
VOH:	4.99 V	VIL:	2.15 V
VIH:	2.33 V	VOL:	-0.01 V
NMH:	4.99 V – 2.15 V = 2.84 V	NML:	2.15 V - -0.01 V = 2.16V
TPHL:	253 nS	TPLH:	259 nS
Tr:	438 nS	Tf:	450 nS

Similar to the 74LS04 and 74HCT04 chips, this chip also forgoes a sharp drop from output high voltage to output low voltage. A crucial difference between this chip and those chips however, is the fact that the transition occurs very close to the 2.5 V range, which allows for very large low and high noise margins. These noise margins are made even bigger by output high and low voltages being extremely close to rail voltages Vdd and ground. The voltage-voltage plot reveals two different areas of steep transition, with a less steep transition region in-between. This seems to suggest that this chip was constructed using two different MOSFET transistors, which is further supported by the fact that output high and low voltages are very close to Vdd and ground respectively. Due to the characteristics, it would most likely be relatively easy to interface the chip with chips from different chip families. This chip appears to have the best voltage-voltage characteristics of the four inverter chips tested. The timing characteristics of this chip appear to be similar to those of the previously documented chips, but are significantly slower than the 74HCT04, which may cause developers to use that chip over this one, even though this chip has very good voltage-voltage characteristics.

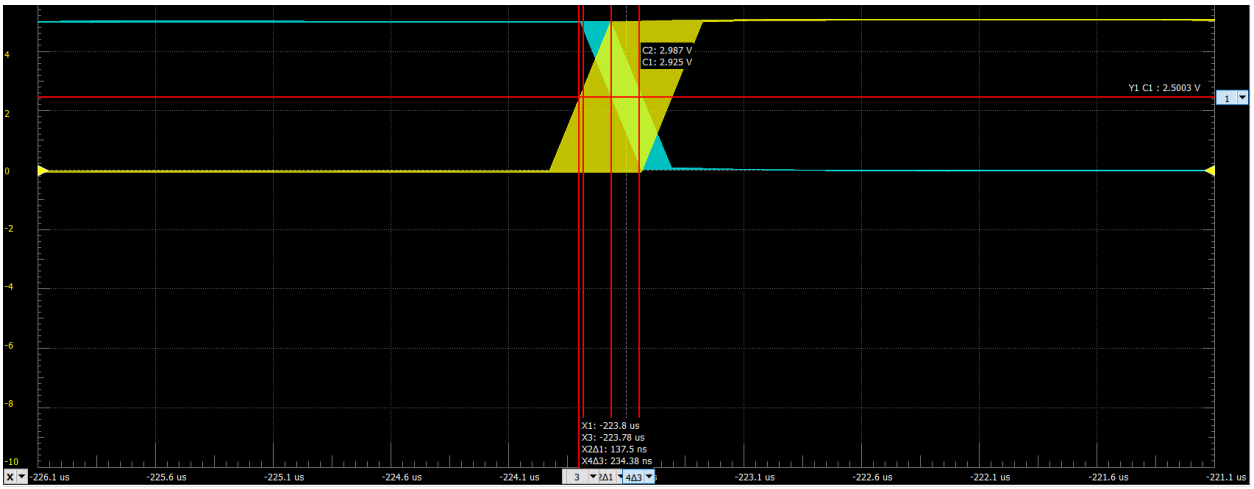
Mitchell Larson
CE 3101
Lab 6
4/21/18

74HCT04

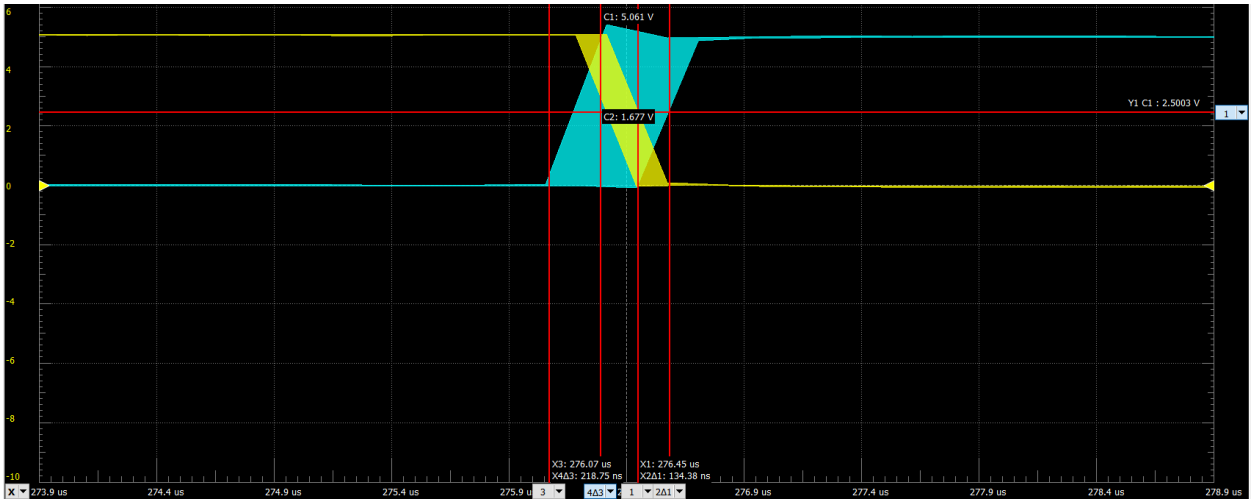
The following plot is data taken from the analog discovery kit and plotted in Excel for its extra analytical functionality. It shows a plot of output voltage against input voltage. The load resistance used for this circuit was 0 Ω, and the load capacitance was 50 pF.



When the input voltage was changed to a square wave, the input and output voltages were observed to have the following propagation characteristics in the time domain.



Mitchell Larson
CE 3101
Lab 6
4/21/18



From the following plots shown above, the key voltage and propagation delay values could be extracted. While they couldn't be extracted as their exact values, best estimations were derived from the available data.

VOH:	5.02 V	VIL:	1.44 V
VIH:	1.51 V	VOL:	-0.3 V
NMH:	5.02 V – 1.51 V = 3.51 V	NML:	1.44 V - -0.3 V = 1.74V
TPHL:	138 nS	TPLH:	134 nS
Tr:	219 nS	Tf:	234 nS

The 74HCT04 voltage-voltage characteristics yield an extremely sharp transition region from output high to output low. In fact, analog discovery had issues finding data points between output high and output low. As a result, it would be extremely unlikely for an input voltage to produce an output voltage that couldn't be interpreted as either logic-0 or logic-1 – an ideal characteristic of a logic gate. While the transition region is the most ideal of all the inverter chips tested, its noise margin low suffers due to the input voltage at which the transition occurred. This would increase the chances of an output low of a chip from falsely appearing as a logic high input. Similar to the 74HC04 chip, this chip had an output high and low voltage very similar to the rail voltages, suggesting very low power consumption of the logic gate. While this gate has less than ideal noise margins, it has by far the best timing characteristics of the chips tested. Both rise times and propagation delays were about twice as quick as the same timing characteristics observed in the CD4069, 74S04, and 74HC04 chips, which may cause developers to choose this chip over the others for applications requiring high speed circuits that can tolerate less than ideal noise margins.

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CE 3101
Lab 6
4/21/18

Conclusion

The purpose of this lab was to explore and document the characteristics of 4 different inverting integrated circuits. Through the use of an analog discovery kit, both the voltage-voltage and time characteristics of each circuit were observed, and key values were derived from the resulting data for each chip. Using this data, unique characteristics for each chip were highlighted, which may cause a developer to choose it over another similar chip. The characteristics of each chip were also used to analyze the feasibility of interfacing chips from different chip families. This laboratory experiment did an outstanding job of providing the objectives and tools for performing this analysis. The material from this lab has helped fortify content taught in lecture and has helped increase confidence in the material. Due to this, and the successful documentation of resulting chip characteristics, it was reasonable to declare this experiment as a success.