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CE 3101
Lab 5
4/15/18

CE 3101 Lab Experiment 5

Abstract

In the field of consumer digital electronics, one of the most important circuits is the invertor. The invertor, while being very simple in its design, allows the design of more complex digital logic gates, which can be formed to build the computers that we use in everyday life. The invertor is simple – it takes the digital binary value of the input, and outputs the opposite of it. This circuit behavior has been implemented in various ways, which differ in the way that they transition from logic high to logic low. Some of these designs are RTL, DTL, TTL, PMOS, and CMOS. To the user, the functionality of these logic gates appears to be the same; when looking at their behavior at the semiconductor level however, there are several distinct differences between the design, which makes some circuits than others depending on the application.

In this lab, these characteristic differences between each invertor gate was explored. Of particular interest was the difference between the designs listed above regarding their following voltage characteristics: VOL, VIL, VM, VIH, VOL, NMH, NML, logic-0 power, and logic-1 power. To do this, each of the invertors was simulated in PSPICE, and the voltage-voltage plots were observed, with key voltage levels annotated. Then simulated circuits were implemented physically, and an Analog Discovery kit was used to measure the characteristics of each invertor using the oscilloscope feature. This helped not only highlight the differences between the simulation results and the physical results, but also the differences between each logic gate.

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Experiment

RTL Invertor Circuit

Simulation

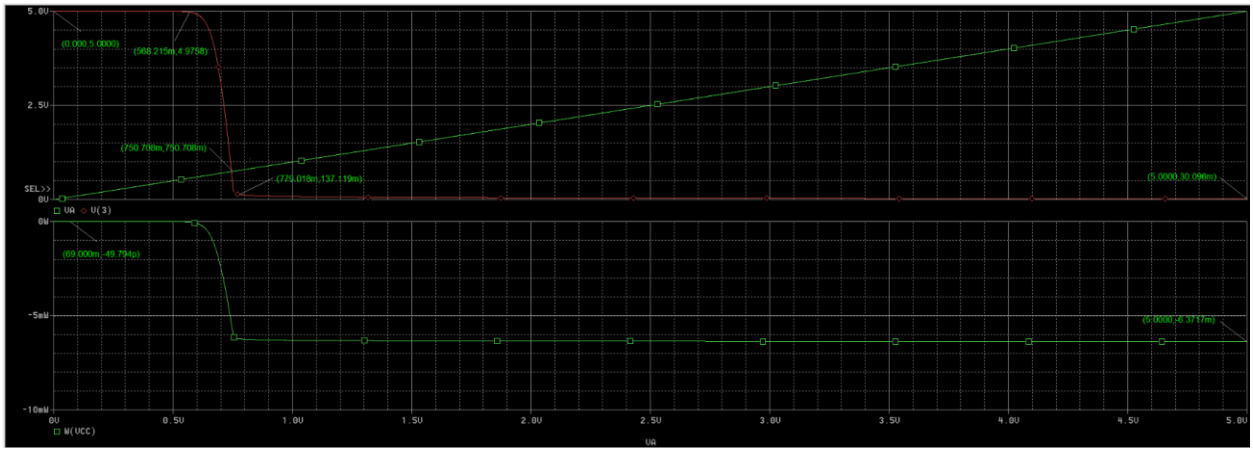

Figure 1 - Simulation Results for the RTL circuit.

VOH:	5.00 V	VIL:	568 mV	VM:	750 mV
VIH:	779 mV	VOL:	30 mV	NMH:	422 V
NML:	538 mV	Logic-0 Power:	-6.37 mW	Logic-1 Power:	0.00 W

Physical Implementation

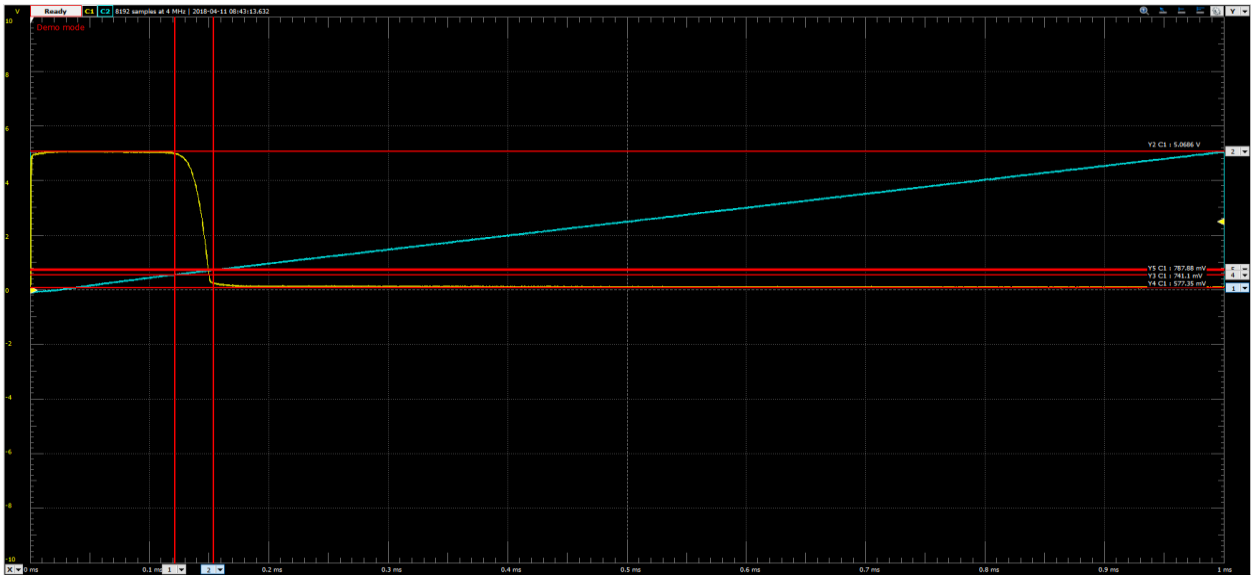

Figure 2 - Oscilloscope view of physical implementation of RTL circuit.

VOH:	5.06 V	VIL:	577 mV	VM:	741 mV
VIH:	788 mV	VOL:	30 mV	NMH:	4.27 V
NML:	547 mV				

For the RTL circuit, it's physical implementation performed very similar to its simulated behavior. VOH, VIL, VM, VIH, VOL, NMH, and NML only differed by millivolts, and this could most likely be explained by minor inefficiencies and imperfections in the actual circuitry. In this circuit, a small transition zone occurs, which makes it less likely that an input would be unreliable and produce an output between low and high. Additionally, this circuit is able to produce VOH and VOL values very close to 5V and 0V, respectively. Where this circuit lacks is its imbalance between its noise margin high and noise margin low. The perfect circuit would have NMH and NML values close to 2.5, but his circuit has a NMH value much larger than NML. This would introduce the possibility of producing a logic-0 output accidently, with a small logic-0 input. Outside of the semiconductor characteristics, this circuit lacks due to resistor size, static power, and the need for a sourced input current (due to design with a BJT).

DTL Invertor Circuit

Simulation

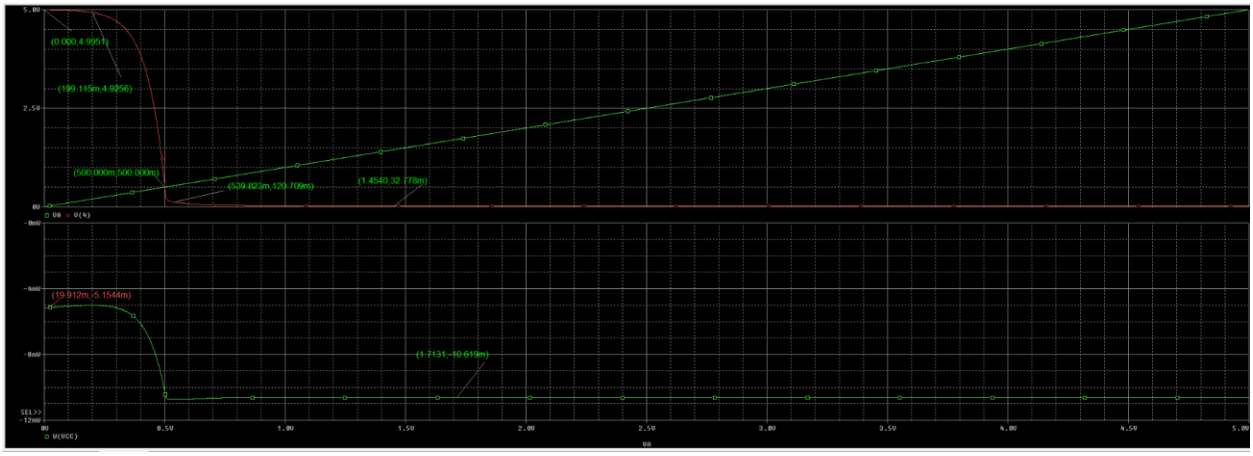

Figure 3 - Simulation results for the DTL circuit.

VOH:	4.99 V	VIL:	199 mV	VM:	500 mV
VIH:	540 mV	VOL:	33 mV	NMH:	4.45 V
NML:	166 mV	Logic-0 Power:	-10.6 mW	Logic-1 Power:	-5.1 mW

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Physical Implementation

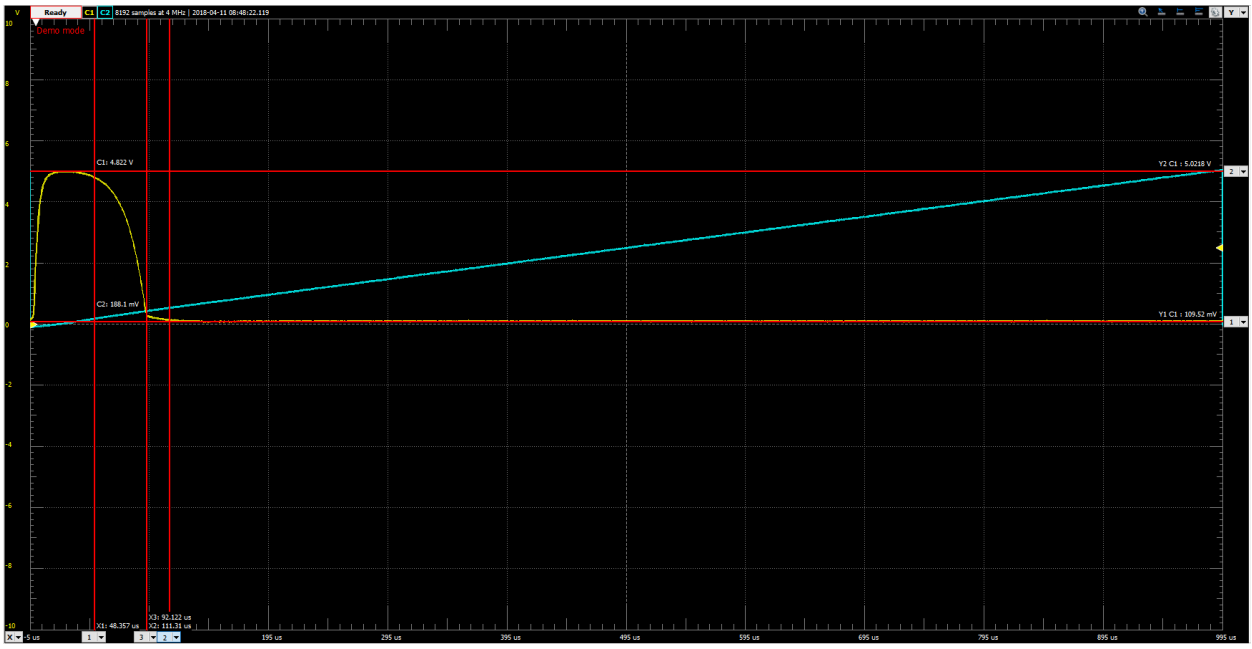

Figure 4 - Oscilloscope view of physical implementation of DTL circuit.

VOH:	5.02 V	VIL:	188 mV	VM:	390 mV
VIH:	545 mV	VOL:	110 mV	NMH:	4.48 V
NML:	78 mV				

The DTL circuit differed quite a bit when it was implemented physically when comparing it against its simulated results. The VM and VOL numbers appeared to be quite different when comparing measurements on waveforms against the simulated results. Not only this, but the shape of the oscilloscope plots appeared significantly different as well. In the simulated results, a logic 0 input corresponds to a logic-1 output. In the actual results however, the lowest logic-0 inputs actually correspond to a logic-0 output – the opposite behavior of a invertor logic gate. Similar to the RTL circuit, this circuit has a very small NML and a very large NMH, making it less than ideal. The transition zone for the DTL circuit appeared to be larger than the transition zone for a comparable RTL circuit. In summary, this circuit experiences the similar drawbacks to the RTL circuit, but with the additional drawback of incorrect behavior for very low input voltages.

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TTL Invertor Circuit

Simulation

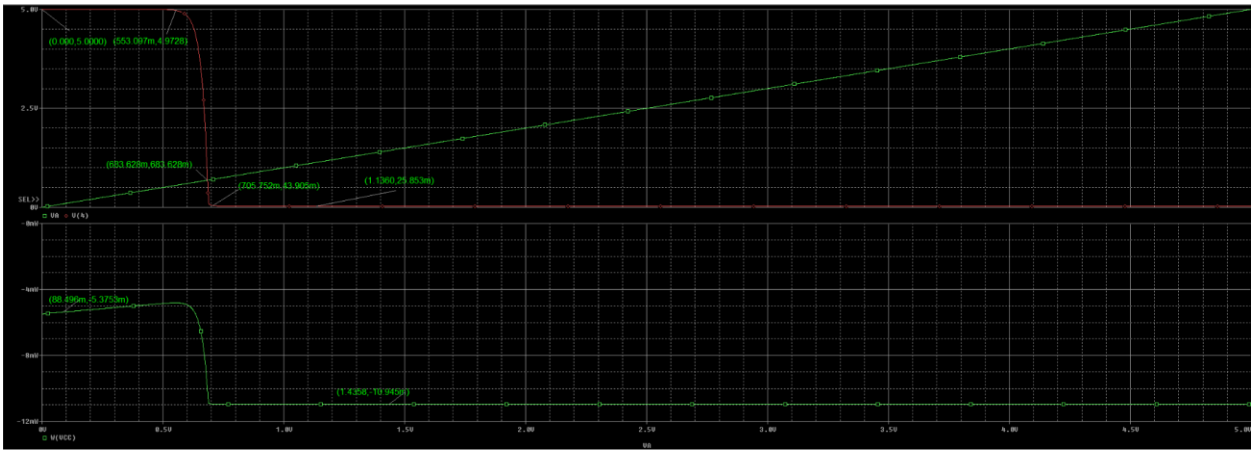

Figure 5 - Simulation results for the TTL circuit.

VOH:	5.00 V	VIL:	553 mV	VM:	684 mV
VIH:	706 mV	VOL:	25.9 mV	NMH:	4.29 V
NML:	527 mV	Logic-0 Power:	-10.9 mW	Logic-1 Power:	-5.4 mW

Physical Implementation

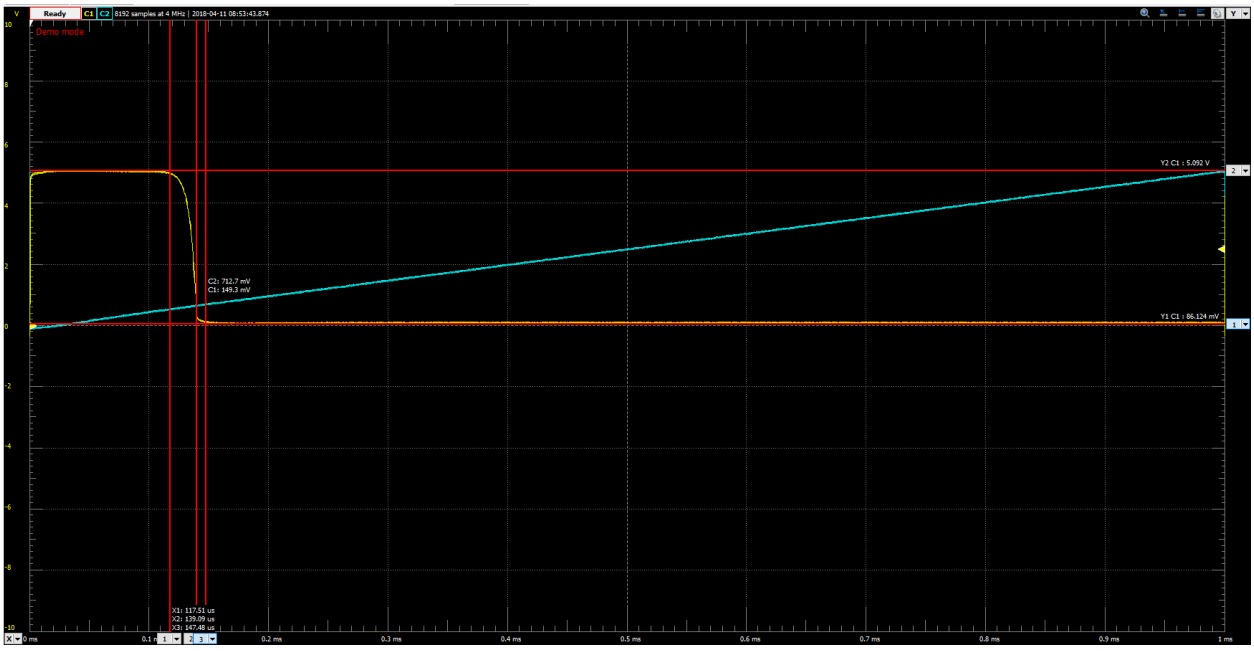

Figure 6 - Oscilloscope view of physical implementation of DTL circuit.

VOH:	5.09 V	VIL:	554 mV	VM:	670 mV
VIH:	712 mV	VOL:	86.1 mV	NMH:	4.38 V
NML:	468 mV				

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When comparing the physically implemented circuit to its simulated equivalent, the major characteristics of the circuit ended up being very similar. Values were only off by a few millivolts. The shape of the physically implemented circuit also took the appearance of the simulated circuit with very little deviance. The TTL circuit was very similar to the RTL circuit in regards to its NMH and NML values. Although they weren't equally proportioned, the proportions were much better than in comparison to the DTL circuit. The width of the transition zone was also very similar to the width of the transition zone of the RTL circuit. While this circuit was very similar to the RTL circuit, and shared many of its disadvantages, the TTL circuit was slightly worse for power consumption.

PMOS Invertor Circuit

Simulation

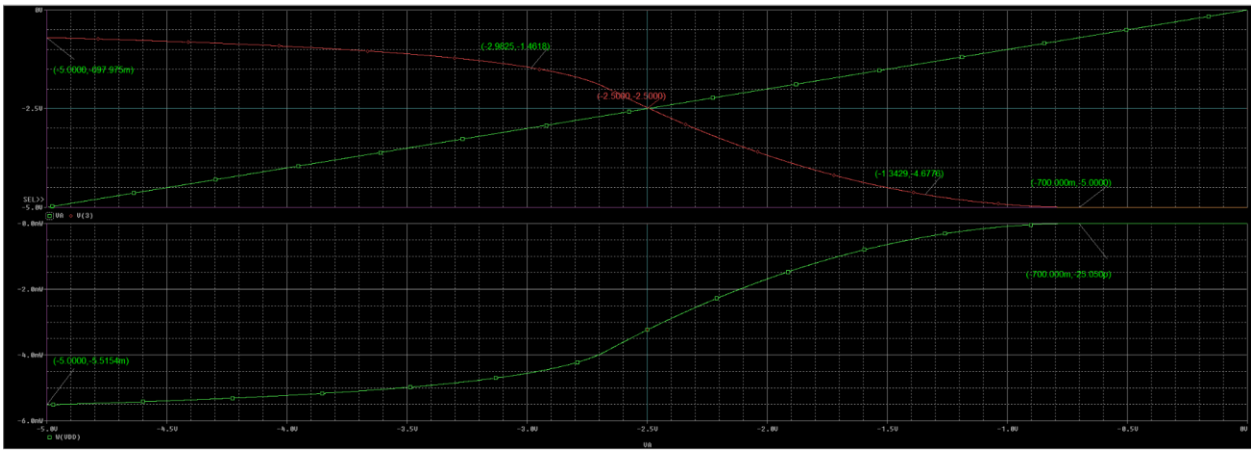

Figure 7 - Simulation results for the PMOS circuit.

VOH:	-698 mV	VIL:	-2.98 V	VM:	-2.5 V
VIH:	-1.34 V	VOL:	-5.00 V	NMH:	2.02 V
NML:	642 mV	Logic-0 Power:	-5.51 mW	Logic-1 Power:	-25 pW

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Physically Implemented

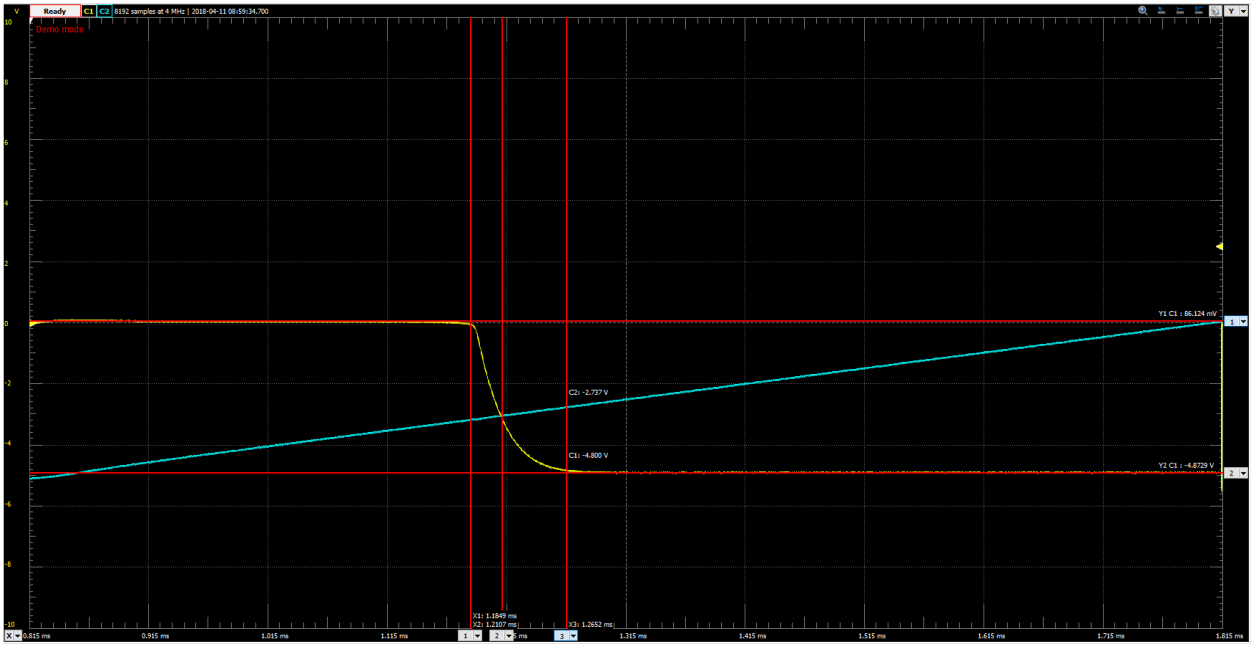

Figure 8 - Oscilloscope view of physical implementation of PMOS circuit.

VOH:	86.1 mV	VIL:	-53.0 mV	VM:	-3.0 V
VIH:	-4.8 V	VOL:	-4.87 V	NMH:	4.89 V
NML:	4.81 V				

The PMOS circuit was unique from the rest of the circuits because it worked with negative voltages; essentially, 0V was logic-1 and -5V was logic-0. This circuit appeared to differ quite differently from its simulated behavior. In it's simulation, not only were the VIL and VOL values significantly different, but the shape was different as well. In simulation, the circuit behaved with a very large transition region. This would be undesired behavior as it would allow a large range of input voltages to result in output voltages in-between logic-0 and logic-1. The physically implemented circuit showed much more desirable behavior however. In the physically implemented circuit, the transmission region was much smaller, and it occurred almost half way between logic-0 and logic-1 for the input voltage. This was a behavior that hadn't been seen in any of the other invertor circuits, giving it an advantage over the others. Additionally, this circuit proved advantageous over the others, as it did not need any input current, vastly reducing the power needed to operate the logic gate. Another advantage that this circuit had over the circuits implemented with BJTs was that the MOSFET allowed for smaller design.

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CMOS Invertor Circuit

Simulation

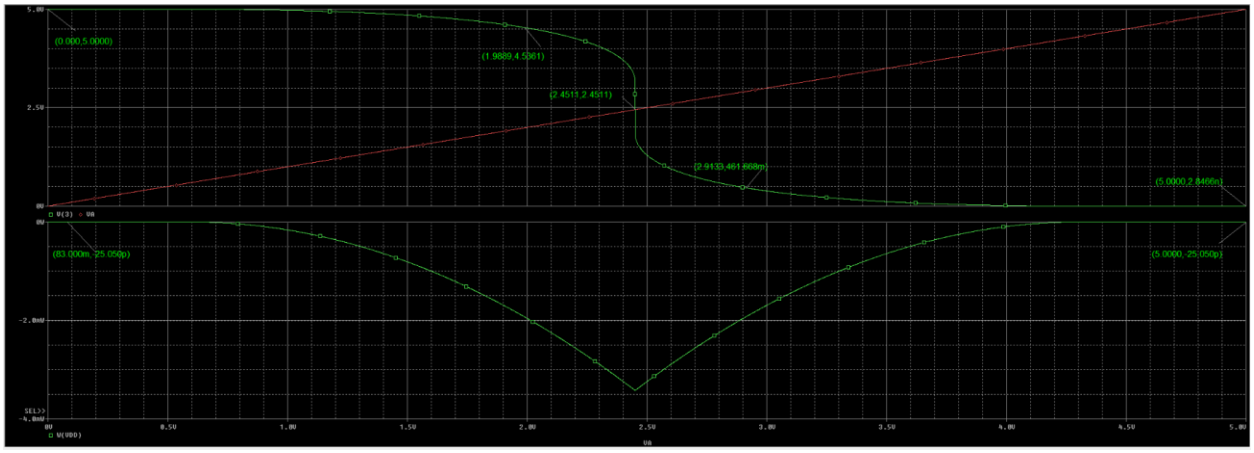

Figure 9 - Simulation results for the CMOS circuit.

VOH:	5.00 V	VIL:	1.99 V	VM:	2.45 V
VIH:	2.91 V	VOL:	2.85 nV	NMH:	2.09 V
NML:	1.99 V	Logic-0 Power:	-25 pW	Logic-1 Power:	-25 pW

Physically Implemented Circuit

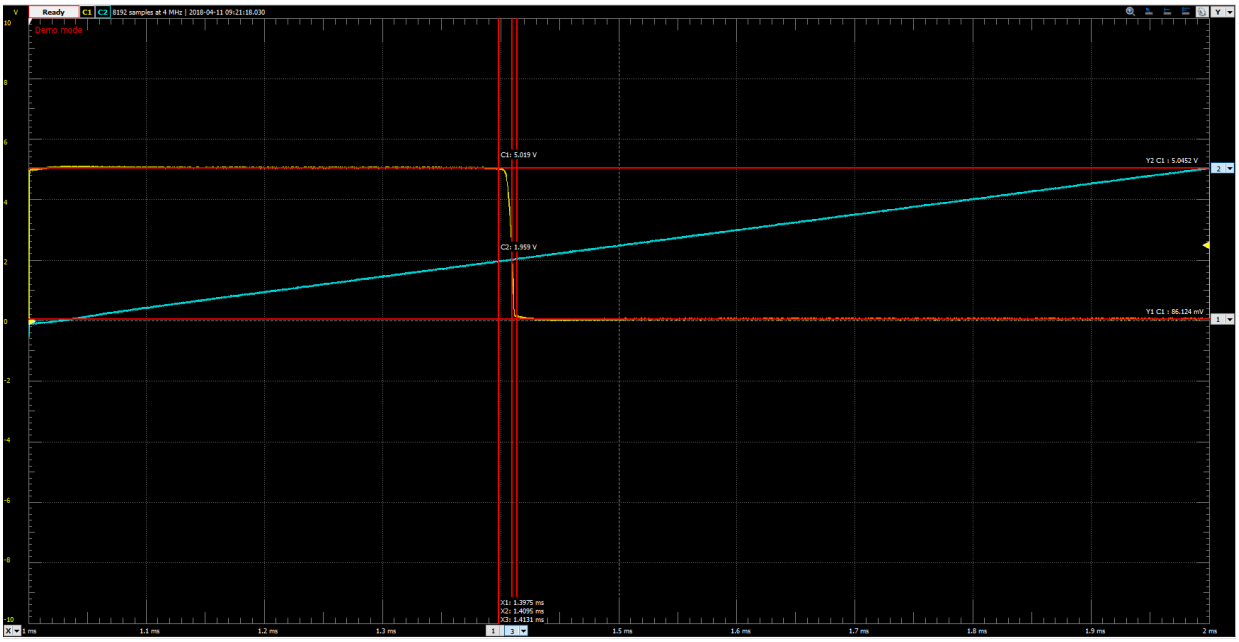

Figure 10 - Oscilloscope view of physical implementation of CMOS circuit.

VOH:	5.05 V	VIL:	1.99 V	VM:	2.03 V
VIH:	2.03 V	VOL:	86.1 mV	NMH:	3.02 V
NML:	1.90 V				

The CMOS differed quite a bit from its simulated results when comparing VM and its shape. The simulation calculated that the transition zone width between output high and output low would actually be relatively large, with a vertical line half way between the transition. The actual results differed, and had a much smaller transition zone than predicted. Additionally, the vertical line that appeared in the simulation did not appear when the circuit was physically implemented. It seemed as if the behavior of the physically implemented circuit was better than simulation, which doesn't occur often. This circuit was the best invertor logic gate build during this experiment. It not only had a very small transition zone with, but it was very close to the middle of the input voltage range, decreasing the chances that a voltage between logic-0 and logic-1 would be on the output node. This circuit also had the lowest output logic-0 voltage by a far margin, and the lowest power consumption of all the built circuits. In fact, unlike all other circuits built in this experiment, no current was drawn from any of the sources when an input logic-0 or logic-1 was provided. This circuit also didn't require any resistors, decreasing the size of the circuit.

Conclusion

This lab experiment did a great job in reinforcing material taught in class. While simulation and lecture provide a solid knowledge base for the behavior of these circuits, it can be much easier to understand and process the behavior of the circuits when they are implemented in a laboratory setting where values can be tweaked, and results can be seen in real time. By completing this experiment, I feel much more confident in my abilities to understand and build circuits both implementing the inverting behavior seen in these circuits, as well as use them in circuits. This laboratory experiment made it simple to compare several different types of inverting circuits and provided an advantage over learning the subject solely through lecture. Due to that, this experiment can be concluded with high confidence to be a success.