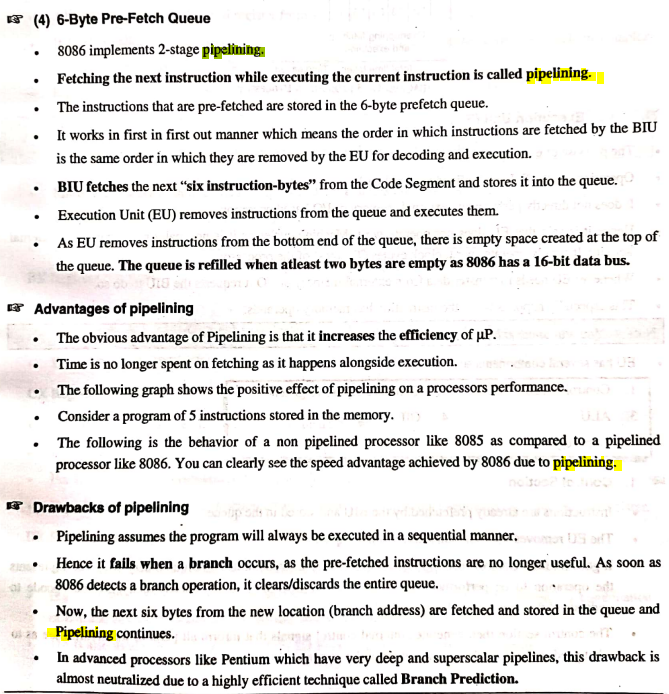
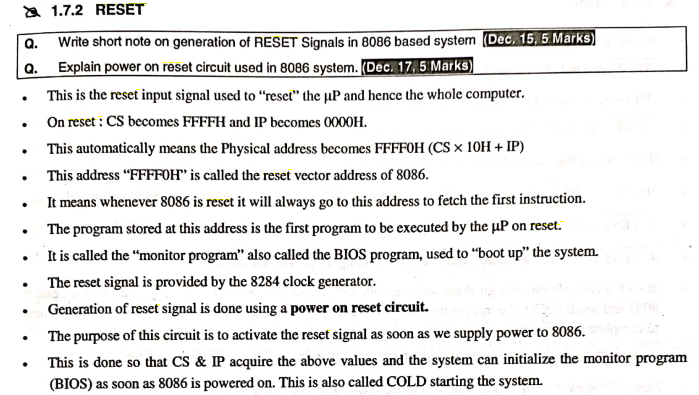
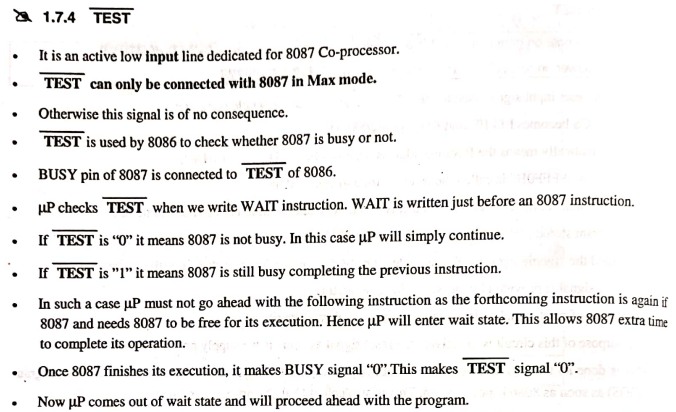
|  |
| --- |
| 8086 minimum mode   * 8086 works in Minimum Mode, when MN/ ¯MX = 1. * Minimum Mode, 8086 is the only processor in the system. The Minimum Mode circuit of 8086 is as shown below: * Clock is provided by the 8284 clock generator, it provides CLK, RESET and READY input to 8086. * Address from the address bus is latched into 8282 8-bit latch. Three such latches are needed, as address bus is 20-bit. The ALE of 8086 is connected to STB of the latch. The ALE for this latch is given by 8086 itself. * The data bus is driven through 8286 8-bit trans-receiver. Two such trans-receivers are needed, as the data bus is 16-bit. The trans-receivers are enabled through the DEN signal, while the direction of data is controlled by the DT/ ¯R signal. ¯DEN is connected to ¯OE and DT/ ¯R is connected to T. Both ¯DEN and DT/ ¯R are given by 8086 itself.   enter image description here   * Control signals for all operations are generated by decoding M/¯IO , ¯RD and ¯WR signals.   enter image description here   * M/¯IO , ¯RD and ¯WR are decoded by a 3:8 decoder like IC 74138. Bus Request (DMA) is done using the HOLD and HLDA signals. * ¯INTA is given by 8086, in response to an interrupt on INTR line. |

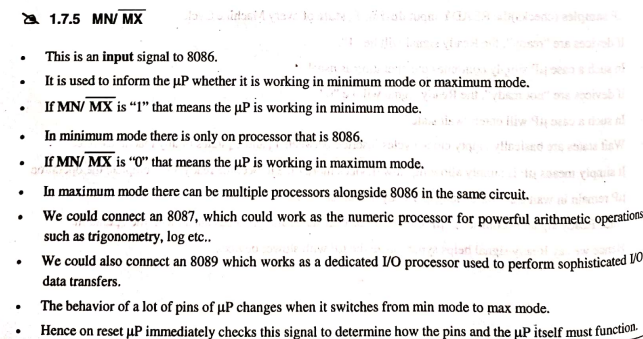
|  |
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| Maximum mode 8086 |

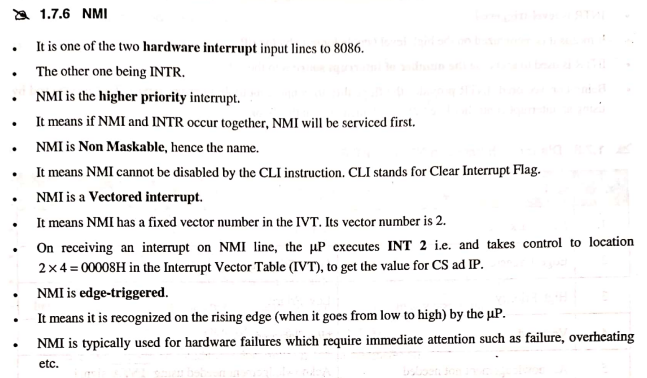
Instruction Set  
<https://www.ques10.com/p/41337/classify-and-explain-8086-instruction-set-1/>

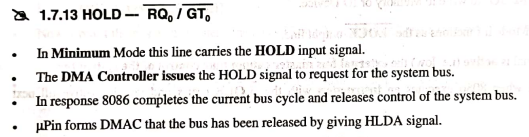
PipeLining

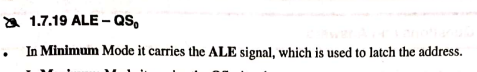
Reset  


Pins:  


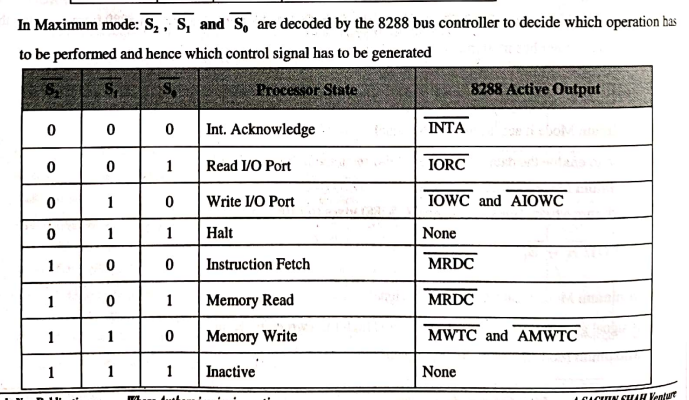


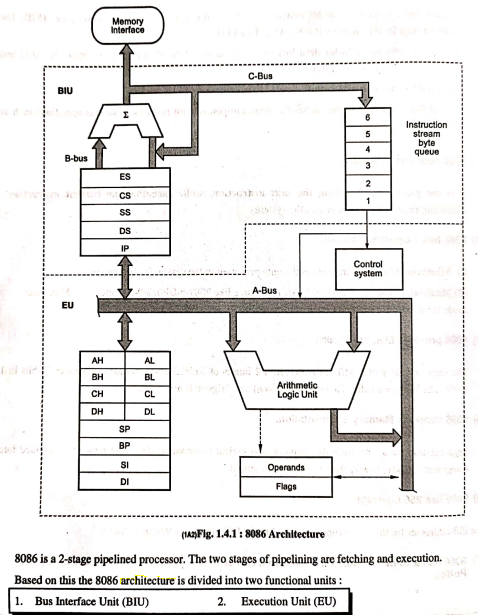


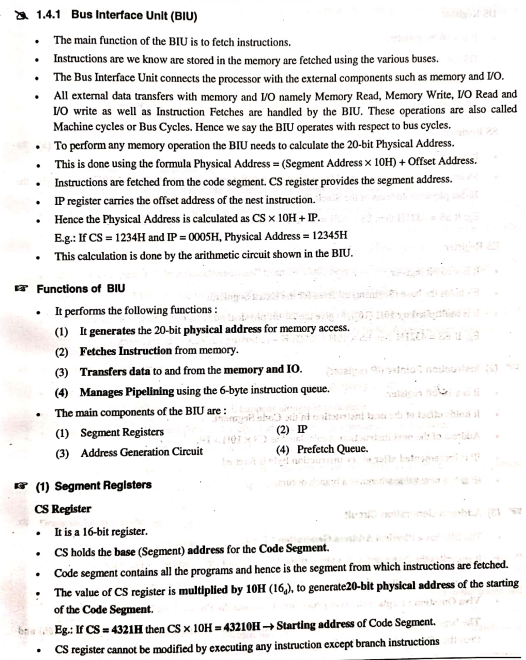
HLDA:  


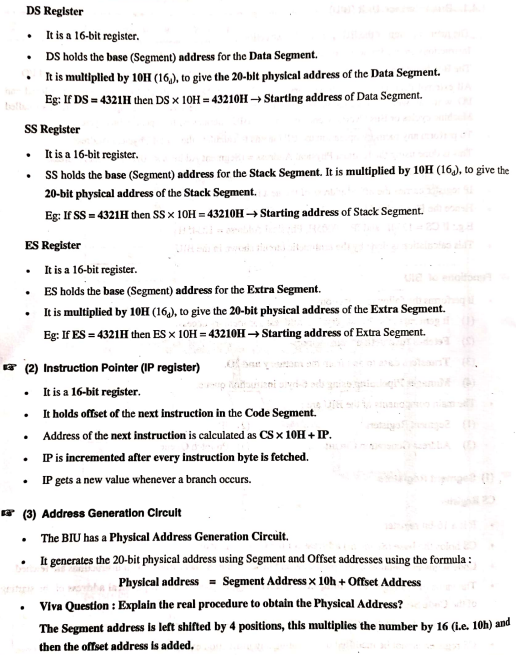
ALE  


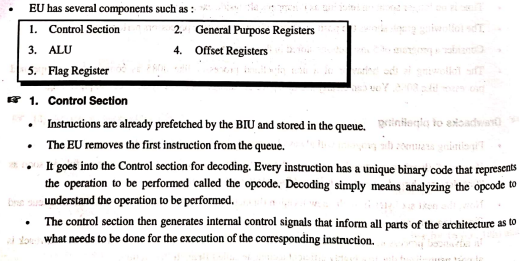
S0,s1,s2

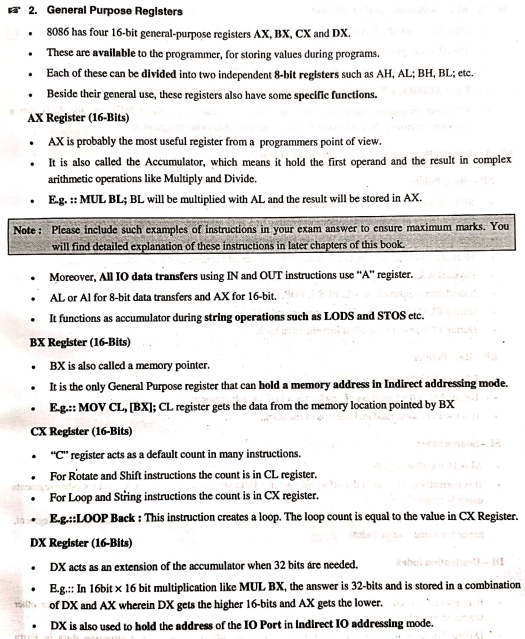


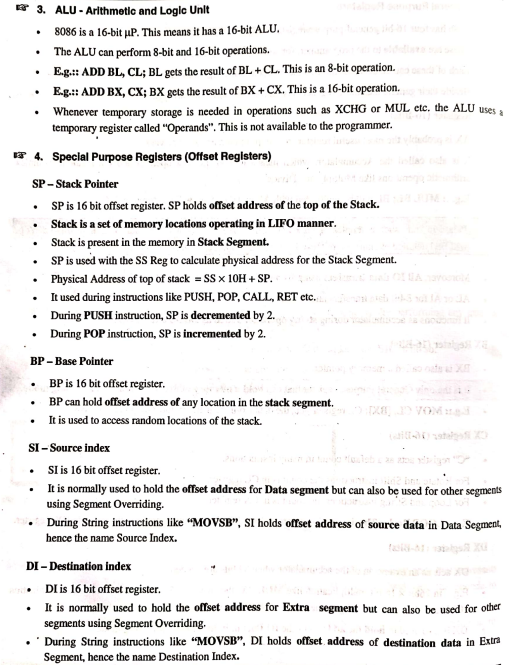












Memory Banking  
