LC-3 Instruction Set Reference

Little Computer 3 — 16-bit, 4-bit opcode, 8 general-purpose registers (R0–R7)

Notation: **DR** = Destination Register · **SR/SR1/SR2** = Source Register · **BaseR** = Base Register · **Imm5** = 5-bit sign-extended immediate · **PCoffset9/11** = PC-relative offset · **offset6** = 6-bit sign-extended offset · **trapvect8** = 8-bit trap vector · **CC** = condition codes {n, z, p}

Mnemonic	Opcode	Format (bits 15–0)	Operands	Description
▸ ARITHMETIC & LOGIC				
ADD	0001	0001|DR|SR1|0|00|SR2	DR, SR1, SR2	DR ← SR1 + SR2. Sets condition codes.
ADD	0001	0001|DR|SR1|1|Imm5	DR, SR1, #imm5	DR ← SR1 + SEXT(imm5). Sets condition codes.
AND	0101	0101|DR|SR1|0|00|SR2	DR, SR1, SR2	DR ← SR1 AND SR2. Sets condition codes.
AND	0101	0101|DR|SR1|1|Imm5	DR, SR1, #imm5	DR ← SR1 AND SEXT(imm5). Sets condition codes.
NOT	1001	1001|DR|SR|111111	DR, SR	DR ← bitwise NOT of SR. Sets condition codes.
▸ MEMORY ACCESS				
LD	0010	0010|DR|PCoffset9	DR, LABEL	DR ← Mem[PC + SEXT(offset9)]. PC-relative load. Sets CC.
LDI	1010	1010|DR|PCoffset9	DR, LABEL	DR ← Mem[Mem[PC + SEXT(offset9)]]. Indirect load. Sets CC.
LDR	0110	0110|DR|BaseR|offset6	DR, BaseR, #offset6	DR ← Mem[BaseR + SEXT(offset6)]. Base+offset load. Sets CC.
LEA	1110	1110|DR|PCoffset9	DR, LABEL	DR ← PC + SEXT(offset9). Load effective address. Sets CC.
ST	0011	0011|SR|PCoffset9	SR, LABEL	Mem[PC + SEXT(offset9)] ← SR. PC-relative store.
STI	1011	1011|SR|PCoffset9	SR, LABEL	Mem[Mem[PC + SEXT(offset9)]] ← SR. Indirect store.
STR	0111	0111|SR|BaseR|offset6	SR, BaseR, #offset6	Mem[BaseR + SEXT(offset6)] ← SR. Base+offset store.
▸ CONTROL FLOW				
BR	0000	0000|n|z|p|PCoffset9	[n][z][p], LABEL	If any specified CC is set: PC ← PC + SEXT(offset9). BRnzp = unconditional branch.
JMP	1100	1100|000|BaseR|000000	BaseR	PC ← BaseR. Unconditional jump to address in register.
RET	1100	1100|000|111|000000	(none)	PC ← R7. Return from subroutine (JMP R7 alias).
JSR	0100	0100|1|PCoffset11	LABEL	R7 ← PC; PC ← PC + SEXT(offset11). Jump to subroutine (PC-relative).
JSRR	0100	0100|0|00|BaseR|000000	BaseR	R7 ← PC; PC ← BaseR. Jump to subroutine (register).

▸ TRAP / SYSTEM				
TRAP	1111	1111|0000|trapvect8	trapvect8	R7 ← PC; PC ← Mem[ZEXT(trapvect8)]. OS service call via trap vector table.
RTI	1000	1000|000000000000	(none)	Return from interrupt. Restores PC and PSR from supervisor stack. (Privileged)
reserved	1101	1101|————————	—	Opcode 1101 is reserved (unused in base LC-3).

Common TRAP Vectors (OS service routines)

Vector	Alias	Function
x20	GETC	Read one char from keyboard into R0 (no echo).
x21	OUT	Write char in R0 to console.
x22	PUTS	Write null-terminated string starting at Mem[R0] to console.
x23	IN	Print prompt, read one char from keyboard into R0 (with echo).
x24	PUTSP	Write packed string (two chars per word) starting at Mem[R0].
x25	HALT	Halt execution and print message to console.