Summary of TTK4155

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An **embedded system** is an electronic system, consisting of one or more microcontroller which interface with various devices. The system may be part of (*embedded into*) a larger electromechanical system. It is generally designed to perform one specific task, often operating in real time.

Embedded systems are often designed for low power consumption, ruggedness, small size and low per-unit cost.

1 Linear voltage regulators

Basic linear regulator Supplies constant voltage with a voltage controlled current source. May need output capacitor to ensure stability. Will have transient error. The pass device is usually made in one of three ways:

NPN Darlington Uses Typically gives a voltage drop of 1.5–2.2 V (worst of all types). However, the ground pin current is the lowest (best) of all types. Can supply more current than other types.

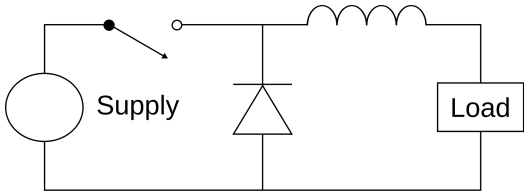
Low-dropout (LDO) Voltage drop typically 0.6 V. Best voltage drop, worst ground pin current.

Quasi-LDO Somewhere in-between.

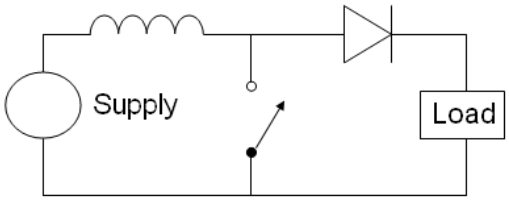
Considerations Max. load current, input voltage source (battery or AC), output voltage tolerance, idle current.

2 Switching voltage regulators

Buck converter Down-converts DC. PWM-controls a switch between V_{in} and an inductor-capacitor-path. **On:** Inductor current to load and capacitor. Capacitor charges. **Off:** Inductor current to load and back through diode. Capacitor discharges. Cannot completely avoid current ripple. 20–30 % typical.



Boost converter Up-converts DC. **On:** Inductor shorted to ground, current increases. Load needs capacitor for power. **Off:** Inductor current must flow through capacitor/load, voltage increases.



Buck-boost Gives a DC output of reverse polarity, and either increased or decreased magnitude. **On:** Capacitor supplies current. **Off:** Inductor supplies current.

Flyback regulator Can give several outputs, some of which can be of opposite polarity. It uses transformers with a PWM voltage on the input side, and separate windings for each output.

3 CPU

RISC Reduced instruction set computing. Low number of instruction types. Quick one-cycle execution and pipelining.

Pipelining Instruction execution partitioned into fixed sequential steps. While one instruction moves to step 2, the next instruction may begin at step 1, i.e. parallell processing.

3.1 Memory architecture

Von Neumann uses the same memory for data and instructions, and cannot fetch both at the same time.

Harvard uses separate memories with separate buses. Can fetch both at the same time. (Used by ATmega162.)

Hybrid caches both, but accesses a shared memory in case of cache miss.

3.2 Memory management

MMU is a unit that decodes logical addresses to physical addresses. Must be used for anything except direct-addressed memory (i.e. physical = logical).

Physical memory > logical memory Divide physical memory into partitions (banks) that are each equal to or less than the logical address space.

Physical memory < logical memory Exploit the entire logical address space by paging: Load data from secondary storage to physical memory.

4 Buses

4.1 Synchronous vs. asynchronous buses

A synchronous bus has a clock signal sent alongside the data (separate wire). An asynchronous bus does not use a separate clock signal. Instead, the receiver and transmitter must operate at an agreed upon speed, and synchronisation information is sent over the data line(s) periodically to sync their clocks.

4.2 VMEbus

32 bit, multi-master, high data transfer rate. Data and address lines can be multiplexed. 7 control lines are used. Runs through a backplane with 1–21 slots for expansion cards. Backplane has a bus controller and some other stuff.

4.3 PC/104

An old-ass standard for PC-compatible boards intended for embedded use. The rationale being that using PC hardware and software could greatly decrease R&D

requirements. Units are stackable (like Arduino shields) and smaller than typical PC hardware.

4.4 I^2C

Two bus lines SDA (data) and SCL (clock), multi-master, 8 bit addressing. Both lines are pulled up.

4.5 1-Wire

Only one wire + ground. Supplies data and power (slaves have a half-wave rectifier and a 800 pF capacitor). Bus is always at V_{cc} when idle, to supply power. Bits are sent as follows:

- Logic one: Pull bus low for less than 15 µs.
- Logic zero: Low for more than 60 µs.
- Bus reset: Low for more than 480 µs.

64 bit serial number fixed to each slave. 48 bits for device address $\rightarrow 2^{48} \approx 10^{14}$ addresses $\rightarrow$ no address collisions. (Also 8 bits to tell the type of the device and 8 bit CRC.)

No slave may speak unless requested by the master. No slave–slave communication except through the master.

Communication is initiated by the master resetting the network. Slaves respond with a presence pulse. Master may access any slave through unique addresses.

4.6 USB

Topology Tiered star, i.e. hubs rather than daisy chain. Many devices have built-in hubs. Max. 127 devices per bus.

Bandwidth USB 3.0: SuperSpeed – 5 Gbps. USB 2.0: High speed – 480 Mbps. USB 1.1: Full speed – 12 Mbps and low speed – 1.5 Mbps.

Transfer modes There are four transfer modes.

Control Used for command and status operations. Bursty. 8 bit for low speed, 64 bit for full speed, inbetween for high-speed.

Interrupt Guaranteed latency transfer, used for HIDs and such. Small amounts of data.

Bulk Used for large data amounts. Error detection and correction, guarantee of delivery. Generally fast, but no bandwidth guarantee.

Isochronous Guaranteed bandwidth, used for streams and such. Bounded latency. Fault detection, but no retransmission.

Connectors V_{bus}, GND, $D+$, $D-$.

4.7 U(S)ART

Universal (Synchronous/)Asynchronous Receiver/Transmitter. A serial communications interface. Sends and receives bits, does not define any protocol. Has, at minimum, TX and RX lines.

4.8 RS-232

Defined in 1969, but still useful and common in embedded systems. Defines signals between two devices: Signal names, purpose, voltage levels, connectors and pinouts. Does not define what is sent on the lines. Commonly 1 start bit, 7–9 data bits, 0–1 parity bits, 1–2 stop bits. Only one sender and one receiver per line (usually uses one transmit and one receive line). Is single ended: One line carries signal, one line is common.

4.9 RS-422

Faster and more robust than RS-232. Two wires per signal (differential signal). Can connect one transmitter to a bus of up to 10 receivers (almost multidrop).

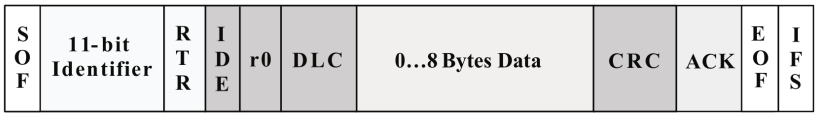
"Quasi" multidrop networks can be used: 4 wires, half duplex. Master addresses a node and receives a reply.

4.10 RS-485

Up to 32 devices on a data line. Any slave can communicate with any other slave without going via a master. True multi-point network on a single (2 wire) bus. Has clever methods to avoid data collision. Can use more devices if impedance is limited.

4.11 Controller Area Network

Two inverse wires, CANL and CANH.



4.11.1 Error detection

If an error is detected, an error frame is sent. The sender must re-send until the message is sent succesfully. If a node is faulty, e.g. it repeats an error many times, it is deactivated. There are five error tests:

- Cyclic redundancy check sent as part of every frame.
- ACK bits.
- Form check (check that all bits that must be zero are indeed zero).
- Each bit it read back by sender and checked.
- Bit stuffing.

4.11.2 Frame types

- Data frame —
- Remote frame —
- Error frame —
- Overload frame —

5 ADC/DAC

5.1 Flash ADC

With n bit resolution, divides V_{ref} into 2^n levels (series resistors), compares each level to V_{in} with comparators, and calculates the digital value through some logic. Extremely fast, quite expensive to make.

5.2 Successive approximation ADC

Compare V_{DAC} to V_{in}. Binary searches through quantisation levels until convergence. (Digital value is run through a DAC for the comparison.)

5.3 Dual slope ADC

Integrate V_{in} for a fixed time. Measure time before integrated value reaches zero again when $-V_{\text{ref}}$ is connected to input instead of V_{in}. Doesn't need a sample-and-hold.

5.4 Types of error

Static error Any error found when V_{in} is DC.

Quantisation error ±1/2 LSB for all ADC types.

Offset error A nonzero input might give a zero output.

Gain error The slope of the gain might be slightly off, giving error proportional to voltage.

Differential non-linearity error Voltage range for each quantisation level might not be of same size for all levels.

Integral non-linearity error Transition between levels can happen at voltages somewhat offset from the correct voltage.

6 Wait states

CPU probably faster than peripherals. Injects extra clock cycles into the bus cycle. Makes sure peripherals are read correctly before the next clock cycle.

7 Memory management

Security Stop access attempts to reserved memory regions and to memory spaces of other threads (if multithreading).