Reconfigurable Complementary Metal-Oxide-Semiconductor Technology based on Silicon-on-Insulator

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***Abstract*—Reconfigurable field effect transistors are multi-mode device which switch between NMOS and PMOS by a control Gate. To investigate the functionality of RFETs. A Reconfigurable metal-Oxide-Semiconductor device is fabricated based on a SOI sample with a top-down approach. The transfer and output characteristic is measured and discussed. The results proves that the RFETs is able to overcome the drawback of doping in conventioanl MOSFET device and ambipolar behavior in SBFETs.**

***Index Terms*—reconfigurable field effect transistor,silicon on isulator, silicidation, lift-off, image reversal process, doping free devices**

I. Introduction

Metal oxide Semiconductor Field effective Transsistor(MOSFET) plays an unignorable role in various fields of application. The performance of such a device increase drastically by scalling it down [1], however, in recent years, conventional scalling method has faced its limitation [2], one of the reason is that conventional MOSET structure needs a doped n or p contact at both source and drain side. In deep nanoscale, build n-/p-region simply by doping is challenged by several issues. The solubility of dopants as well as the increased ionization energy leads to a high parasitic resistance in deep nanoscale device [3]. Furthermore, due to the statistical nature of the doping process, device fabricated by utilizing the conventional doping method always shows an highly variability in its threshold voltage V_{th}, which could lead to unpredictable error in higher level functionality.

In recent years, Reconfigurable Field effective transistor is attracting increasing attention which is considered as a method to solve those issues. Different from the conventional MOSFET which has only one gate contact, at least two gates are applied on the RFETs [4], namely the "program gate" and the "control gate"' [5]. The functionality of control gate is similar with the conventional FET while the design of the "program gate" is the main feature of RFETs. By apply bias voltage with different polarity on the program gate, both conduct band and valence band are moving up /downwards, with the help of the Schottky contact, a virtual p-/n- region on the source and drain side is then formed. With such a structure. The RFETs realize the same function as the conventional FETs without doping. And the issues caused by high parasitic resistance as well as variability between different devices are avoid.

In this paper, We will discuss the working principle of the RFET at first. To realize and verify the features of RFETs, we also fabricated several RFETs with different structure on a sample, The fabrication process of this sample will be given detailed in the followed section. After this, the transfer characteristic as well as the SEM picture is presented and at the end of this paper, a conclusion and some possible challenge related to our work is given.

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II. Operational Principles of Reconfigurable FETs

As mentioned in section I, The RFET is programmed electrically in n- or p- configuration depending on the voltage applied on the program gate. The control gate's function is similar with the gate electrode in conventional MOSFET. To illustrate the working principle of the RFET. The carrier injection mechanism with different band structure for p-type configuration is introduced. The n-type configuration is basically the same as P-type but with a different bias polarity. For P-type configuration, a negative biased voltade is applied on the program gate contact and raises the conduction band at the drain contact. As a result, An energy well is thus formed and the Thermionic emission of the electron from drain into the channel is blocked. If a negative bias is applied on the control gate. The band will bend upwards and as the consequence, the Schottky barrier for hole injection is reduced and the requirement for both quantum mechanical tunneling and thermal assisted tunneling is full filled. thus the device is turned on in p-type configuration. On the other hand. If control gate bias is increased, i.e to the flat band voltage. The thicken barrier will block the tunneling effect. And with a further increasing control gate voltage, thermionic emission into the valence band is shutting down as well. and the off-state operation mode is achieved. This is indeed how a conventional PFET works.

III. Device Fabrication

Reconfigurable FET is fabricated base on a silicon on insulator(SOI) wafer with a top-down approach. During the fabrication process different etching, lithography and deposition method was applied. We first introduce the determination of the etching rate and relation between the oxide layer thickness and the reaction time. Then the consequences and

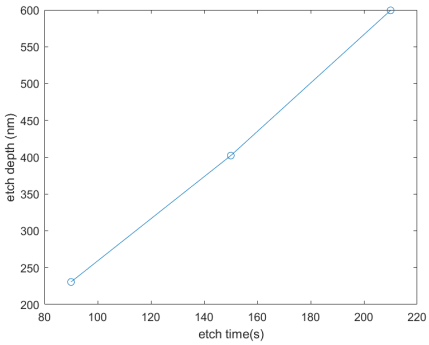


Fig. 1: etch depth in nm as a function of etching time

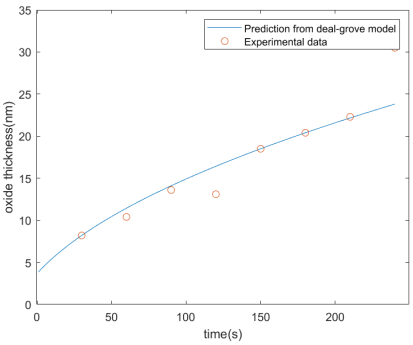


Fig. 2: Oxide layer thickness in nm as a function of reaction time in sec, the solid blue line depict the expected value from the Deal-Grove model(A = 7.66, B = 2.95 τ = 14.07) and the orange dot indicates the measured value.

the detail of different process will be introduced in the rest part of this section.

To determine the etching rate, three different dummy sample is placed in the inductively coupled plasma reactive ion etching tool. Except the etching time, all samples are etched with a same environment setting, the etch depth is measured and their relation with the each time is shown in figure 1. The etch depth is proportional to the etch time, hence the each rate can be obtained by calculating the ratio between time and depth.

The Gate-oxide is grown by a Rapid thermal oxidation(RTO) process, The oxidation reaction is considered to be taken place at the interface between the silicon and the oxide layer, which means that the oxygen atoms have to diffuse through the oxide layer to complete the reaction. As a result, the growth rate is reducing during the entire RTO process. To predict the reaction time for a certain oxide layer thickness. Deal-Grove model is used to determine the relation between thickness and time. The details of Deal-Grove model is shown in following equation:

$$d_{ox}(t) = \frac{A}{2}(\sqrt{1 + \frac{4B}{A^2}(t+\tau)} - 1) \quad (1)$$

A, B is constant that can be later extract from the experiment data (see figure 2), d_{ox} represents the oxide layer thickness, τ indicate the native oxide layer thickness.

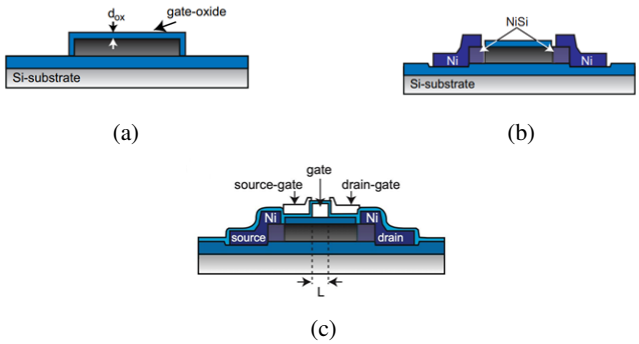
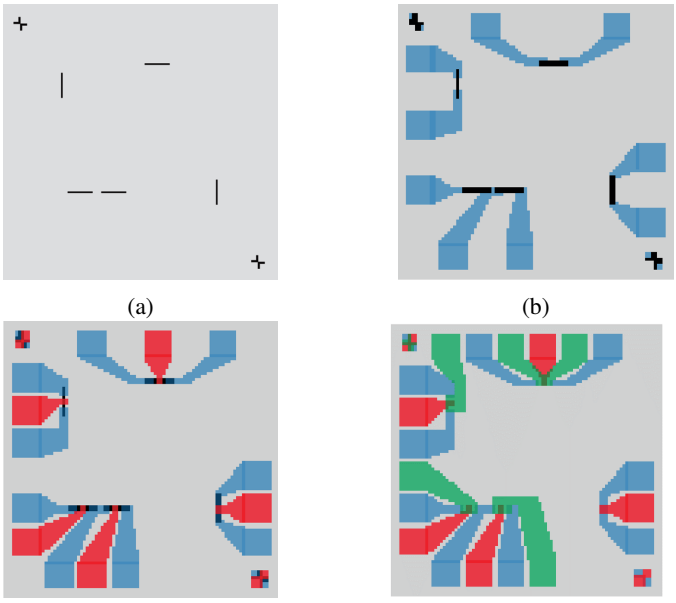


Fig. 3: Cross section View of the fabricated RFET device after (a) gate oxide layer formation (b): NiSi formation (c): fabrication finished

The first step of the fabrication procedure is partial removal of the SOI layer that left only the silicon for channel and source drain contact. To do so, The SOI wafer is spin coated by HDMS and photon resist. Then a positive exposure with 405nm wavelength is apply on the sample. The exposed resistance is removed by AZ726 MIF developer and the silicon layer underneath the removed resist is then etched away by a Reactive Ion Etching (RIE) process. Before the formation of the gate oxide layer, the oxide, organic as well as metallic contamination is removed by the RCA clean procedure. Figure 3a shows the sample layout after the gate-oxide formation. The next step is to build the Nisi region which is necessary for the formation of virtual p and n doped region. Again, the photon resist is coated on the sample. After a soft bake for 90 sec an exposure with 405 nm wavelengths is done. Different from the former lithography, an image reverse process is done for this step. Once again, the resist above the source and drain contact is removed by AZ726 developer. The metal deposit later for the silicidation require a direct contact with the silicon layer, thus the formal gate-oxide layer is then etched away with BOE-dip, the part which is necessary for the gate contact remained due the protection of the resist. Now, the sample is ready for the metal deposition. The Nickel layer is deposited with a 70nm e-beam evaporator. The useless nickel residual beyond the resist and the resist itself is then is removed with a lift-off process in acetone. The Nisi layer under the contact is formed by a silicidation process and the resulting sample layout is shown in figure 3b.The formation of control gate and program gate is required to complete this fabrication process. Similar as before, the sample is exposed by a image reversal process and the control gate contact is deposited with a e-beam deposition process and the resist is removed by the lift-off process. The oxide underneath the program gate contact is growth by a Atomic layer Deposition (ALD) process. 150 cycles are implemented in the ALD and a Al2O3 layer with thickness of 15nm is grown. Finally, another image reversal, e-beam deposition and lift-off in acetone process is executed to farm the program gate. The final cross section view of the fabricated device in shown in figure 3c.

Four different lithography process is necessary for the fabrication to form different structure in the device. Lithography



(a) (b) (c) (d)

Fig. 4: The bird eye view of the mask for (a): mesa and marker. (b) source/drain contact. (c) control-gate. (d) program gate. Different contact is denoted by different colour, the small square on the lower left and the upper right side of the mask is used for the alignment of different masks so that the device would be destroyed by the misalignment.

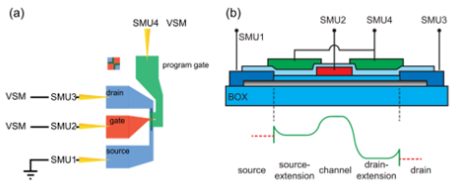
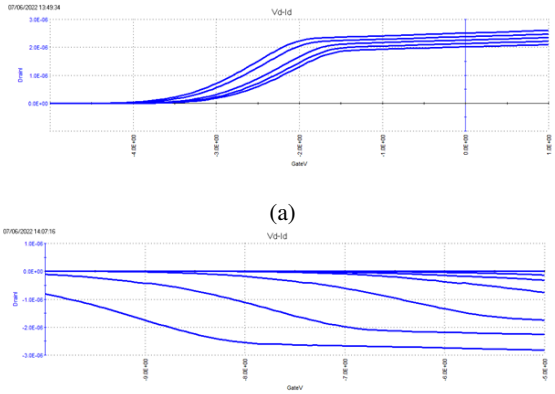


Fig. 5: measurement set up for the electrical characteristic of the RFET in (a) bird eyes view and (b) cross section view

for different level demands a different design of the mask. The bird eye view of the masks is given in figure 4, .

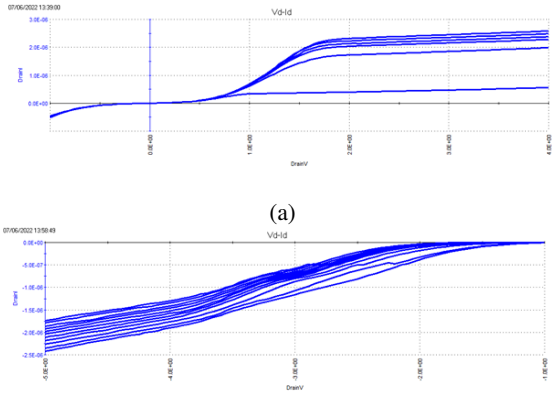
IV. Device Characterization and Discussion

The electrical characterization of the fabricated device is carried out by a semiconductor parameter analyzer. The sample is hold on a probe station with four probes. Each probe is connected to a source-measure unit (SMU) that can provide constant voltage and measure the current or vice versa. Each of these four probes is connected with a different contact in a way shows in figure 5. The n/p-mode of the RFET is controlled by the voltage of SMU4: +5 volt for the n-type configuration and -5 volt for the p-type configuration. To measure the transfer curve, the voltage of SMU3 which indicates the drain voltage is set to a constant whereas the voltage of SMU2 is increasing with a small step. Similarly, the output characteristic is obtained by set the V_{gs} to constant and measure the I_d for a varying V_{ds} supply.



(a) (b)

Fig. 6: Transfer curve for the RFET in (a) n-type configuration. (b) p-type configuration



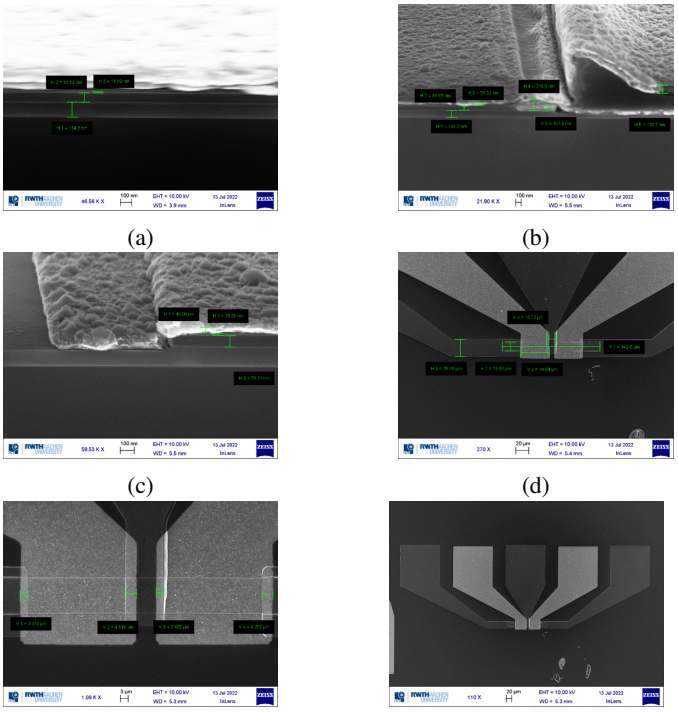
(a) (b)

Fig. 7: Transfer curve for the RFET in (a) n-type configuration. (b) p-type configuration

Figure 6a and 6b shows the transfer characteristic for the RFET with a constant program gate voltage. The n-type configuration transfer curve is similar with a conventional MOSFET, the drain current is linearly depend on the source drain voltage and a distinct saturation region as well as threshold voltage (around -4 volt) can be observed. However, In the p-type transfer curve, both threshold voltage and saturation voltage could not be defined clearly since their location lies outside the measurement range. The difference between these two values for n-type configuration is smaller than the p-type configuration. One possible explanation for this phenomenon is that the Schottky-barrier hight for electron is lower than the barrier for the hole.

The output characteristics of the RFET is measured as well and its result are shown in figure 7a and 7b. Similar as the transfer curve. The output curve for n-type configurations is more idealistic than the p-type configurations. the current increment of the n-type configuration after saturation region is smaller than the p-type configuration.

A scanning electron microscopy(SEM) has also been implemented to get the geometrical information about the RFET.



(a) (b) (c) (d) (e) (f)

Fig. 8: (a) SEM for the cross section with (b) cross section image of the interface between program gate and control gate (c) cross section image of the metal contact (d) The aerial view for the RFET device (e) More detailed view about the contact (f) Top view of a RFET

The cross section image was shown in figure 8a,8c and 8e, The thickness of different layer are marked on the picture. As shown in figure 8a, even a rather long time was spend on the ALD process, the gate oxide layer thickness is still small. However, as the trade off, the quality of such a layer is also better. The aerial view of the device is shown in figure 8b,8d and 8f, some contamination particles can be observed. But since they are not dropped on the device, the performance of the devices is not influenced. In figure 8d, a misalignment of the metal contact can be observed(the overlay of the metal contact on different side shows a slight difference). But since the designed structure is not damaged by such a difference. This deviation is considered as tolerable.

V. Conclusion

Reconfiguratble FETs is fabricated based on SOI wafer with a top-down approach. The procedure of fabrication is introduced. The transfer characteristic and output characteristic for both n and p type configuration was measured and proved that the fabricated device is able to work as both NFET and PFET mode by applying voltage with different polarity on the program gate. An obvious rising current is observed when the device is working is PMOS mode in the on-state. At the end, serials of pictures were taken by the SEM device to provide more direct view of the device structure.

Acknowledgments

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