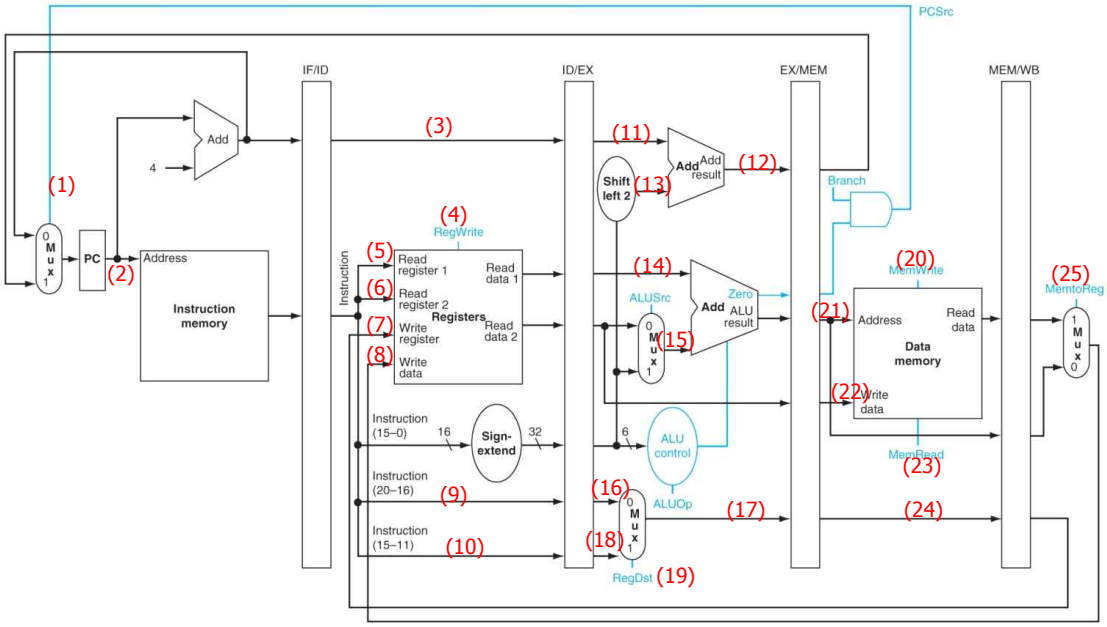
컴퓨터구조 Assignment-3 (Fall 2015)

1. **sw** 명령어가 WB stage에 있을 때 (1)~(25)의 값을 십진수 또는 16진수로 표시하라. 메모리 m 번지(0 ≦m<FE_{hex})의 값은 m+2이고, register $r(0≤r≤$31_{ten}$)에는 r*2가 저장되어 있다고 하자. 어떤 값이 될지 알 수 없는 경우는 ?로 표시하라. (각 0.5점)

```
        500ten: sw  $1,4($0)
Label:  504ten: add $2,$3,$10
        508ten: sub $6,$7,$8
        512ten: lw  $10,2($15)
        516ten: beq $11,$12,Label
```



2. 각 stage에 걸리는 시간이 다음과 같을 때,

IF	ID	EX	MEM	WB
25ps	20ps	23ps	25ps	20ps

2.1 What is the clock cycle time in a pipelined and nonpipelined processor? (2점)

2.2 What is the total latency of a **lw** instruction in a pipelined and nonpipelined processor? (2점)

2.3 Instead of a single-cycle organization, we can use a multi-cycle organization where each instruction takes multiple cycles but one instruction finishes before another is fetched. In this organization, an instruction only goes through stages it actually needs (4 cycles for R-type, 4 cycles for **sw**, 5 cycles for **lw**, 3 cycles for **beq**). Find clock cycle times with single-cycle, multi-cycle, and pipelined organization. (3점)

2.4 Calculate execute times of the program with single-cycle, multi-cycle, and pipelined organization. The program executes $5x10^9$ R-type instructions, $1x10^9$ **sw** instructions, $3x10^9$ **lw** instructions, and $2x10^9$ **beq** instructions. (6점)

3. Theses problems refer to the following instruction sequence: (Register and memory contents are unknown and you don't have to worry about memory alignment.)

```
and $1,$2,$3
sub $4,$5,$6
or  $7,$6,$1
add $8,$9,$4
slt $10,$11,$4
xor $12,$8,$10
sw  $14,12($8)
```

3.1 Draw a data dependence graph. (2점)

3.2 Find all hazards in this instruction sequence for a 5-stage pipeline without forwarding. List all the instruction pairs that have hazards. You don't have to show the type of the hazards. (2점)

3.3 Draw the single-cycle pipeline diagram for this code for a 5-stage pipeline without forwarding. At clock cycle 0, **and** instruction is in IF stage. (5점)

3.4 Draw the single-cycle pipeline diagram for this code for a 5-stage pipeline with forwarding. At clock cycle 0, **and** instruction is in IF stage. (5점)

3.5 Show the values of ForwardA and ForwardB during clock cycles 3 ~ 7. (5점)

4. Repeat Problem 3 for the following instruction sequence: (Register and memory contents are unknown and you don't have to worry about memory alignment. Assume 5-stage MIPS pipeline with hazard detection unit.)

```
and $1,$2,$3
lw  $4,0($6)
or  $7,$4,$1
add $8,$9,$4
lw  $8,0($6)
xor $12,$8,$10
sw  $14,22($5)
```

5. Theses problems refer to the following instruction sequence: (Register and memory contents are unknown and you don't have to worry about memory alignment. Assume 5-stage MIPS pipeline with forwarding unit and hazard detection unit.) (각 5점)

```
        add  $1,$2,$3
YY:     sw   $4,37($5)
        bne  $6,$7,XX     ; not taken
        xor  $8,$9,$10
        add  $11,$8,$12
        beq  $17,$18,YY    ; Taken
        sub  $19,$10,$15
XX:     slt  $21,$22,$23
```

5.1 Draw the single-cycle pipeline diagram for this code, assuming there are no delay slots and that branches execute in the ID stage.

5.2 Draw the single-cycle pipeline diagram for this code, assuming there are no delay slots and that branches execute in the EX stage.

5.3 Draw the single-cycle pipeline diagram for this code, assuming there are no delay slots and that branches execute in the MEM stage.

5.4 Repeat Problem 5.1, but assume that delay slots are used. In the given code, the instruction that follows the branch is now the delay slot instruction for that branch.

5.5 Repeat Problem 5.2, but assume that delay slots are used. In the given code, two instructions that follow the branch are now the delay slot instructions for that branch.

6. The importance of having a good branch predictor depends on how often conditional branches are executed. Together with branch predictor accuracy, this will determine how much time is spent stalling due to mispredicted branches. In these problems, assume that the breakdown of dynamic instructions into various instruction categories is as follows: (각 2점)

R-Type	beq	lw	sw
50%	5%	35%	10%

Also, assume the following branch predictor accuracies:

Always-taken	Always not-taken	2-bit
40%	60%	70%

6.1 Stall cycles due to mispredicted branches increase the CPI. What is the extra CPI due to mispredicted branches with the always-taken predictor? Assume that branches execute in the ID stage, that there are no data hazards, and that no delay slots are used.

6.2 Repeat Problem 6.1 for the "always not-taken" predictor.

6.3 Repeat Problem 6.1 for the 2-bit predictor.