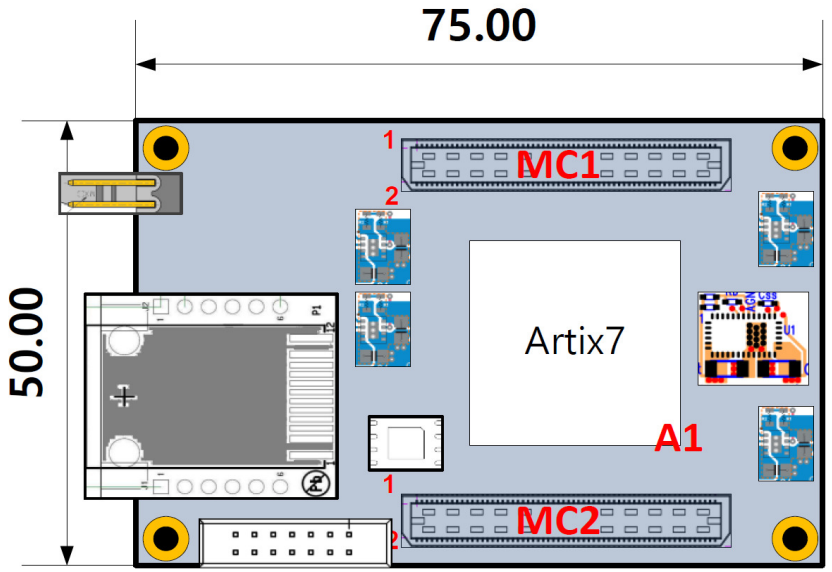
< [MLCC] MHVSU FPGA Module >

Designed By: YK SEOL
Checked & Approved By: JH Cho

Ver 1.0: 2020.07.01
Ver 1.1: 2020.08.12

검정색 TEXT :회로도 설명
붉은색 TEXT :회로도 수정포인트 (두꺼운 박스 - 이번 버전에서 수정된 부분)
(얇은박스 - 수정이력)
파란색 TEXT : PCB Silk 표시층괄호 앤TEXT
보라색 TEXT :회로블럭 이름



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Title:	[MLCC] FPGA Module	TEAM			
		TM1			
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A3	01.COVER	Seol YK	Seol YK	Cho SE	1.1
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<Revision History >

Date	Version	Editor	Revision
2020.07.01	1.0	YK SEOL	First Disign, 상 용 품 대체용, Foot Print 변경
2020.08.12	1.1	YK SEOL	ADJ 레 귤 레 이 터 설 정 R 값 수정-B JTAG 커 넥 터 변경 P7 FPGA BOOT 순 서 관련 C 추가 - 7P 보 조 전 원 입 력 커넥터 변경 - 8P

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A3	02.Revision History		Seol YK	Seol YK	Cho SE	1.1
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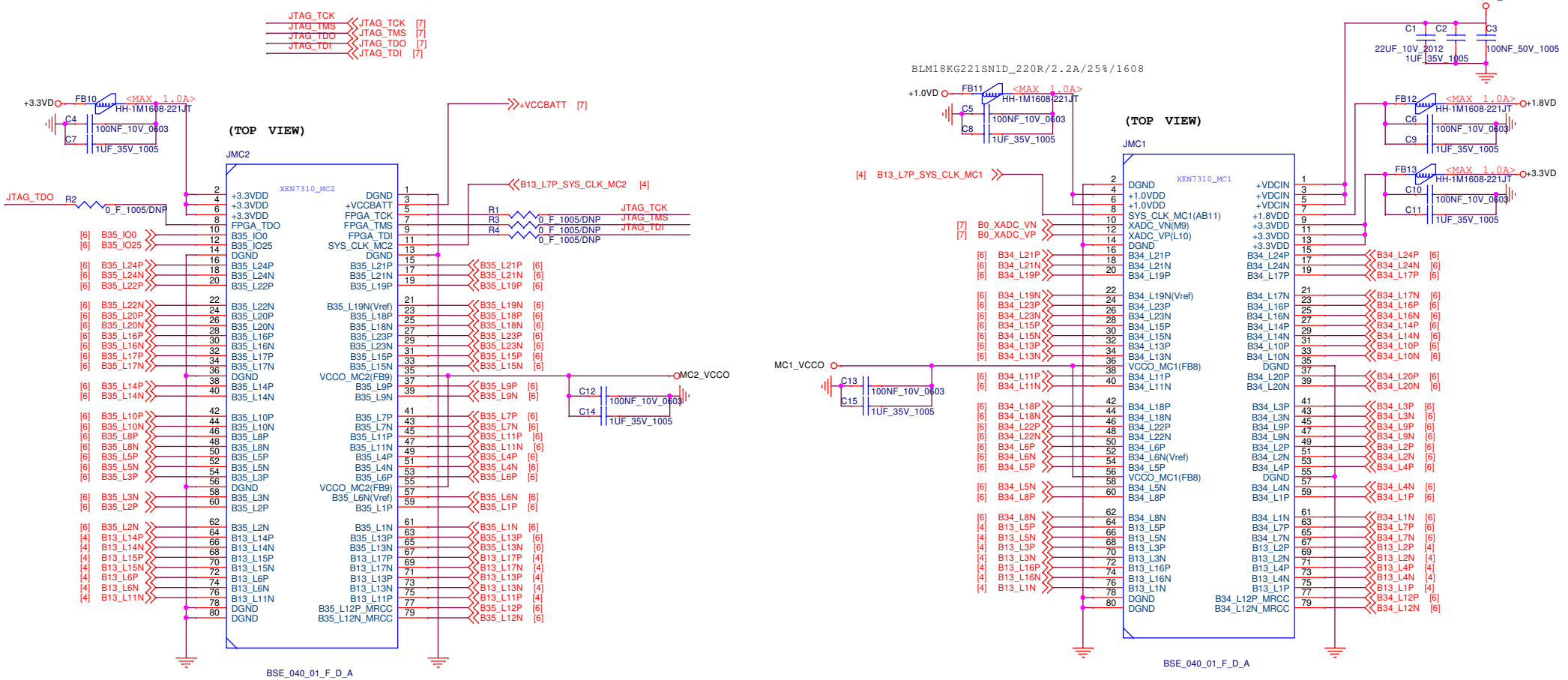
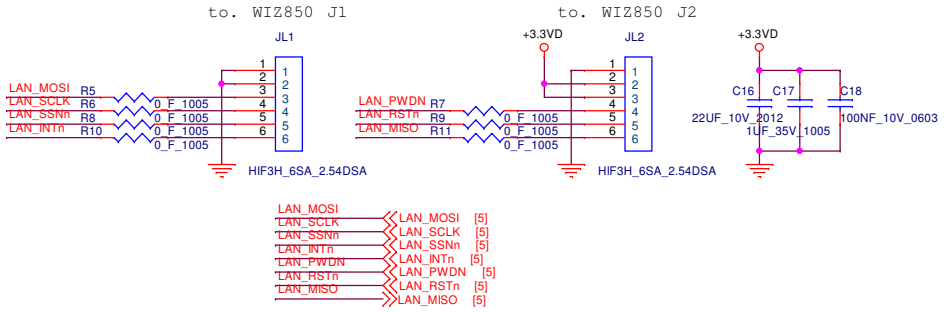
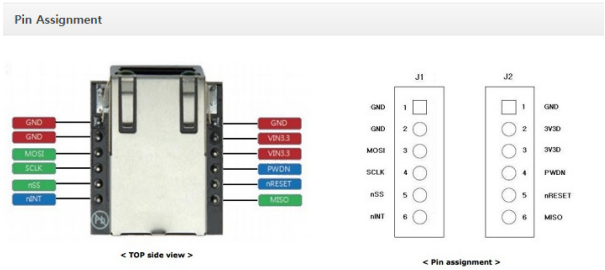
MHVSU BASE BD 뒤 (BOTTOM)



LAN 뚤 Connector





폴링 방식 으로 구동
RST 핀에 여 initia liz e or re-initia lize W 0
또 INT 핀에 하여 동 작 적 용

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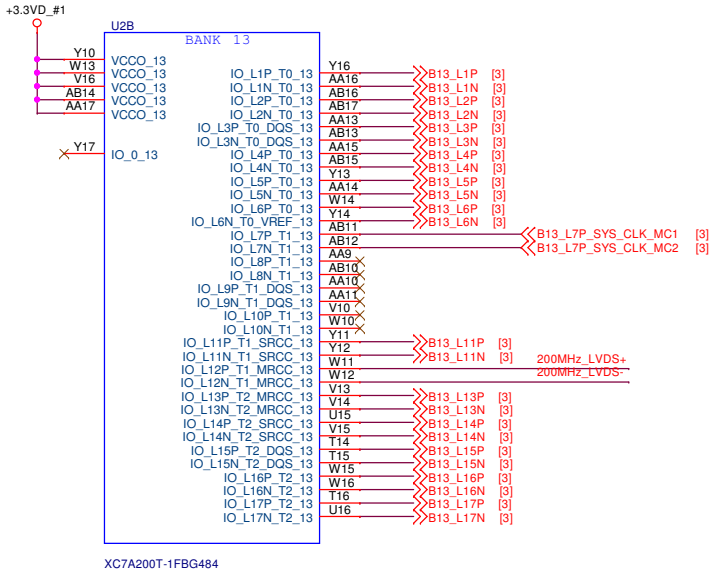
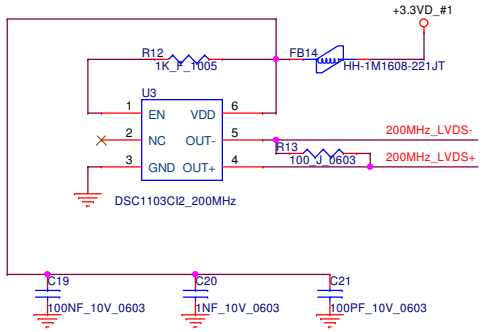
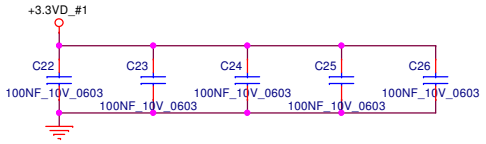
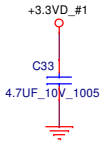
FPGA - BANK 13

BANK 13 : MC1 & MC2



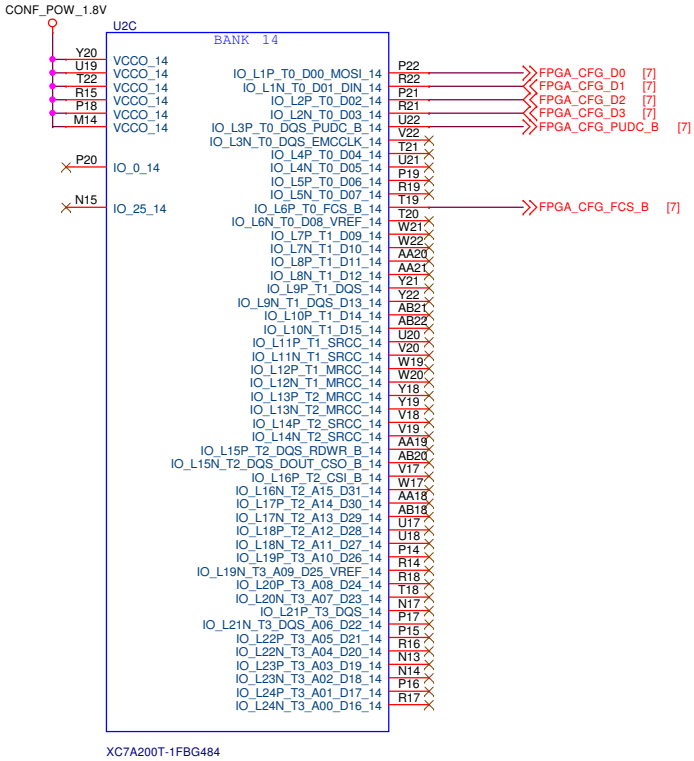


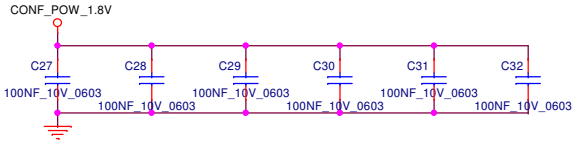


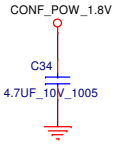


FPGA - BANK 14

BANK 14 : FPGA CONFIG & GPIO







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Title: [MLCC] FPGA Module		TEAM TM1			
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A3	04.FPGA#1	Seol YK	Seol YK	Cho SE	1.1
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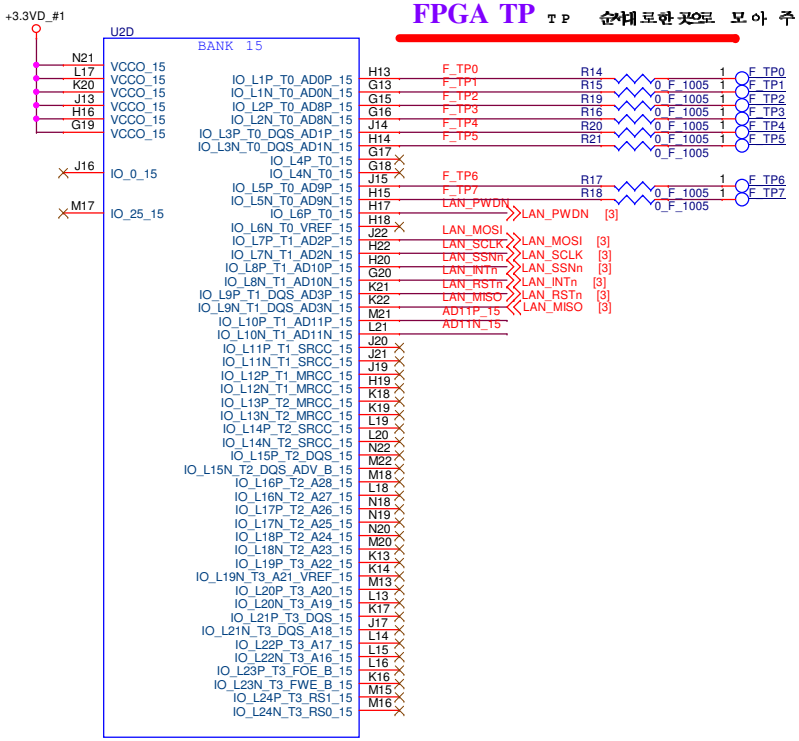
FPGA - BANK 15

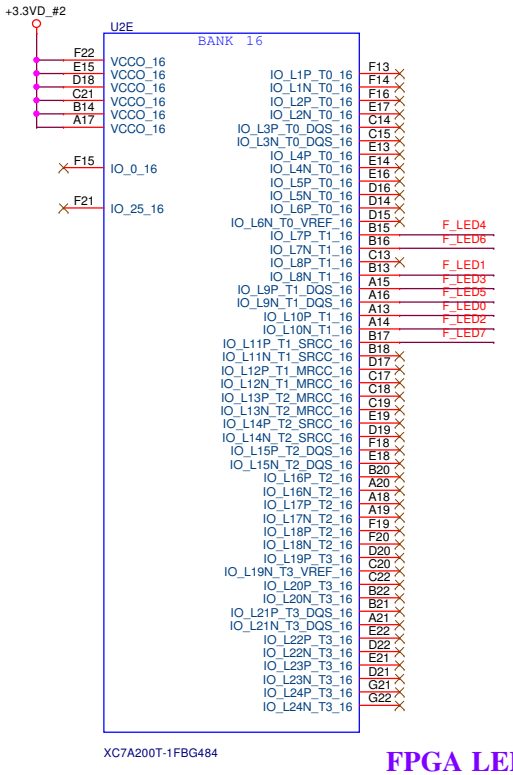
FPGA - BANK 16

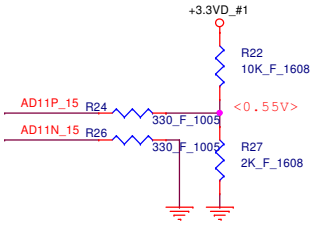
BANK 15 : LAN CONTROL

BANK 16 : TP & LED

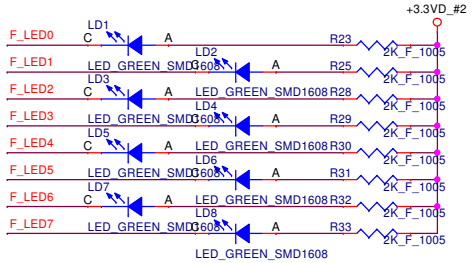
FPGA TP TP 순서대로한곳으로 모아 주 세 요

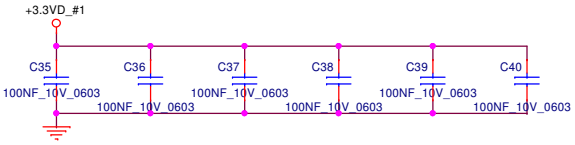


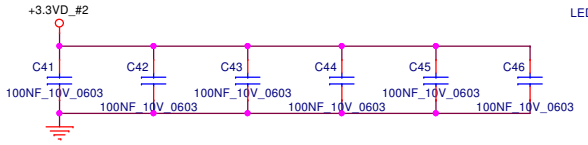


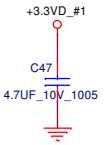


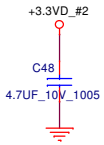
FPGA LED LED 순서대로한곳으로 모 아 주











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Title:	[MLCC] FPGA Module	TEAM TM1			
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A3	05.FPGA#2	Seol YK	Seol YK	Cho SE	1.1
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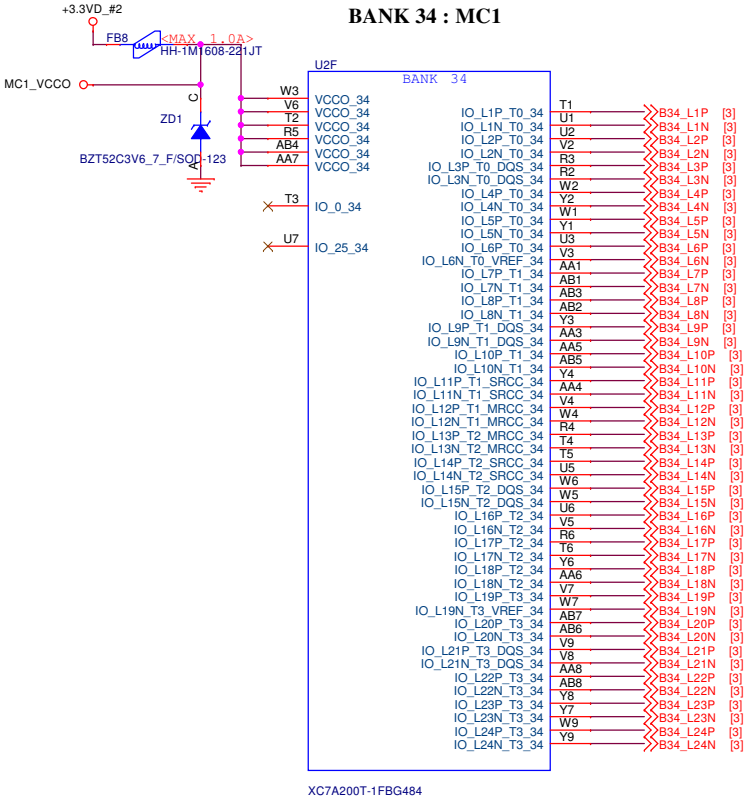
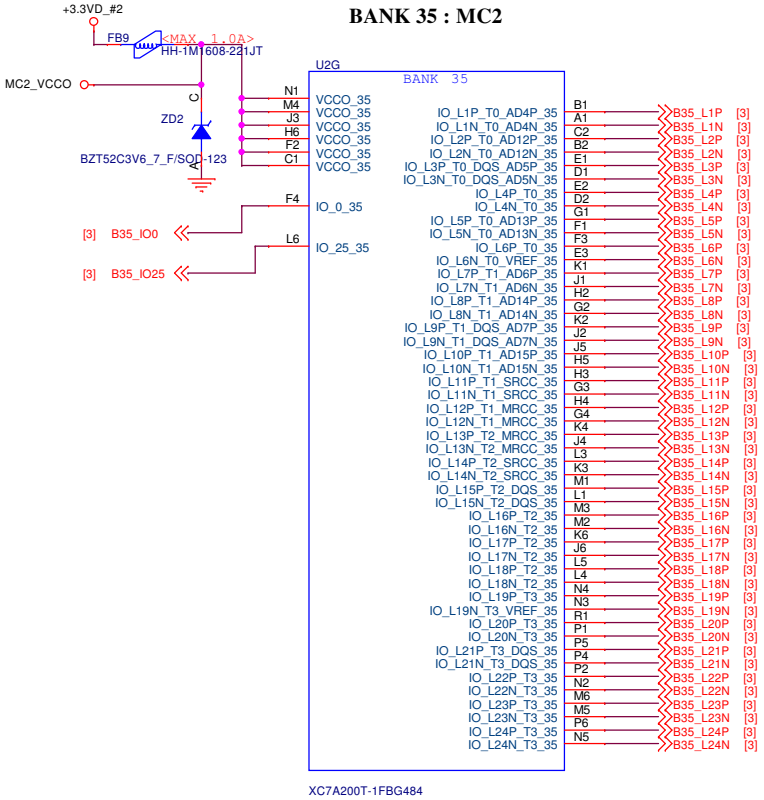
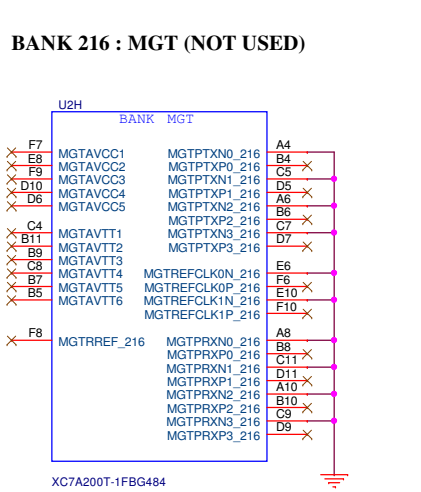
FPGA - BANK 34



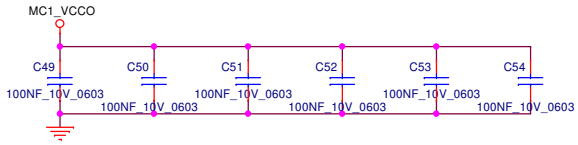
FPGA - BANK 35

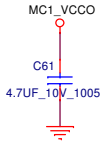


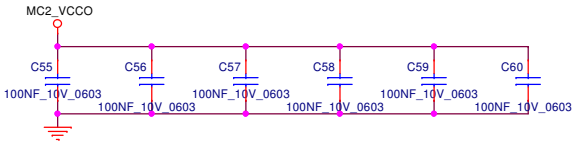
FPGA - BANK 216

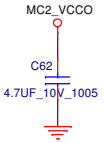


[FPGA Power]
MGTAVCC = 1.0V
MGTAVTT = 1.25V









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Title:	[MLCC] FPGA Module	TEAM TM1			
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A3	06.FPGA#3	Seol YK	Seol YK	Cho SE	1.1
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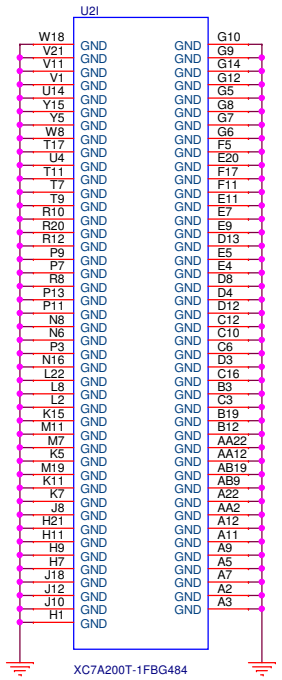
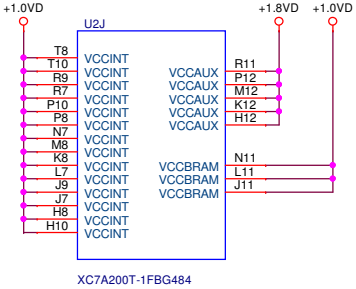
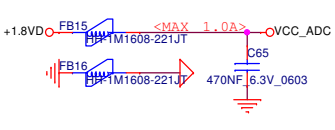
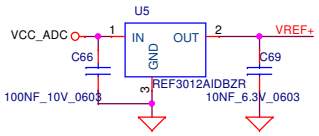
FPGA - POWER

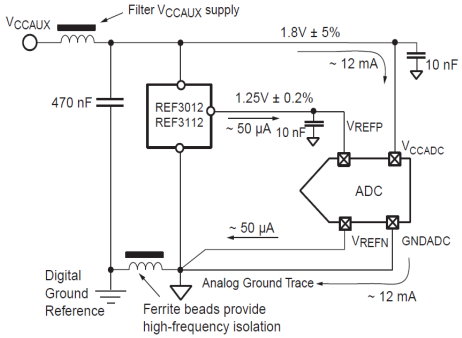


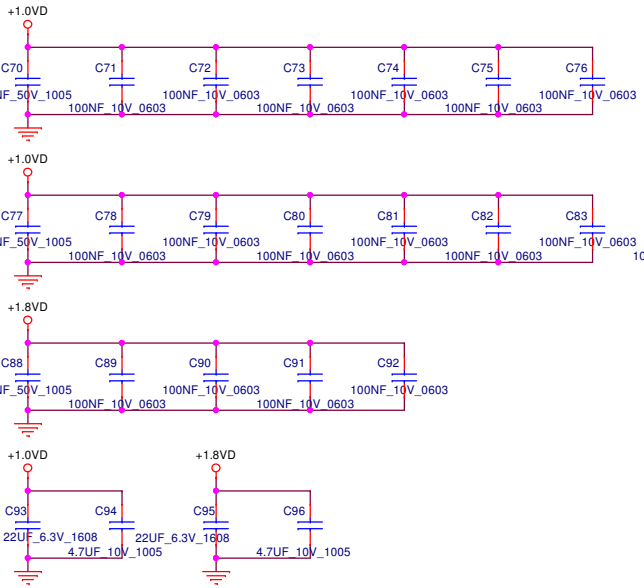


[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7제외)
VCCBATT = -0.5 ~ 2.0V [1.8V]
VCCADC = -0.5 ~ 2.0V [1.8V]

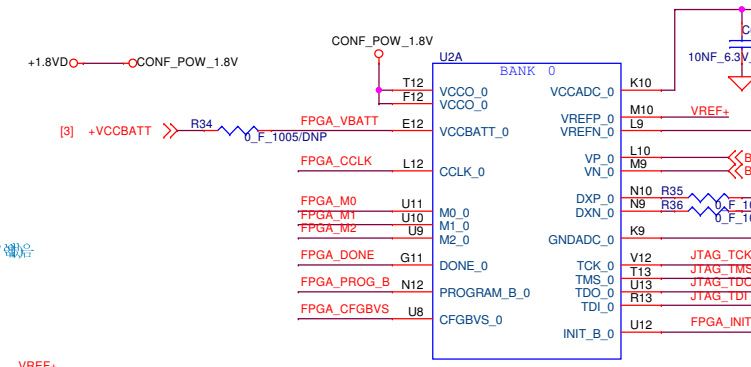








FPGA - Configuration Part



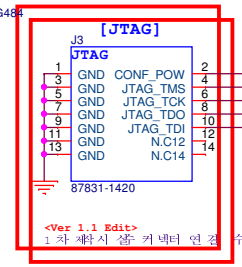
[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7제외)
VCCBATT = -0.5 ~ 2.0V [1.8V]

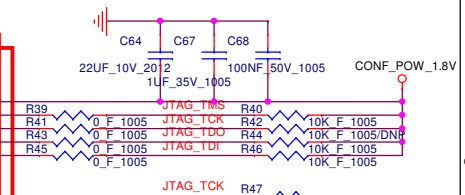
[FPGA Power]
VCCADC = -0.5 ~ 2.0V [1.8V]
VREF = -0.5 ~ 2.0V [1.25V]
to GNDADC

Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND.

VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

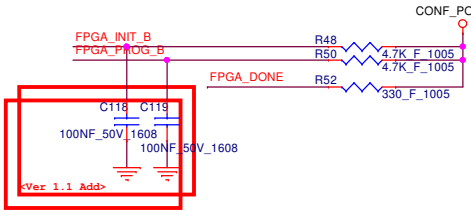
If the VCCO_0 supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High (i.e. connected to VCCO_0). Tie CFGBVS to Low (i.e. connected to GND), only if the VCCO_0 for bank 0 is less than or equal to 1.8V. If used during configuration, banks 14 and 15 should match the VCCO level applied to bank 0

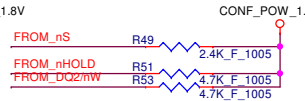


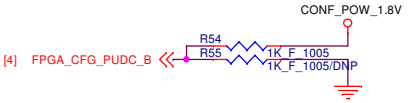


If the TCK signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.

If the TMS signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.







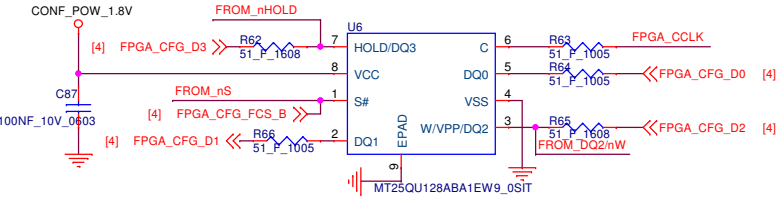
Pull-Up During Configuration (bar)
Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
> When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
> When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1kΩ to VCCO_14 or GND.
Caution! Do not allow this pin to float before and during configuration

Configuration Mode Sel (M2:0)
- Master SPI: 001
- Master Serial: 000
- JTAG: 101

Program (bar)
Active-Low reset to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge.
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.

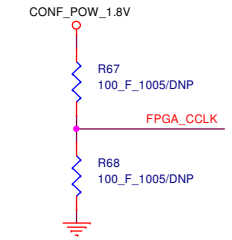
Initialization (bar)
Active-Low FPGA initialization pin or configuration error signal. The FPGA drives this pin Low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High. INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a High is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M[2:0] pin settings.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

Done
A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.



MT25QU256ABA1EW9_0SIT MT25QL = 2.7V ~ 3.6V
MT25QU = 1.7V ~ 2.0V

S25FL128SAGNFI001
S25FL256SAGNFI001



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		TM1	
Size	Document_Number	Designed	Checked	Approved	Rev
A3	07.FPGA#4	Seol YK	Seol YK	Cho SE	1.1
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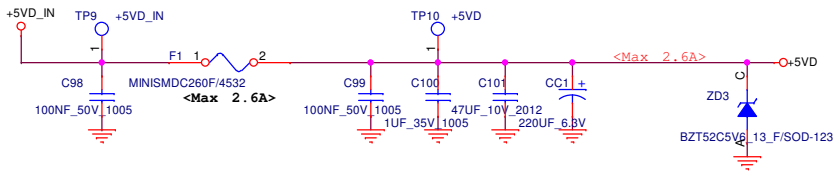
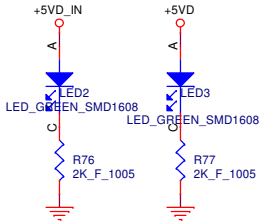
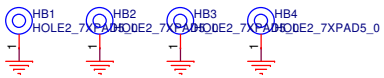
FUSE



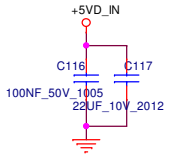
[+5VD_IN] [+5VD]

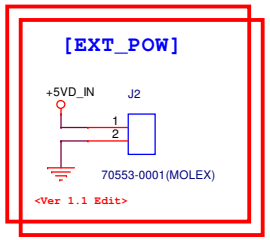


보드 고정 홀



보조 전원 커넥터





Regulator

<Ver 1.1 Edit>

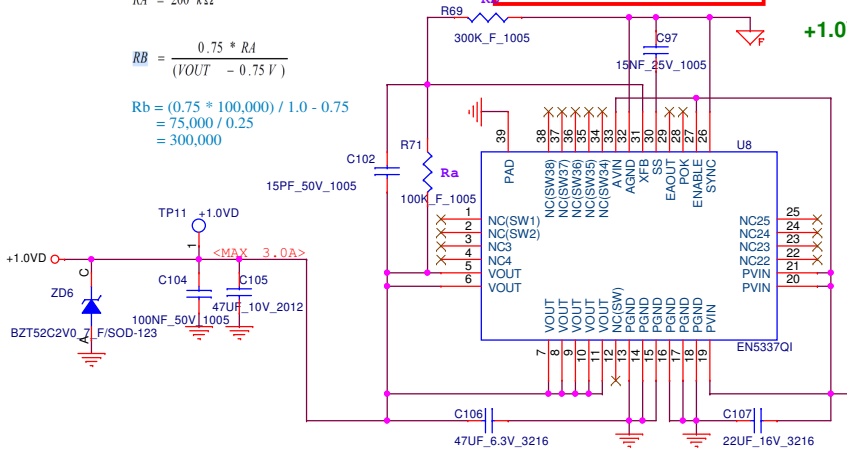
1 차 제작 시 살짝 저항 수 정 되 어 야 함
30K ~ 300K

$$RA = 200\ k\Omega$$

$$RB = \frac{0.75 * RA}{(VOUT - 0.75\,V)}$$

Rb = (0.75 * 100,000) / 1.0 - 0.75
= 75,000 / 0.25
= 300,000

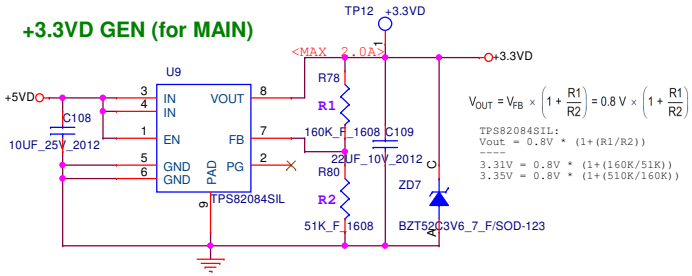
+1.0VD GEN



[FPGA Power]
VCCINT = 1.0V
VCCBRAM = 1.0V
VAUX = 1.8V
VAUX_IO = 1.8V
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7에 없음)
VCCBATT = 1.8V
VCCADC = 1.8V

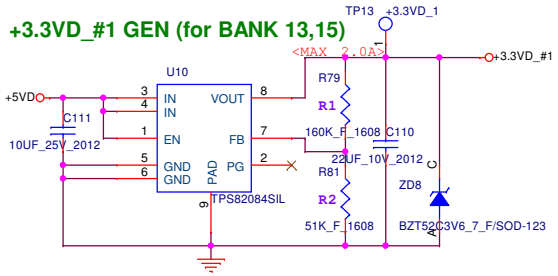
DATASHEET의 LAYOUT 참고 ! !!

+3.3VD GEN (for MAIN)

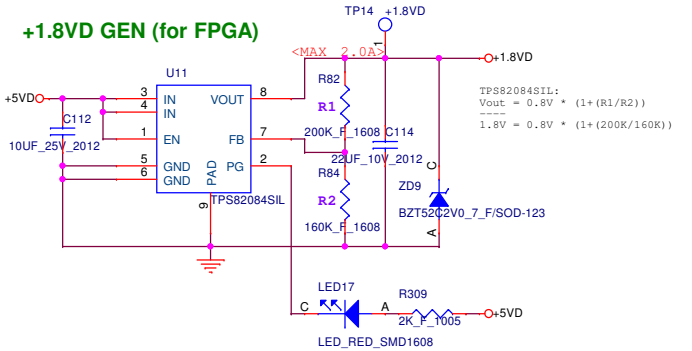


$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right)$$

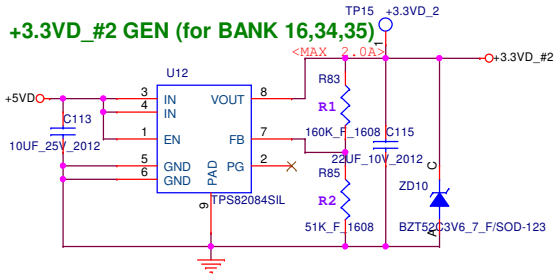
+3.3VD_#1 GEN (for BANK 13,15)



+1.8VD GEN (for FPGA)



+3.3VD_#2 GEN (for BANK 16,34,35)



TPS82084SIL:
Vout = 0.8V * (1+(R1/R2))
1.0V = 0.8V * (1+(40.2K/160K))

TPS82084SIL:
Vout = 0.8V * (1+(R1/R2))
1.2V = 0.8V * (1+(80.6K/160K))

TPS82084SIL:
Vout = 0.8V * (1+(R1/R2))
1.35V = 0.8V * (1+(110K/160K))

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Title: [MLCC] FPGA Module		TEAM TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	08.Power	Seol YK	Seol YK	Cho SE	1.1
Date: Wednesday, August 12, 2020		Sheet 8 of 8			