# <Revision History >

| Date | Version | Editor | Revision |
|---|---|---|---|
| 2020.02.04 | 1.0 | YH YI | 80Vpp, 40V@60ns slew rate HVPGU |
| 2020.10.20 | 1.1 | YH YI | 80Vpp, 40V@30ns slew rate HVPGU, Overcurrent/overheat detection Output switch |
| 2021.03.02 | 1.2 | YH YI | Output switch modification, Zener diode voltage reference Capacitors for high speed |
| 2021.07.26 | 1.3 | YH YI | S3100 interface |
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| Title: Revision history | | TEAM TT | | | |
| Size | Document Number | Designed | Checked | Approved | Rev |
| A3 | DD | Y. YI | - | ___ | 1.0 |
| Date: Thursday, July 29, 2021 | | Sheet 1 of 7 | | | |

# < High Voltage PGU >

Designed By: YH YI
Checked & Approved By:
Ver 1.3 : 2021.07.23



## <Notice>

Black TEXT : Comment
Blue TEXT : PCB Silk [TEXT]
Violet TEXT : Block name
- Neither power plane nor ground plane under analog signal path
- No shield around signal path
- Larger TP radius
- Red block routing instruction
- 2.54mm pitch
- DNP : do not place



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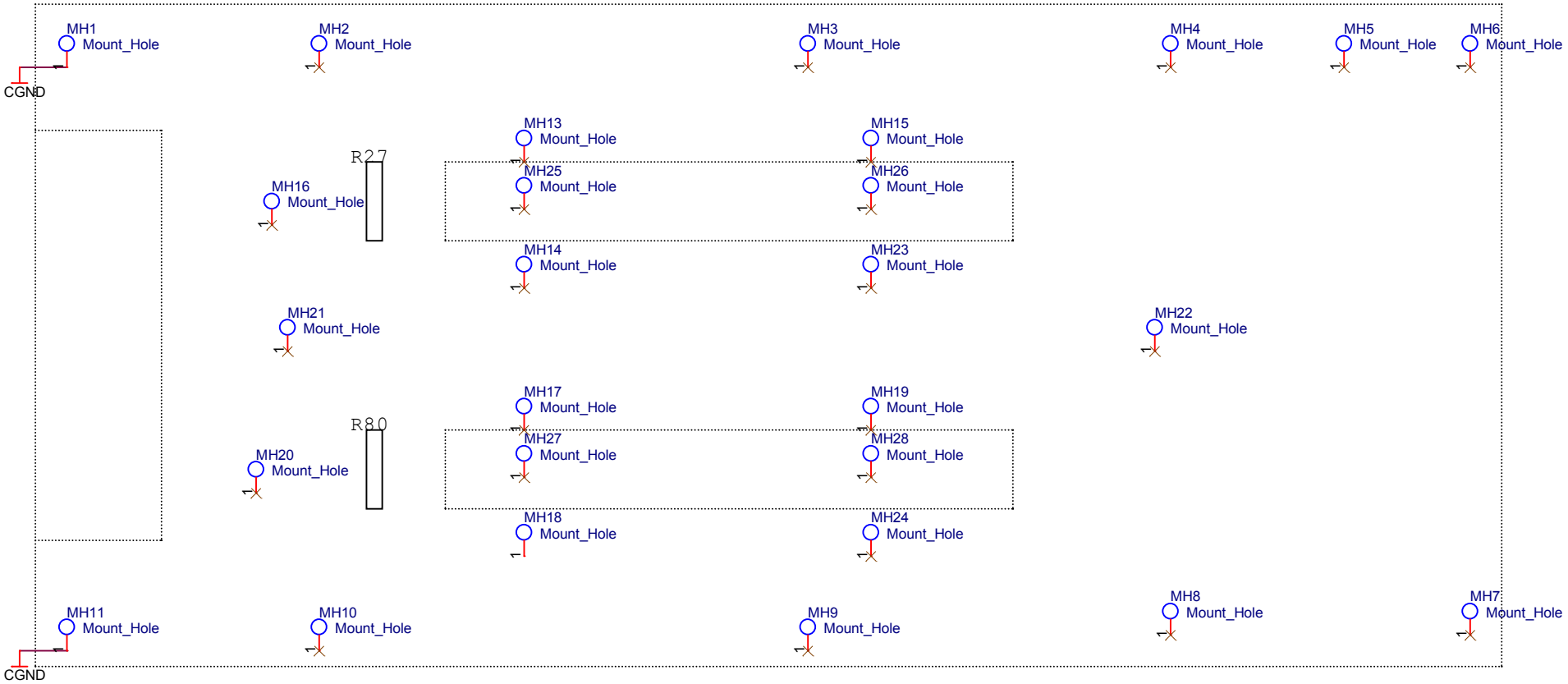


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| Title: BOARD_OUTLINE | | TEAM TT | | | |
| Size | Document Number | Designed | Checked | Approved | Rev |
| A4 | DD | Y. YI | - | ___ | 1.3 |
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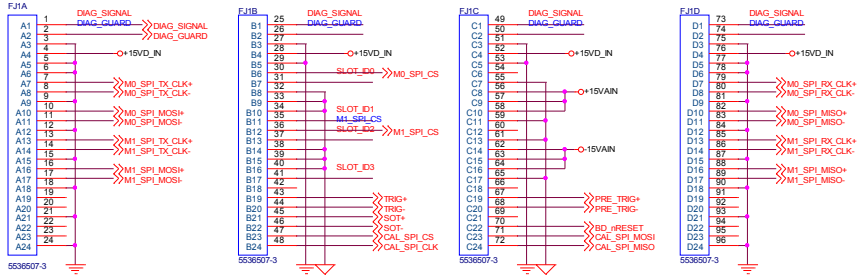
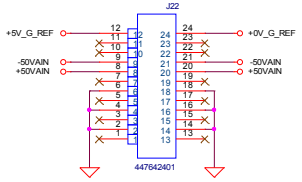
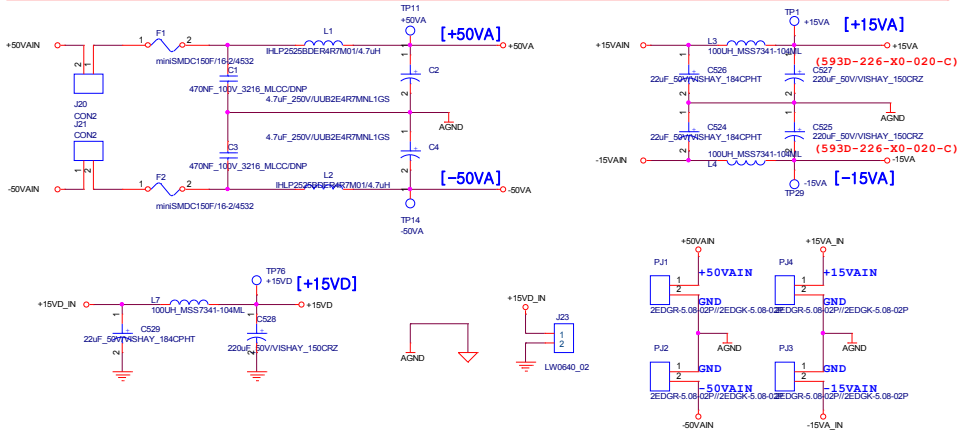
## INPUT CONNECTOR



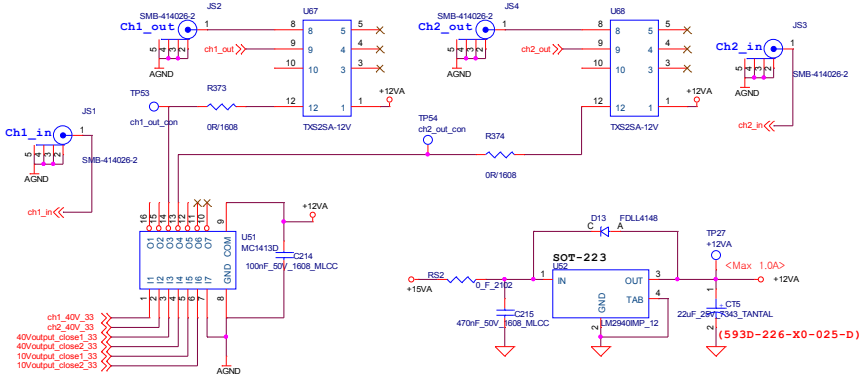




## POWER FILTER

커 패 시 터 간 격 유의할것 Artwork

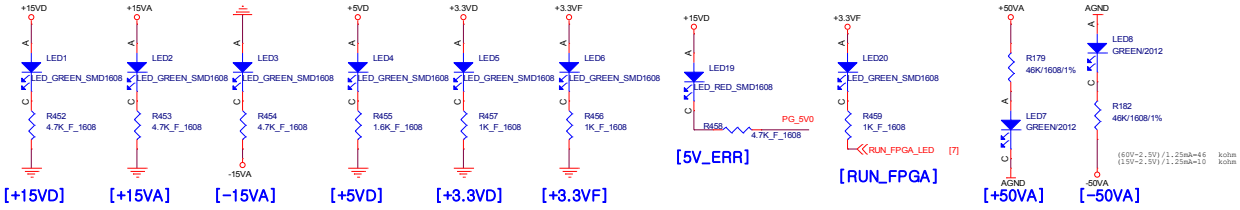



## SIGNAL SELECTOR

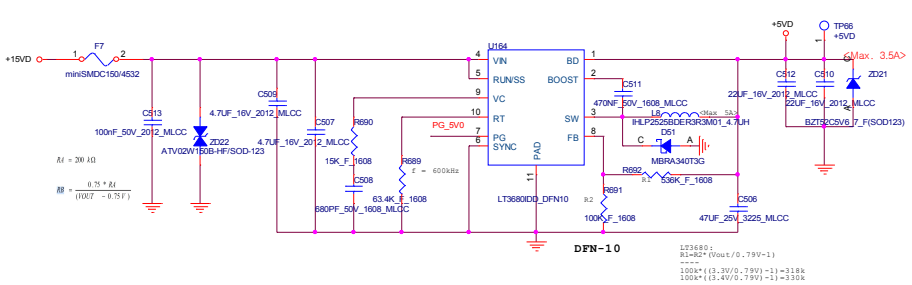


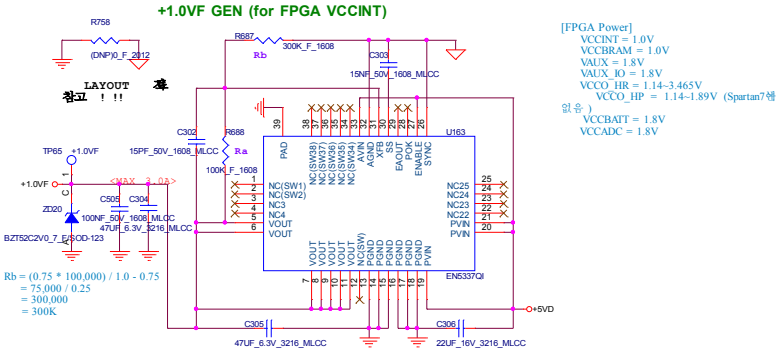

## POWER LED & RUN LED

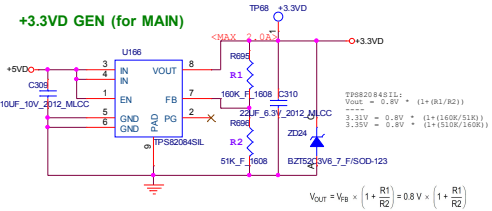
LED에 전원 이름 표 시

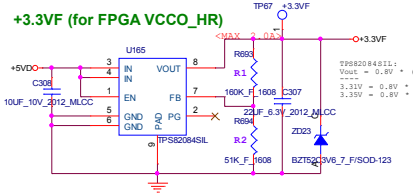


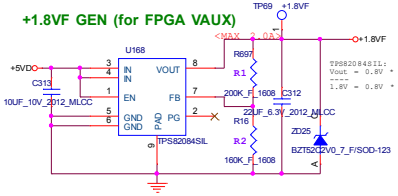

## REGULATORS



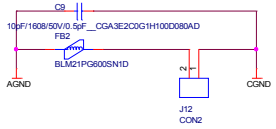



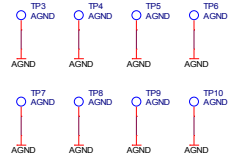




## GND 연 결




## TP

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| Title: Connector and Power | | | TEAM: IT | | |
| Size | Document Number | Designed | Checked | Approved | Rev |
| A2 | DD | Y. Yi | | | 1.0 |
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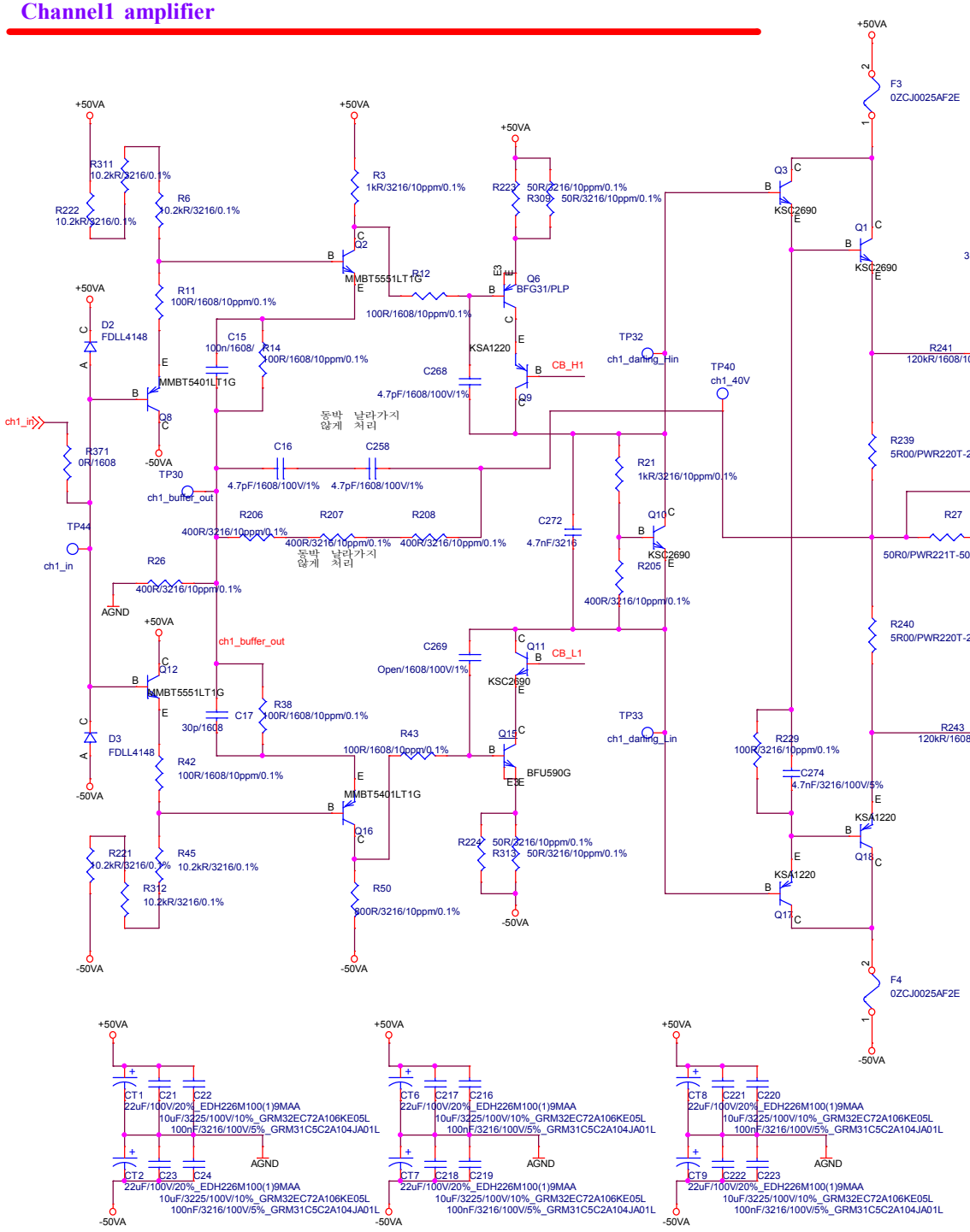
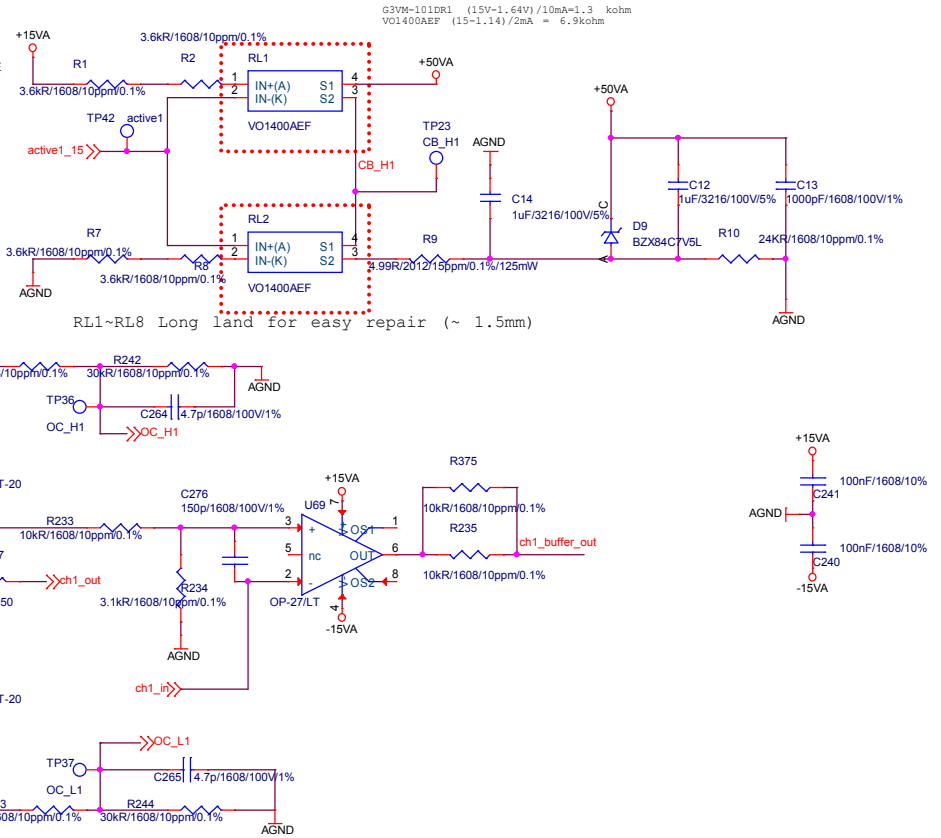
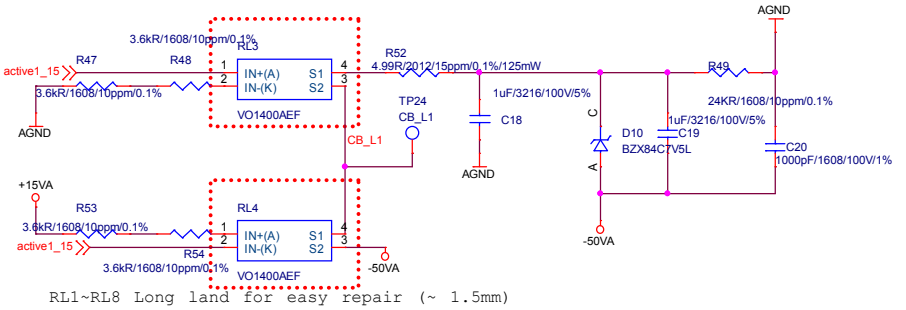
## Channel1 amplifier




## Positive bias voltage




## Negative bias voltage







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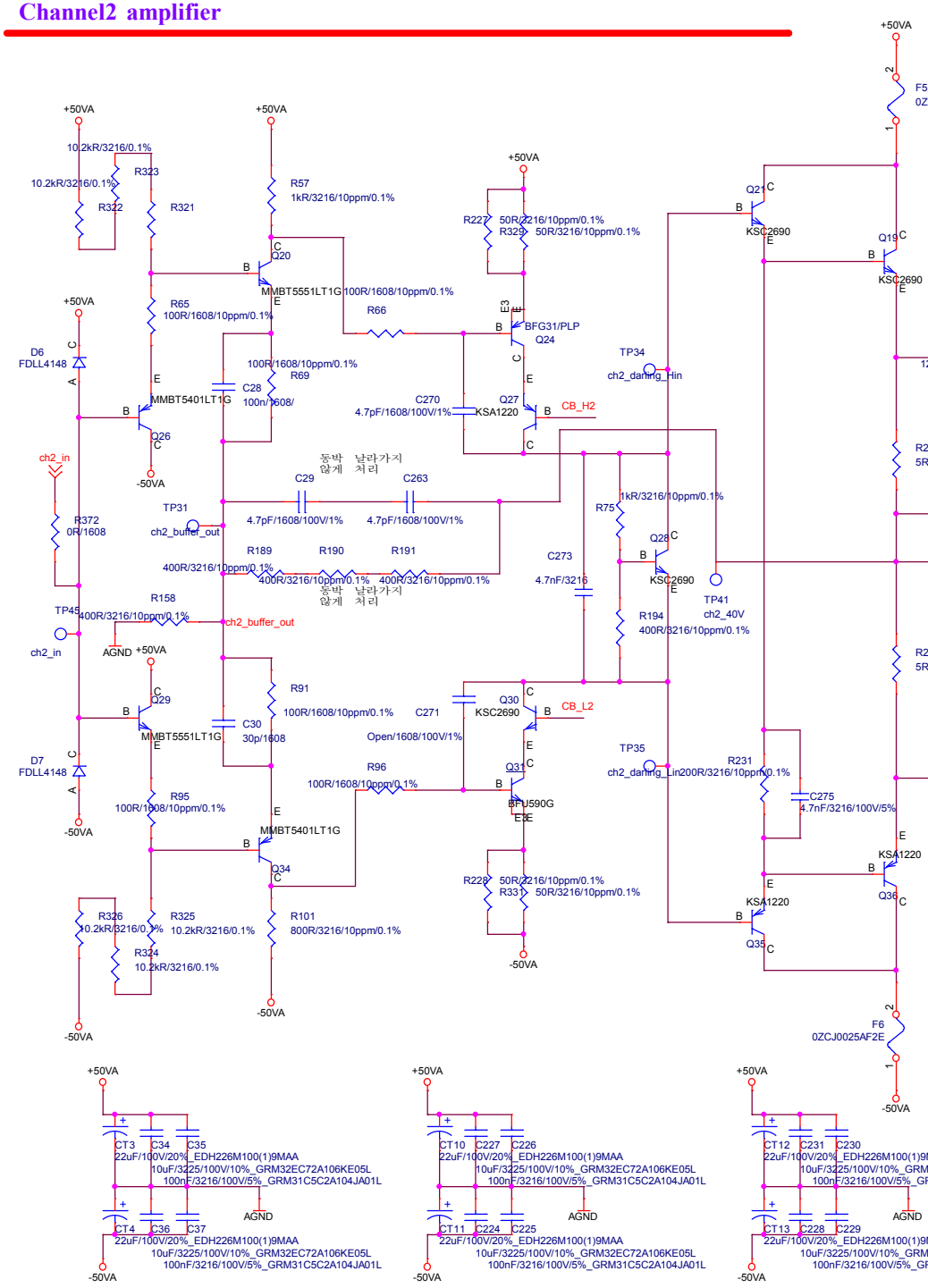
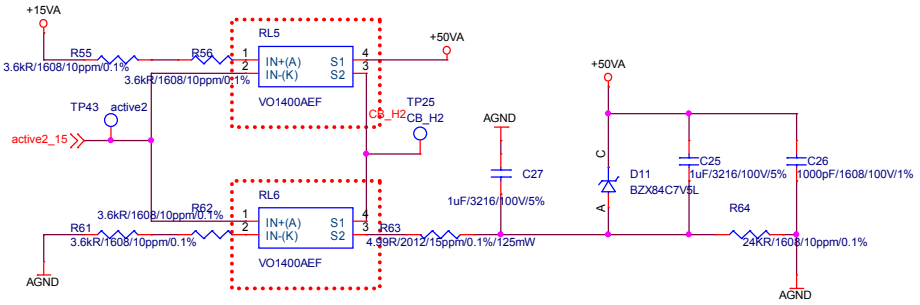
|---|---|---|---|---|---|
| Title: PGU_40Vamp1 | | | TEAM TT | | |
| Size | Document Number | | Designed | Checked | Approved | Rev |
| A3 | DD | | Y. Yi | | | 1.3 |
| Date: | Thursday, July 29, 2021 | | Sheet 4 | of 9 | | |

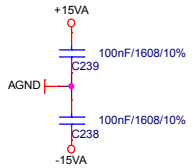
# Channel2 amplifier



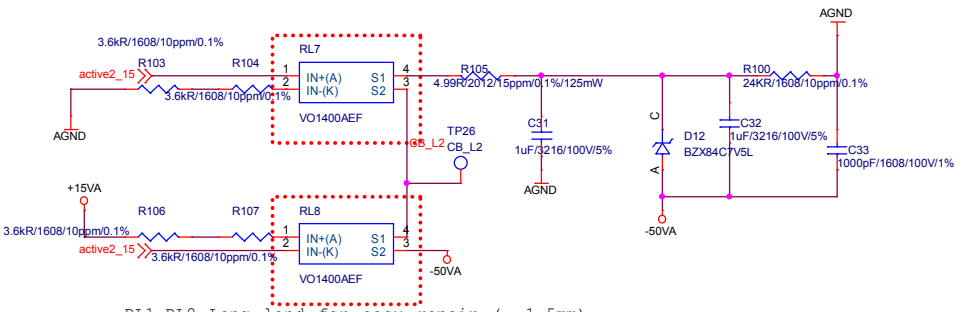

# Positive bias voltage




RL1~RL8 Long land for easy repair (~ 1.5mm)




# Negative bias voltage




RL1~RL8 Long land for easy repair (~ 1.5mm)



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| Title: PGU_40Vamp2 | | | TEAM TT | | |
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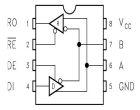
| A3 | DD | | Y. Yi | - | ___ | 1.3 |
| Date: | Thursday, July 29, 2021 | | Sheet 5 of 9 | | |

## RS-422 RX(1CH)

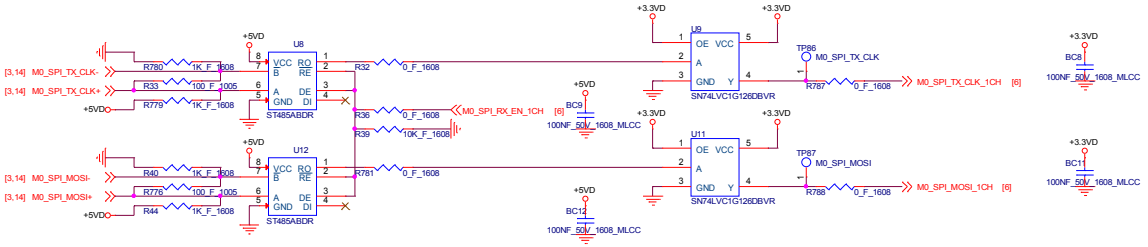
Table 4. Truth table (receiver)

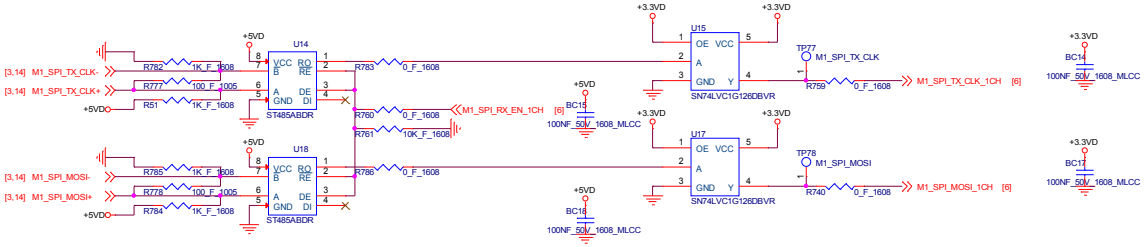
| Inputs | | | Outputs | Mode |
|---|---|---|---|---|
| $\overline{RE}$ | DE | A-B | RO | |
| L | L | ≥ -0.2 V | H | Normal |
| L | L | ≤-0.2 V | L | Normal |
| L | L | Inputs open | H | Normal |

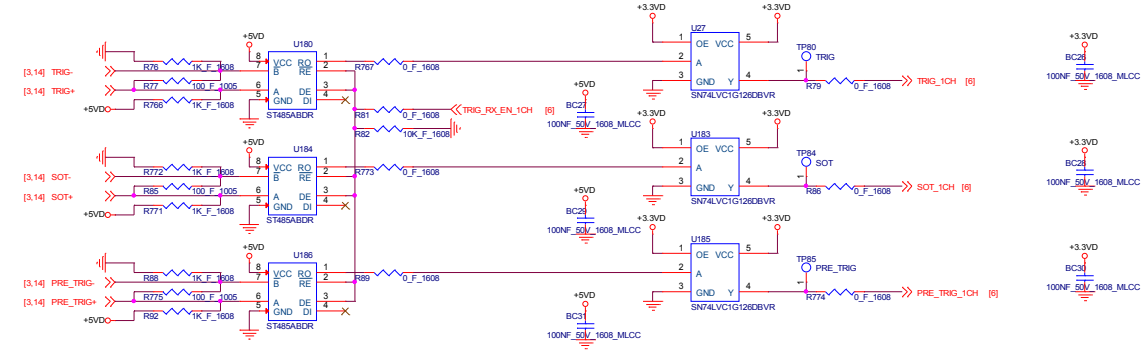



Differential 신 호 는 패 턴 길 이 등 를

덤 저 항 및 풀 업 풀 다 운 저 항 은 수 신 측



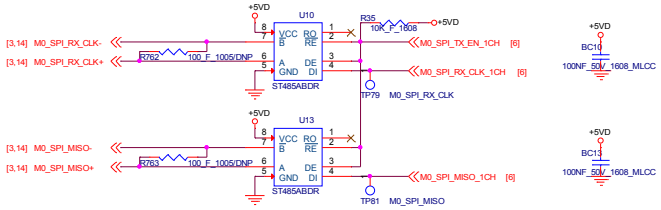



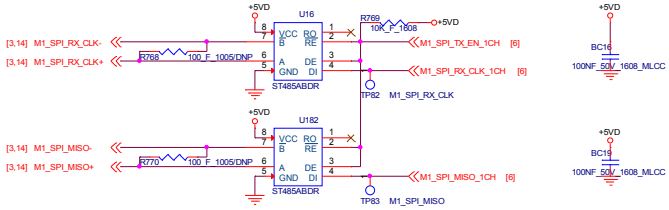

## RS-422 TX(1CH)

Table 3. Truth table (driver)

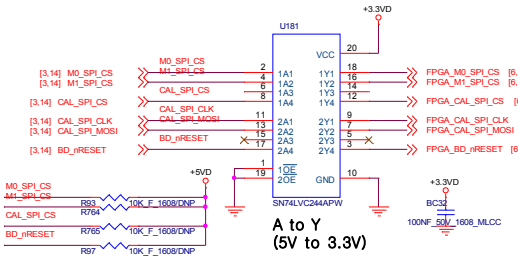
| Inputs | | | Outputs | | Mode |
|---|---|---|---|---|---|
| $\overline{RE}$ | DE | DI | B | A | A |
| X | H | H | L | H | Normal |
| X | H | L | H | L | Normal |
| L | L | X | Z | Z | Normal |

*Note:* *X = Don't care; Z = High impedance*

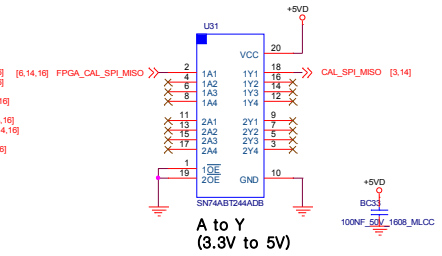



## SIGNAL RX (5V to 3.3V)(1CH)




## SIGNAL TX (3.3V to 5V)(1CH)

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| Title: <Title> | | | TEAM <OrgName> | |
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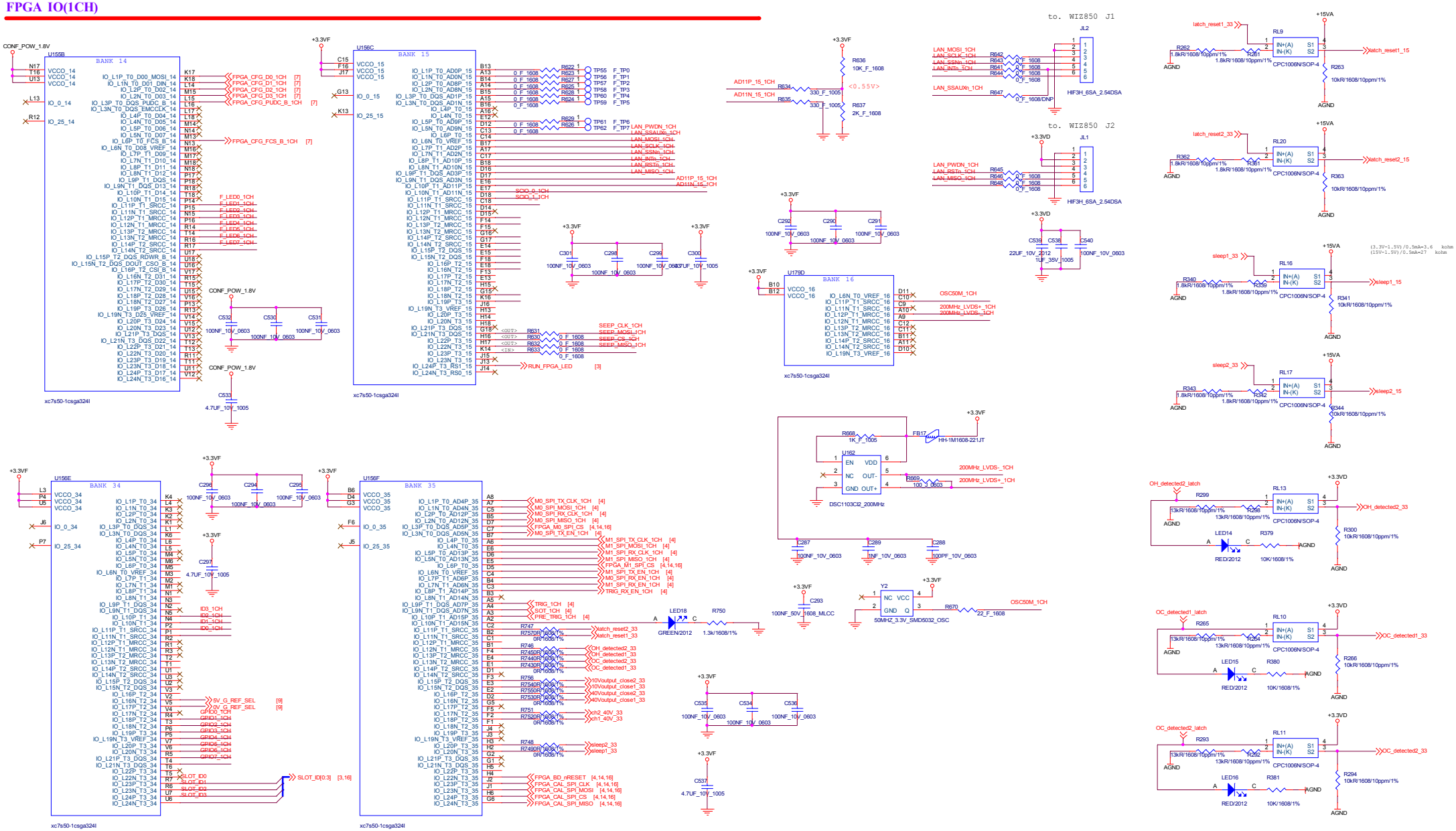
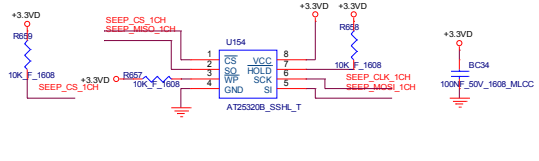
| A2 | 04. 1CH_BUFFER | <OrgAddr> | <OrgAddr> | <OrgAddr> 1.3 |
| Date: Thursday, July 29, 2021 | | Sheet 6 of 9 | | |

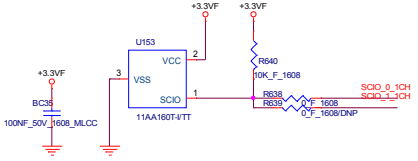
# FPGA IO(1CH)

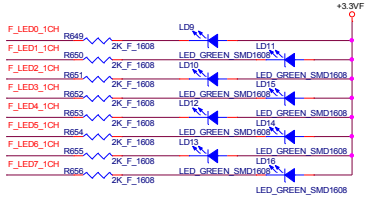



# SPI EEPROM(1CH) Calibration DATA 저 장 용 Serial EEPROM




# EEPROM 16K 2048X8 1.8V SERIAL EE IND(1CH)

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| A2 | DD | | | Y. YI | | 1.3 |
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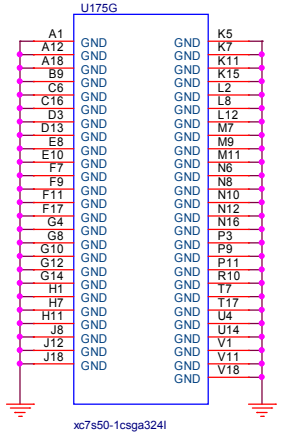
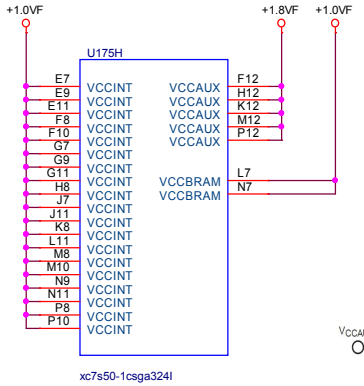
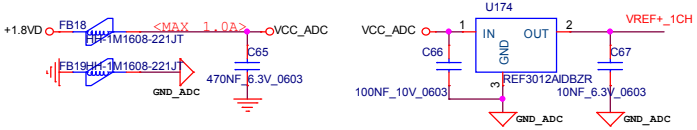
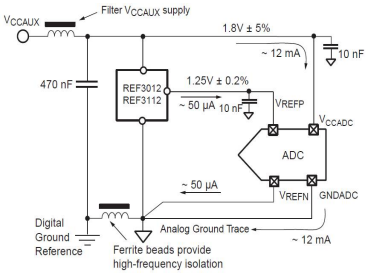
# FPGA - POWER(1CH)



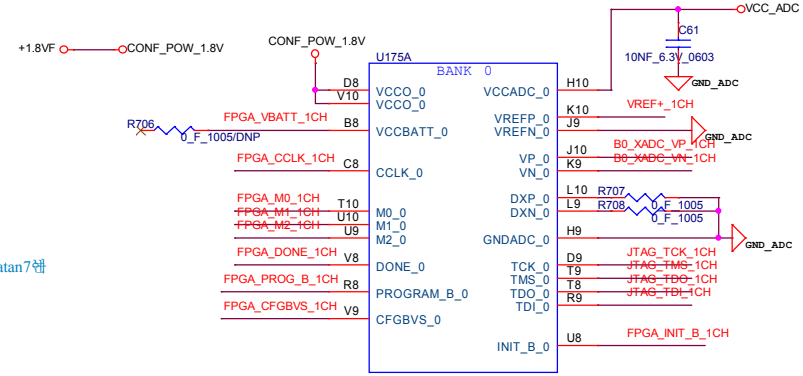




[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Spatan7쎈 없음 )
VCCBATT = -0.5 ~ 2.0V [1.8V]
VCCADC = -0.5 ~ 2.0V [1.8V]




# FPGA - Configuration Part(1CH)

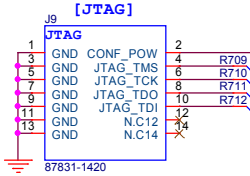



[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7쎈 없음 )
VCCBATT = -0.5 ~ 2.0V [1.8V]
[FPGA Power]
VCCADC = -0.5 ~ 2.0V [1.8V]
VREF = -0.5 ~ 2.0V [1.25V]
to GNDADC

Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND.

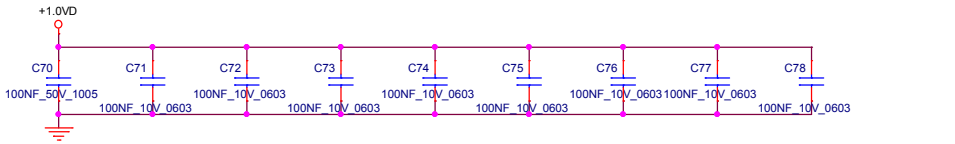
VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

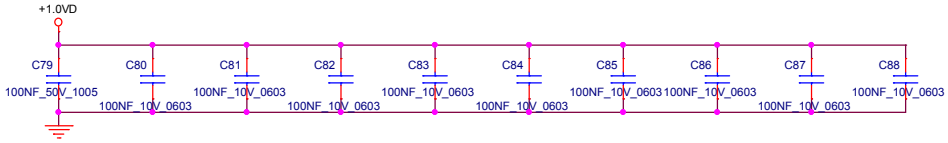
If the VCCO_0 supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High (i.e. connected to VCCO_0). Tie CFGBVS to Low (i.e. connected to GND), only if the VCCO_0 for bank 0 is less than or equal to 1.8V. If used during configuration, banks 14 and 15 should match the VCCO level applied to bank 0

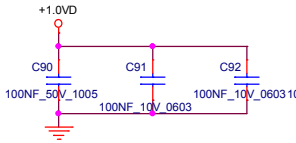


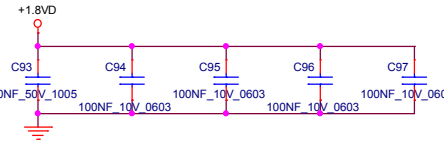

If the TCK signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ ) pull-up resistor to maintain a valid High when no cable is connected.

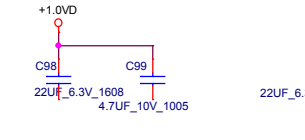
If the TMS signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ ) pull-up resistor to maintain a valid High when no cable is connected.

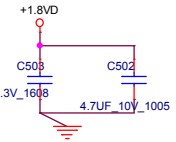


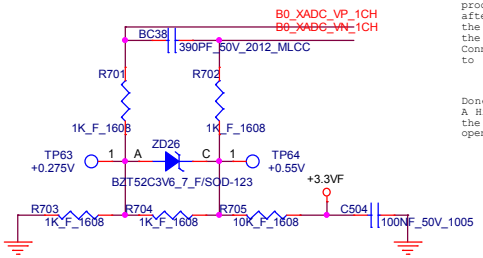








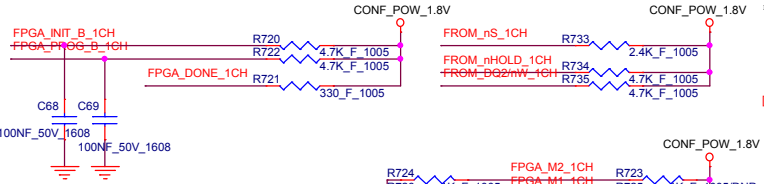





Program (bar)
Active-Low reset to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge.
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.

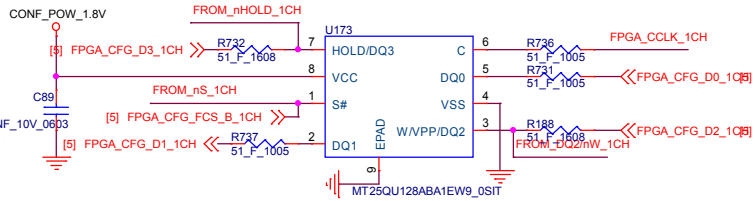
Initialization (bar)
Active-Low FPGA initialization pin or configuration error signal. The FPGA drives this pin Low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High. INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a High is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M[2:0] pin settings.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO0 to ensure clean Low-to-High transitions.

Done
A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.



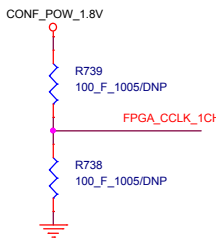
Configuration Mode Sel (M2:0)
- Master SPI: 001
- Master Serial: 000
- JTAG: 101

Pull-Up During Configuration (bar)
Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
> When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
> When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1kΩ to VCCO_14 or GND.
Caution! Do not allow this pin to float before and during configuration




MT25QU256ABA1EW9_0SIT MT25QL = 2.7V ~ 3.6V
MT25QU = 1.7V ~ 2.0V

S25FL128SAGNFI001
S25FL256SAGNFI001



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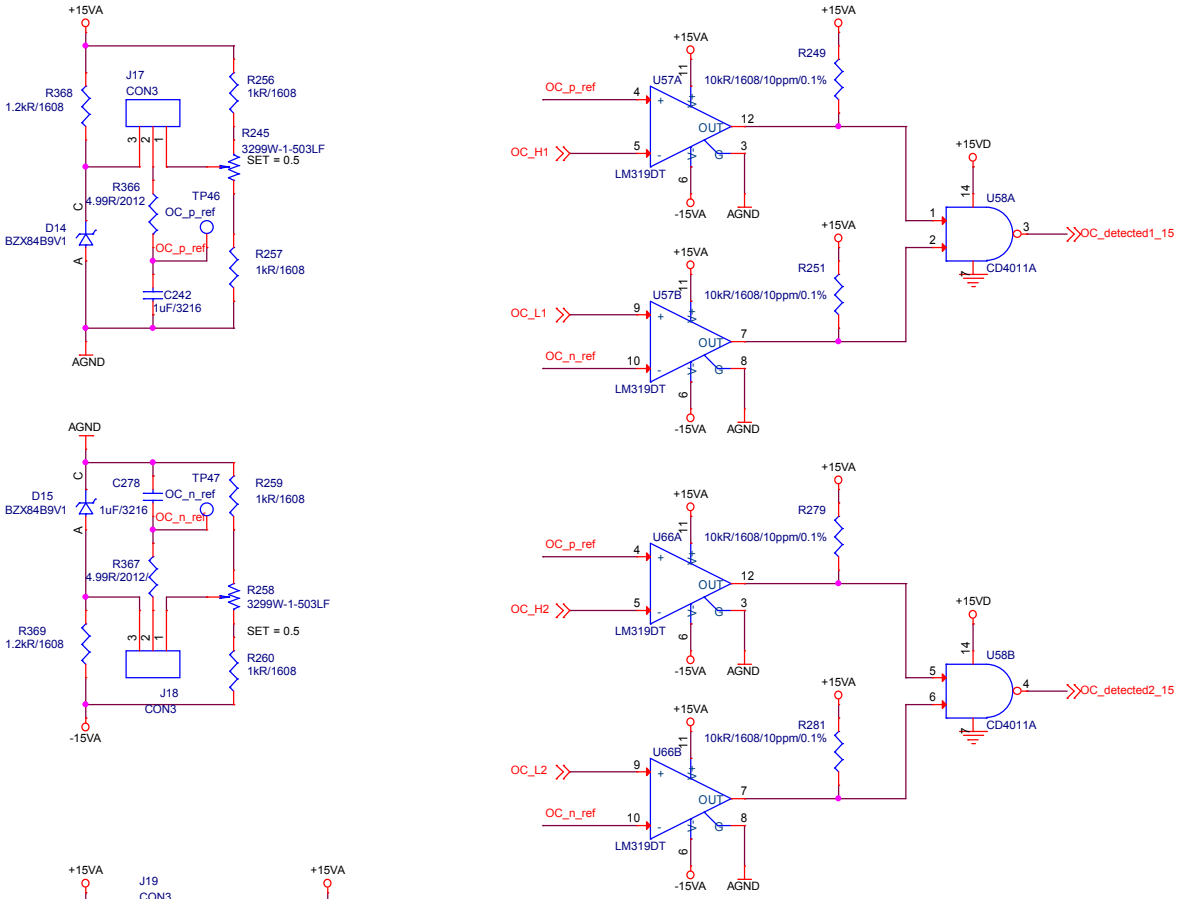
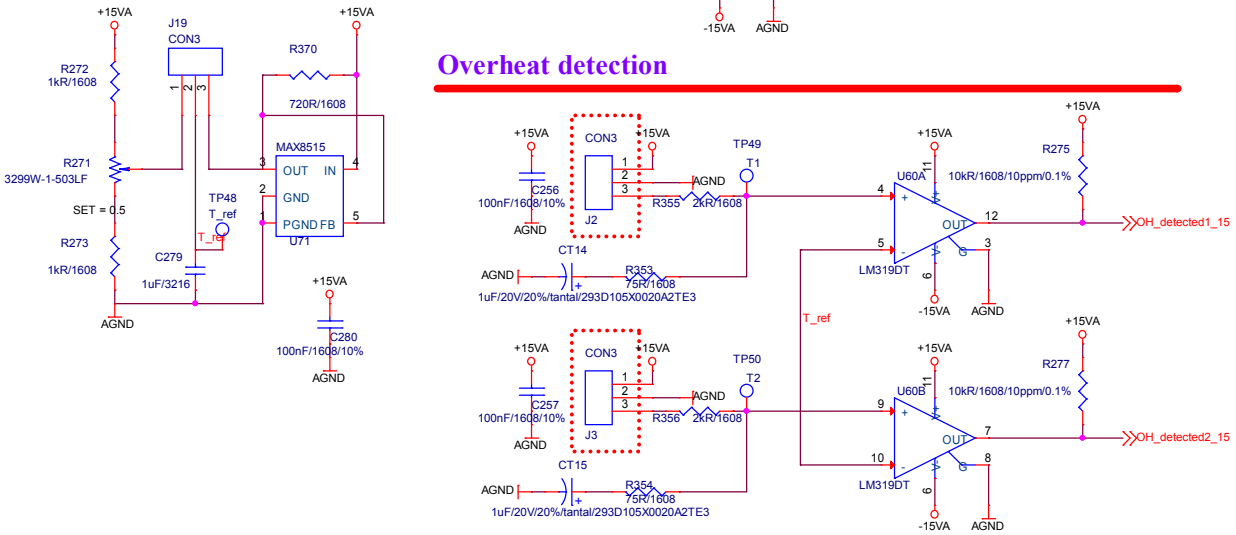
| Date: | Thursday, July 29, 2021 | Sheet 8 of 9 | | | |

## Overcurrent detection

All CD4000 series package : SOP



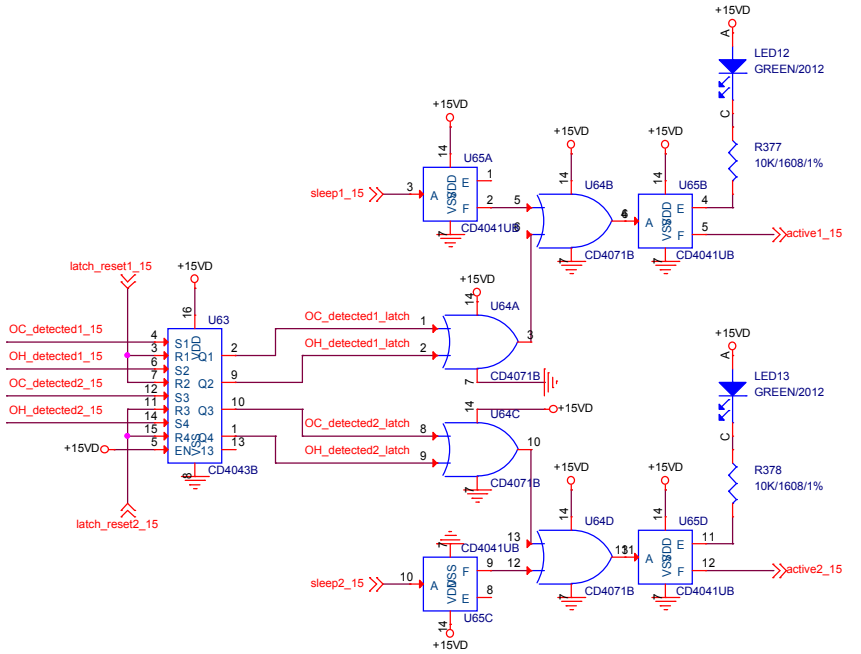

## Overheat detection

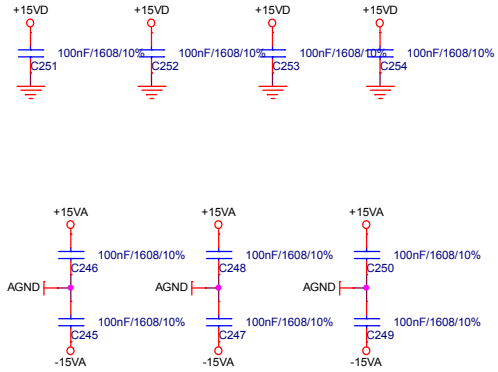



J2 : LM35 temp sensor. Pin1 : 15V, Pin2 : Gnd, Pin3 : signal
J3 : LM35 temp sensor. Pin1 : 15V, Pin2 : Gnd, Pin3 : signal

## OC/OH logic

CD4000 series package : SOP

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| Date: | Thursday, July 29, 2021 | | Sheet 9 of 9 | | | |