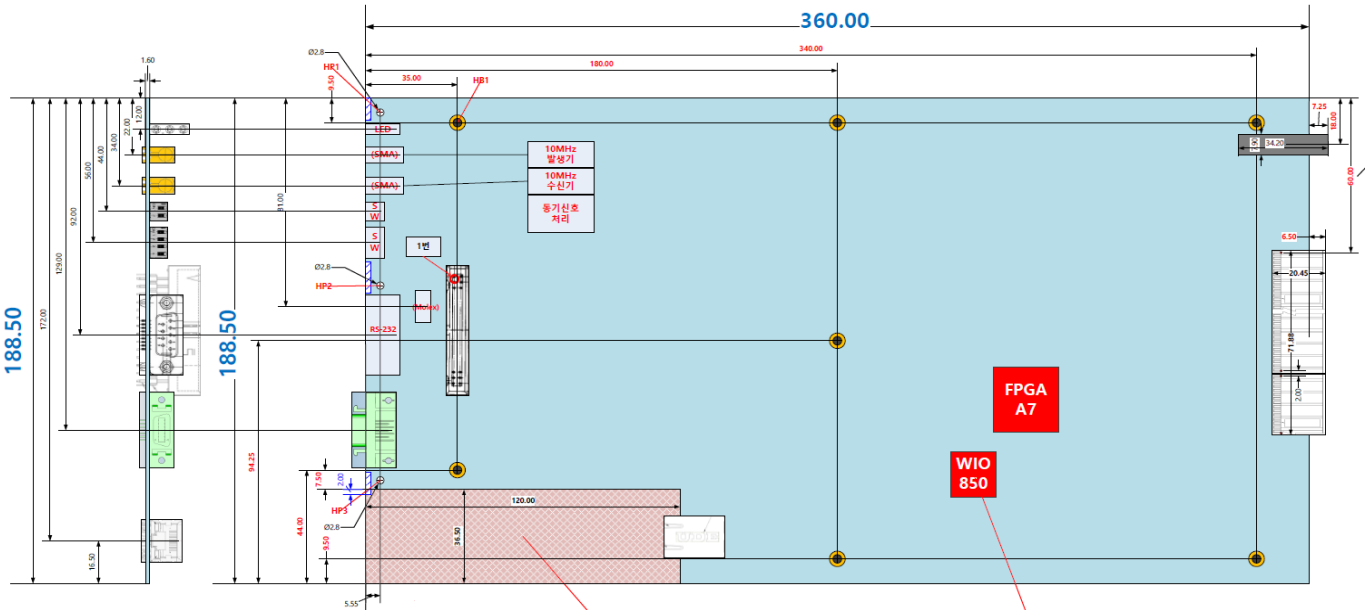
< [S3100] CPU_BASE BOARD >

Designed By: YKSeol
Checked & Approved By: YKSeol, JHCho
Ver 1.0 : 2021.03.19 S3100 CPU_BASE

검정색 TEXT : 회로도 설명
붉은색 TEXT : 회로도 수정포인트 (두꺼운 박스 - 이번버전에서 수정된 부분)

파란색 TEXT : PCB Silk 표시 [중괄호 안에 TEXT]
보라색 TEXT : 회로블럭 이름

01. Cover
02. Revision History
03. Core IO & Connector
04. Power
05. Bus Buffer
06. FPGA#1
07. FPGA#2
08. FPGA#3
09. FPGA#4
10. LAN
11. GPIB
12. Peripherals
13. Backplane Transceiver#1
14. Backplane Transceiver#2
15. Backplane and Sub Connetor



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Title: [S3100] CPU_BASE			TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	01. Cover		Seol YK	Seol YK	Cho JH	1.0
Date:	Thursday, March 25, 2021	Sheet 1 of 15				

<Revision History >

Date	Version	Editor	Revision
2021.03.19	1.0	YK SEUL	S3100 CPU BASE 보드

Title:		TEAM			
[S3100] CPU_BASE		TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	02. Revison History	Seol YK	Seol YK	JOH JH	1.0
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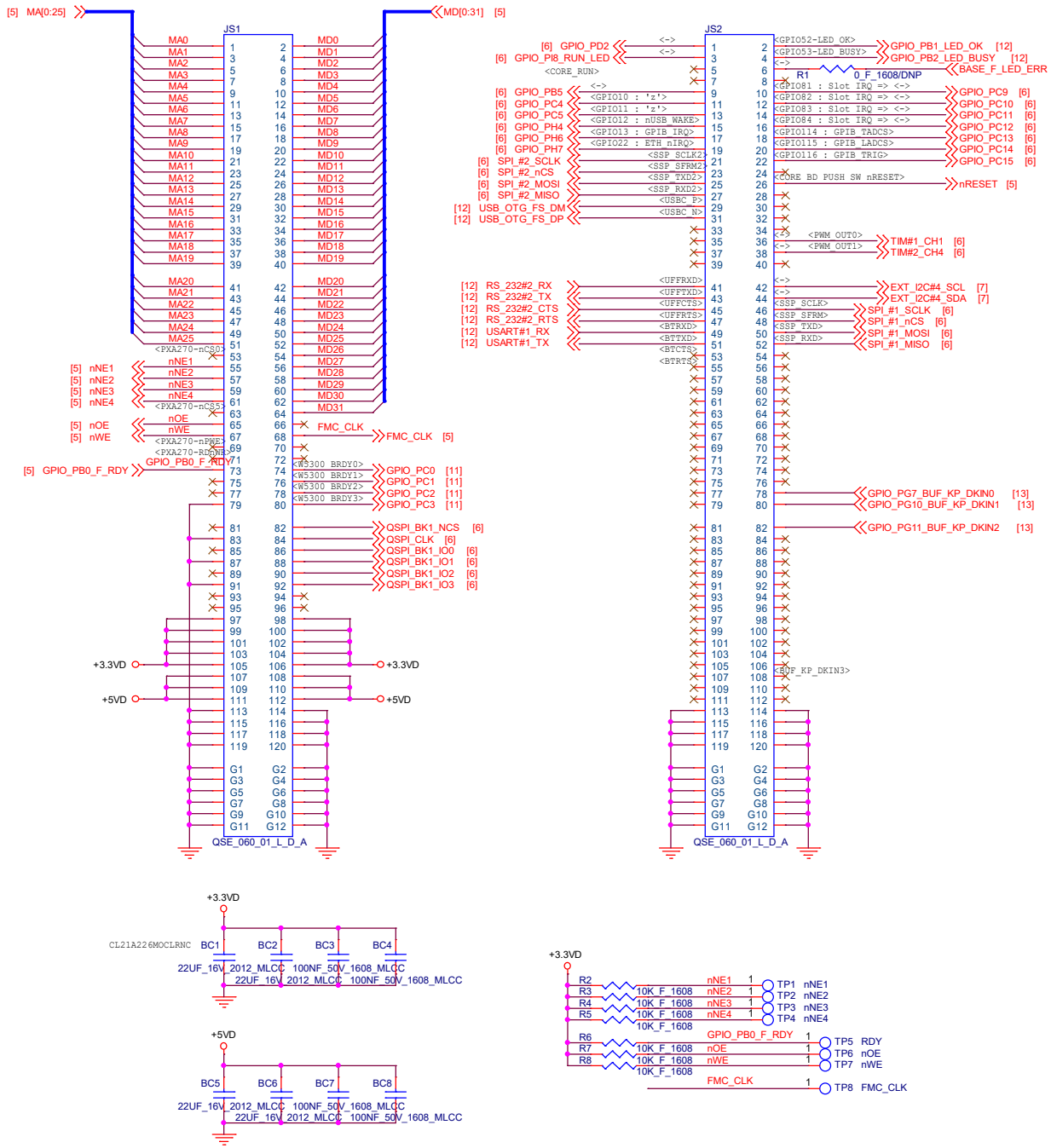
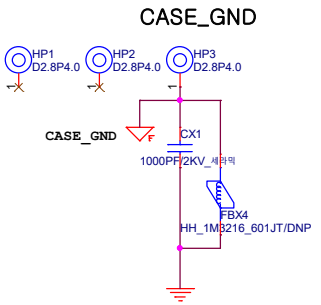
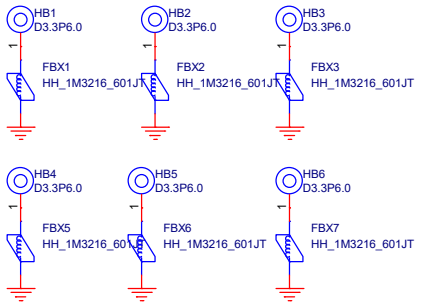
CORE BD (Cortex-M7) CONNECTOR



전면판 고정 홀



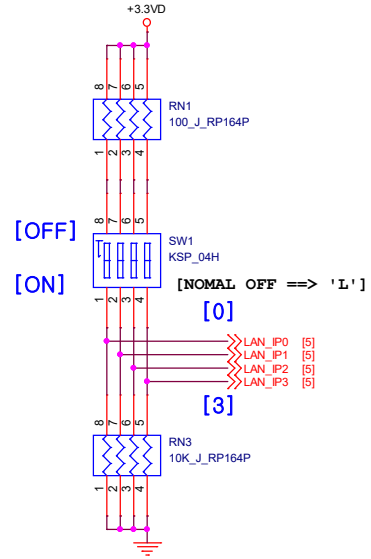
CPU BASE 보드 커버 및 방열판 고정 홀



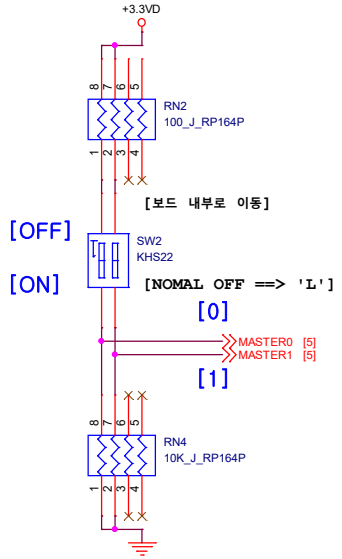
CPU CORE 고정 홀

고정 홀 위치는 LAYOUT 자료 참고!

LAN IP SETTING



MASTER SETTING



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Title:		TEAM			
[S3100] CPU_BASE		TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	03. Core IO & Connector	Seol YK	Seol YK	JOH JH	1.0
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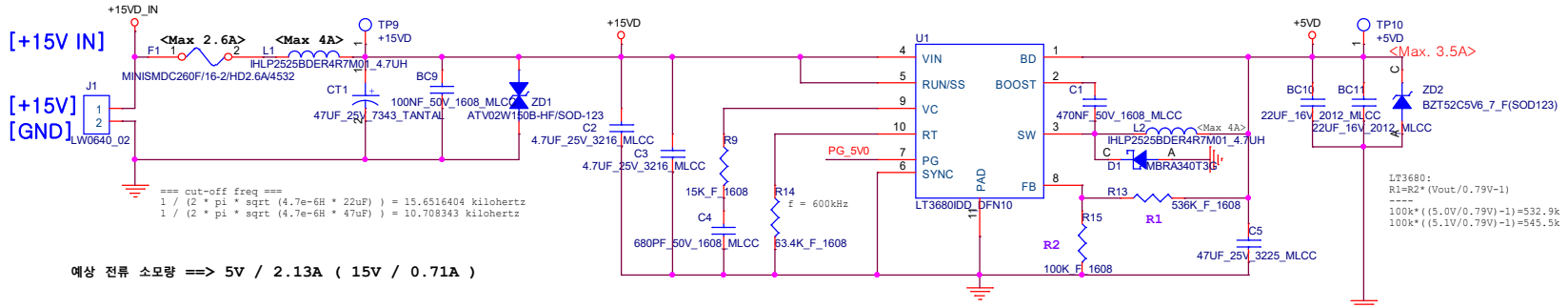
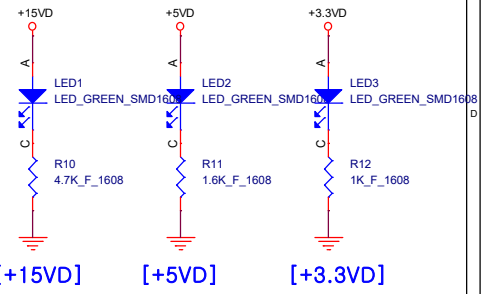
REGURATOR

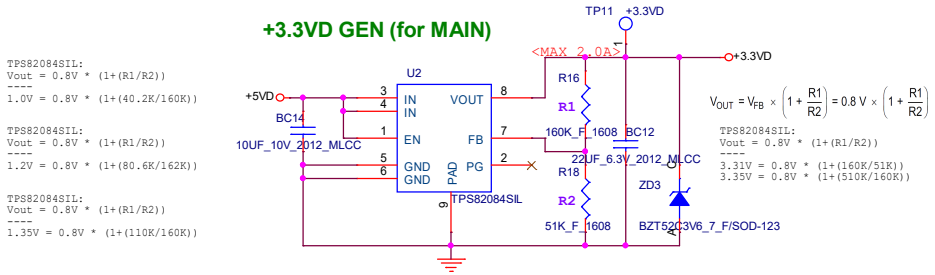


예상 전류 소모량 ==> 5V / 2.13A (15V / 0.71A)

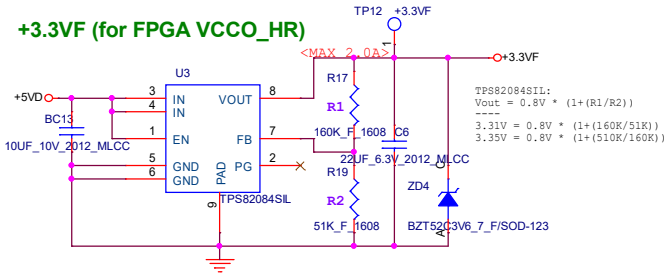
POWER LED & RUN LED

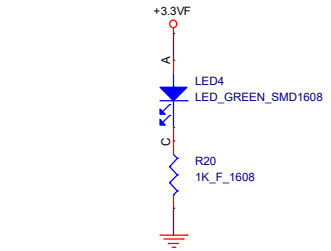


+3.3VD GEN (for MAIN)

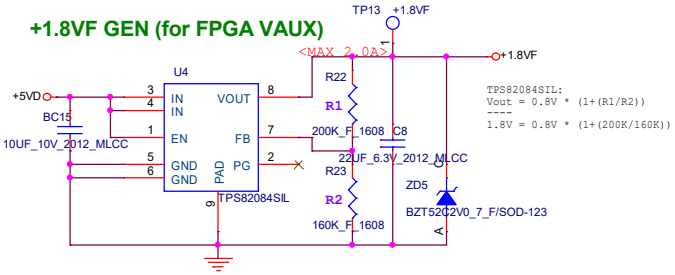


+3.3VF (for FPGA VCCO_HR)

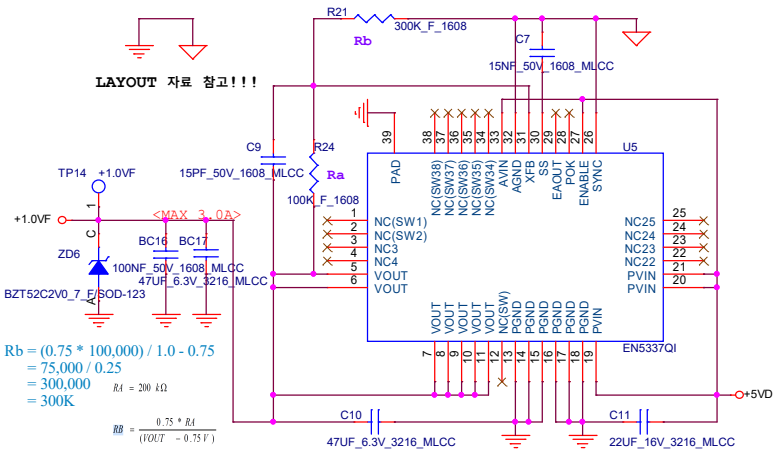


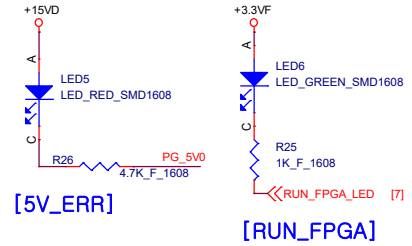


+1.8VF GEN (for FPGA VAUX)



+1.0VF GEN (for FPGA VCCINT)

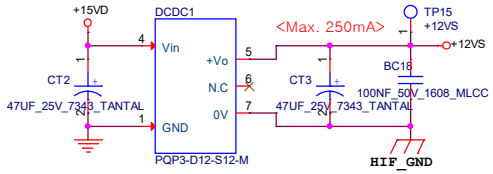




[FPGA Power]
VCCINT = 1.0V
VCCBRAM = 1.0V
VAUX = 1.8V
VAUX_IO = 1.8V
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7에는 없음)
VCCBATT = 1.8V
VCCADC = 1.8V

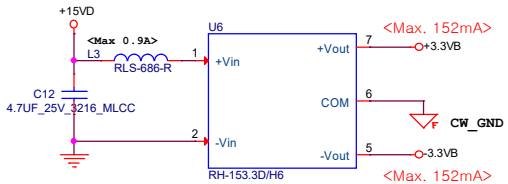
DC/DC

for EXT_CONNECTOR

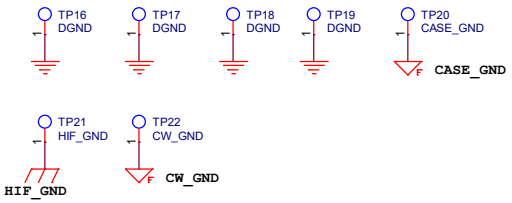


DC/DC

for EXT TRIG CW Signal



TP - GND



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Title: [S3100] CPU_BASE		TEAM TM1			
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A3	04. Power	Seol YK	Seol YK	JOH JH	1.0
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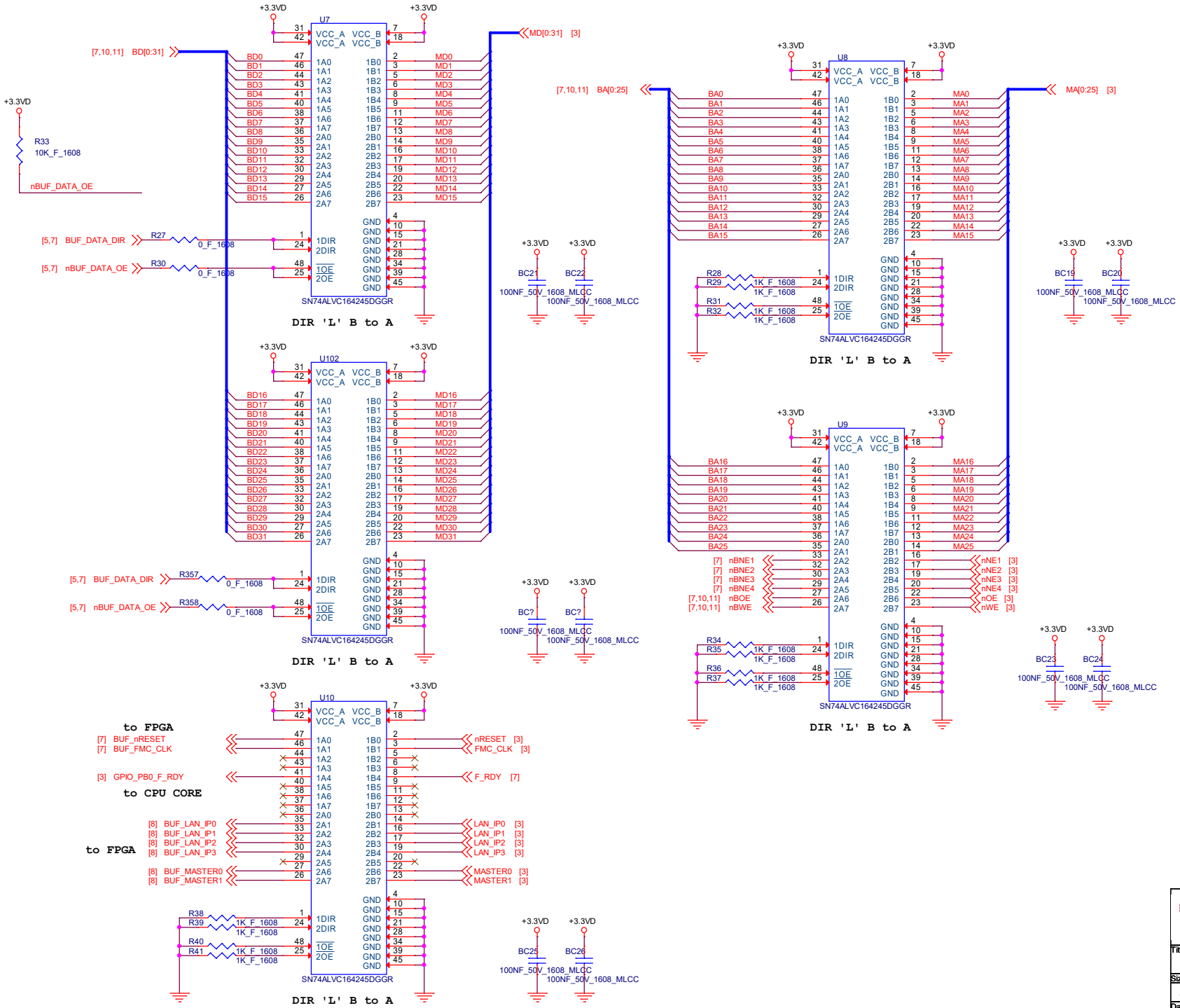
BUFFER

CORE to BASE BD



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Title: [S3100] CPU_BASE		TEAM TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	05. Bus Buffer	Seol YK	Seol YK	JOH JH	1.0
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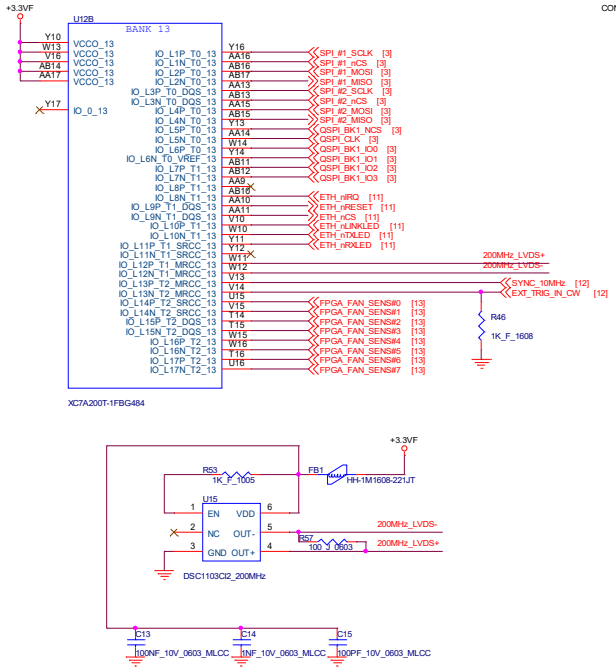
FPGA - BANK 13

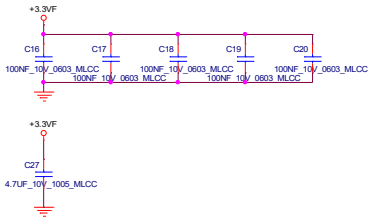
BANK 13 : CORE SPI I/F & QSPI I/F
BANK 13 : BASE W5300 & FAN SENS

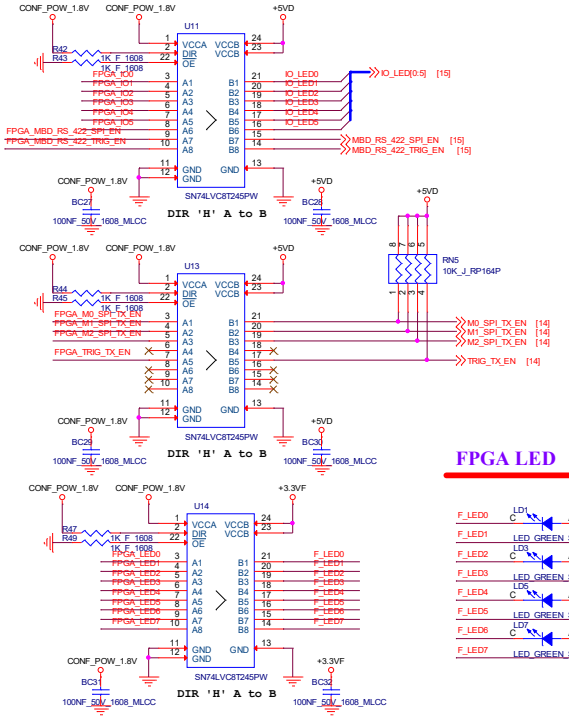


FPGA - BANK 14

BANK 14 : FPGA CONFIG & LED & GPIO

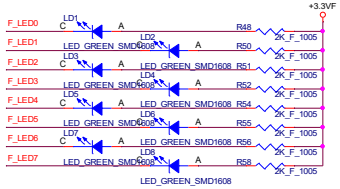
<-> Cortex-M7 에서는 사용하지 않음 (GPIO 목적으로 사용가능)

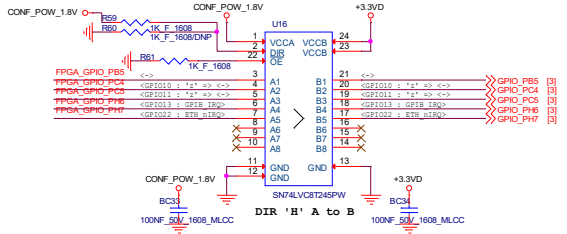


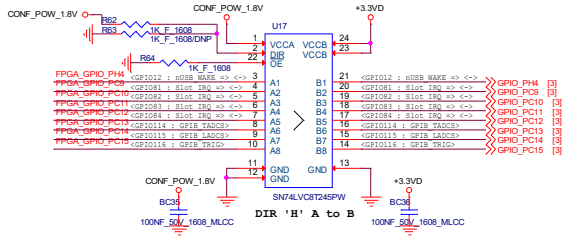


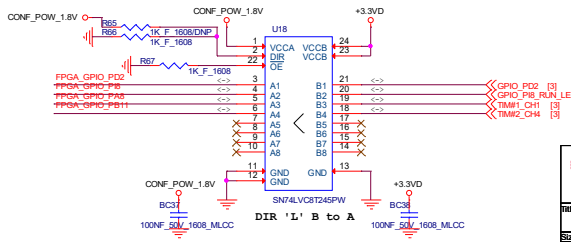
FPGA LED

LED 순서대로 한곳으로 모아주세요









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Title: [S3100] CPU_BASE		TEAM: TM1			
Size: A2	Document Number: 06. FPGA#1	Designed: Seol YK	Checked: Seol YK	Approved: JOH JH	Rev: 1.0
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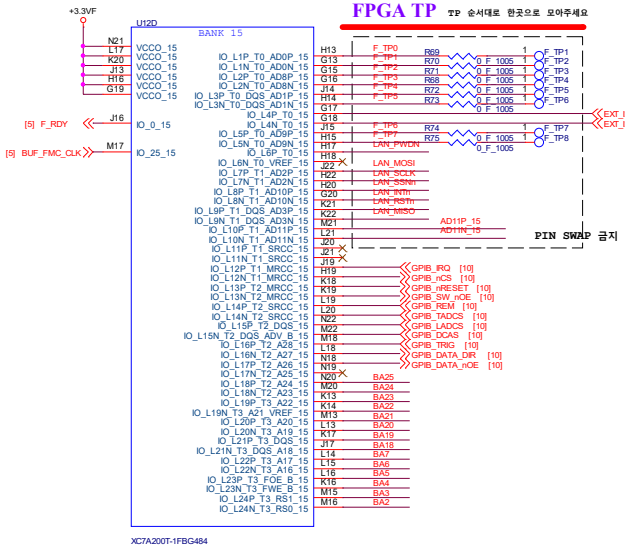
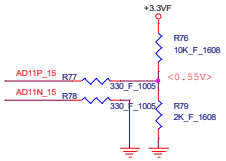
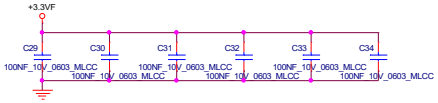
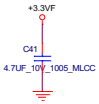
FPGA - BANK 15

BANK 15 : TP & LAN MODULE CONTROL
BANK 15 : H I/F & GPIB I/F



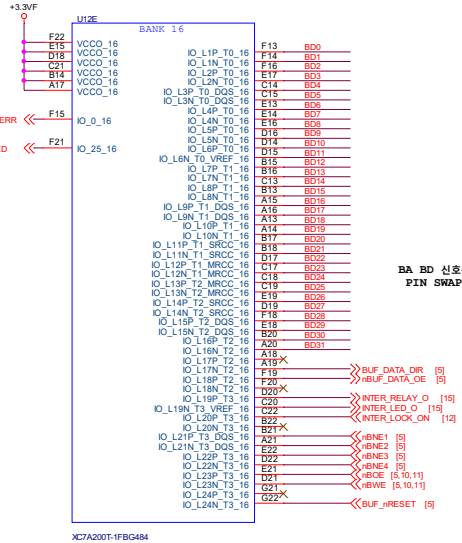


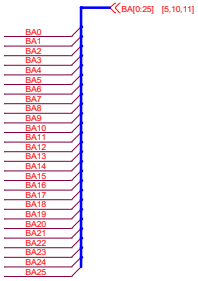


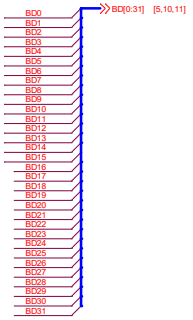


FPGA - BANK 16

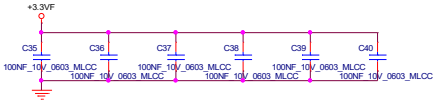
BANK 16 : CORE HOST I/F

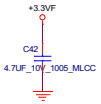




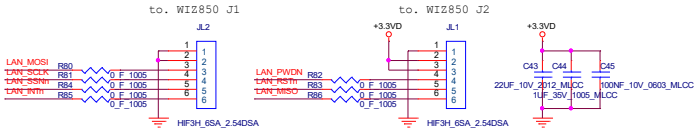


BA BD 신호는 BANK 내에서
PIN SWAP 가능

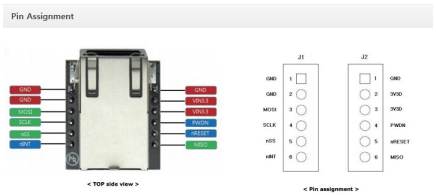




LAN 모듈 Connector



동작방식으로 구동
RST를 제어하여 initialize or re-initialize W5200
또는 INT를 제어하여 INT동작적용



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Title: [S3100] CPU_BASE		TEAM ITM1			
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A2	07. FPGA#2	Seol YK	Seol YK	JOH JH	1.0
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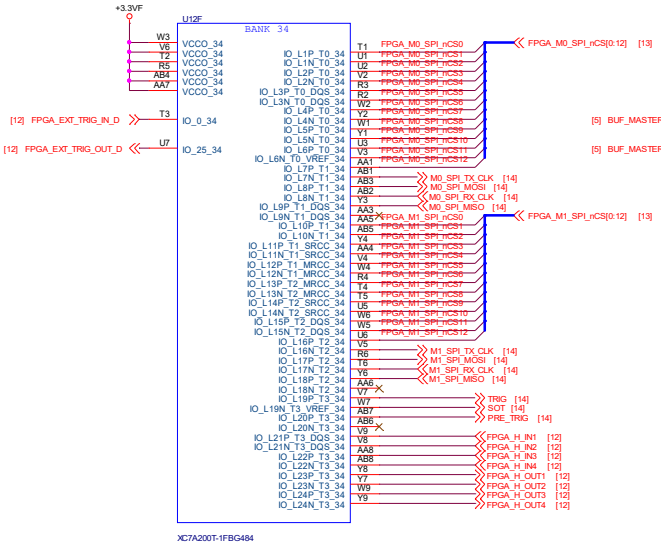
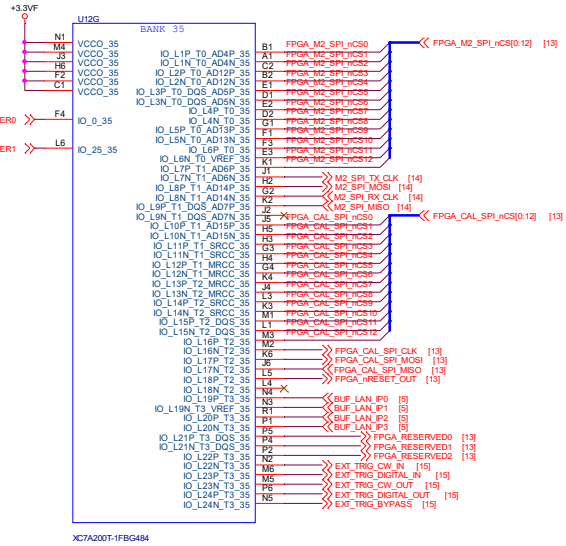
FPGA - BANK 34

BANK 34 : OUT M0 SPI
BANK 34 : OUT M1 SPI



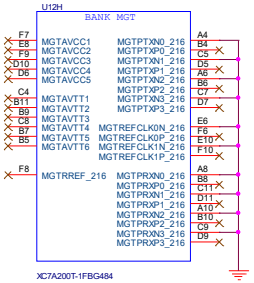
FPGA - BANK 35

BANK 35 : OUT CAL SPI
BANK 35 : OUT M2 SPI

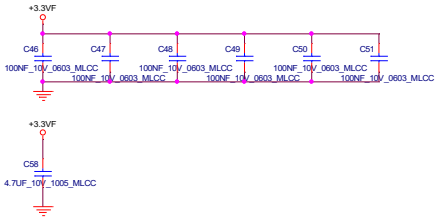


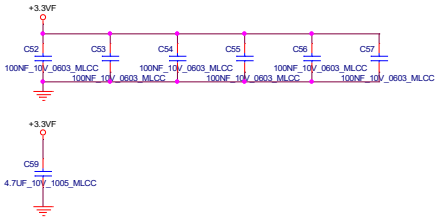
FPGA - BANK 216

BANK 216 : MGT (NOT USED)



[FPGA Power]
MGTAVCC = 1.0V
MGTAVTT = 1.25V





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Title: [S3100] CPU_BASE			TEAM ITM1		
Size	Document Number		Designed	Checked	Approved	Rev
A2	08. FPGA#3		Seol YK	Seol YK	JOH JH	1.0
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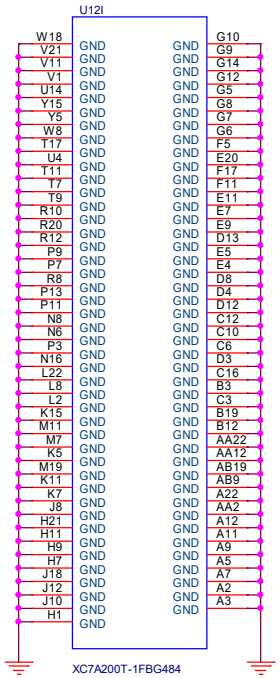
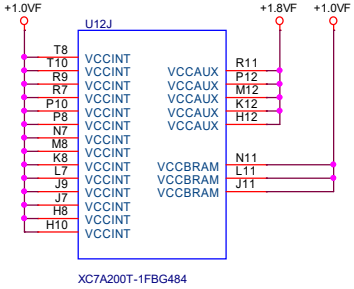
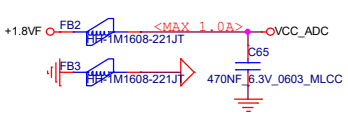
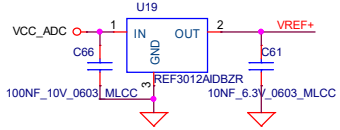
FPGA - POWER

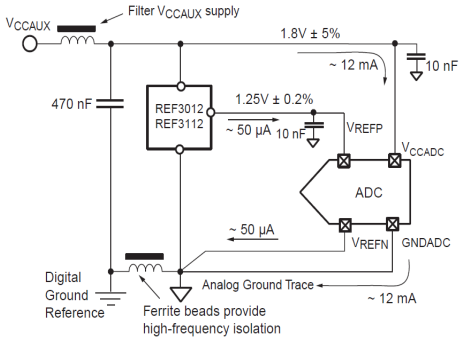


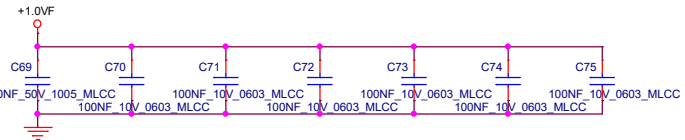


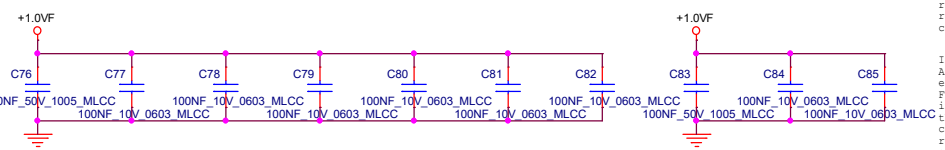
[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7에는 없음)
VCCBATT = -0.5 ~ 2.0V [1.8V]
VCCADC = -0.5 ~ 2.0V [1.8V]

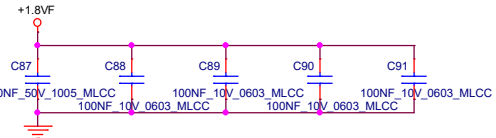


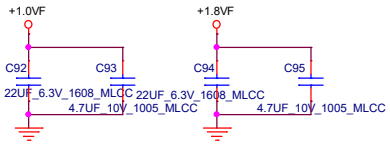


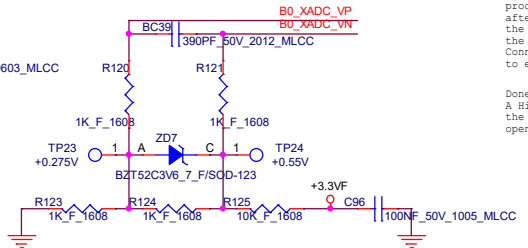










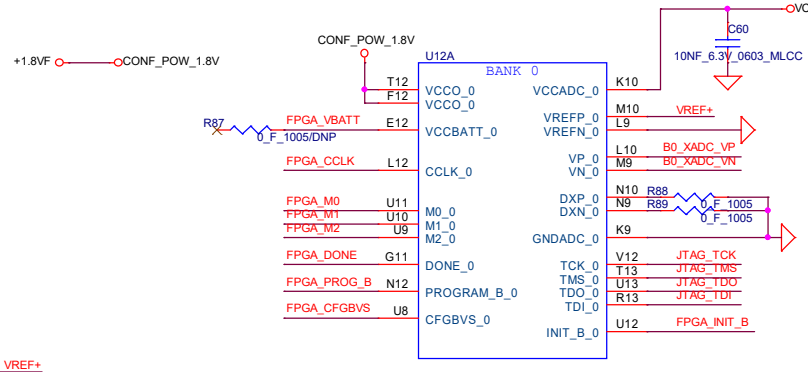


Program (bar)
Active-Low reset to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge.
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.

Initialization (bar)
Active-Low FPGA initialization pin or configuration error signal. The FPGA drives this pin Low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High. INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a High is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M[2:0] pin settings.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

Done
A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

FPGA - Configuration Part



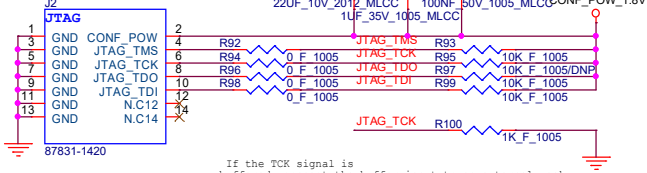
[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7에는 없음)
VCCBATT = -0.5 ~ 2.0V [1.8V]

[FPGA Power]
VCCADC = -0.5 ~ 2.0V [1.8V]
VREF = -0.5 ~ 2.0V [1.25V]
to GNDADC

Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND.

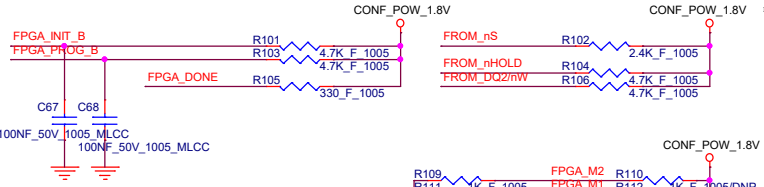
VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

If the VCCO_0 supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High (i.e. connected to VCCO_0). Tie CFGBVS to Low (i.e. connected to GND), only if the VCCO_0 for bank 0 is less than or equal to 1.8V. If used during configuration, banks 14 and 15 should match the VCCO level applied to bank 0



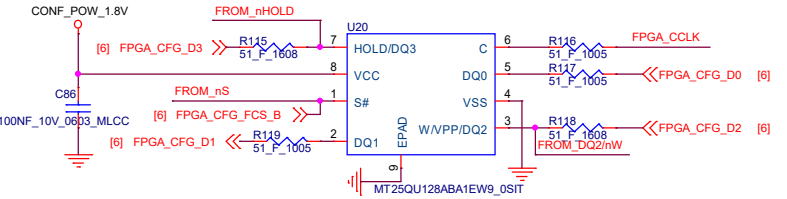
If the TCK signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.

If the TMS signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.



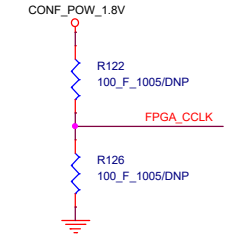
Configuration Mode Sel (M2:0)
- Master SPI: 001
- Master Serial: 000
- JTAG: 101

Pull-Up During Configuration (bar)
Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
> When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
> When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1kΩ to VCCO_14 or GND.
Caution! Do not allow this pin to float before and during configuration



MT25QU256ABA1EW9_0SIT MT25QL = 2.7V ~ 3.6V
MT25QU = 1.7V ~ 2.0V

S25FL128SAGNFI001
S25FL256SAGNFI001



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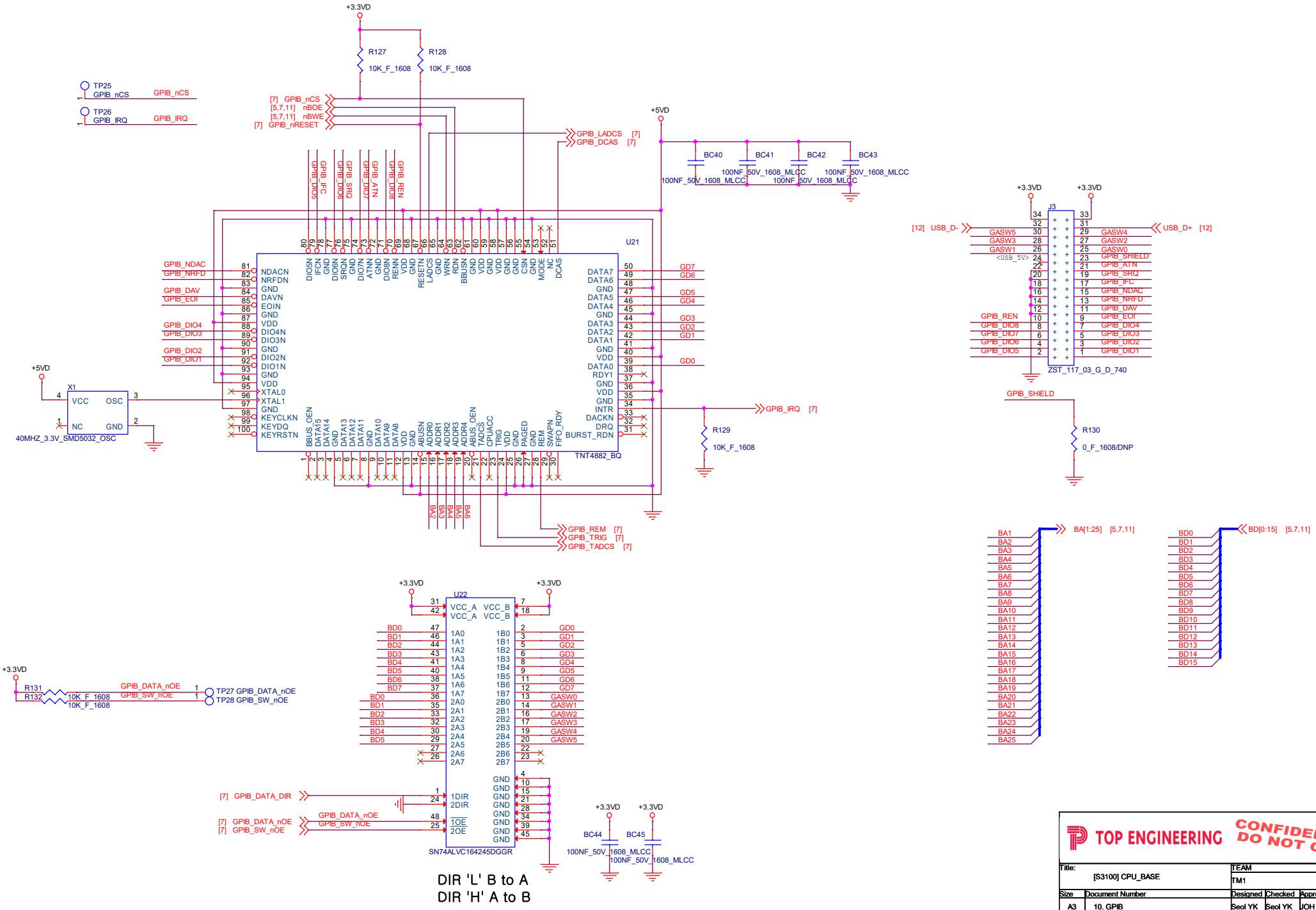
Title:	[S3100] CPU_BASE		TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	09. FPGA#4		Seol YK	Seol YK	JOH JH	1.0
Date:	Thursday, March 25, 2021	Sheet	9	of	15	

GPIB (Option)



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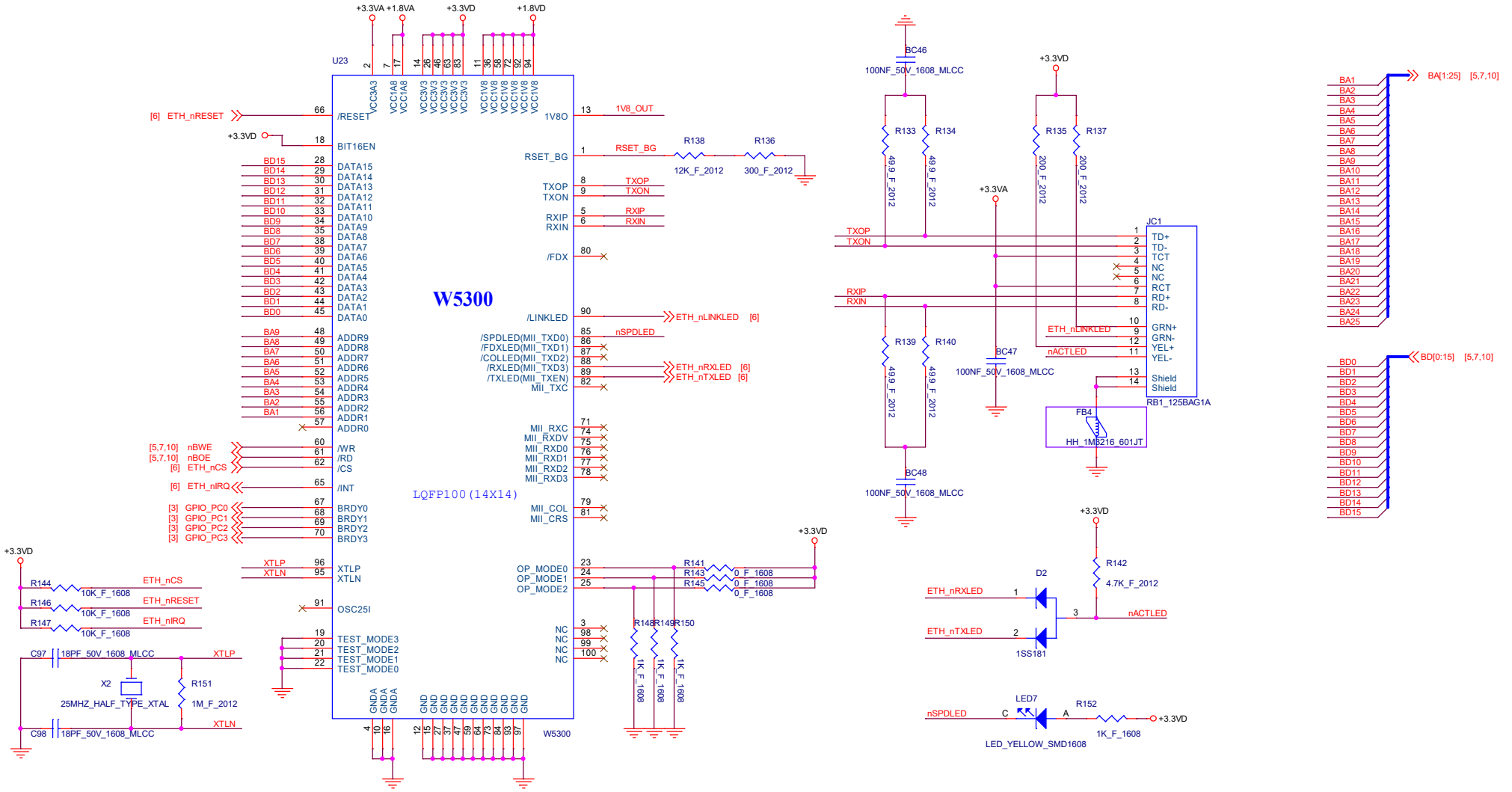
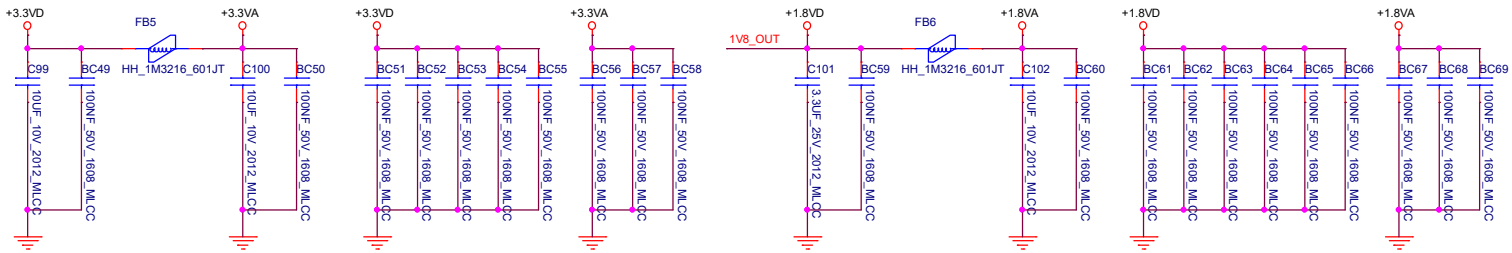
Title: [S3100] CPU_BASE		TEAM TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	10. GPIB	Seol YK	Seol YK	JOH JH	1.0
Date: Thursday, March 25, 2021		Sheet 10 of 15			

LAN I/F





Place FB1, CT4, C58, CT5, C59 as close to each power pin as possible.

Place CT6, C60, FB2 close to +1V8_OUT and place CT7, C61 close to +1.8VA pin.

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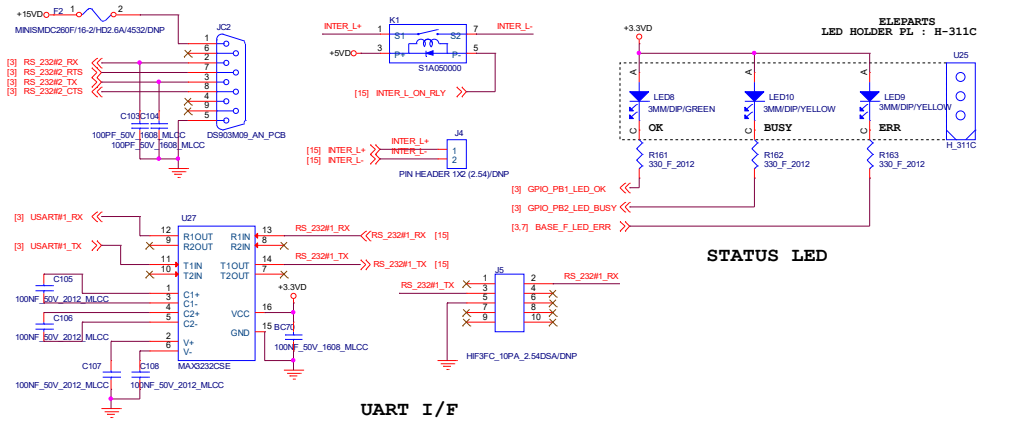
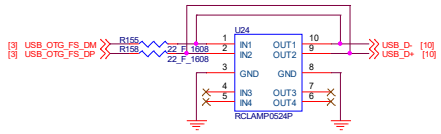
Title: [S3100] CPU_BASE		TEAM TM1			
Size	Document Number	Designed	Checked	Approved	Rev
A3	11. LAN	Seol YK	Seol YK	JOH JH	1.0
Date: Thursday, March 25, 2021		Sheet 11 of 15			

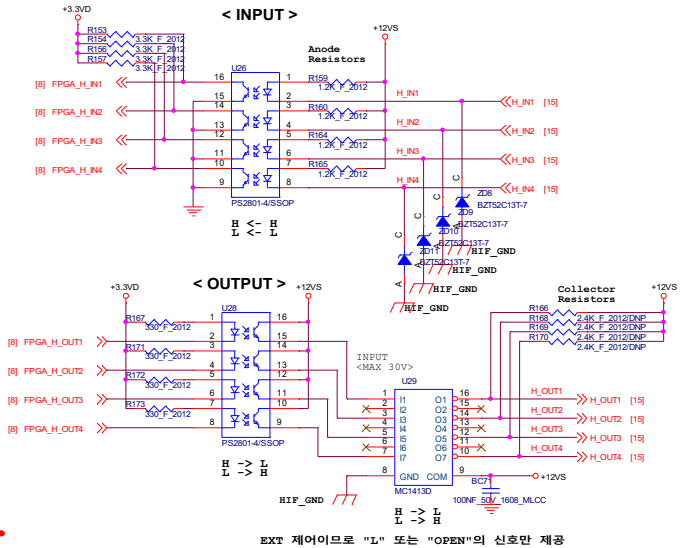
Other I/F



USB

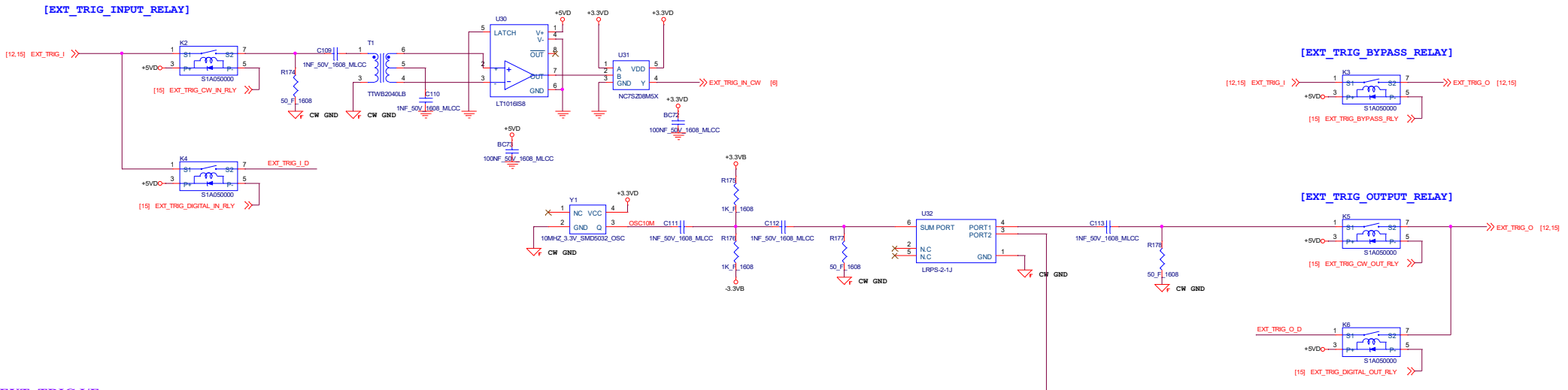


EXT_Handler I/F



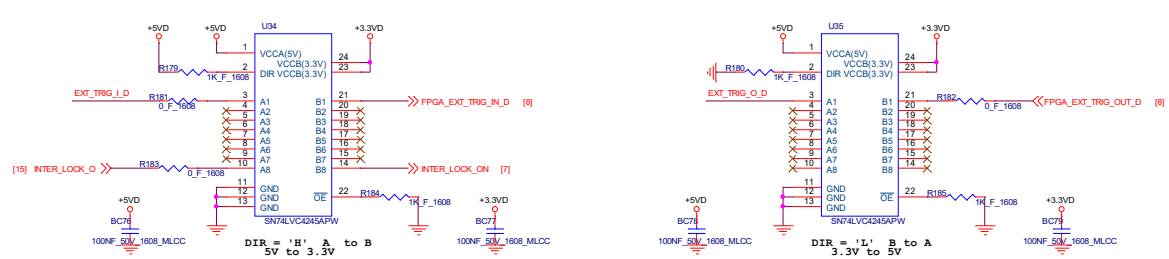
EXT_TRIG I/F

EXT TRIG가 CW Signal 인경우



EXT_TRIG I/F

EXT TRIG가 Digital 5V 인경우



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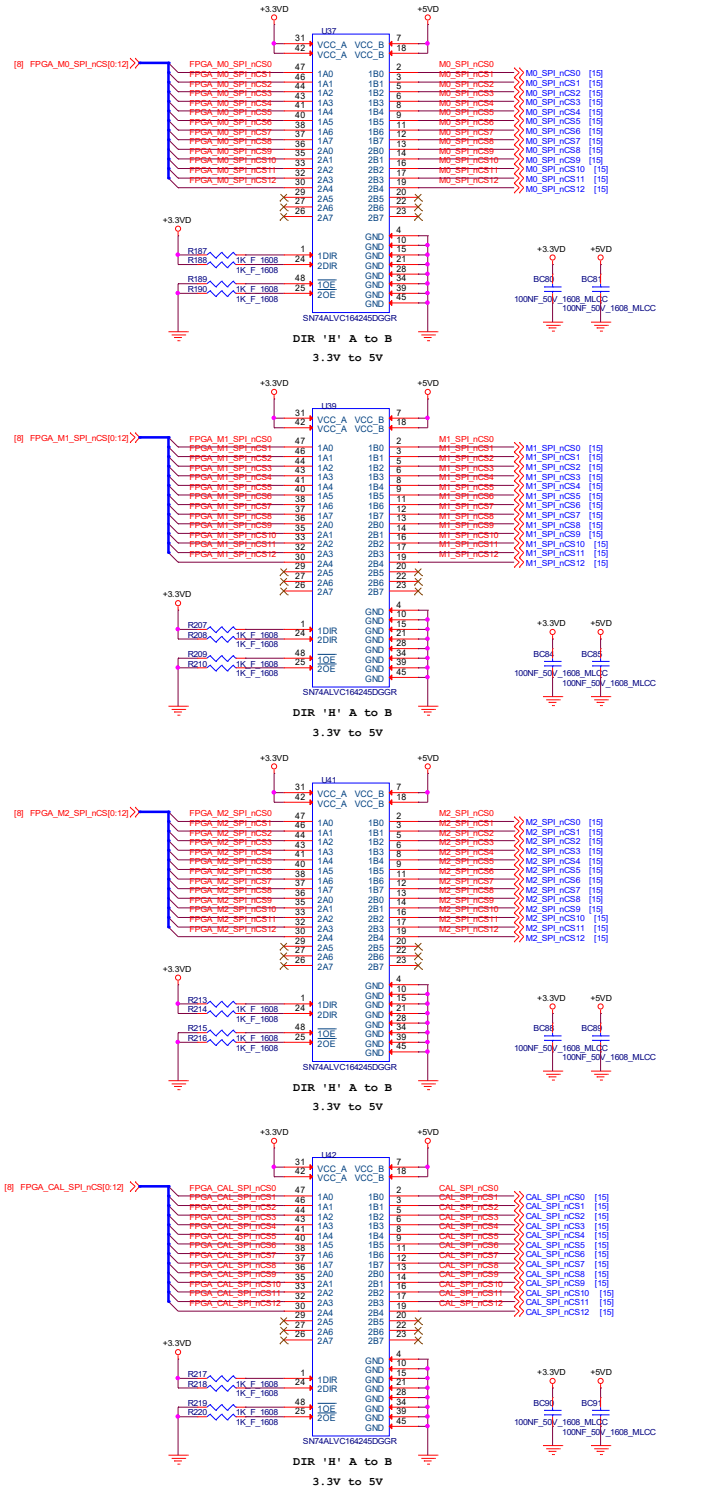
Title: [S3100] CPU_BASE				TEAM ITM1	
Size	Document Number		Designed	Checked	Approved	Rev
A2	12. Peripherals		Seol YK	Seol YK	JOH JH	1.0
Date:	Thursday, March 25, 2021	Sheet	12	of	15	

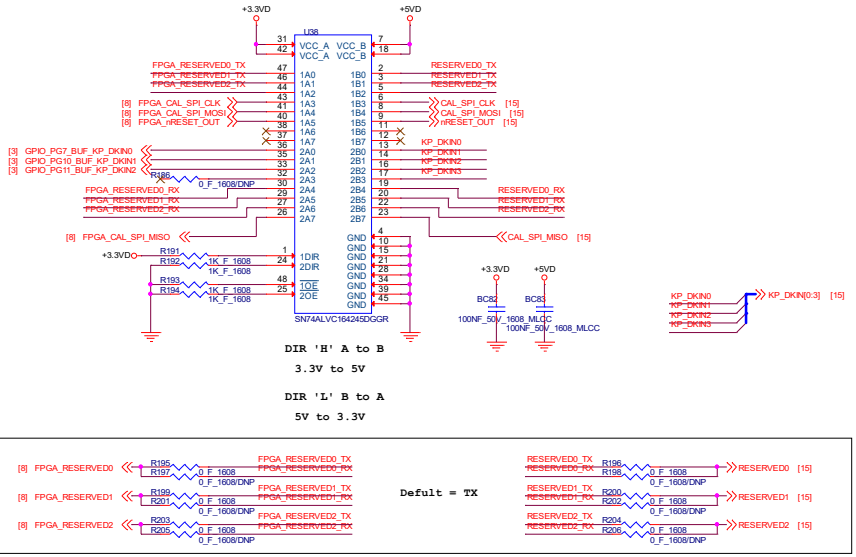
LEVEL SHIFT (CS)

BASE to MOTHER BD



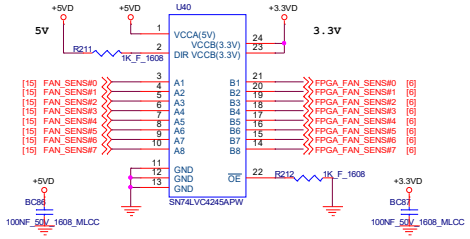
LEVEL SHIFT (LED & KEY) (CAL SPI I/F)

BASE to MOTHER (LED & KEY)



LEVEL SHIFT (RX)

MOTHER to BASE (FAN SENS)



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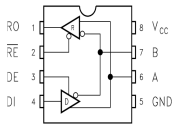
Title: [S3100] CPU_BASE			TEAM ITM1		
Size	Document Number		Designed	Checked	Approved	Rev
A2	13. Backplane Transceiver#1		Seol YK	Seol YK	JOH JH	1.0
Date:	Thursday, March 25, 2021	Sheet	13	of	15	

RS-422 TX

Table 3. Truth table (driver)

Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B	A	A
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal

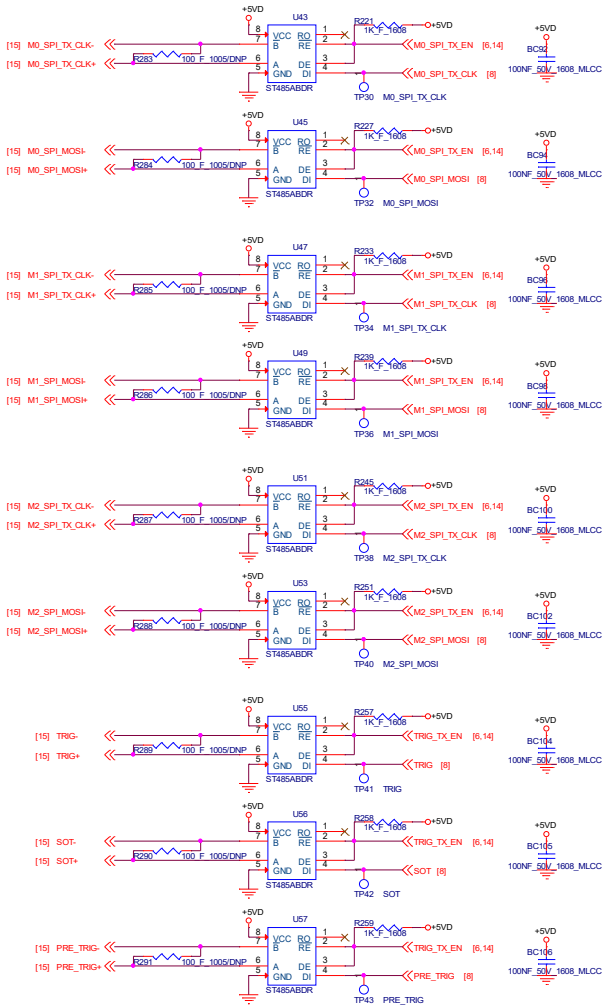
Note: X = Don't care; Z = High impedance

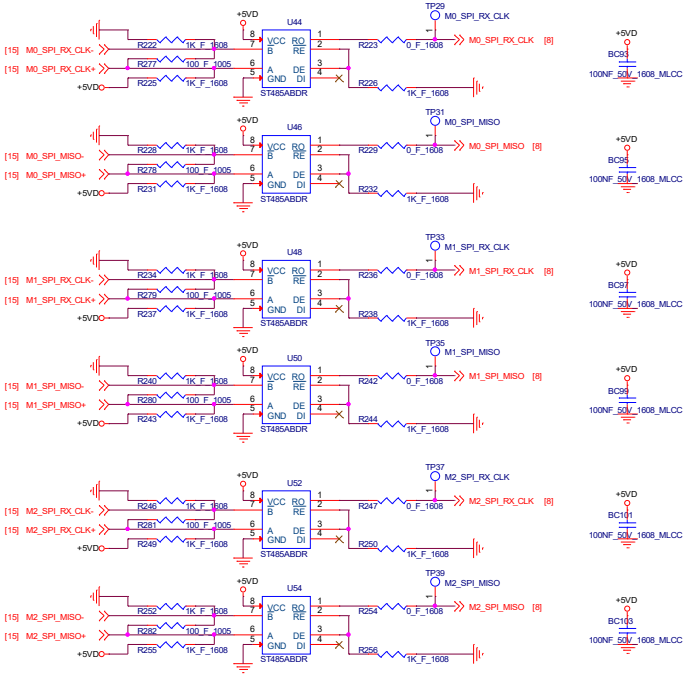


RS-422 RX

Table 4. Truth table (receiver)

Inputs			Outputs	Mode
$\overline{RE}$	DE	A-B	RO	
L	L	≥ -0.2 V	H	Normal
L	L	≤-0.2 V	L	Normal
L	L	Inputs open	H	Normal





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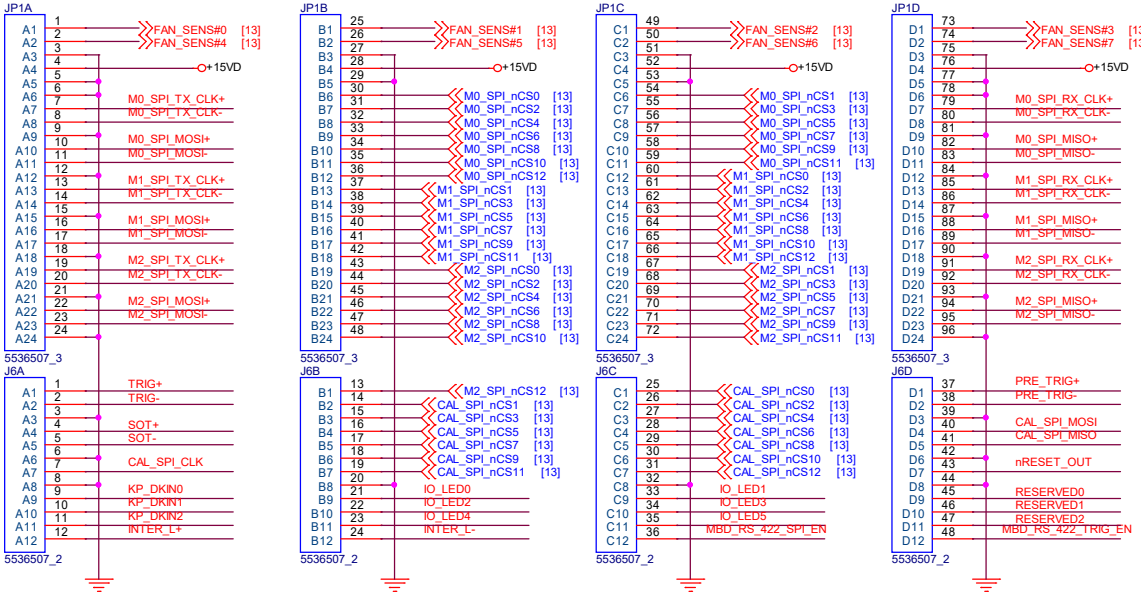
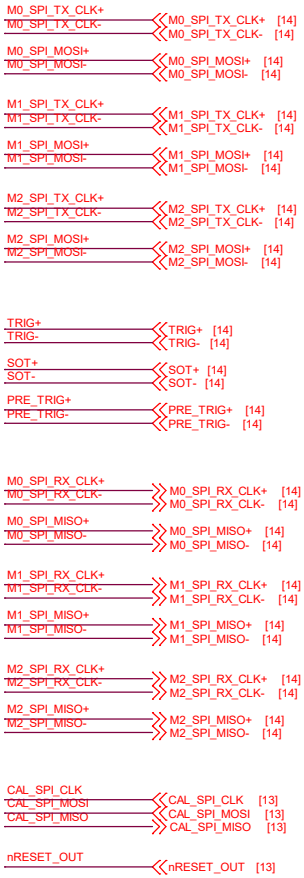
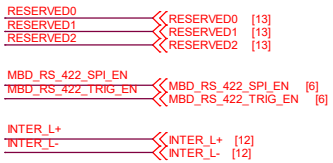
Title: [S3100] CPU_BASE		TEAM ITM1		
Size	Document Number	Designed	Checked	Approved	Rev
A2	14. Backplane Transceiver#2	Seol YK	Seol YK	JOH JH	1.0
Date: Thursday, March 25, 2021		Sheet 14 of 15			

SYSTEM BUS CONNECTOR

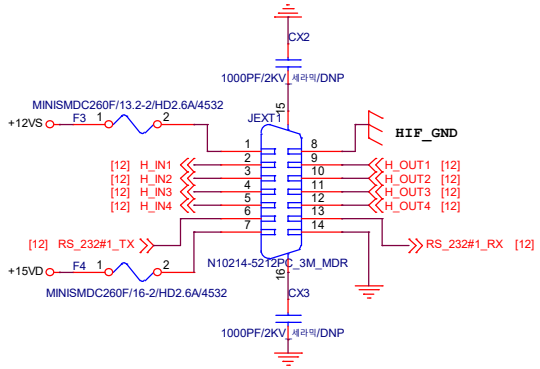




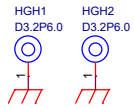


EXT_CONNECTOR

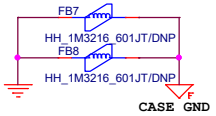
handler



가이드 핀 고정홀

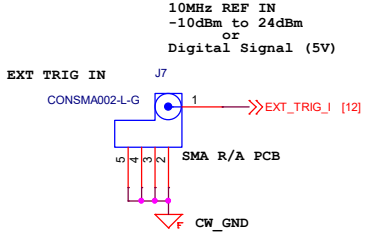


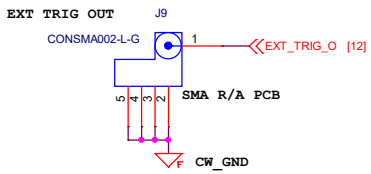
GND



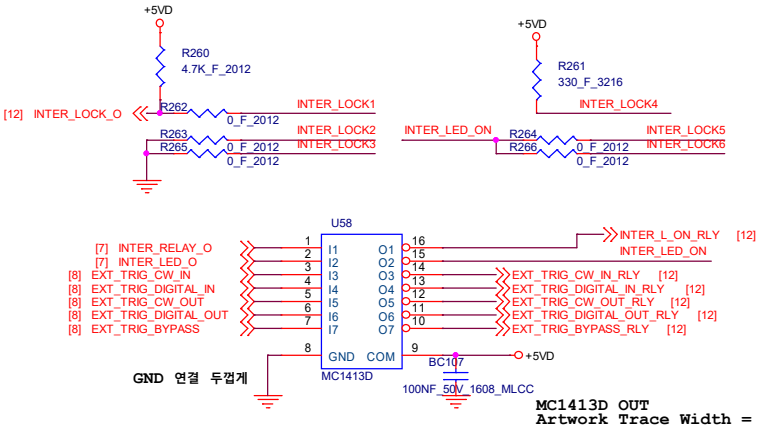
TRIG_CONNECTOR

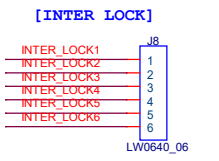
전면판과 접촉안되게끔 설계시 주의!





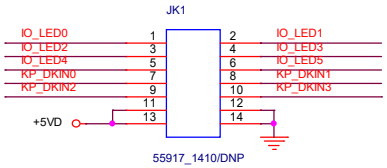
INTERLOCK

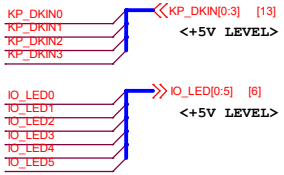




LED and KEY

for LED and KEY





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Title:	[S3100] CPU_BASE		TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	15. Backplane and Sub Connetor		Seol YK	Seol YK	JOH JH	1.0
Date:	Thursday, March 25, 2021	Sheet	15	of	15	