

< High Speed Low Voltage SMU >

Designed By: YK Seul & DH Yoo & SH Yoon

Checked & Approved By: KW Kim

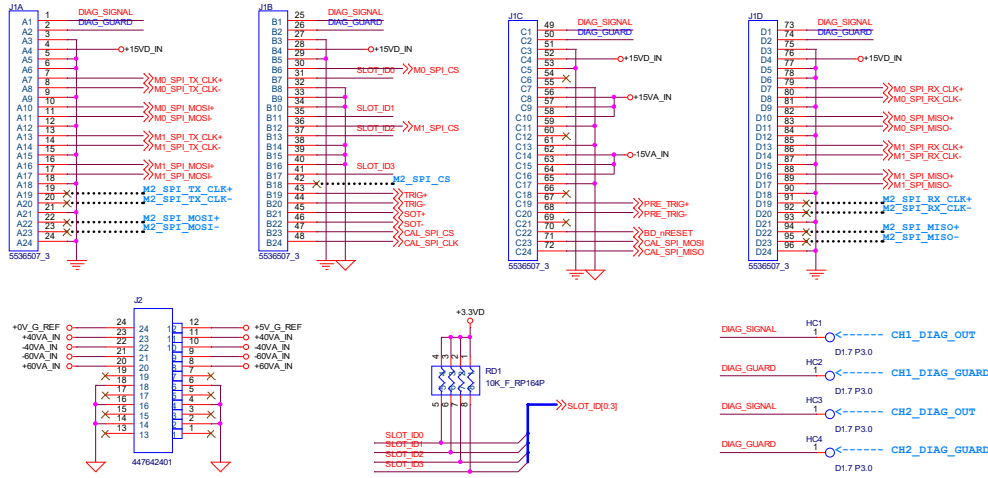
Ver 1.0 : 2021.07.12

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13. ADC and DAC (CH2)
14. ERROR AMP (CH2)
15. POWER AMP (CH2)
16. OUTPUT CONTROL (CH2)
17. OUTPUT (CH2)

<Revision History >

Date	Version	Editor	Revision
2021.07.12	1.0	Y00 DH	24bit Resoultion DAC

INPUT CONNECTOR



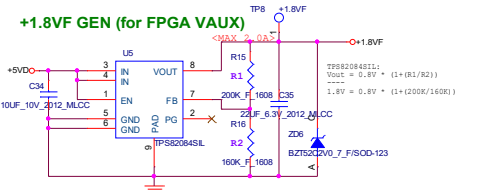
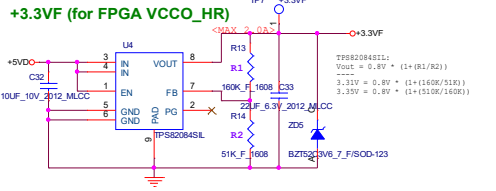
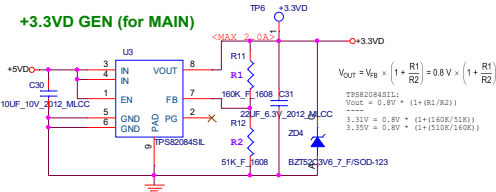
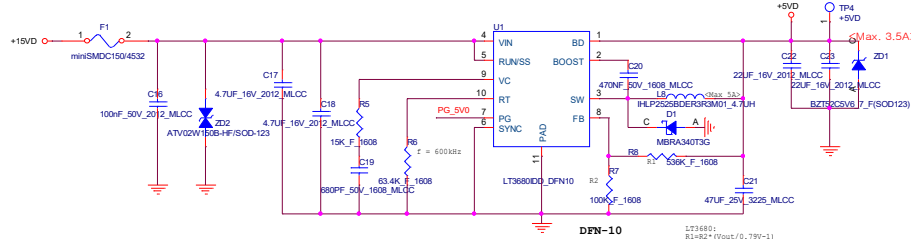
GND 연결



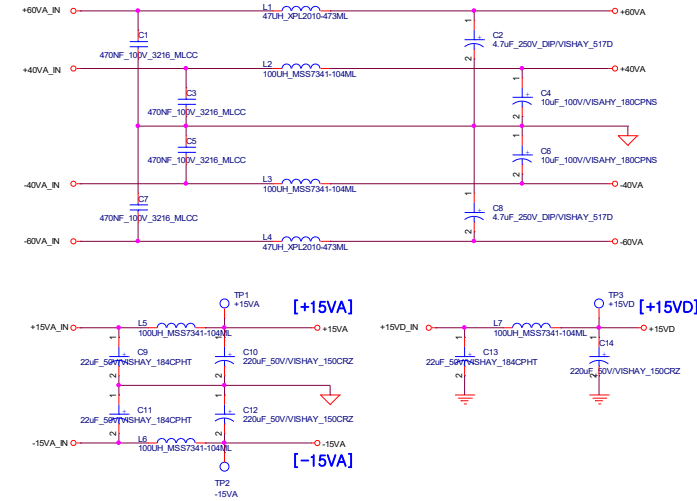
15VD IN



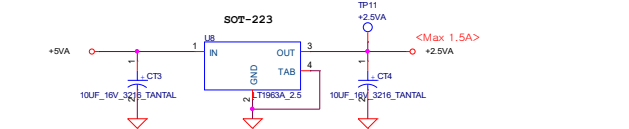
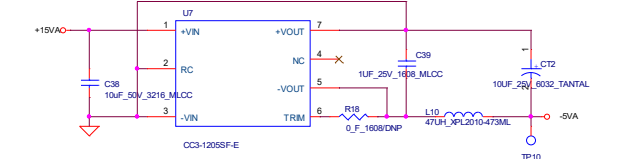
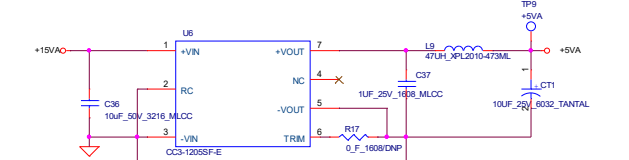
REGULATOR



POWER FILTER



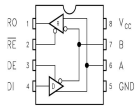
TP - GND



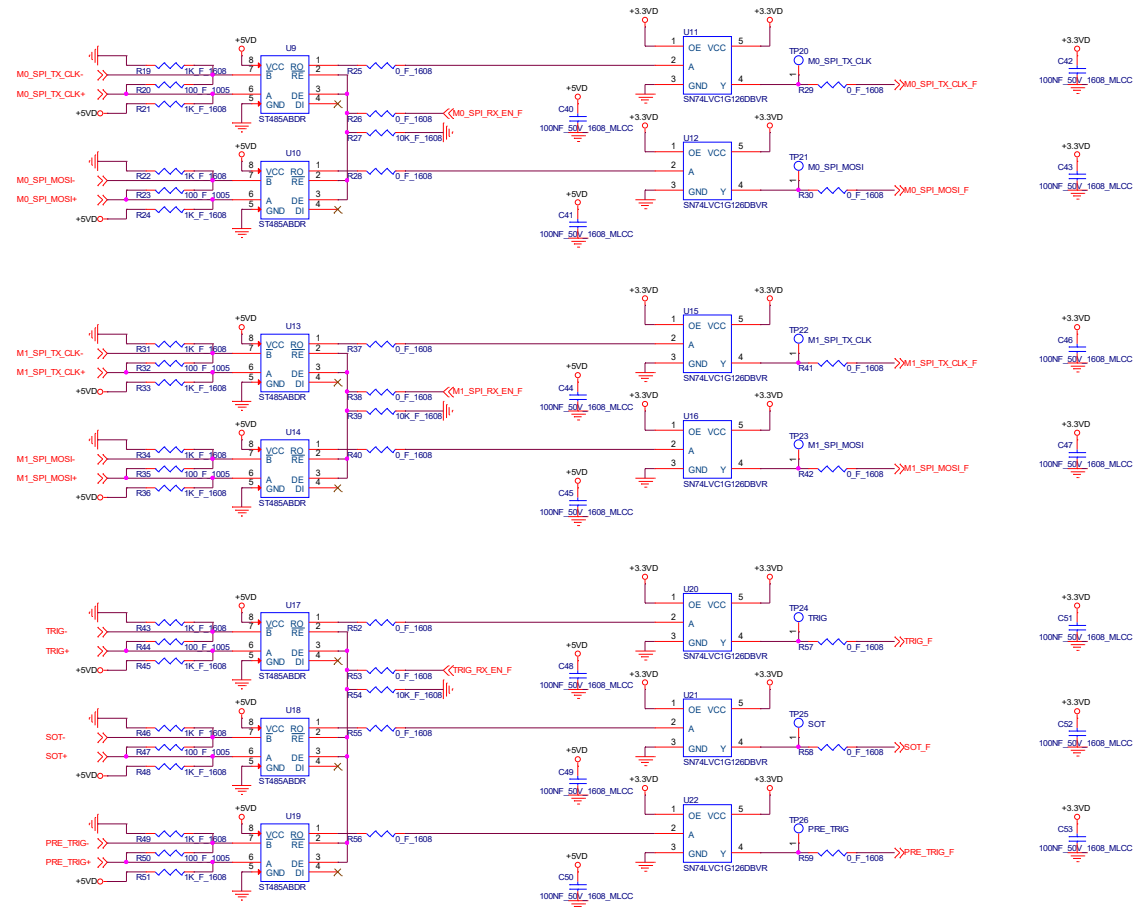
RS-422 RX(1CH)

Table 4. Truth table (receiver)

Inputs			Outputs	Mode
RE	DE	A-B	RO	
L	L	≥ -0.2 V	H	Normal
L	L	≥ 0.2 V	L	Normal
L	L	Inputs open	H	Normal

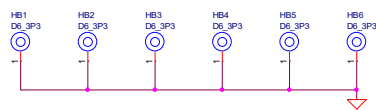


Differential 신호는 패턴 길이 동일하게 적용
터미저항 및 풀업 풀다운 저항은 수신측 근처

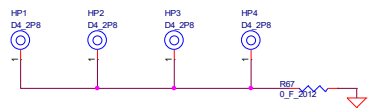


HOLE

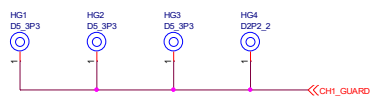
BOARD CASE (D=6, Drill=3.3)



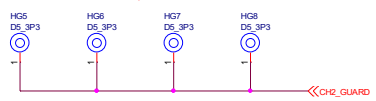
FRONT PANEL (D=4, Drill=2.8)



GUARD CASE (D=5, Drill=3.3)



GUARD CASE (D=5, Drill=3.3)

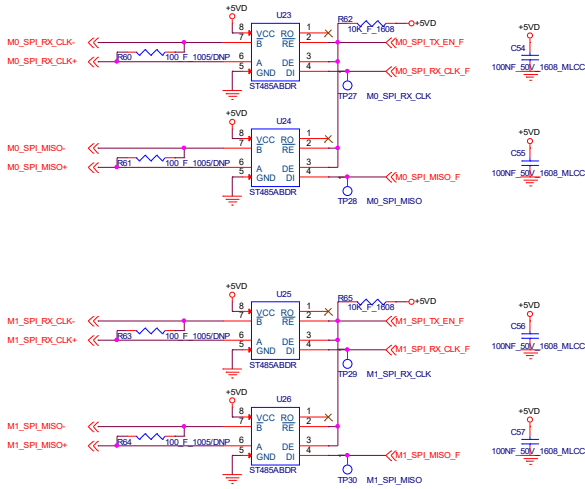


RS-422 TX(1CH)

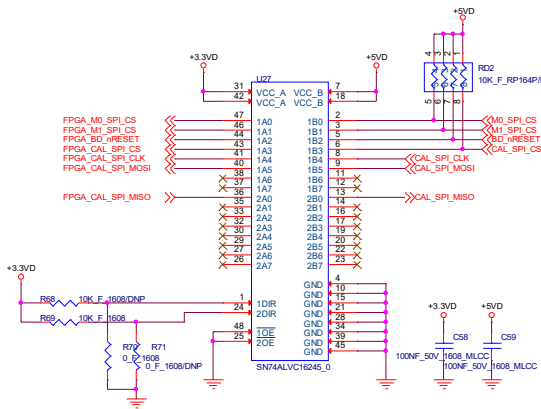
Table 3. Truth table (driver)

Inputs			Outputs		Mode
RE	DE	DI	B	A	
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal

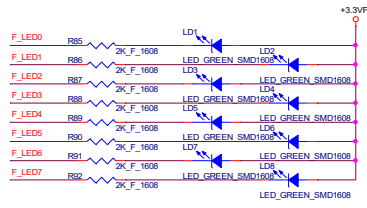
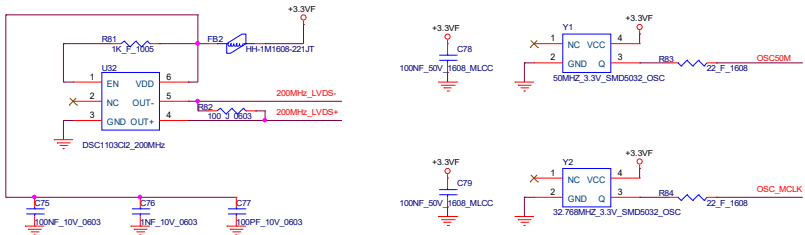
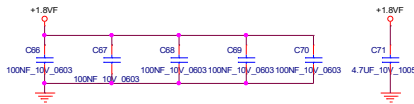
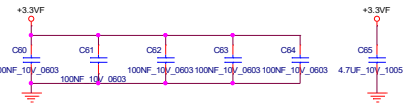
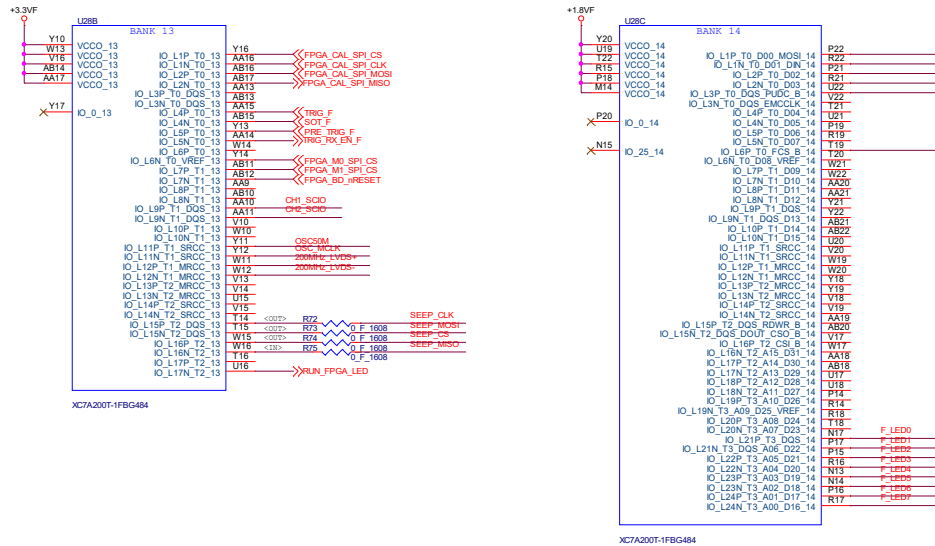
Note: X = Don't care; Z = High impedance



SIGNAL RX (5V to 3.3V)(1CH)

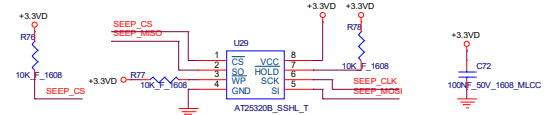


FPGA IO

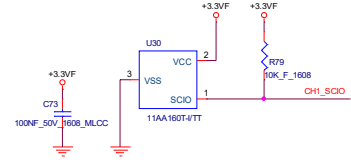


SPI EEPROM

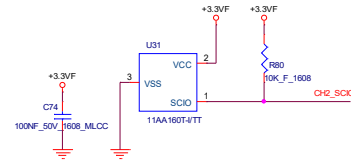
Calibration DATA 저장용 Serial EEPROM



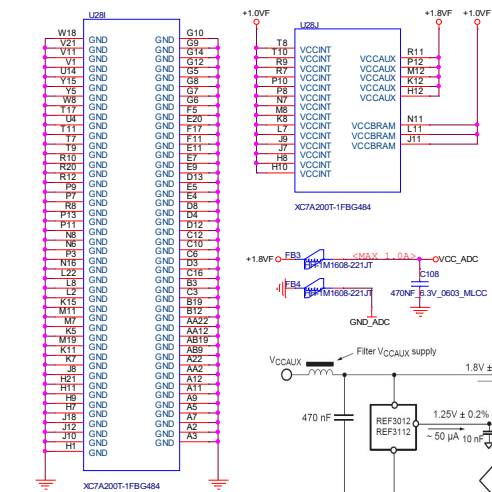
EEPROM 16K 2048X8 1.8V SERIAL EE IND(CH1)



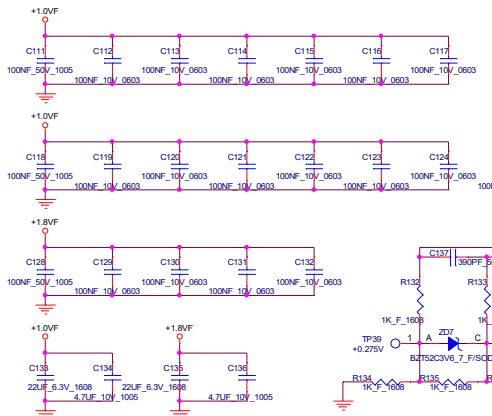
EEPROM 16K 2048X8 1.8V SERIAL EE IND(CH2)



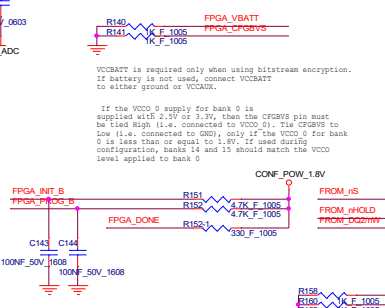
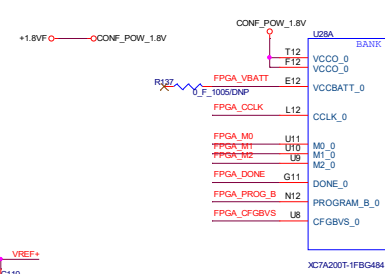
FPGA - POWER



[FPGA Power]
VCCINT = -0.5 ~ 1.1 [1.0V]
VCCBRAM = -0.5 ~ 1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCIO = -0.5 ~ 2.0V [1.8V]
VCCIO HP = 1.14 ~ 1.89V (Arria7는 88)
VCCBATT = -0.5 ~ 2.0V [1.8V]
VCCADC = -0.5 ~ 2.0V [1.8V]



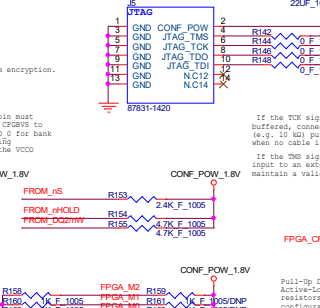
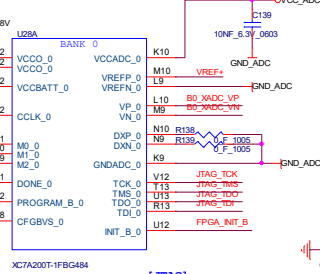
FPGA - Configuration Part



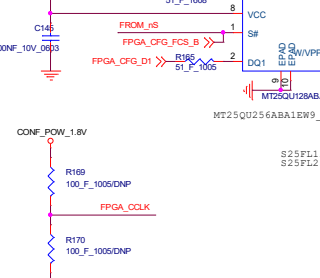
Program (bar)
Active-low reset to configuration logic. When PROGRAM_B is pulled low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e., programming) sequence begins upon the following rising edge.
Connect PROGRAM_B to an external 5 ~ 7 kΩ pull-up resistor to VCCIO_0 to ensure a stable high input, and recommend push-button to GND to enable manual configuration reset.

Initialization (bar)
Active-low FPGA initialization pin or configuration error signal. The PDSB drives this pin low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-2 at which time an external resistor is expected to pull INIT_B high. INIT_B can externally be held low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a high is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M2(10) pin settings.
Connect INIT_B to a 5 ~ 7 kΩ pull-up resistor to VCCIO_0 to ensure clean low-to-high transitions.

Done
A high signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.



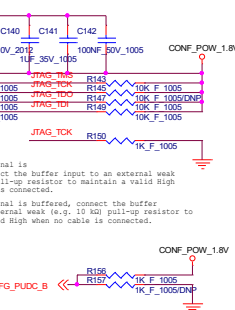
Configuration Mode Sel (M2:0)
- Master SPI: 001
- JTAG: 101



[FPGA Power]
VCCINT = -0.5 ~ 1.1 [1.0V]
VCCBRAM = -0.5 ~ 1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCIO = -0.5 ~ 2.0V [1.8V]
VCCIO HP = 1.14 ~ 1.89V (Arria7는 88)
VCCBATT = -0.5 ~ 2.0V [1.8V]

[FPGA Power]
VCCADC = -0.5 ~ 2.0V [1.8V]
VREF = -0.5 ~ 2.0V [1.25V]
to GNDADC

Temperature-sensing diode pins (Anode: D0P; Cathode: D0N). The thermal diode is accessed by using the D0P and D0N pins in bank 0. When not used, tie to GND.



Pull-Up During Configuration (bar)
Active-low PDSB input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
> When PDSB is Low, internal pull-up resistors are enabled on each SelectIO pin.
> When PDSB is High, internal pull-up resistors are disabled on each SelectIO pin.
PDSB must be tied either directly, or via a 5 kΩ to VCCIO_0 or GND.
Caution! Do not allow this pin to float before and during configuration

MT25QU128ABA1EW9_OSIT MT25QL = 2.7V ~ 3.6V
MT25QU = 1.7V ~ 2.0V

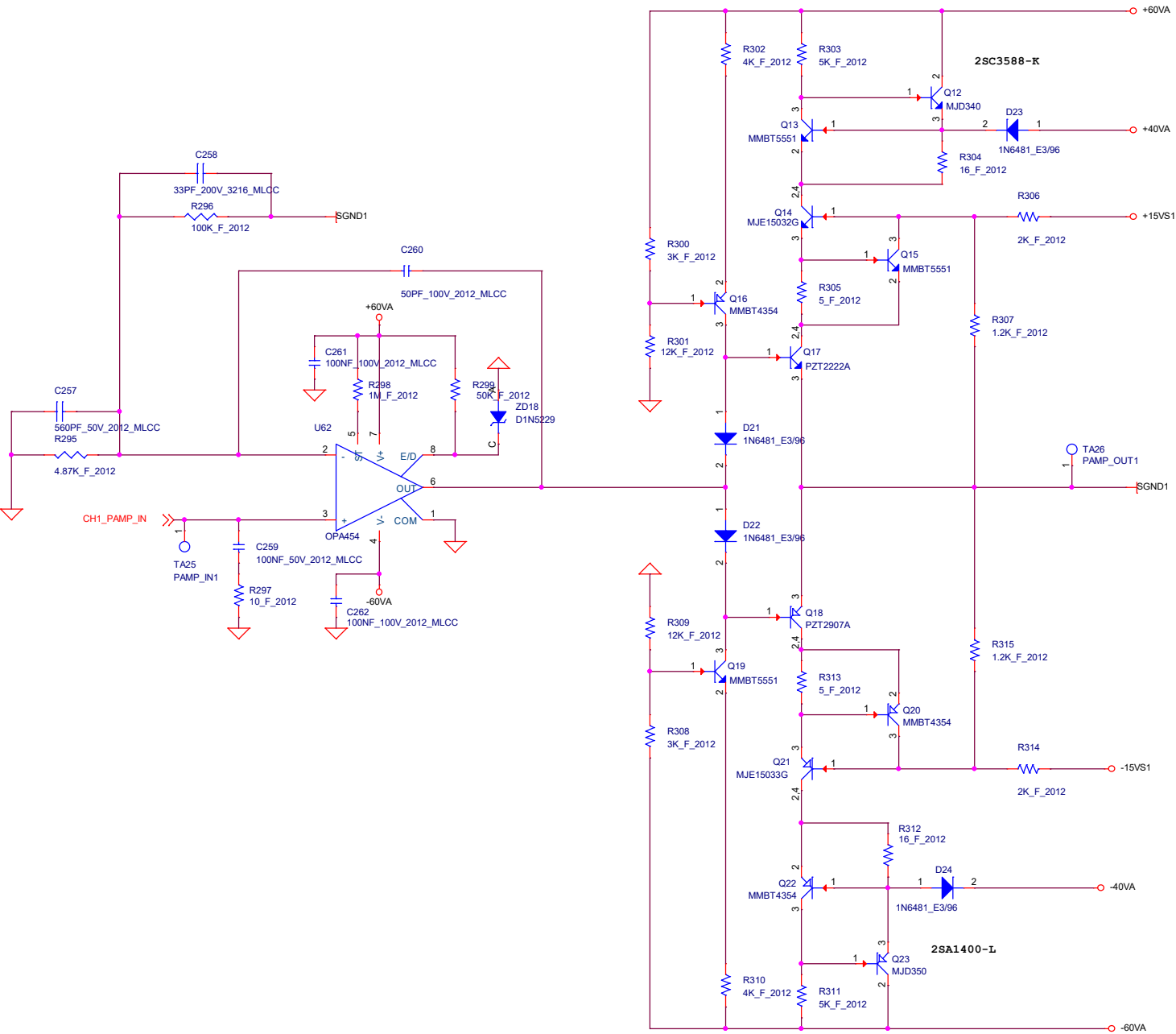
S25FL128AGNFI1001
S25FL256AGNFI1001


Daten(Min.) for 15V/1
10kohn(Max.) for 1.3..7V/5

The schematic diagram illustrates the LTC6945 based 100MHz clock divider circuit. It features an LTC6945-24 clock divider, an LTC4245 level shifter, and an LTC1062-24 DAC. The circuit is powered by a 1.5V supply and includes various passive components like resistors and capacitors for impedance matching and signal conditioning. The output is a 100MHz clock divider output.

[illegible]

POWER AMP

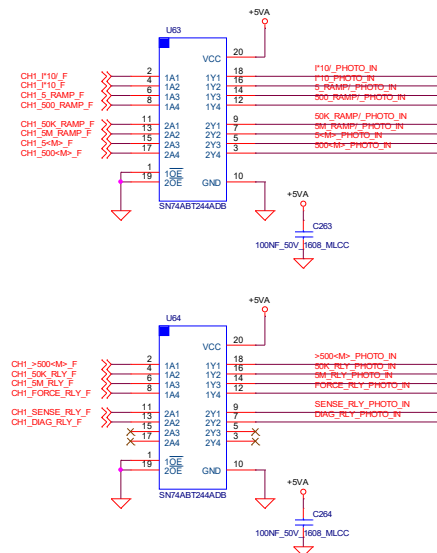


**TOP ENGINEERING**

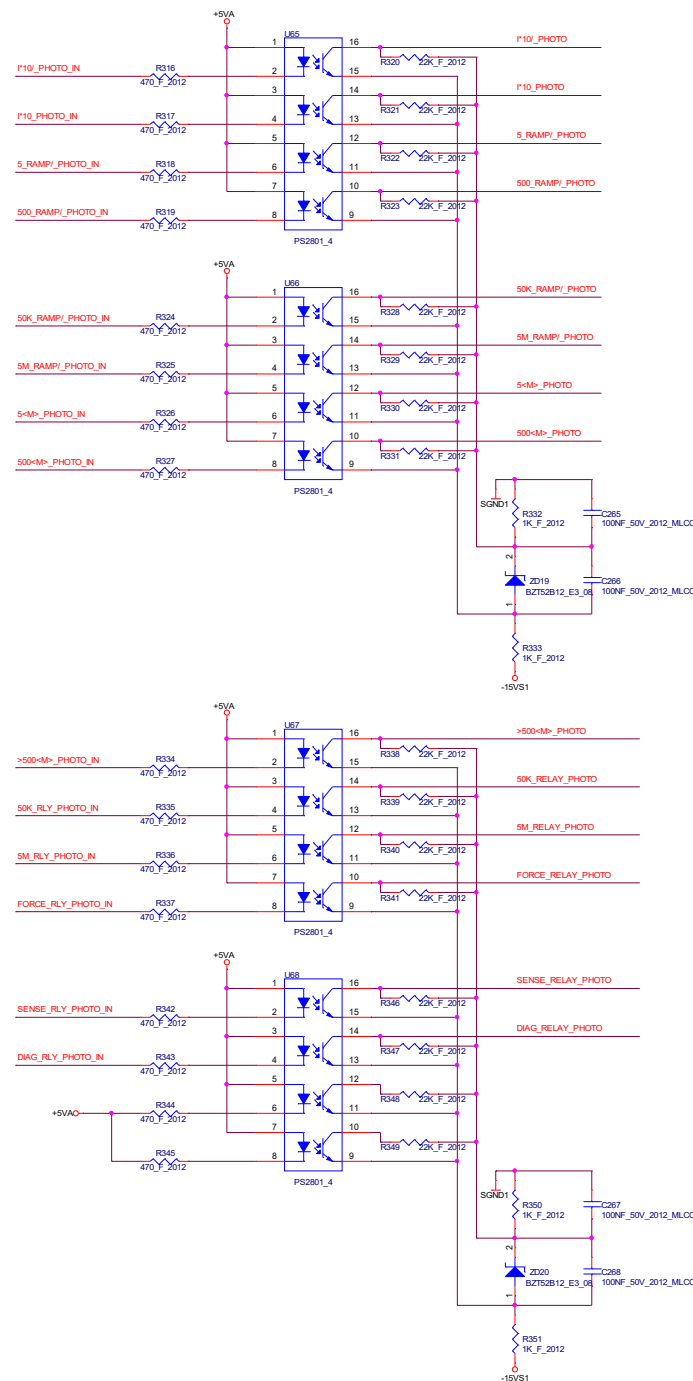
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Title: High Speed & Low Voltage SMU		TEAM			
Size: A3		TM: 10/10			
Document Number	10. POWER AMP (CH1)	Designed	Checked	Approved	Rev
Date: Tuesday, July 27, 2021		DH YOO	Seol YK	DH YOO	1.0
Sheet		10 of 17			

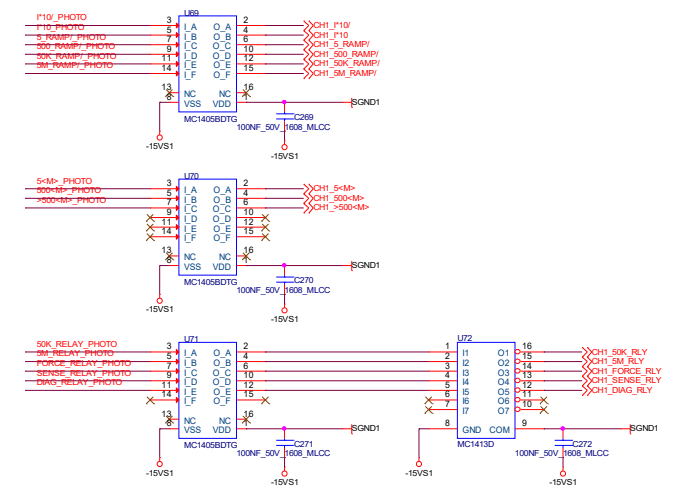
CONTROL SIGNAL BUFFER

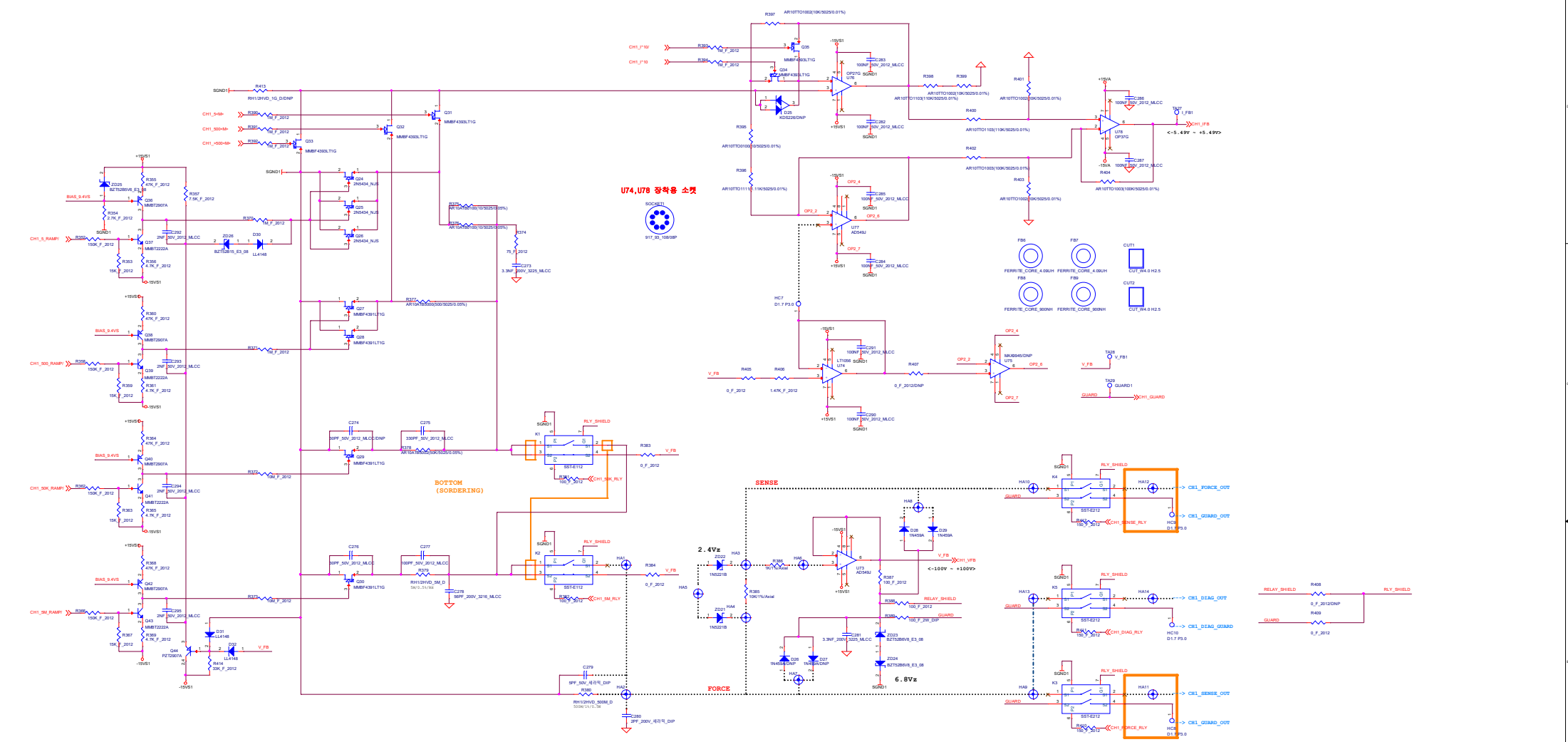


SIGNAL ISOLATE

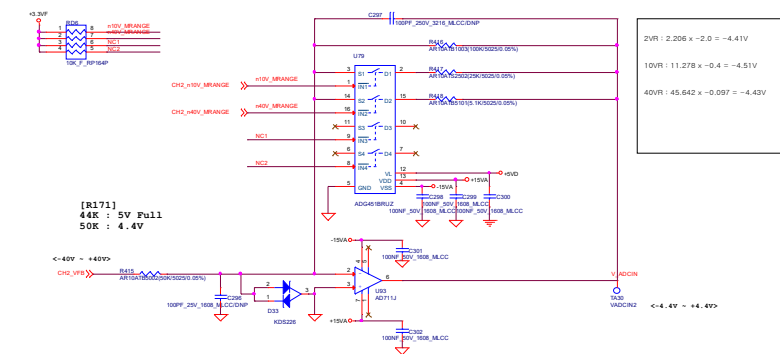


I RANGE CONTROL

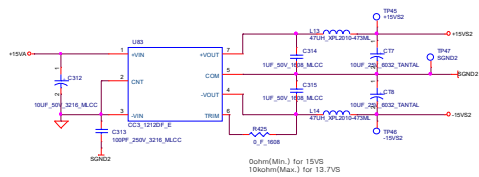




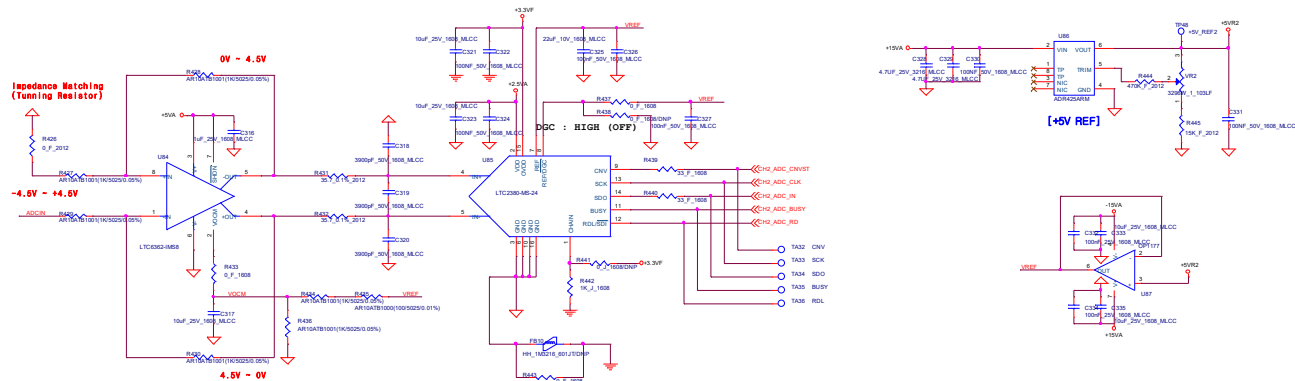
VM RANGE



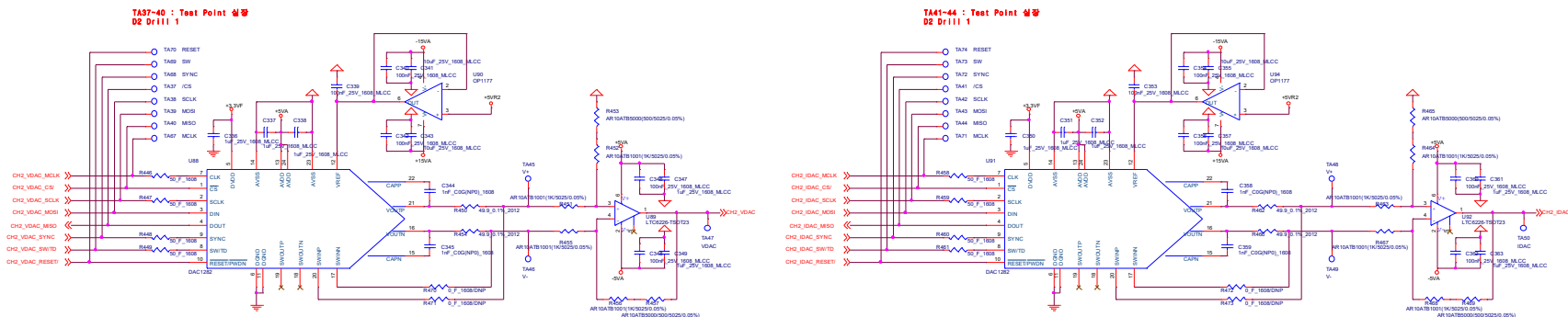
Isolated DC-DC Converter (Floating Power)



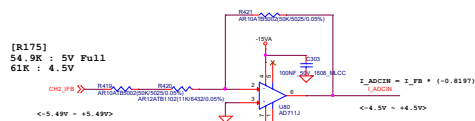
ADC (24bit)



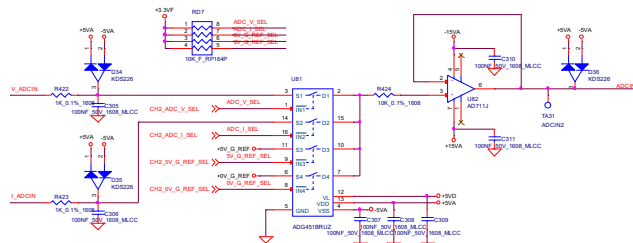
DAC (24bit)



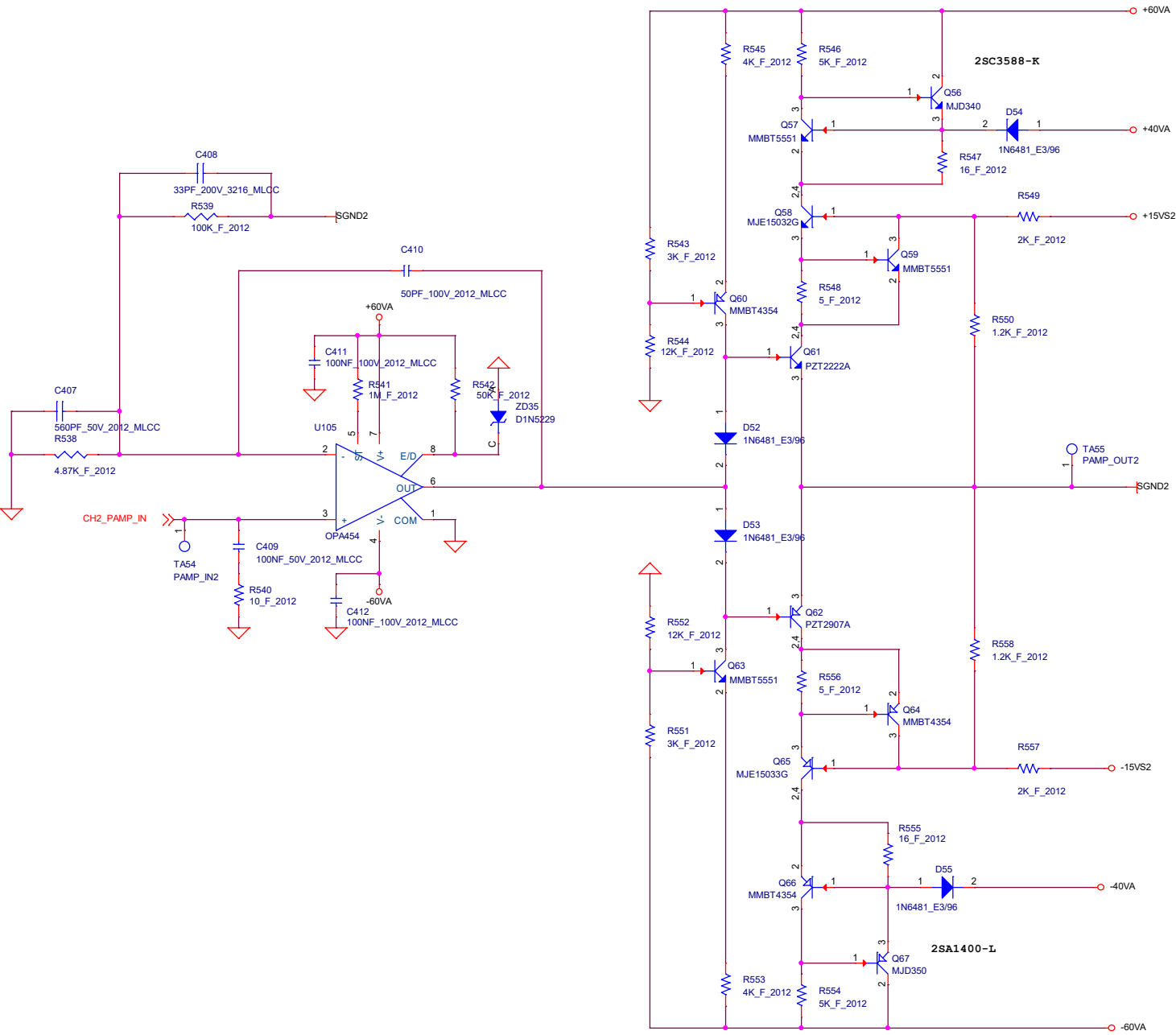
I_ADCIN




ADC SEL



POWER AMP

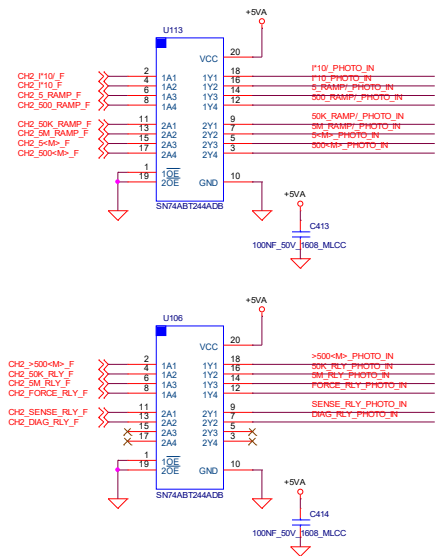


**TOP ENGINEERING**

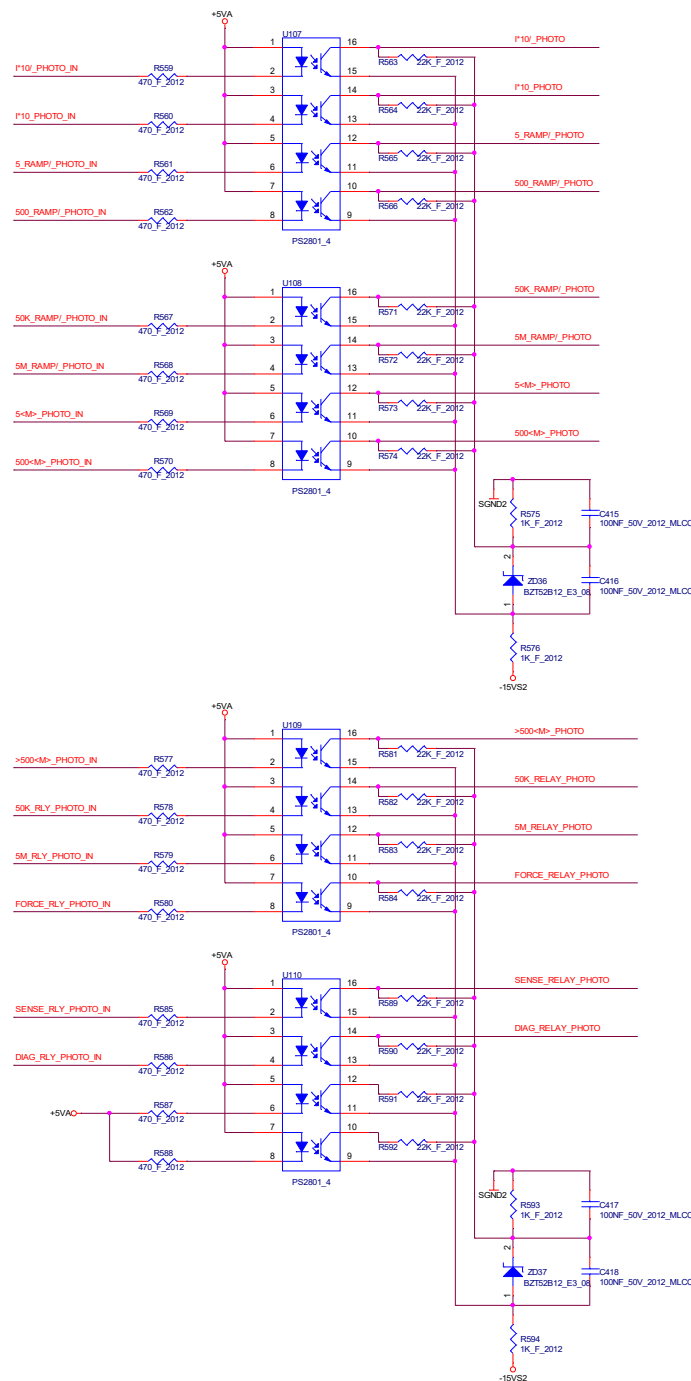
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Title: High Speed & Low Voltage SMU		TEAM			
Size: A3		TM: 1st			
Document Number: 15. POWER AMP (CH2)	Designed: DH YOO	Checked: DH YOO	Approved: DH YOO	Rev: 1.0	
Date: Tuesday, July 27, 2021	Sheet: 15	of 17			

CONTROL SIGNAL BUFFER



SIGNAL ISOLATE



I RANGE CONTROL

