< CPU_CORE_CORTEX_M7 BD>

Designed By: YK SEOL
Checked & Approved By:

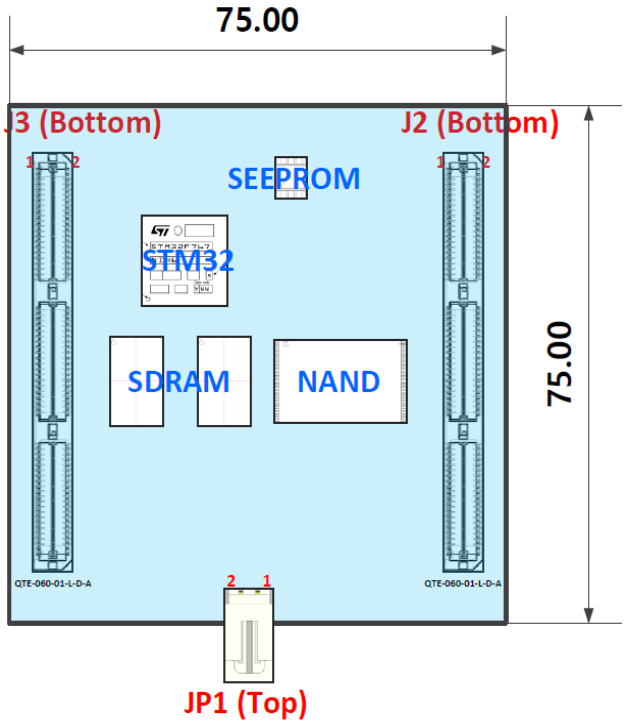
Ver 1.0: 2020.10.29, First Design

검정색 TEXT : 회로도 설명

붉은색 TEXT : 회로도 수정포인트 (두꺼운 박스 - 이번버전에서 수정된 부분)

파란색 TEXT : PCB Silk 표시 [중괄호 안에 TEXT]

보라색 TEXT : 회로블럭 이름



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Title: CPU_CORE_CORTEX_M7_BD			TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	01. COVER		Seol YK	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, November 12, 2020	Sheet 1 of 7				

<Revision History >

Date	Version	Editor	Revision
2020.10.29	1.0	YK SEOL	New

Title: CPU_CORE_CORTEX_M7_BD			TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	02. Revision History		Seol YK	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, November 12, 2020	Sheet 2 of 7				

MCU (1/3)

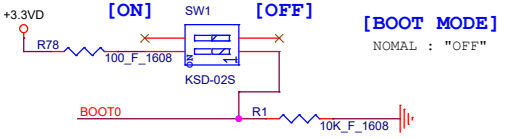
MCU PIN DEFINE

U1A

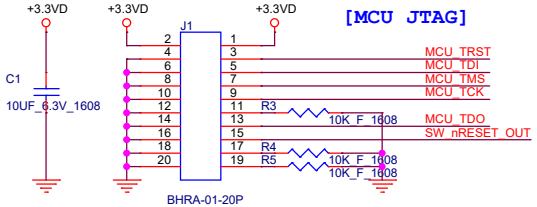
[6] USART#2_CTS	N3	PA00/USART2_CTS/UART4_TX/SAI2_SD_B/ETH_MII_CRS/ADC123_IN0/WKUP1	BOOT0/VPP	E6	BOOT0
[6] USART#2_RTS	N2	PA01/USART2_RTS/UART4_RX/ETH_MII_RX_CLK/ETH_RMII_REF_CLK/ADC123_IN1			
[6] USART#2_TX	P2	PA02/USART2_TX/ETH_MDIO/MDIOS_MDIO/ADC123_IN2/WKUP2	NRST	J1	SW_nRESET_OUT
[6] USART#2_RX	R2	PA03/USART2_RX/OTG_HS_ULPI_D0/ETH_MII_COL/ADC123_IN3			
SPI_#1_nCS [7] SPI_#1_nCS	N4	PA04/SPI1_NSS/I2S1_WS/SPI3_NSS/I2S3_WS/USART2_CK/SPI6_NSS/OTG_HS_SOF/ADC12_IN4	PDR_ON	E5 R2	10K_F_1608 +3.3VD
SPI_#1_SCLK [7] SPI_#1_SCLK	P4	PA05/SPI1_SCK/I2S1_CK/SPI6_SCK/OTG_HS_ULPI_CK/ADC12_IN5			
SPI_#1_MISO [7] SPI_#1_MISO	P3	PA06/SPI1_MISO/SPI6_MISO/ADC12_IN6			
SPI_#1_MOSI [7] SPI_#1_MOSI	R3	PA07/SPI1_MOSI/I2S1_SD/SPI6_MOSI/ETH_MII_RX_DV/ETH_RMII_CRS_DV/FMC_SDNWE/ADC12_IN7			
[7] TIM#1_CH1	F15	PA08/MCO1/I2C3_SCL/USART1_CK/OTG_FS_SOF/UART7_RX			
[7] USART#1_TX	E15	PA09/I2C3_SMBA/SPI2_SCK/I2S2_CK/USART1_TX/OTG_FS_VBUS			
[7] USART#1_RX	D15	PA10/USART1_RX/LCD_B4/OTG_FS_ID			
[7] USB_OTG_FS_DM	C15	PA11/SPI2_NSS/I2S2_WS/UART4_RX/USART1_CTS/OTG_FS_DM			
[7] USB_OTG_FS_DP	B15	PA12/SPI2_SCK/I2S2_CK/UART4_TX/USART1_RTS/OTG_FS_DP			
MCU_TMS	A15	PA13/JTMS-SWDIO			
MCU_TCK	A14	PA14/JTCK-SWCLK			
MCU_TDI	A13	PA15/JTDI/SPI1_NSS/I2S1_WS/SPI3_NSS/I2S3_WS/SPI6_NSS/UART4_RTS/UART7_TX			
[7] GPIO_PB0_F_RDY	R5	PB00/UART4_CTS/OTG_HS_ULPI_D1/ETH_MII_RXD2/ADC12_IN8			
[7] GPIO_PB1_LED_OK	R4	PB01/OTG_HS_ULPI_D2/ETH_MII_RXD3/ADC12_IN9			
[7] GPIO_PB2_LED_BUSY	M5	PB02/SAI1_SD_A/SPI3_MOSI/I2S3_SD			
MCU_TDO	A10	PB03/JTDO/SPI1_SCK/I2S1_CK/SPI3_SCK/I2S3_CK/SPI6_SCK/UART7_RX			
MCU_TRST	A9	PB04/NJTRST/SPI1_MISO/SPI3_MISO/SPI2_NSS/I2S2_WS/SPI6_MISO/UART7_TX			
[7] GPIO_PB5	A8	PB05/UART5_RX/I2C1_SMBA/SPI1_MOSI/I2S1_SD/SPI3_MOSI/I2S3_SD/SPI6_MOSI/ETH_PPS_OUT/FMC_SDCKE1			
[5] EEPROM_I2C1_SCL	B6	PB06/UART5_TX/I2C1_SCL/USART1_TX/I2C4_SCL/FMC_SDNE1			
[5] EEPROM_I2C1_SDA	B5	PB07/I2C1_SDA/USART1_RX/I2C4_SDA/FMC_NL			
[7] EXT_I2C4_SCL	A7	PB08/I2C4_SCL/I2C1_SCL/UART5_RX/ETH_MII_TXD3			
[7] EXT_I2C4_SDA	B4	PB09/I2C4_SDA/I2C1_SDA/SPI2_NSS/I2S2_WS/UART5_TX/I2C4_SMBA			
QSPI_BK1_NCS [7] QSPI_BK1_NCS	P12	PB10/I2C2_SCL/SPI2_SCK/I2S2_CK/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER			
[7] TIM#2_CH4	R13	PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_MII_TX_EN/ETH_RMII_TX_EN/DSI_TE			
SPI_#2_nCS [7] SPI_#2_nCS	L13	PB12/I2C2_SMBA/SPI2_NSS/I2S2_WS/USART3_CK/UART5_RX/ETH_MII_TXD0/ETH_RMII_TXD0/OTG_HS_ID			
SPI_#2_SCLK [7] SPI_#2_SCLK	K14	PB13/SPI2_SCK/I2S2_CK/USART3_CTS/UART5_TX/OTG_HS_ULPI_D6/ETH_MII_TXD1/ETH_RMII_TXD1/OTG_HS_VBUS			
SPI_#2_MISO [7] SPI_#2_MISO	R14	PB14/USART1_TX/SPI2_MISO/USART3_RTS/UART4_RTSOTG_HS_DM			
SPI_#2_MOSI [7] SPI_#2_MOSI	R15	PB15/RTC_REFIN/USART1_RX/SPI2_MOSI/I2S2_SD/UART4_CTS/OTG_HS_DP			
[7] GPIO_PC0	M2	PC00/SAI2_FS_B/OTG_HS_ULPI_STP/FMC_SDNWE/ADC123_IN10			
[7] GPIO_PC1	M3	PC01/SPI2_MOSI/I2S2_SD/SAI1_SD_A/ETH_MDC/ADC123_IN11/RTC_TAMP3/WKUP3			
[7] GPIO_PC2	M4	PC02/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/FMC_SDNE0/ADC123_IN12			
[7] GPIO_PC3	L4	PC03/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/FMC_SDCKE0/ADC123_IN13			
[7] GPIO_PC4	N5	PC04/I2S1_MCK/SPDIF_RX2/ETH_MII_RXD0/ETH_RMII_RXD0/FMC_SDNE0/ADC12_IN14			
[7] GPIO_PC5	P5	PC05/SPDIF_RX3/ETH_MII_RXD1/ETH_RMII_RXD1/FMC_SDCKE0/ADC12_IN15			
[7] USART#6_TX	H15	PC06/I2S2_MCK/USART6_TX/FMC_NWAIT			
[7] USART#6_RX	G15	PC07/I2S3_MCK/USART6_RX/FMC_NE1			
R11 0_F_1005 FMC_NE2 [7] FMC_NE2	G14	PC08/UART5_RTS/USART6_CK/FMC_NE2/FMC_NCE			
[7] GPIO_PC9	F14	PC09/MCO2/I2C3_SDA/I2S_CKIN/UART5_CTS			
[7] GPIO_PC10	B14	PC10/SPI3_SCK/I2S3_CK/USART3_TX/UART4_TX			
[7] GPIO_PC11	B13	PC11/SPI3_MISO/USART3_RX/UART4_RX			
[7] GPIO_PC12	A12	PC12/SPI3_MOSI/I2S3_SD/USART3_CK/UART5_TX			
[7] GPIO_PC13	D1	PC13/RTC_TAMP1/RTC_TS/RTC_OUT/WKUP4			
[7] GPIO_PC14	E1	PC14/OSC32_IN			
[7] GPIO_PC15	F1	PC15/OSC32_OUT			
[5,7] FMC_DATA2	B12	PD00/UART4_RX/FMC_D2			
[5,7] FMC_DATA3	C12	PD01/UART4_TX/FMC_D3			
[7] GPIO_PD2	D12	PD02/UART5_RX			
R12 0_F_1005 FMC_CLK [7] FMC_CLK	C11	PD03/SPI2_SCK/I2S2_CK/USART2_CTS/FMC_CLK			
[5,7] FMC_NOE FMC_NOE	D11	PD04/USART2_RTS/FMC_NOE			
[5,7] FMC_NWE FMC_NWE	C10	PD05/USART2_TX/FMC_NWE			
[5] FMC_NWAIT	B11	PD06/SPI3_MOSI/I2S3_SD/SAI1_SD_A/USART2_RX/FMC_NWAIT			
R13 0_F_1005 FMC_NE1 [7] FMC_NE1	A11	PD07/SPI1_MOSI/I2S1_SD/USART2_CK/SPDIF_RX0/FMC_NE1			
[5,7] FMC_DATA13	L15	PD08/USART3_TX/SPDIF_RX1/FMC_D13			
[5,7] FMC_DATA14	L14	PD09/USART3_RX/FMC_D14			
[5,7] FMC_DATA15	K15	PD10/USART3_CK/FMC_D15			
[5,7] FMC_ADDR16_FMC_CLE	N10	PD11/I2C4_SMBA/USART3_CTS/SAI2_SD_A/FMC_A16/FMC_CLE			
[5,7] FMC_ADDR17_FMC_ALE	M10	PD12/I2C4_SCL/USART3_RTS/SAI2_FS_A/FMC_A17/FMC_ALE			
[7] FMC_ADDR18	M11	PD13/I2C4_SDA/SAI2_SCK_A/FMC_A18			
[5,7] FMC_DATA0	L12	PD14/UART8_CTS/FMC_D0			
[5,7] FMC_DATA1	K13	PD15/UART8_RTS/FMC_D1			
[5] FMC_NBL0	A6	PE00/UART8_RX/SAI2_MCLK_A/FMC_NBL0			
[5] FMC_NBL1	A5	PE01/UART8_TX/FMC_NBL1			
[7] FMC_ADDR23	A3	PE02/SPI4_SCK/SAI1_MCLK_A/ETH_MII_TXD3/FMC_A23			
[7] FMC_ADDR19	A2	PE03/SAI1_SD_B/FMC_A19			
[7] FMC_ADDR20	A1	PE04/SPI4_NSS/SAI1_FS_A/FMC_A20			
[7] FMC_ADDR21	B1	PE05/SPI4_MISO/SAI1_SCK_A/FMC_A21			
[7] FMC_ADDR22	B2	PE06/SPI4_MOSI/SAI1_SD_A/SAI2_MCLK_B/FMC_A22			
[5,7] FMC_DATA4	R8	PE07/UART7_RX/FMC_D4			
[5,7] FMC_DATA5	N9	PE08/UART7_TX/FMC_D5			
[5,7] FMC_DATA6	P9	PE09/UART7_RTS/FMC_D6			
[5,7] FMC_DATA7	R9	PE10/UART7_CTS/FMC_D7			
[5,7] FMC_DATA8	P10	PE11/SPI4_NSS/SAI2_SD_B/FMC_D8			
[5,7] FMC_DATA9	R10	PE12/SPI4_SCK/SAI2_SCK_B/FMC_D9			
[5,7] FMC_DATA10	R12	PE13/SPI4_MISO/SAI2_FS_B/FMC_D10			
[5,7] FMC_DATA11	P11	PE14/SPI4_MOSI/SAI2_MCLK_B/FMC_D11			
[5,7] FMC_DATA12	R11	PE15/FMC_D12			

STM32F767NI

BOOT Option

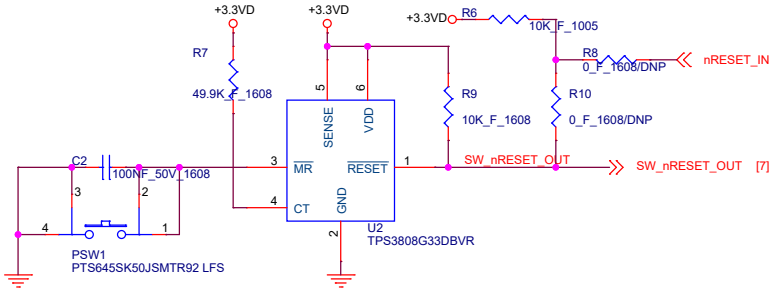


MCU JTAG



10x2 PIN HEADER BOX R/A (2.54mm)

RESET S/W



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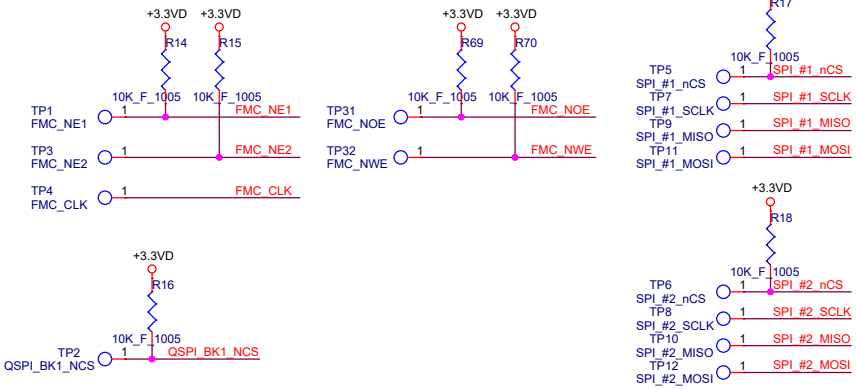

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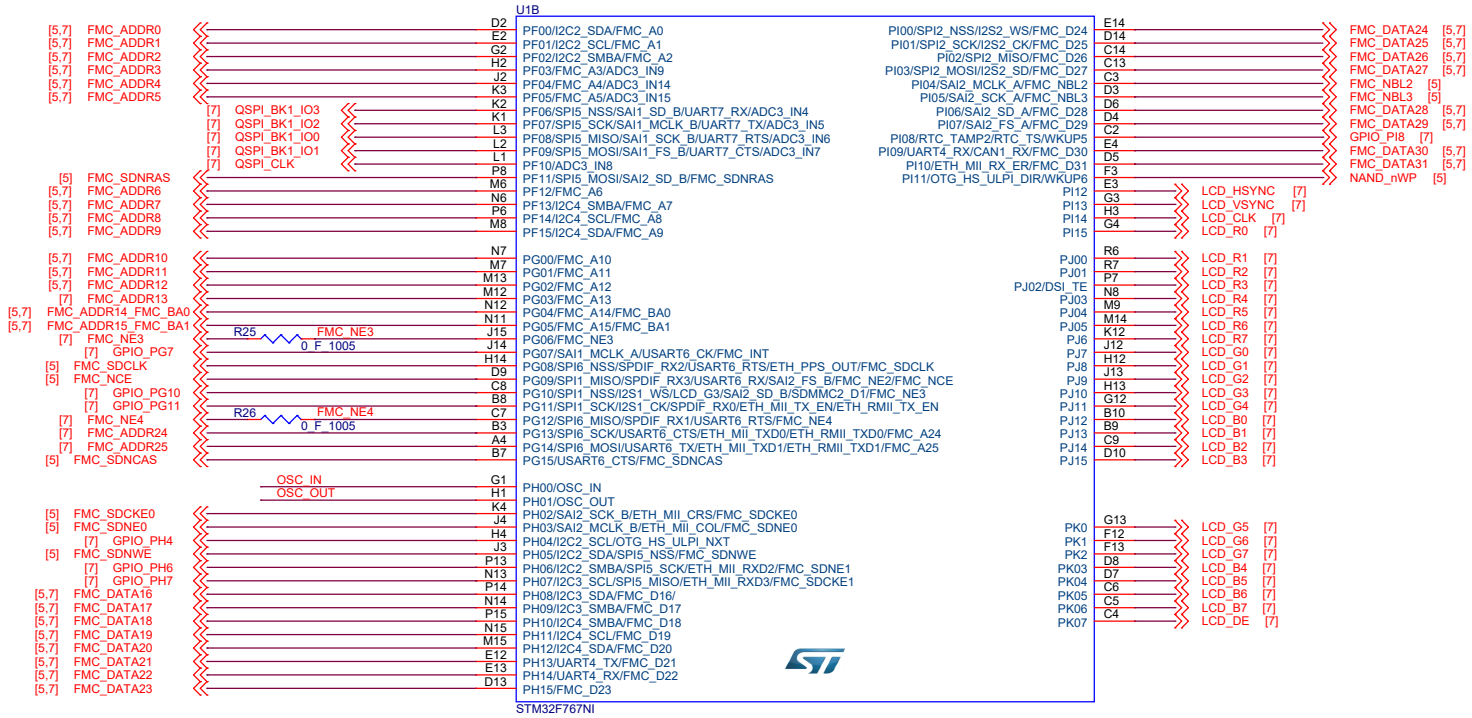
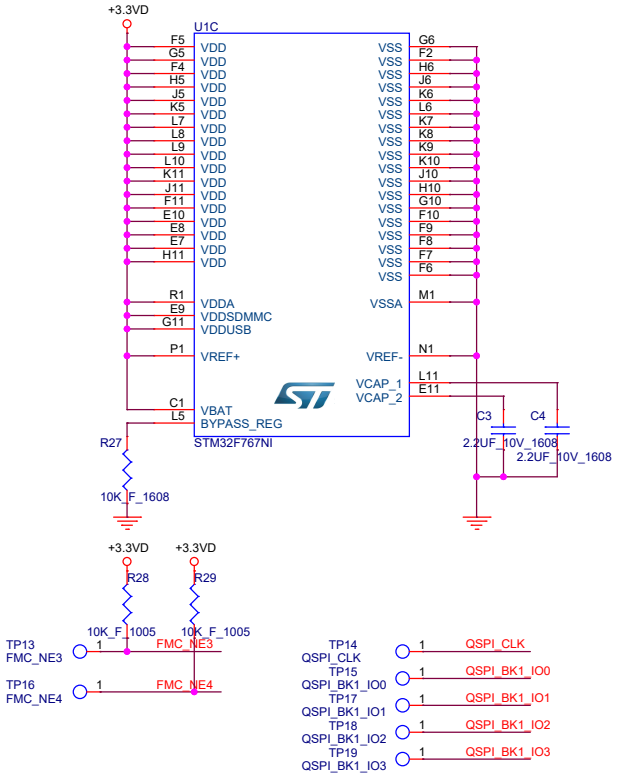
Size	Document Number	Designed	Checked	Approved Rev
A3	03. CORTEX_M7 CORE	Seol YK	JOH JH	<OrgAddr3> 1.0
Date: Thursday, November 12, 2020		Sheet 3 of 7		

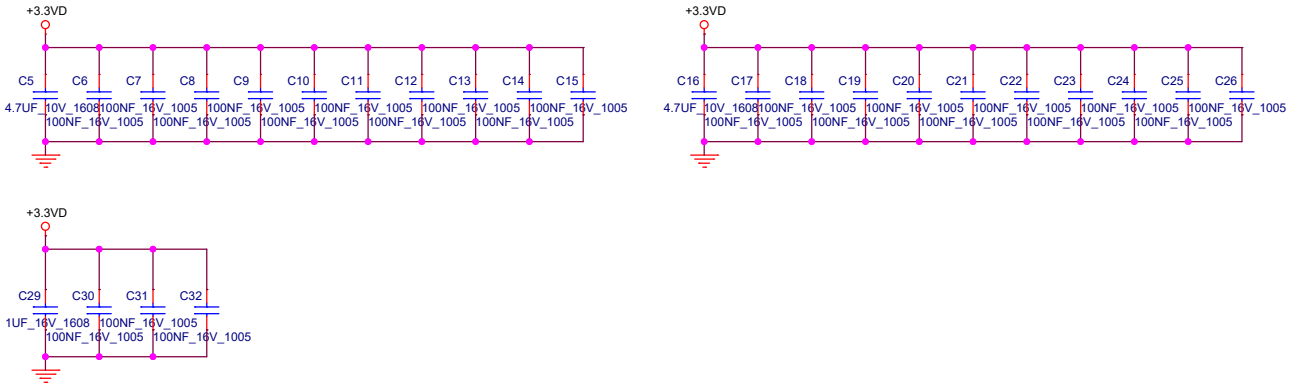
MCU (2/3)



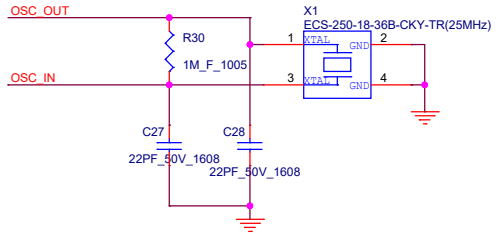
MCU (3/3)



MCU POWER CAP



Crystal IN



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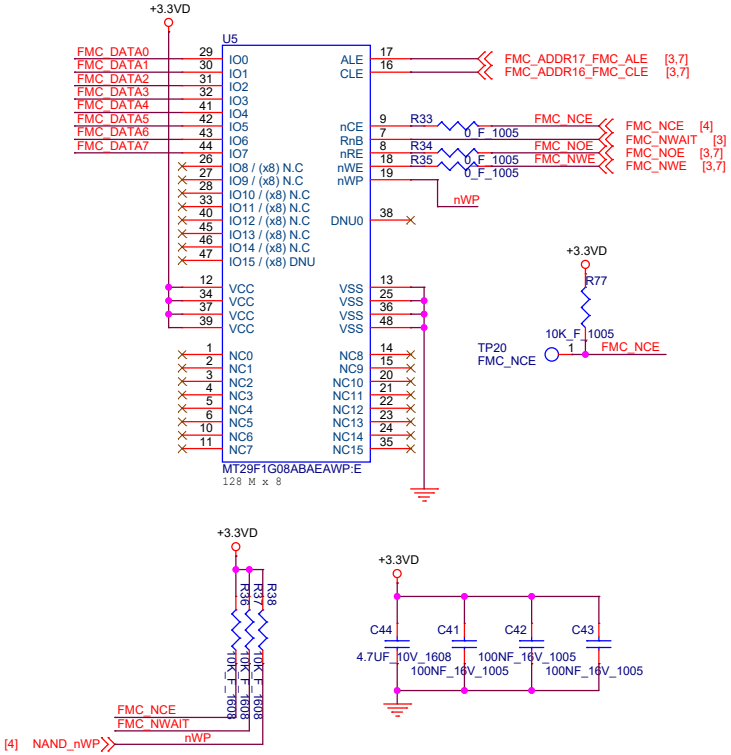
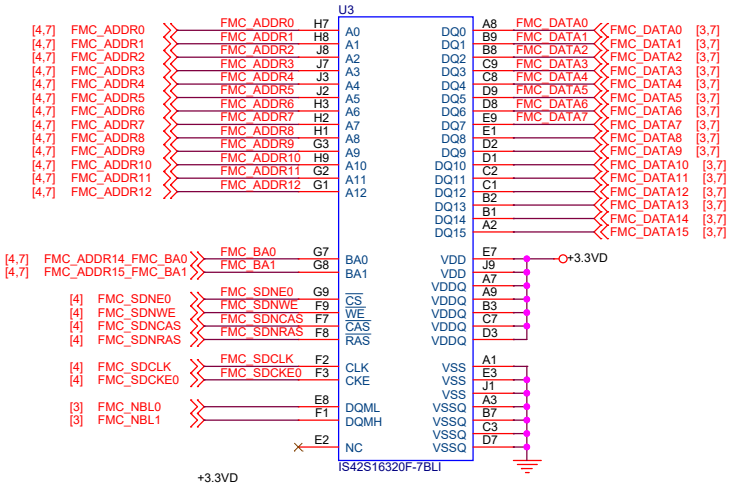
Size	Document Number		Designed	Checked	Approved	Rev
A3	04. POWER & SYSTEM		Seol YK	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, November 12, 2020	Sheet 4 of 7				

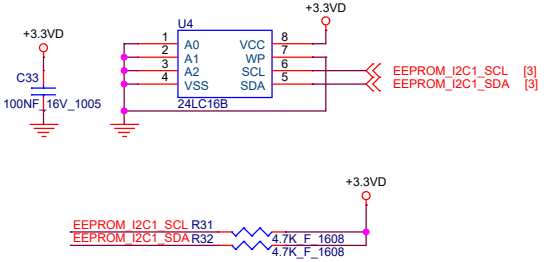
NAND FLASH (x8)



SDRAM



SEEP ROM



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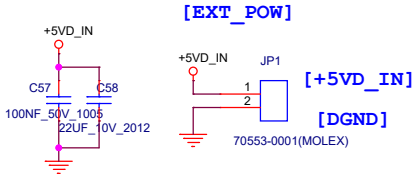
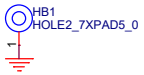
Size	Document Number		Designed	Checked	Approved	Rev
A3	05. FLASH & SDRAM		Seol YK	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, November 12, 2020	Sheet 5 of 7			

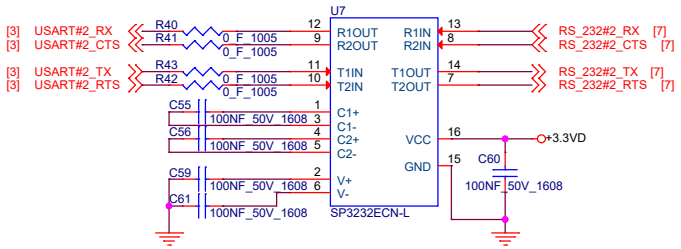
보조전원 커넥터



보드 고정 홀

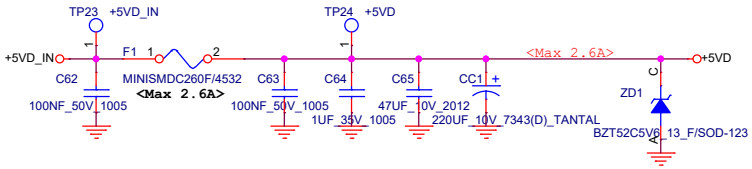


USART#2 RS-232

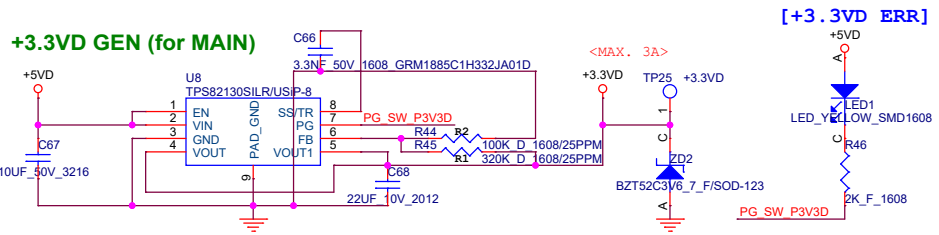


Bootload Download USART#1#2#3

FUSE



REGULATOR




```
=== TPS82130SILR/uSiP-8 ===
Vout = 0.8 * (1 + R1/R2)
0.8 * (1 + 100k/100k) = 1.60V
0.8 * (1 + 320k/100k) = 3.36V
0.8 * (1 + 536k/100k) = 5.09V
```

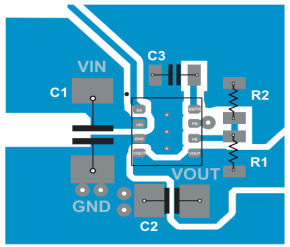
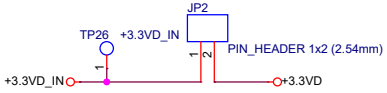
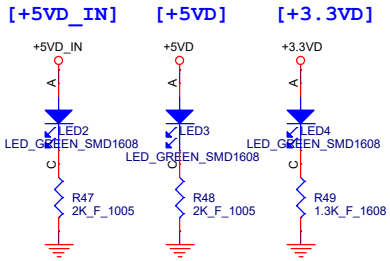


Figure 29. TPS82130 PCB Layout

[+3.3VD_IN]



전원 LED



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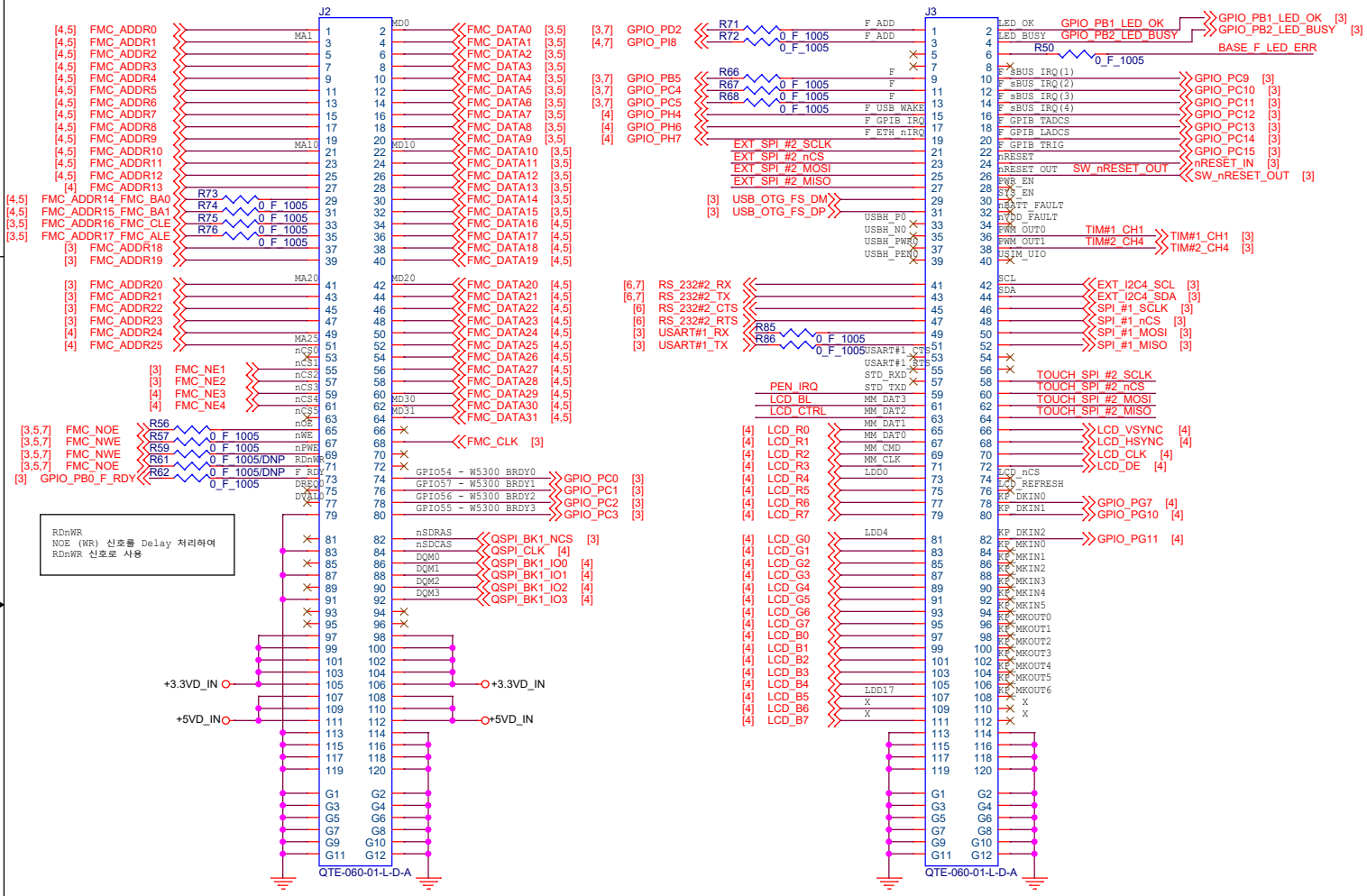
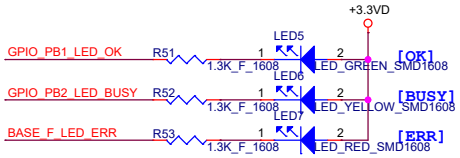
Title: CPU_CORE_CORTEX_M7_BD			TEAM TM1		
Size	Document Number		Designed	Checked	Approved	Rev
A3	06. UART & BASE IO		Seol YK	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, November 12, 2020	Sheet 6 of 7				

CONNECTOR (BOTTOM)

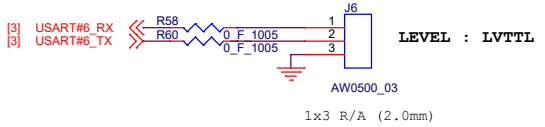


상태표시 LED



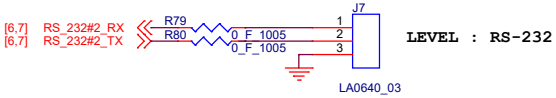
USART#6 CONNECTOR

[UART #6 (LVTTL)]



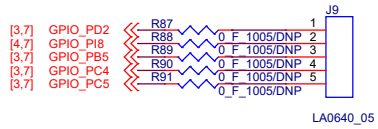
RS-232#2 CONNECTOR

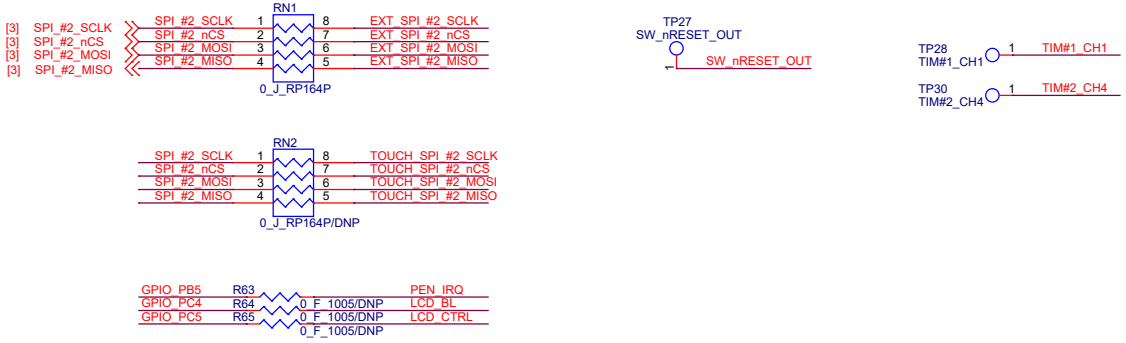
[RS-232 #2]



GPIO CONNECTOR

[GPIO]





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Size: A3	Document Number: 06. UART & BASE IO	Designed: Seol YK	Checked: JOH JH
Approved: <OrgAddr3>	Rev: 1.0		
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