< High Resolution SMU >

Designed By: Yuheon Yi
Checked & Approved By: YK Seul & Donghyuk Yoo
Ver 1.1 : 2021.07.23

검정색 TEXT:
회로도 설명
붉은색 TEXT :회로도 수정포인트 (두꺼운 박스 - 이번버전 에서 수정된 부분)

파랑색 TEXT : PCB Silk표시(중 괄호 안에 TEXT)
보라색 TEXT:
회로블럭 이름

02. Revision History
03. Connector and Power
04. Buffer
05. FPGA #1
06. FPGA #2
07. FPGA #3
08. DAC
09. ADC and Measurement Circuit
10. ERROR AMP
11. POWER AMP
12. OUTPUT CONTROL
13. OUTPUT
14. JIG

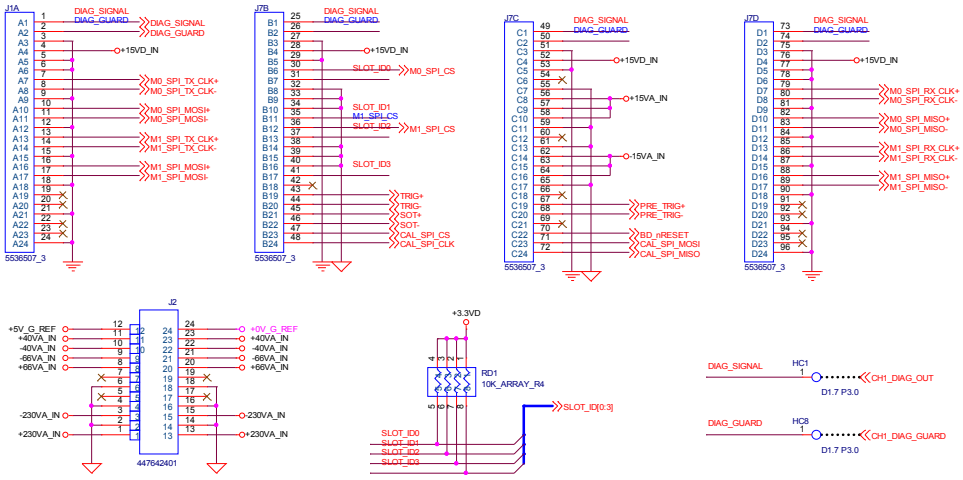
Title: High Resoultion SMU		TEAM: fM개발1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A2	01. Title	DH YOO	Seol YK	DH YOO	1.0
Date: Monday, July 26, 2021		Sheet 1 of 12			

<Revision History >

Date	Version	Editor	Revision
2019.09.16	1.0	YOO DH	24bit Resoultion ADC & New Range (500mV, 10pA)
2021.07.20	1.1	YH YI	200V 10mA max range. S3100 interface. 20bit DAC

Title: High Resoultion SMU			TEAM ITM개발1팀		
Size	Document Number		Designed	Checked	Approved	Rev
A2	02. Revision History		DH YOO	Seol YK	DH YOO	1.0
Date: Monday, July 26, 2021			Sheet 2 of 12			

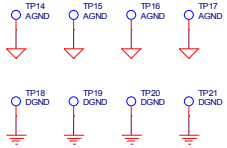
INPUT CONNECTOR



GND 연 결

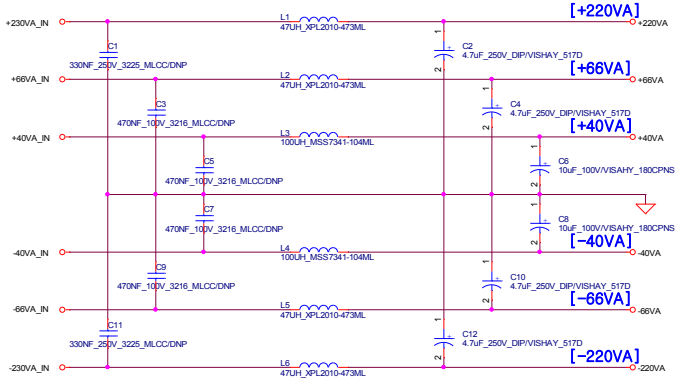
15VD IN

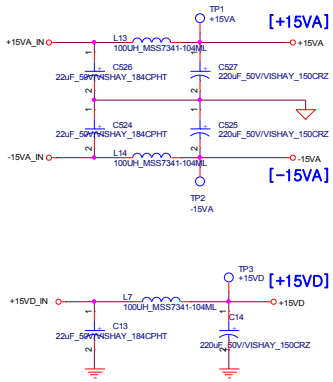
TP - GND



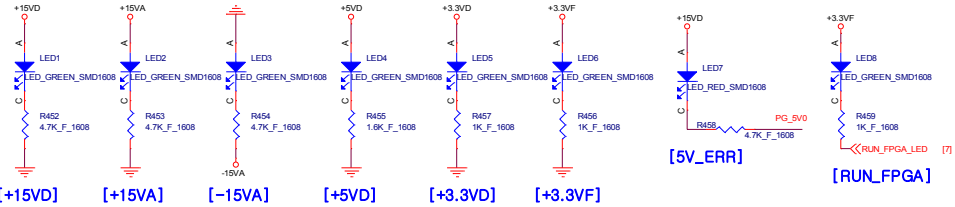
POWER FILTER

커 패 시 터 간 격 유의하여 Artwork

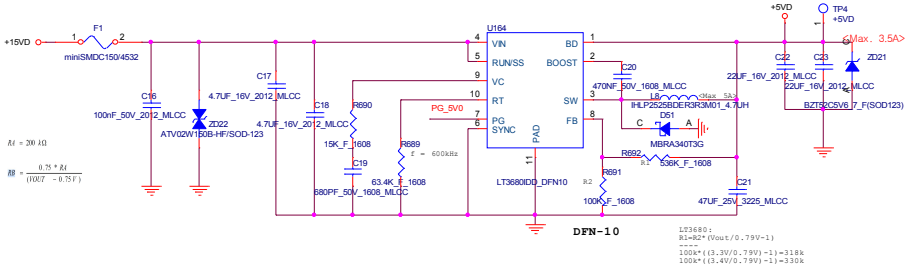


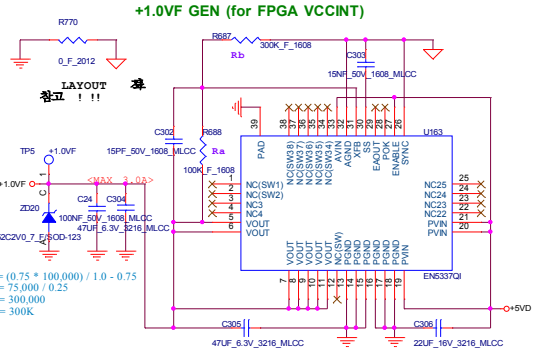


POWER LED & RUN LED

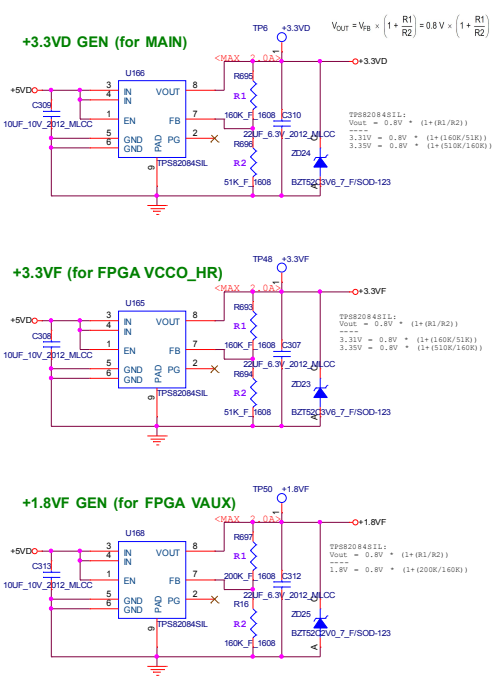


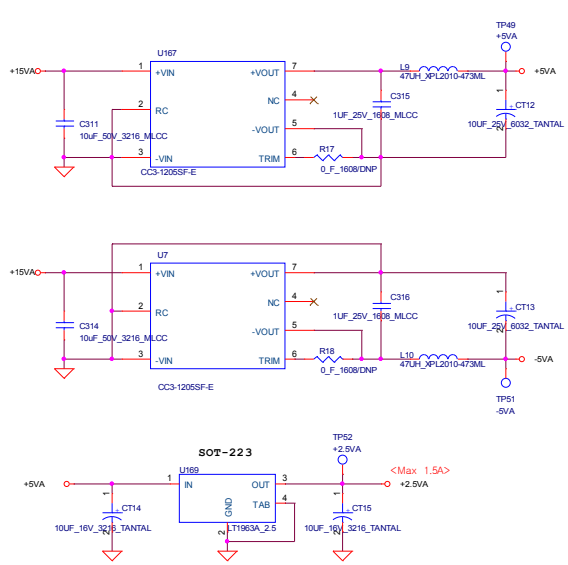
REGURATOR





[FPGA Power]
VCCINT = 1.0V
VCCBRAM = 1.0V
VAUX = 1.8V
VAUX_IO = 1.8V
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Spartan7에 없음)
VCCBATT = 1.8V
VCCADC = 1.8V





Title:		TEAM			
High Resolution SMU		fM개발1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A2	03. Connector and Power	DH YOO	Seol YK	DH YOO	1.0
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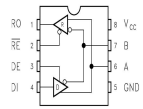
RS-422 RX(1CH)

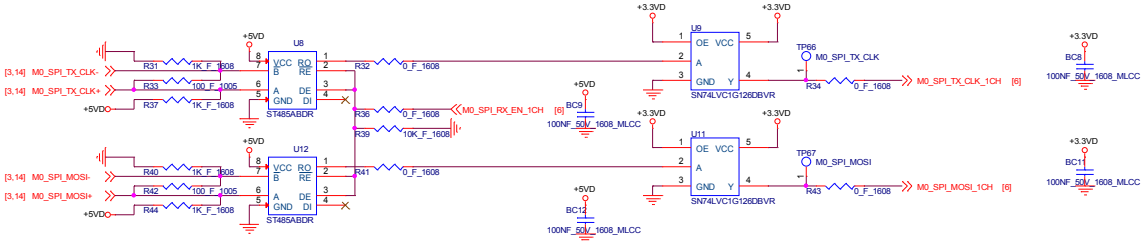
Table 4. Truth table (receiver)

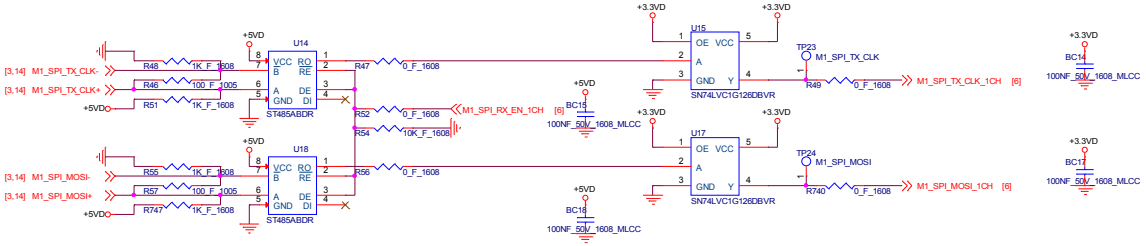
Inputs			Outputs	Mode
$\overline{RE}$	DE	A-B	RO	
L	L	≥ -0.2 V	H	Normal
L	L	≤-0.2 V	L	Normal
L	L	Inputs open	H	Normal

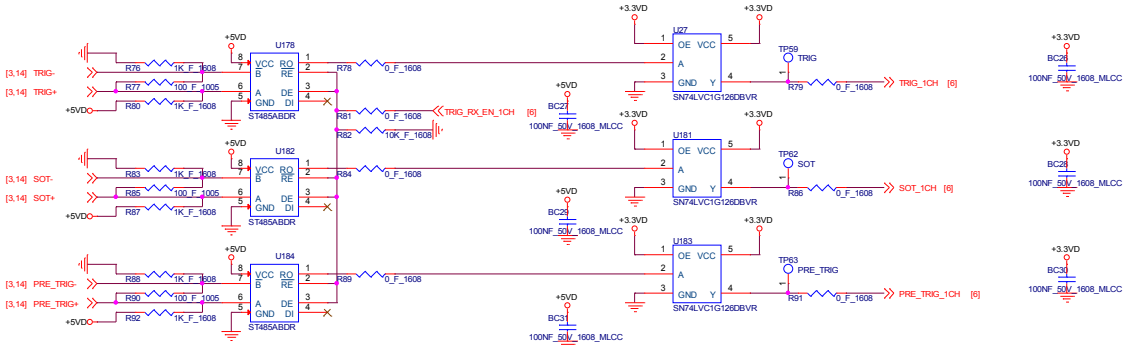


Differential 신 호 는 패 턴 길 이 동 를

멀 저 항 및 풀 업 풀 다 운 저 항 은 수 신 측





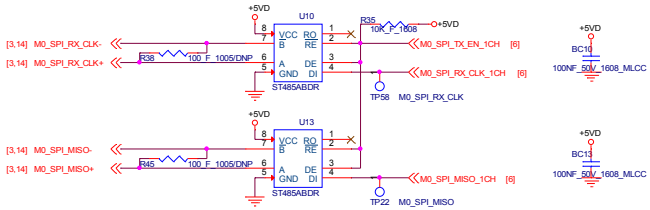


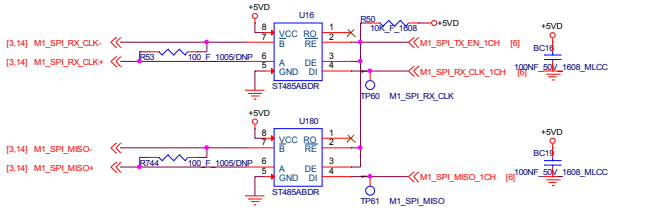
RS-422 TX(1CH)

Table 3. Truth table (driver)

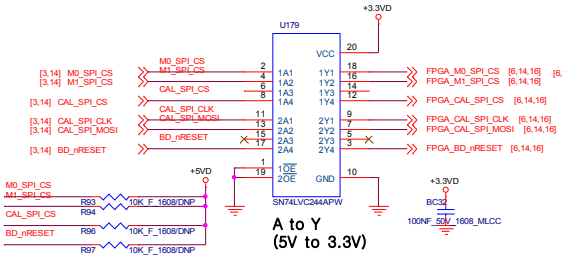
Inputs			Outputs		Mode
$\overline{RE}$	DE	DI	B	A	A
X	H	H	L	H	Normal
X	H	L	H	L	Normal
L	L	X	Z	Z	Normal

Note: *X = Don't care; Z = High impedance*

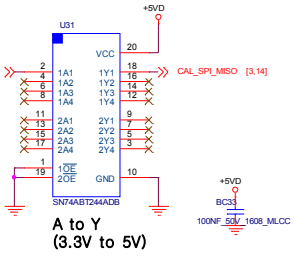




SIGNAL RX (5V to 3.3V)(1CH)

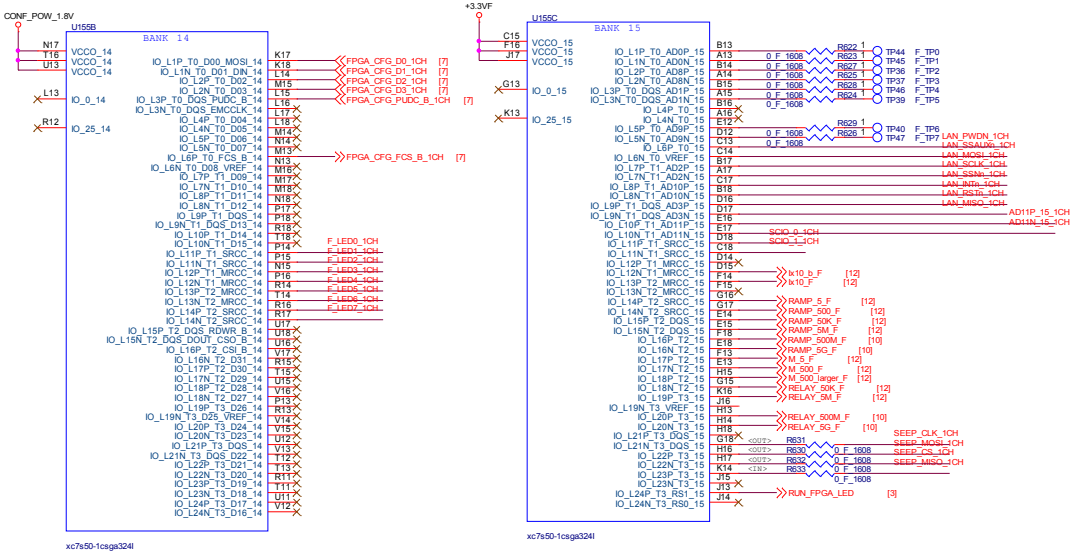


SIGNAL TX (3.3V to 5V)(1CH)

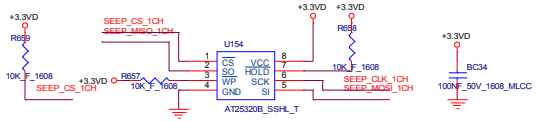


TOP ENGINEERING	CONFIDENTIAL DO NOT COPY		
Title: [E8000]HL-SMU		TEAM: fM개발1팀	
Size: A2	Document Number: 04. 1CH_BUFFER	Designed: YUNSH	Checked: JOH JH
Approved: <OrgAddr>	Rev: 1.0		
Date: Thursday, July 29, 2021	Sheet: 4 of 24		

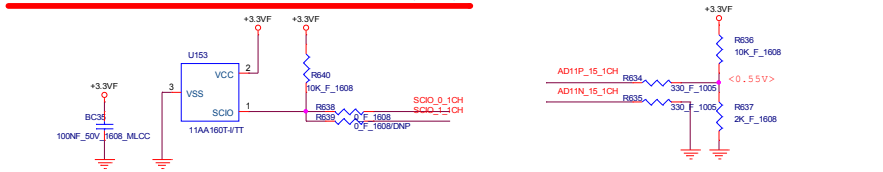
FPGA IO(1CH)

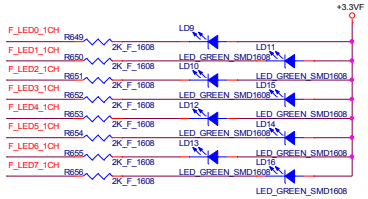


SPI EEPROM(1CH) Calibration DATA 저 장 용 Serial EEPROM

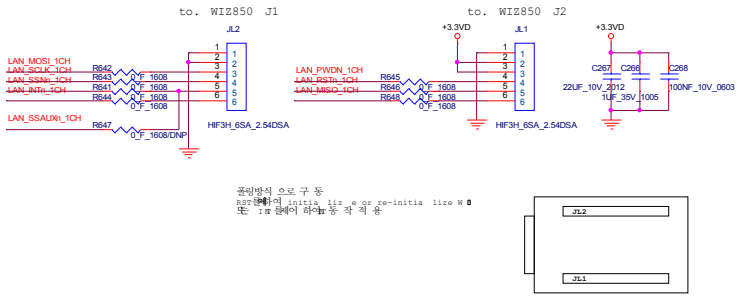


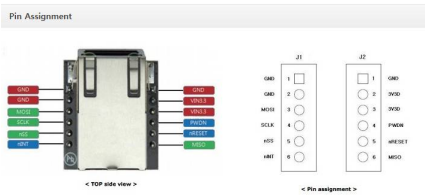
EEPROM 16K 2048X8 1.8V SERIAL EE IND(1CH)





LAN 용 Connector(1 CH)





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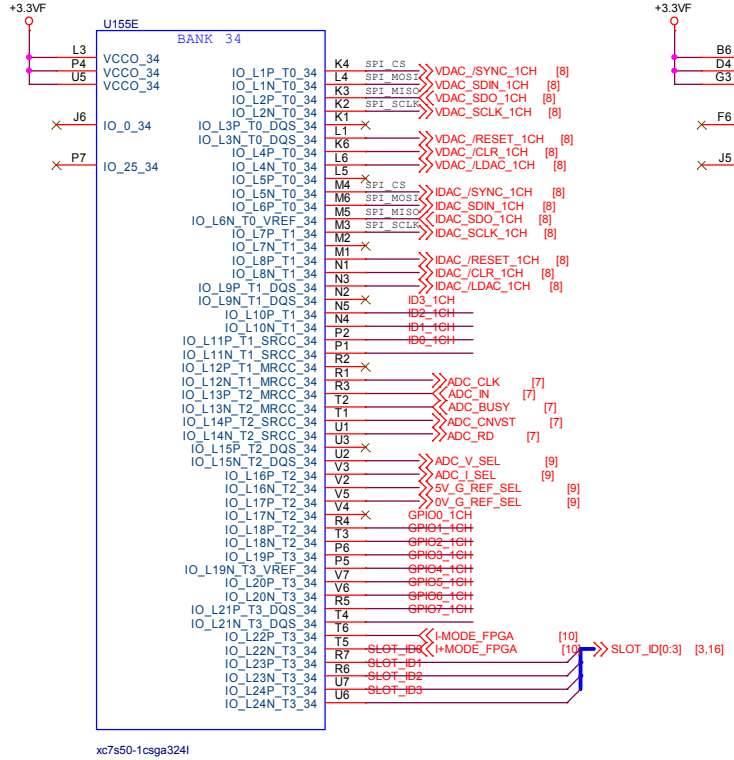
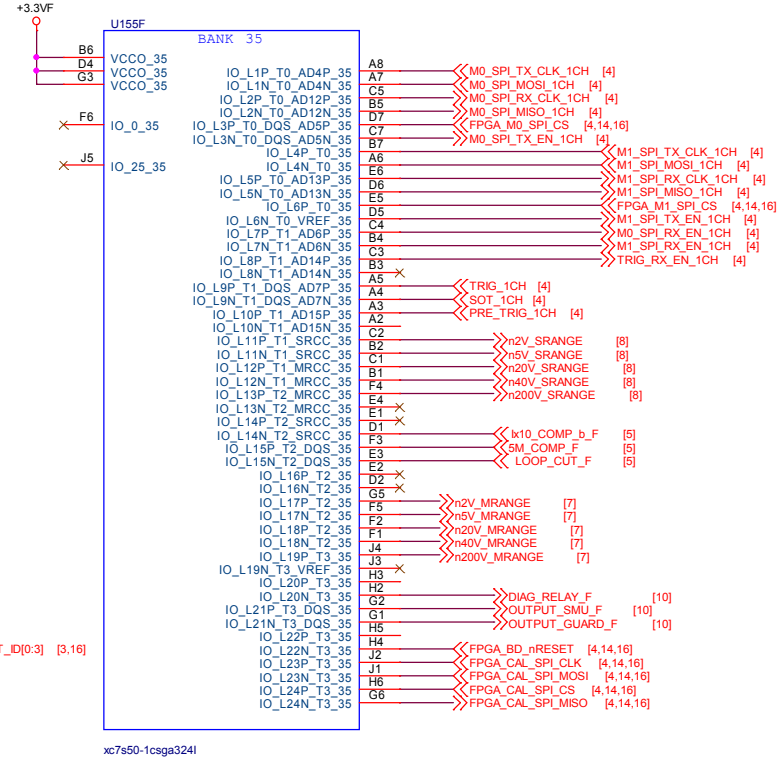
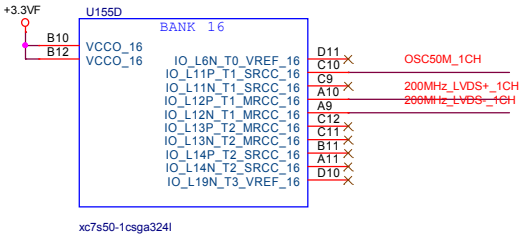
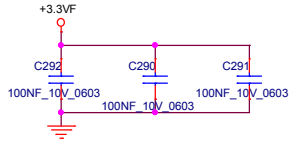
Title: High Resolution SMU		TEAM: fM계발1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A2	05. FPGA #1 (XC6SLS9)	DH YOO	Seol YK	DH YOO	1.0
Date: Tuesday, July 27, 2021		Sheet 5 of 12			

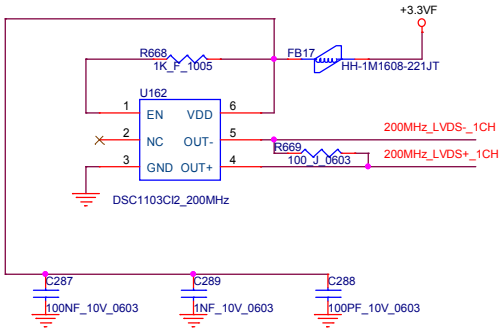
FPGA IO(1CH)

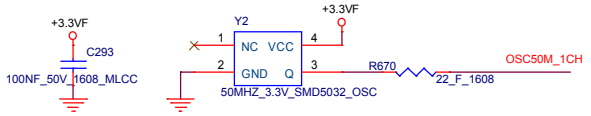


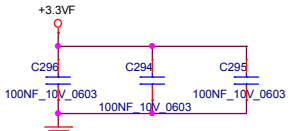


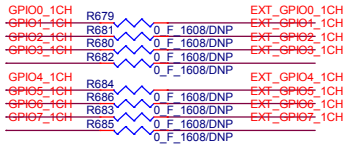


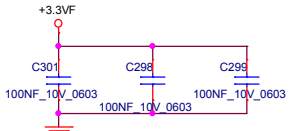


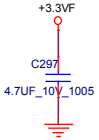


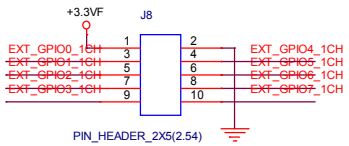


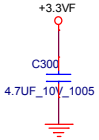








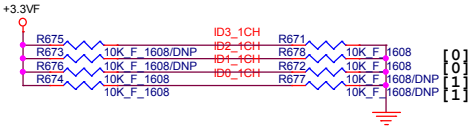




Artwork 작 업 시 한 곳 에 모아주세요

Silk : SMU BD ID : 0x0?

<LSB 4Bits>



SMU BD ID 확 인 하 여 저 항 풀 업 /다 운 할

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Title: High Resoultion SMU			TEAM TM개발1팀		
Size	Document Number		Designed	Checked	Approved	Rev
A3	06. FPGA #2 (XC6SLS9)		DH YOO	Seol YK	DH YOO	1.0
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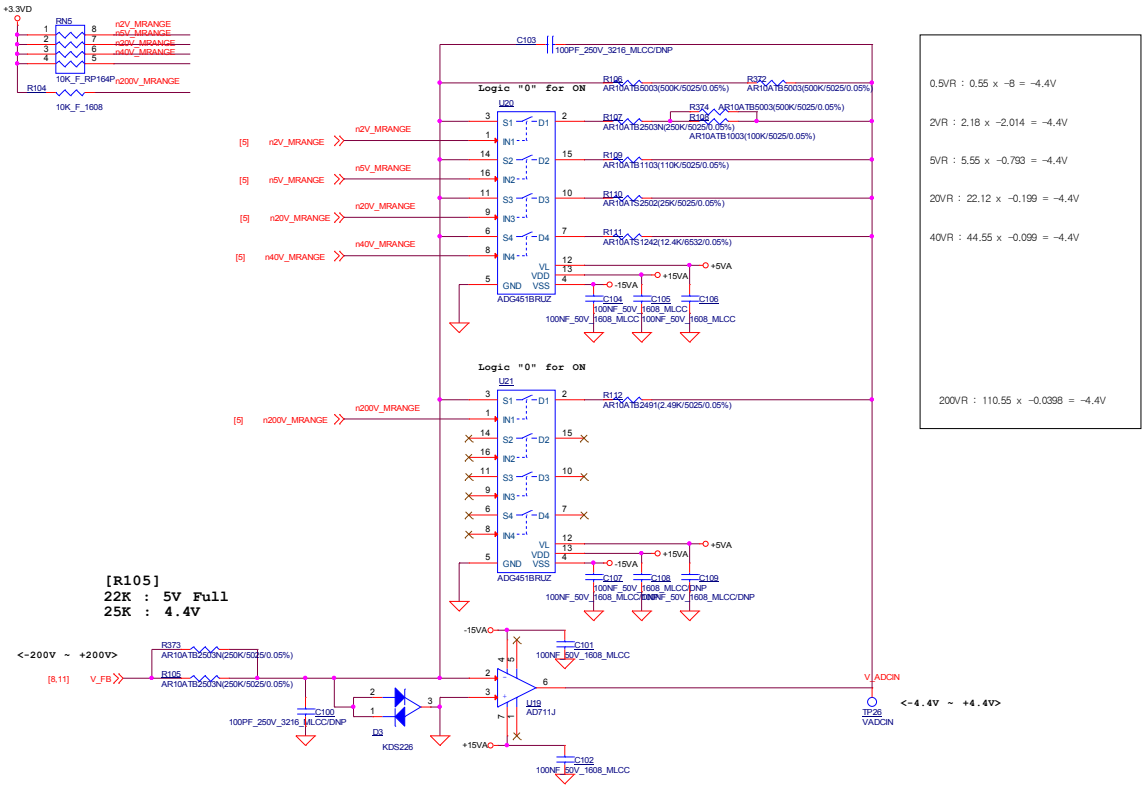
VM RANGE



0.5VR : 0.55 x -8 = -4.4V

2VR : 2.18 x -2.014 = -4.4V

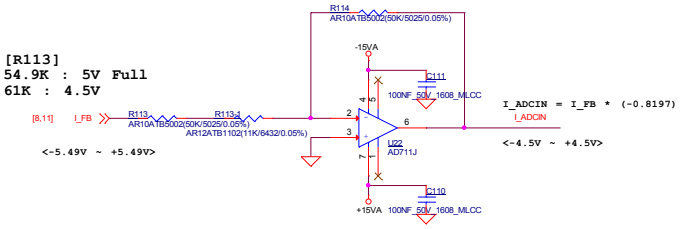
5VR : 5.55 x -0.793 = -4.4V

20VR : 22.12 x -0.199 = -4.4V

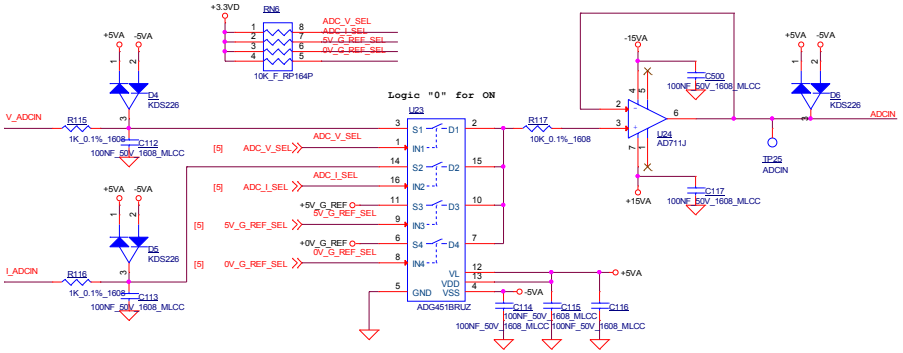
40VR : 44.55 x -0.099 = -4.4V

200VR : 110.55 x -0.0398 = -4.4V

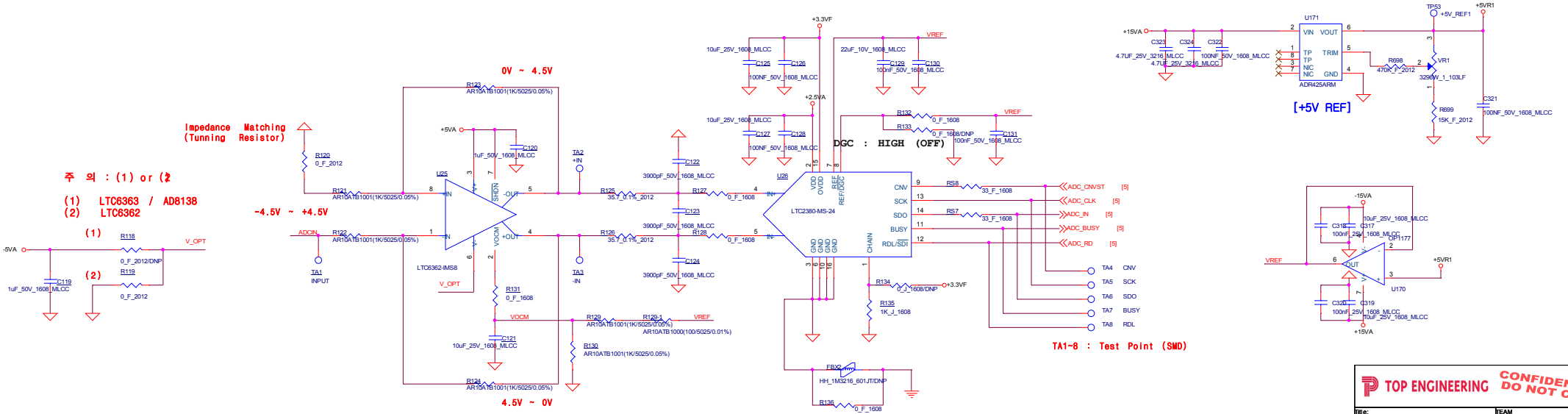
I_ADCIN



ADC SEL



HR ADC



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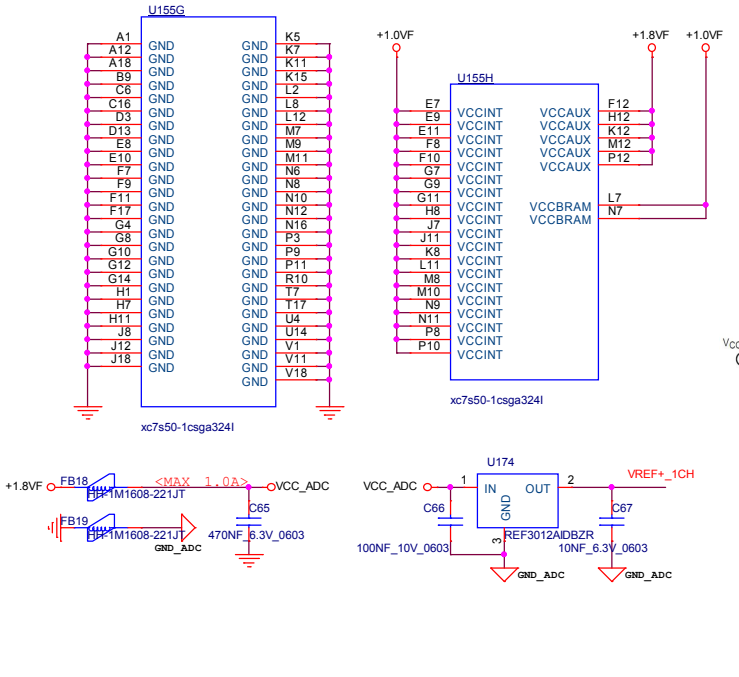
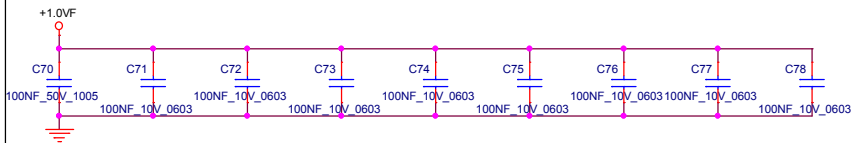
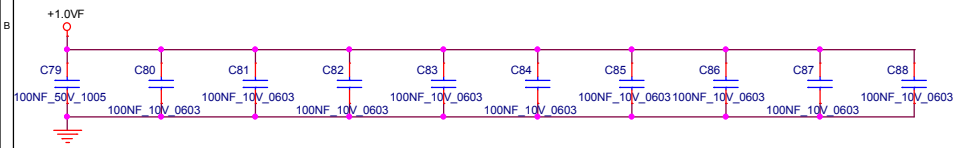
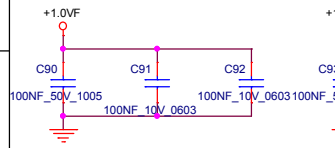
Title: High Resolution SMU		TEAM: fM개발1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A2	07. ADC and Measurement Circuit	DH YOO	Seol YK	DH YOO	1.0
Date: Monday, July 26, 2021		Sheet 7 of 12			

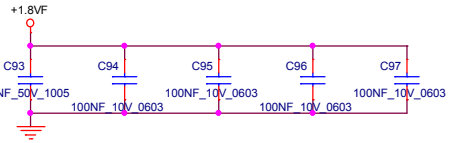
FPGA - POWER(1CH)

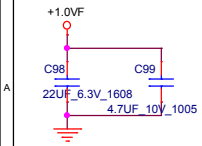


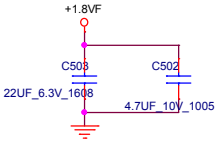


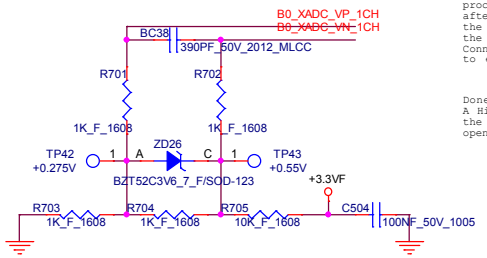










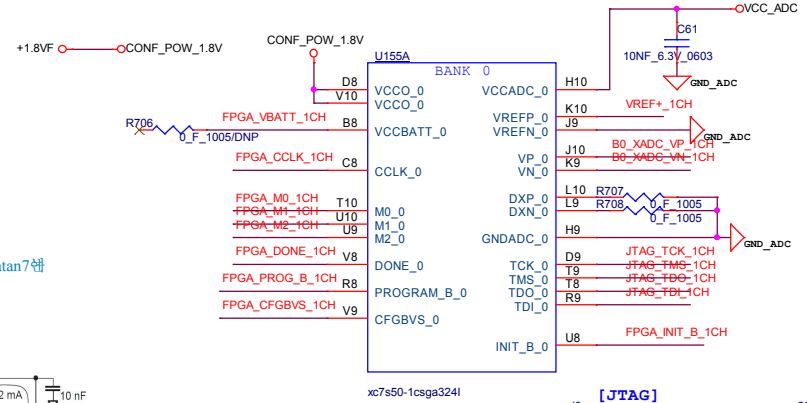


Program (bar)
Active-Low reset to configuration logic. When PROGRAM_B is pulsed Low, the FPGA configuration is cleared and a new configuration sequence is initiated. Configuration reset initiated upon falling edge, and configuration (i.e. programming) sequence begins upon the following rising edge.
Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure a stable High input, and recommend push-button to GND to enable manual configuration reset.

Initialization (bar)
Active-Low FPGA initialization pin or configuration error signal. The FPGA drives this pin Low when the FPGA is in a configuration reset state, when the FPGA is initializing (clearing) its configuration memory, or when the FPGA has detected a configuration error. Upon completing the FPGA initialization process, INIT_B is released to high-Z at which time an external resistor is expected to pull INIT_B High. INIT_B can externally be held Low during power-up to stall the power-on configuration sequence at the end of the initialization process. When a High is detected at the INIT_B input after the initialization process, the FPGA proceeds with the remainder of the configuration sequence dictated by the M[2:0] pin settings.
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to VCCO_0 to ensure clean Low-to-High transitions.

Done
A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

FPGA - Configuration Part(1CH)

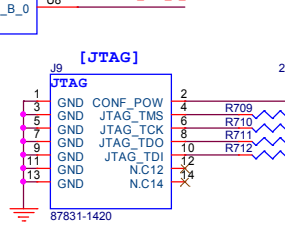


[FPGA Power]
VCCINT = -0.5~1.1 [1.0V]
VCCBRAM = -0.5~1.1 [1.0V]
VCCAUX = -0.5 ~ 2.0V [1.8V]
VCCAUX_IO = -0.5 ~ 2.0V [1.8V]
VCCO_HR = 1.14~3.465V
VCCO_HP = 1.14~1.89V (Artix7엔 없음)
VCCBATT = -0.5 ~ 2.0V [1.8V]
[FPGA Power]
VCCADC = -0.5 ~ 2.0V [1.8V]
VREF = -0.5 ~ 2.0V [1.25V] to GNDADC

Temperature-sensing diode pins (Anode: DXP; Cathode: DXN). The thermal diode is accessed by using the DXP and DXN pins in bank 0. When not used, tie to GND.

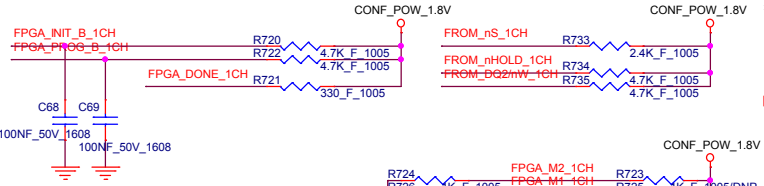
VCCBATT is required only when using bitstream encryption. If battery is not used, connect VCCBATT to either ground or VCCAUX.

If the VCCO_0 supply for bank 0 is supplied with 2.5V or 3.3V, then the CFGBVS pin must be tied High (i.e. connected to VCCO_0). Tie CFGBVS to Low (i.e. connected to GND), only if the VCCO_0 for bank 0 is less than or equal to 1.8V. If used during configuration, banks 14 and 15 should match the VCCO level applied to bank 0

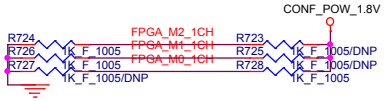


If the TCK signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.

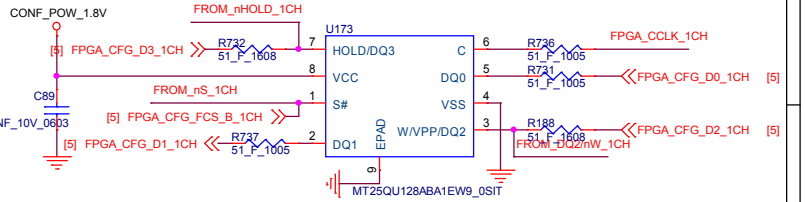
If the TMS signal is buffered, connect the buffer input to an external weak (e.g. 10 kΩ) pull-up resistor to maintain a valid High when no cable is connected.



Pull-Up During Configuration (bar)
Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.
> When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
> When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.
PUDC_B must be tied either directly, or via a ≤ 1kΩ to VCCO_14 or GND.
Caution! Do not allow this pin to float before and during configuration

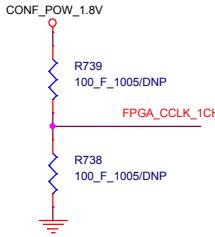


Configuration Mode Sel (M2:0)
- Master SPI: 001
- Master Serial: 000
- JTAG: 101



MT25QU256ABA1EW9_0SIT MT25QL = 2.7V ~ 3.6V
MT25QU = 1.7V ~ 2.0V

S25FL128SAGNFI001
S25FL256SAGNFI001



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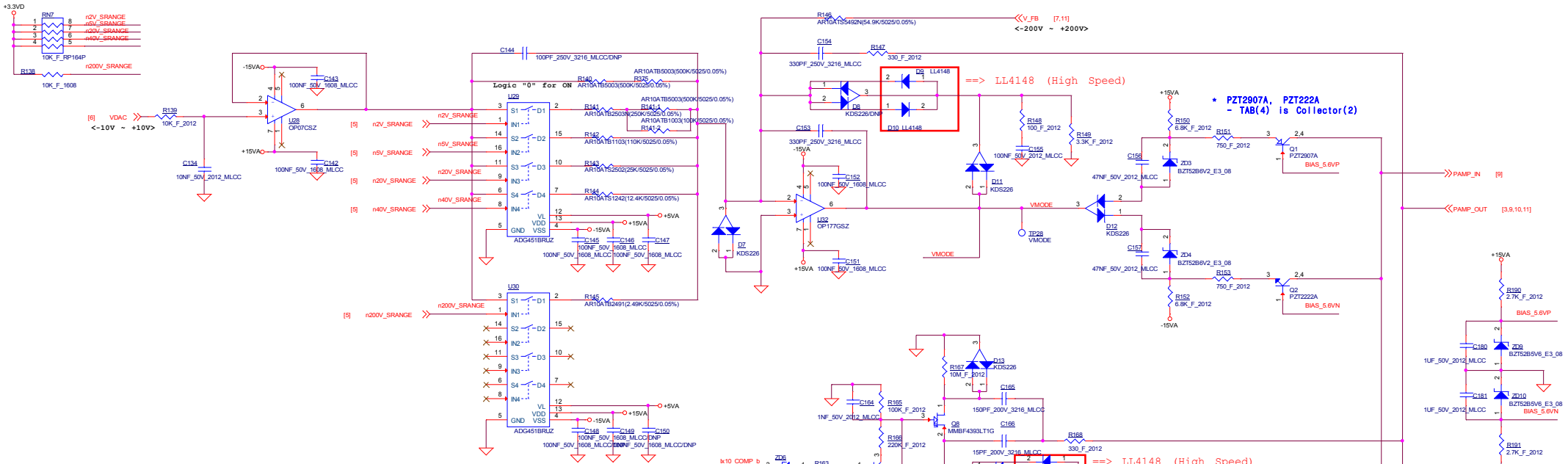
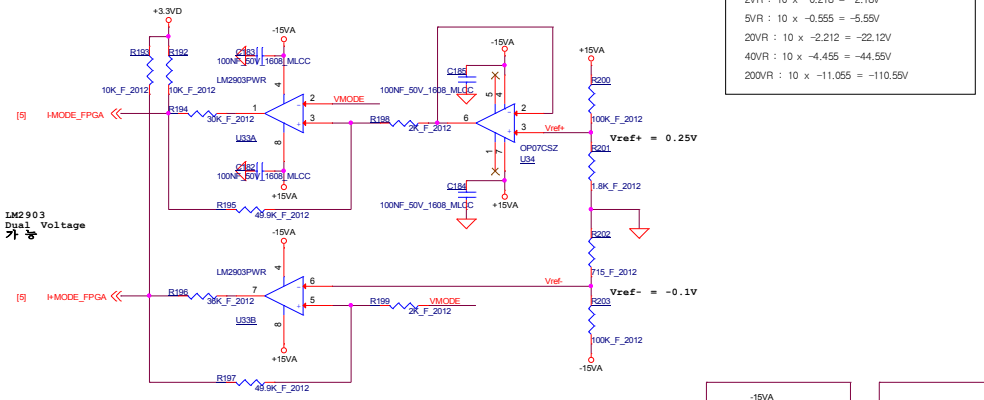
Title: [E8000]HL-SMU		TEAM TM개발1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A3	07. 1CH_FPGA #3 (XC7S50)	YUNSH	JOH JH	<OrgAddr3>	1.0
Date:	Thursday, July 29, 2021	Sheet 7	of 24		

S RANGE



MODE DETECT CIRCUIT

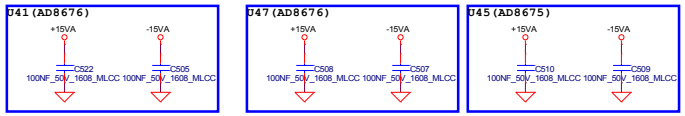


0.5VR : 10 x −0.055 = −0.55V
2VR : 10 x −0.218 = −2.18V
5VR : 10 x −0.555 = −5.55V
20VR : 10 x −2.212 = −22.12V
40VR : 10 x −4.455 = −44.55V
200VR : 10 x −11.055 = −110.55V

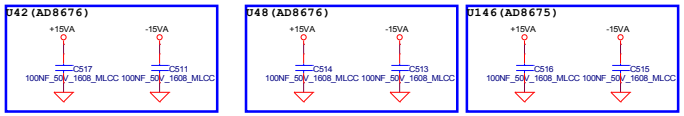
ERROR AMP CONTROL

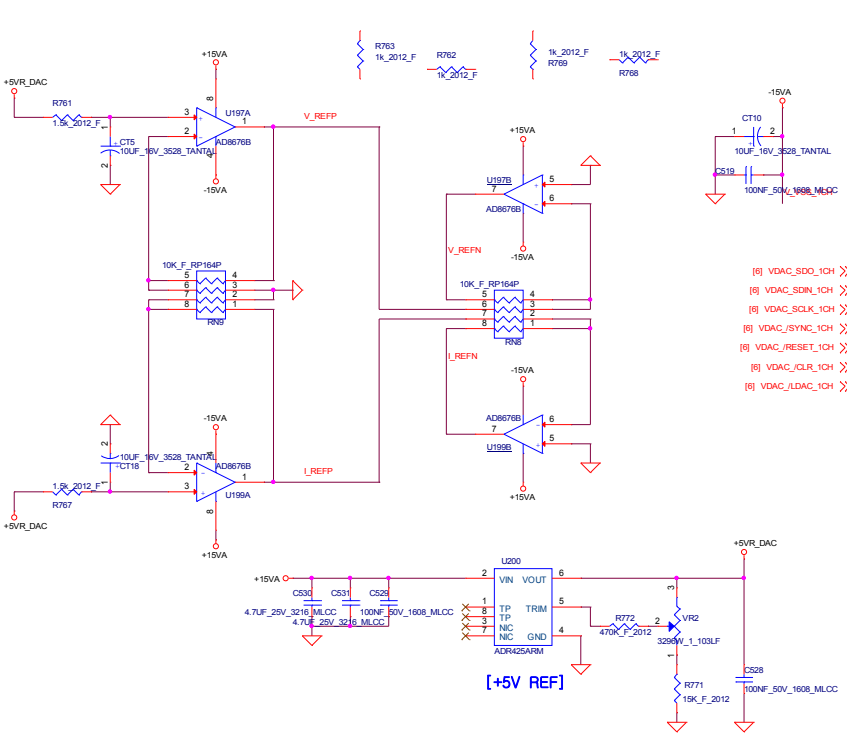
Title: High Resolution SMU		TEAM	ITM개발1팀		
Size	Document Number	Designed	Checked	Approved	Rev
A2	08. ERROR AMP	DH YOO	Seol YK	DH YOO	1.0
Date: Tuesday, July 27, 2021		Sheet 8 of 12			

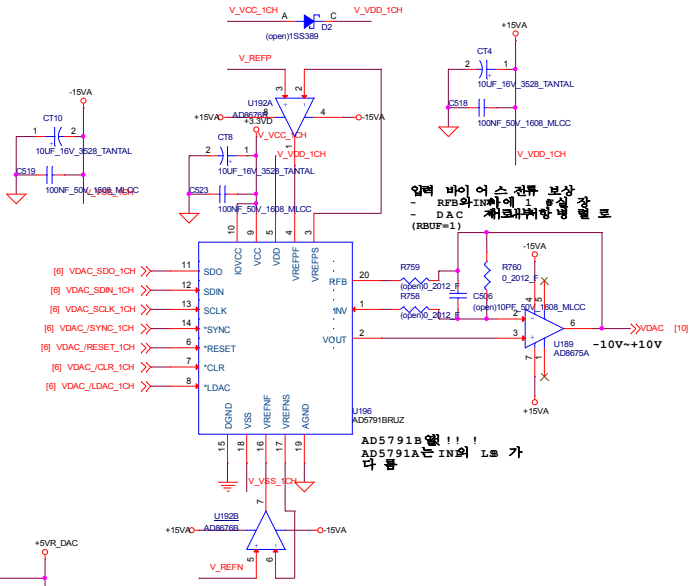
VDAC(1CH)

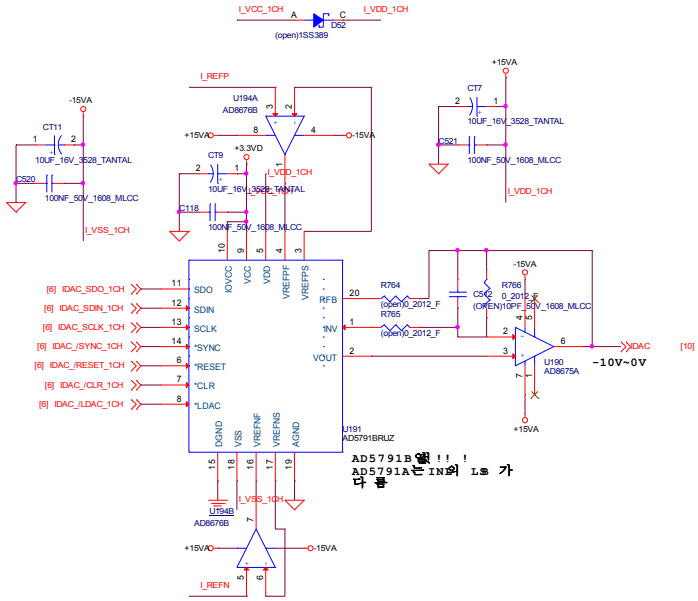


IDAC(1CH)

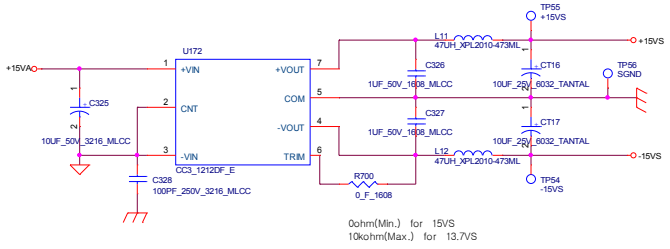






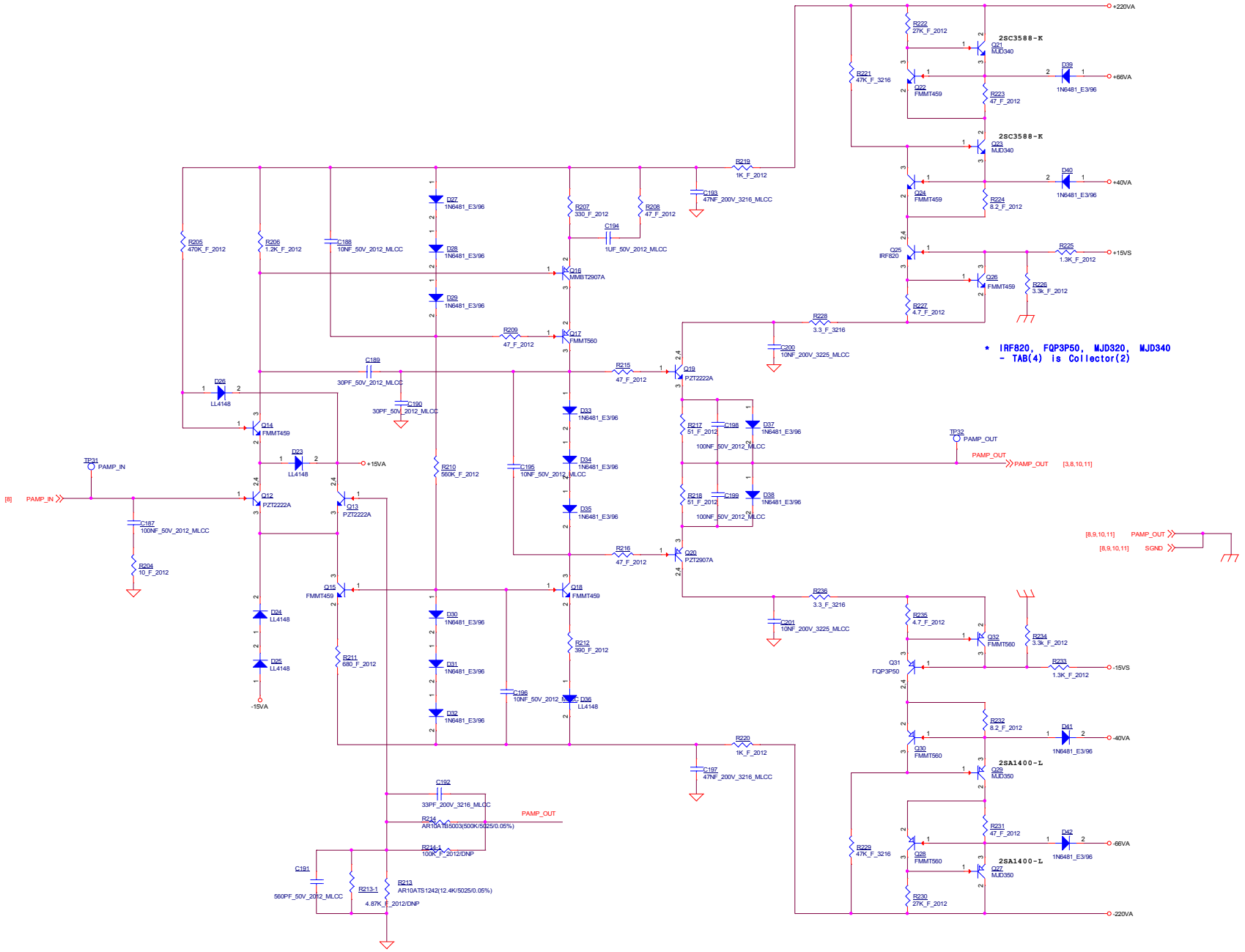


Isolated DC-DC Converter (Floating Power)



Title	[E8000]HL-SMU		
Size A2	Document Number 06.1CH_DAC		Rev 1.0
Date: Thursday, July 29, 2021	Sheet 8 of 24		

POWER AMP



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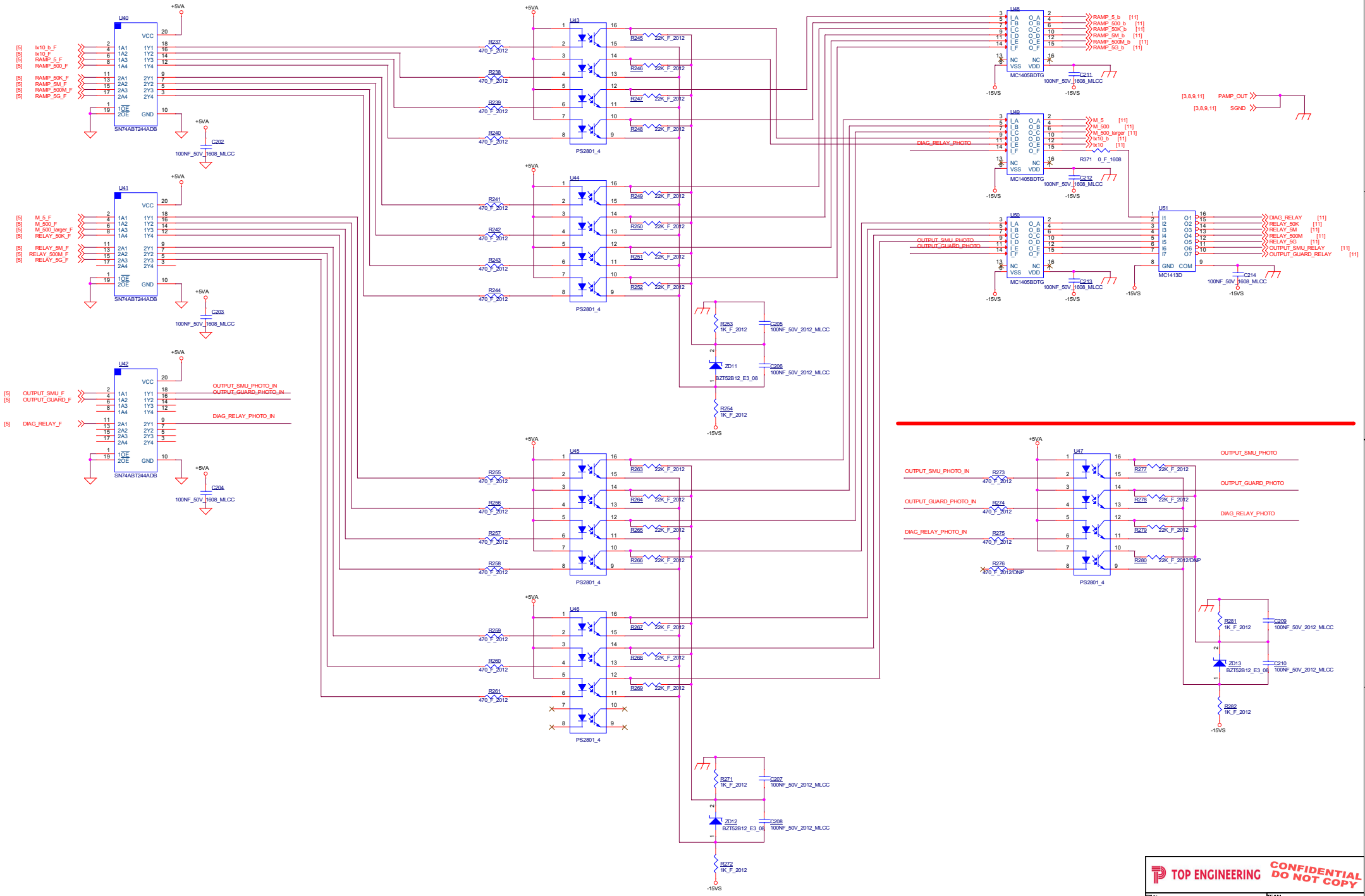
Title: High Resolution SMU		TEAM 제2기 받1팀			
Size	Document Number	Designed	Checked	Approved	Rev
A2	09. POWER AMP	DH YOO	Seol YK	DH YOO	1.0
Date: Monday, July 26, 2021		Sheet 9 of 12			

CONTROL SIGNAL BUFFER

SIGNAL ISOLATE

I RANGE CONTROL



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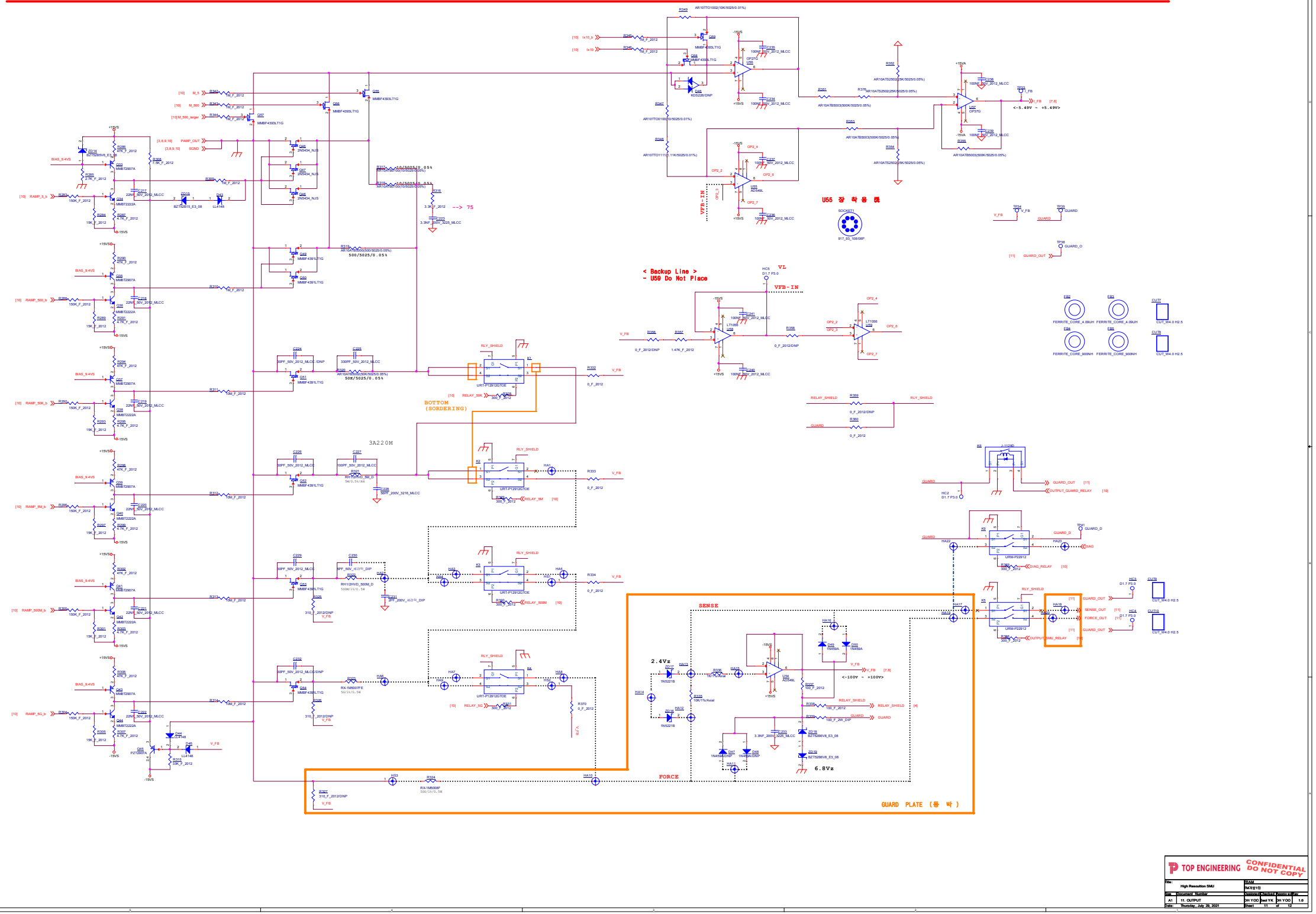
Title: High Resolution SMU			TEAM		
			개인 1팀		
Size	Document Number		Designed	Checked	Approved	Rev
A2	10. OUTPUT CONTROL		DH YOO	Seol YK	DH YOO	1.0
Date:	Monday, July 26, 2021	Sheet	10	of	12	


< Backup Line >
- U59 Do Not Place
U55 장 착 용 캡
SOCKET1
917_93_108/08P
BOTTOM
(SORDERING)
SENSE
FORCE
GUARD PLATE (동 박)
2.4Vz
6.8Vz
<-5.49V ~ +5.49V>
<-100V ~ +100V>
VFB-IN
VL
3A220M
FERRITE_CORE_4.09UH
FERRITE_CORE_900NH
CUT_W4.0 H2.5
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High Resolution SMU
TEAM
Document Number
Revision
Sheet of
Date: Thursday, July 29, 2021

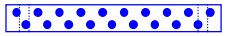
JIG1

PERPIN_POGO_PIN_COVER

JIG2

HRSMU_INPUT_SHIELD_COVER

JIG3



HRSMU_SHIELD_COVER

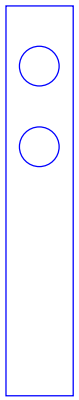
JIG4

HRSMU_BOTTOM

JIG5

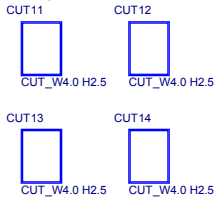
HRSMU_AMP_COVER

JIG6

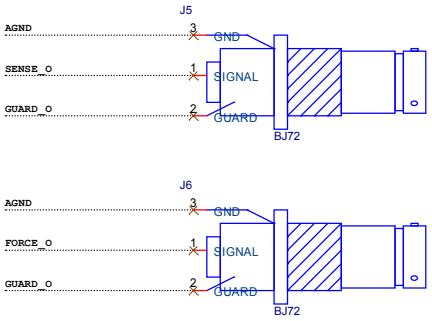


HRSMU_FRONT_COVER

Tri Axial 케이블 고정 홀



전면판 커넥터



PST에서는 전면판 Triaxial 커넥터 (BJ72)에 연결

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Title: High Resoultion SMU			TEAM TM개발1팀		
Size	Document Number		Designed	Checked	Approved	Rev
A3	12. JIG		Seol YK	Seol YK	DH YOO	1.0
Date: Monday, July 26, 2021			Sheet 12 of 12		