SNES S-DSP Pinout by <u>Jonathon W. Donaldson (jwdonal)</u> (special thanks to <u>Martin Korth (nocash)</u>)

Color Colo	Designator	Name	Desc	QFP80P1870X2470-	90M	Type	Owner	Show	Number Name
2	Designator					Туре			
MXK	1	DKD		1	Output	1	True	True	DKD
C. 4.576MH-120 INC.	2	MVK		2	Output	1	Truo	Truo	MVV
MX1	2	IVIAN	(3.6188 = 1.608) 3.07210172	2	Output	1	rrue	True	WAN
Phase/duty shifted (NC)	3	MX1		3	Output	1	True	Truo	MX1
MX	١	IVIZ		3	Output	•	Truc	TIUC	WAT
Description Phase duty shifted NC September NC Septe	4	MX2		4	Output	1	True	True	MX2
Phase/duty shifted NC SMP/DSP Multiplexed 6					- mp				
Phase/duty shifted NC SMP/DSP Multiplexed 6	5	MX3	24.576MHz/24 (3pins:	5	Output	1	True	True	MX3
SRAM Data			phase/duty shifted) (NC)		·				
MO	6	MD2		6	I/O	1	True	True	MD2
SRAM Data	_		SRAM Data						ND.
MOD SMP/DSP Multiplexed SMP/DSP Multiplexed SRAM Address SMP/DSP Multiplexed	7	MD1		7	I/O	1	True	True	MD1
SRAM Data SMP/DSF Multiplexed 9	0	MDO		0	1/0	1	Truo	Trus	MDO
SAMPOSP Multiplexed SCAM Address SCAM SCAM Address SCAM Address SCAM Address SCAM Address SCAM Address SCAM Address SCAM Data S	o	MDO		0	1/0	1	rrue	True	MIDU
SRAM Address True	a	ΜΔΩ	SMP/DSP Multipleyed	Q	Output	1	True	Truo	ΜΔΩ
MA1		1417 (0			Odipai	•	1140	1100	1417.10
SRAM Address	10	MA1		10	Output	1	True	True	MA1
SRAM Address 12			SRAM Address	-					
12	11	MA2	SMP/DSP Multiplexed	11	Output	1	True	True	MA2
13									
SRAM Address						-			
MA	13	MA3		13	Output	1	True	True	MA3
SRAM Address	4.4	NAA 4	SRAM Address	4.4	Ott	4	Т	Т	NAA 4
15	14	IVIA4	SDAM Address	14	Output	1	rrue	True	WA4
SRAM Address	15	MA5	SMP/DSP Multiplexed	15	Output	1	True	True	MA5
16	'0	1417 (0		10	Odipai	•	1140	1100	1417.10
SRAM Address 17	16	MA6	SMP/DSP Multiplexed	16	Output	1	True	True	MA6
SRAM Address			SRAM Address						
18	17	MA7		17	Output	1	True	True	MA7
SRAM Address			SRAM Address						
19	18	MA12		18	Output	1	True	True	MA12
SRAM Address SRAM Address SRAM Address SRAM Address NC)	10	NAA 4 4		40	Ott	4	T	T	NAA 4
20	19	WA14		19	Output	1	True	True	WA14
SRAM Address (NC)	20	ΜΔ15	SMP/DSP Multipleyed	20	Output	1	True	True	MA15
Cinstead, upper/lower 32KB Selected via /CE1 and /CE0 21	20	IVIAIO		20	Output	'	Tiue	Tiue	WATS
Selected via /CE1 and /CE0									
DIP									
Column			/CE0)						
22 MD3 SMP/DSP Multiplexed SRAM Data 22 I/O 1 True True MD3 23 MD4 SMP/DSP Multiplexed SRAM Data 23 I/O 1 True True MD4 24 MD5 SMP/DSP Multiplexed SRAM Data 24 I/O 1 True True MD5 25 MD6 SMP/DSP Multiplexed SRAM Data 25 I/O 1 True True MD6 26 MD7 SMP/DSP Multiplexed SRAM Data 26 I/O 1 True True MD7 SRAM Data	21	DIP		21	Passive	1	True	True	DIP
SRAM Data 23			(NC)						
23 MD4 SMP/DSP Multiplexed 23 I/O 1 True True MD4	22	MD3		22	I/O	1	True	True	MD3
SRAM Data	22	MD4		22	1/0	1	Truo	Truo	MD4
24 MD5 SMP/DSP Multiplexed 24 I/O 1 True True MD5 SRAM Data 25 MD6 SMP/DSP Multiplexed 25 I/O 1 True True MD6 SRAM Data 26 MD7 SMP/DSP Multiplexed 26 I/O 1 True True MD7 SRAM Data	23	IVID4		23	1/0	ı	rrue	rrue	IVID4
SRAM Data	24	MD5	SMP/DSP Multipleved	24	I/O	1	True	True	MD5
25 MD6 SMP/DSP Multiplexed 25 I/O 1 True True MD6 SRAM Data 26 MD7 SMP/DSP Multiplexed 26 I/O 1 True True MD7 SRAM Data		נטואו		4 -7	., 0		TTUC	TIUC	WIDO
SRAM Data 26 MD7 SMP/DSP Multiplexed 26 I/O 1 True True MD7 SRAM Data	25	MD6		25	I/O	1	True	True	MD6
SRAM Data	_	-			-				
	26	MD7		26	I/O	1	True	True	MD7
27 C\E\1\ SMP/DSP Multiplexed 27 Output 1 True True C\E\1\									
	27	C\E\1\	SMP/DSP Multiplexed	27	Output	1	True	True	C\E\1\

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Designator	Name	Desc	QFP80P1870X2470-	80M	Туре	Owner	Show	Number Name
		SRAM Chip-Enable (Active-Low) (to upper 32KB)						
28	C/E/0/	SMP/DSP Multiplexed SRAM Chip-Enable (Active-Low) (to lower 32KB)	28	Output	1	True	True	C/E/0/
29	MA10	SMP/DSP Multiplexed SRAM Address	29	Output	1	True	True	MA10
30	O/E/	SMP/DSP Multiplexed SRAM Output-Enable (Active-Low)	30	Output	1	True	True	O/E/
31	MA11	SMP/DSP Multiplexed SRAM Address	31	Output	1	True	True	MA11
32	MA9	SMP/DSP Multiplexed SRAM Address	32	Output	1	True	True	MA9
33	VCC	Supply	33	Power	1	True	True	VCC
34	MA8	SMP/DSP Multiplexed SRAM Address	34	Output	1	True	True	MA8
35	MA13	SMP/DSP Multiplexed SRAM Address	35	Output	1	True	True	MA13
36	W/E/	SMP/DSP Multiplexed SRAM Write-Enable (Active-Low)	36	Output	1	True	True	W\E\
37	TF	Unknown (GND) (wiring TF and/or TK to VCC crashes the SPC700, ie. they seem to mess up CPUK clock or SRAM bus)	37	Input	1	True	True	TF
38	TK	Unknown (GND) (wiring TF and/or TK to VCC crashes the SPC700, ie. they seem to mess up CPUK clock or SRAM bus)	38	Input	1	True	True	TK
39	M\U\T\E\	Mute (to audio amplifier circuit)	39	Output	1	True	True	M\U\T\E\
40	MCK	64000Hz (24.576MHz/24/16) (NC)	40	Output	1	True	True	MCK
41	SCLK	3.072MHz (24.576MHz/8) (via inverters to CIC chip)	41	Output	1	True	True	SCLK
42	BCK	DAC Bit Clock, 1.536MHz (24.576/16) (to uPD6376)	42	Output	1	True	True	BCK
43	LRCK	DAC Left/Right Clock, 32000Hz (24.576MHz/16/48) (to uPD6376)	43	Output	1	True	True	LRCK
44	DATA	DAC Serial Data (8xZeroPadding+16xData) (to uPD6376)	44	Output	1	True	True	DATA
45	XTALO	24.576MHz Osc	45	Output	1	True	True	XTALO
46	XTALI	24.576MHz Osc	46	Input	1	True	True	XTALI
47			47	Output	1	True	True	RIEISIEITI
48	CPUK	2.048MHz (24.576MHz/12) (to S-SMP)	48	Output	1	True	True	СРИК
49	PD2	MD Bus tri-state control signal used when S-SMP is accessing SRAM (from	49	Input	1	True	True	PD2

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Designator	Name	Desc	QFP80P1870X24	70-80M	Туре	Owner	Show	Number Name
Designator	Ivaille	S-SMP)	Q11 001 1070A24	7 0-00IVI	Турс	OWITE	SHOW	Nullipel Name
50	PD3	CPUK Clock-Enable used	50	Output	1	True	True	PD3
30	1 03	to create effective SMP	30	Output	'	True	Tiue	1 03
		frequency of 1.024MHz (to						
		S-SMP)						
51	D0	S-SMP SRAM Data	51	I/O	1	True	True	D0
52	VSS	Supply	52	Power	1	True	True	VSS
53	D1	S-SMP SRAM Data	53	I/O	1	True	True	D1
54	D2	S-SMP SRAM Data	54	I/O	1	True	True	D2
55	D3	S-SMP SRAM Data	55	I/O	1	True	True	D3
56	D4	S-SMP SRAM Data	56	I/O	1	True	True	D4
57	D5	S-SMP SRAM Data	57	I/O	1	True	True	D5
58	D6	S-SMP SRAM Data	58	I/O	1	True	True	D6
59	D7	S-SMP SRAM Data	59	I/O	1	True	True	D7
60	A0	S-SMP SRAM Address	60	Input	1	True	True	A0
61	A1	S-SMP SRAM Address	61	Input	1	True	True	A1
62	A2	S-SMP SRAM Address	62	Input	1	True	True	A2
63	A3	S-SMP SRAM Address	63	Input	1	True	True	A3
64	A4	S-SMP SRAM Address	64	Input	1	True	True	A4
65	A5	S-SMP SRAM Address	65	Input	1	True	True	A5
66	A6	S-SMP SRAM Address	66	Input	1	True	True	A6
67	A7	S-SMP SRAM Address	67	Input	1	True	True	A7
68	A8	S-SMP SRAM Address	68	Input	1	True	True	A8
69	A9	S-SMP SRAM Address	69	Input	1	True	True	A9
70	A10	S-SMP SRAM Address	70	Input	1	True	True	A10
71	A11	S-SMP SRAM Address	71	Input	1	True	True	A11
72	A12	S-SMP SRAM Address	72	Input	1	True	True	A12
73	VCC	Supply	73	Power	1	True	True	VCC
74	A13	S-SMP SRAM Address	74	Input	1	True	True	A13
75	A14	S-SMP SRAM Address	75	Input	1	True	True	A14
76	A15	S-SMP SRAM Address	76	Input	1	True	True	A15
77	XCK	24.576MHz (24.576MHz/1)	77	Output	1	True	True	XCK
		(NC)						
78	DCK	8.192MHz (24.576MHz/3)	78	Output	1	True	True	DCK
		(to Expansion Port)						
79	CK1	12.288MHz (24.576MHz/2)	79	Output	1	True	True	CK1
		(NC)						
80	CK2	6.144MHz (24.576MHz/4)	80	Output	1	True	True	CK2
		(NC)						

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