SNES S-WRAM Pinout by [Jonathon W. Donaldson (jwdonal)](#) (special thanks to [Martin Korth (nocash)](#))

Designator	Name	Desc	SOP80P1425-64M	Type	Owner	Show	Number	Name
1	VCC	Supply	1	Power	1	True	True	VCC
2	D4	5A22 Data Bus	2	I/O	1	True	True	D4
3	D5	5A22 Data Bus	3	I/O	1	True	True	D5
4	D6	5A22 Data Bus	4	I/O	1	True	True	D6
5	D7	5A22 Data Bus	5	I/O	1	True	True	D7
6	SYSCK	5A22 System Clock (most likely the current memory access cycle clock, i.e. 3.58MHz, 2.68MHz, or 1.79MHz)	6	Input	1	True	True	SYSCK
7	REFRESH	DRAM Refresh (from 5A22)	7	Input	1	True	True	REFRESH
8	R\E\S\E\T\	Reset (Active-Low) (from System)	8	Input	1	True	True	R\E\S\E\T\
9	NC		9	Passive	1	False	True	NC
10	CS1	Chip-Select 1 (VCC)	10	Input	1	True	True	CS1
11	CS2	Chip-Select 2 (VCC)	11	Input	1	True	True	CS2
12	CS3	Chip-Select 3 (VCC)	12	Input	1	True	True	CS3
13	C\S\1\	Chip-Select 1 (Active-Low) (GND)	13	Input	1	True	True	C\S\1\
14	C\S\2\	Chip-Select 2 (Active-Low) (GND)	14	Input	1	True	True	C\S\2\
15	C\S\3\	Chip-Select 3 (Active-Low) (from 5A22)	15	Input	1	True	True	C\S\3\
16	VCC	Supply	16	Power	1	True	True	VCC
17	GND	Supply	17	Power	1	True	True	GND
18	NC		18	Passive	1	False	True	NC
19	NC		19	Passive	1	False	True	NC
20	NC		20	Passive	1	False	True	NC
21	NC		21	Passive	1	False	True	NC
22	NC		22	Passive	1	False	True	NC
23	A0	5A22 A-Bus Address	23	Input	1	True	True	A0
24	A9	5A22 A-Bus Address	24	Input	1	True	True	A9
25	A1	5A22 A-Bus Address	25	Input	1	True	True	A1
26	A10	5A22 A-Bus Address	26	Input	1	True	True	A10
27	A2	5A22 A-Bus Address	27	Input	1	True	True	A2
28	A11	5A22 A-Bus Address	28	Input	1	True	True	A11
29	A3	5A22 A-Bus Address	29	Input	1	True	True	A3
30	A12	5A22 A-Bus Address	30	Input	1	True	True	A12
31	A4	5A22 A-Bus Address	31	Input	1	True	True	A4
32	VCC	Supply	32	Power	1	True	True	VCC
33	GND	Supply	33	Power	1	True	True	GND
34	A13	5A22 A-Bus Address	34	Input	1	True	True	A13
35	A5	5A22 A-Bus Address	35	Input	1	True	True	A5
36	A14	5A22 A-Bus Address	36	Input	1	True	True	A14
37	A6	5A22 A-Bus Address	37	Input	1	True	True	A6
38	A15	5A22 A-Bus Address	38	Input	1	True	True	A15
39	A7	5A22 A-Bus Address	39	Input	1	True	True	A7
40	A16	5A22 A-Bus Address	40	Input	1	True	True	A16
41	A8	5A22 A-Bus Address	41	Input	1	True	True	A8
42	ENA	Enable (from 5A22)	42	Input	1	True	True	ENA
43	P\S\1\	5A22 B-Bus Address	43	Input	1	True	True	P\S\1\
44	P\S\2\	5A22 B-Bus Address	44	Input	1	True	True	P\S\2\
45	P\S\3\	5A22 B-Bus Address	45	Input	1	True	True	P\S\3\
46	P\S\4\	5A22 B-Bus Address	46	Input	1	True	True	P\S\4\

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47	P\S\5\	5A22 B-Bus Address	47	Input	1	True	True	P\S\5\
48	GND	Supply	48	Power	1	True	True	GND
49	VCC	Supply	49	Power	1	True	True	VCC
50	PS1	5A22 B-Bus Address	50	Input	1	True	True	PS1
51	PS2	VCC	51	Input	1	True	True	PS2
52	PS3	VCC	52	Input	1	True	True	PS3
53	PA0	5A22 B-Bus Address	53	Input	1	True	True	PA0
54	PA1	5A22 B-Bus Address	54	Input	1	True	True	PA1
55	G	NC	55	Passive	1	True	True	G
56	P\A\R\D\	5A22 B-Bus Read Strobe (Active-Low)	56	Input	1	True	True	P\A\R\D\
57	R\D\	5A22 A-Bus Read Strobe (Active-Low)	57	Input	1	True	True	R\D\
58	P\A\W\R\	5A22 B-Bus Write Strobe (Active-Low)	58	Input	1	True	True	P\A\W\R\
59	W\R\	5A22 A-Bus Write Strobe (Active-Low)	59	Input	1	True	True	W\R\
60	D0	5A22 Data Bus	60	I/O	1	True	True	D0
61	D1	5A22 Data Bus	61	I/O	1	True	True	D1
62	D2	5A22 Data Bus	62	I/O	1	True	True	D2
63	D3	5A22 Data Bus	63	I/O	1	True	True	D3
64	GND	Supply	64	Power	1	True	True	GND