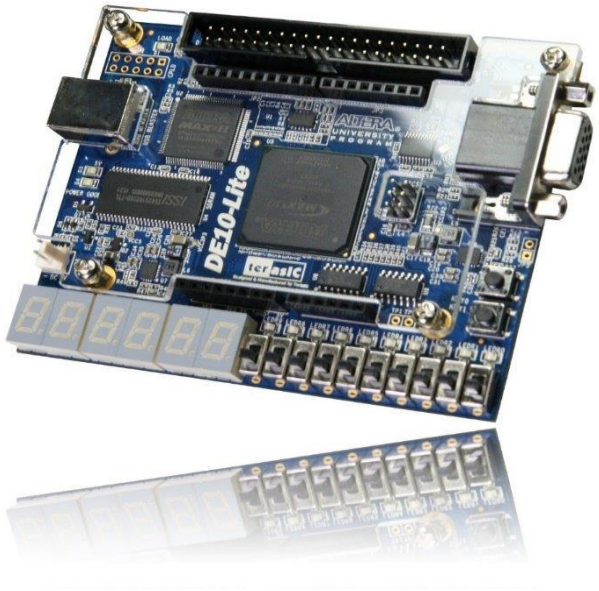



# Sequential

CSIE MIAT Lab.

# 作業

- 請使用七段顯示器，完成一個計數器：

  (1) 範圍為 0 ~ 99

  (2) 當值為 99，下次觸發進位顯示 00，並繼續循環。

  (3) 例如：99 ➔ 00 ➔ 01 ……

- 同組一起完成DEMO，且由一位代表上傳專案壓縮檔，檔名：lab14_Gxx.zip (xx為組別)。

- 註：有DEMO才算分，若當週未完成DEMO，統一於日後公布之日期補DEMO。

# 作業腳位參考

- clk: in std_logic
- btn: in std_logic
- hex0: out std_logic_vector(7 downto 0)
- hex1: out std_logic_vector(7 downto 0)

# 加分

- 請利用作業新增以下功能：

  (1) button[0]：歸零

  (2) button[1]：每次減1

  當值為 00，下次觸發進位顯示 99，並繼續循環。

  例如：00 ➔ 99 ➔ 98 .....

- 同組一起完成DEMO，且由一位代表上傳專案壓縮檔，檔名：lab14_Gxx_bonus.zip (xx為組別)。

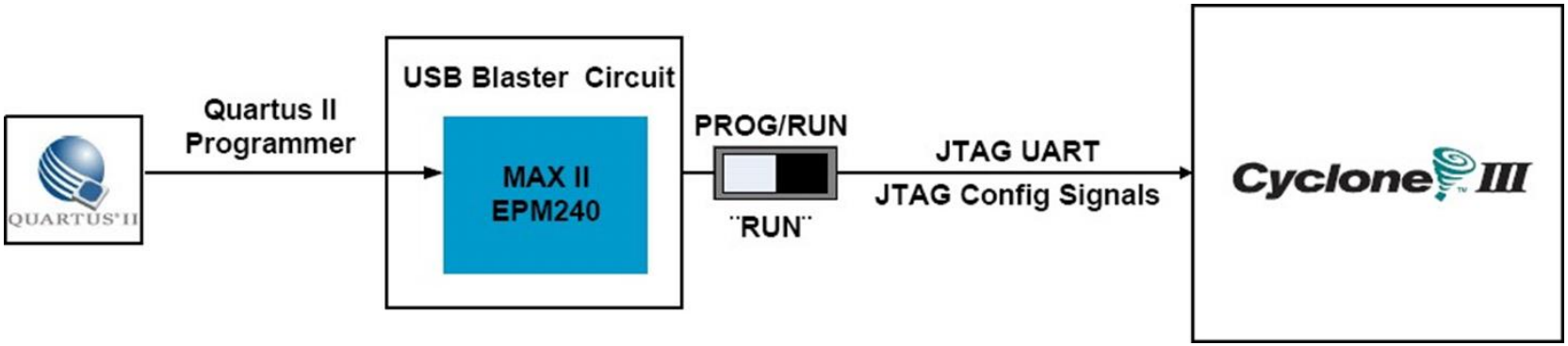
- 註：有DEMO才算分，若當週未完成DEMO，統一於日後公布之日期補DEMO。

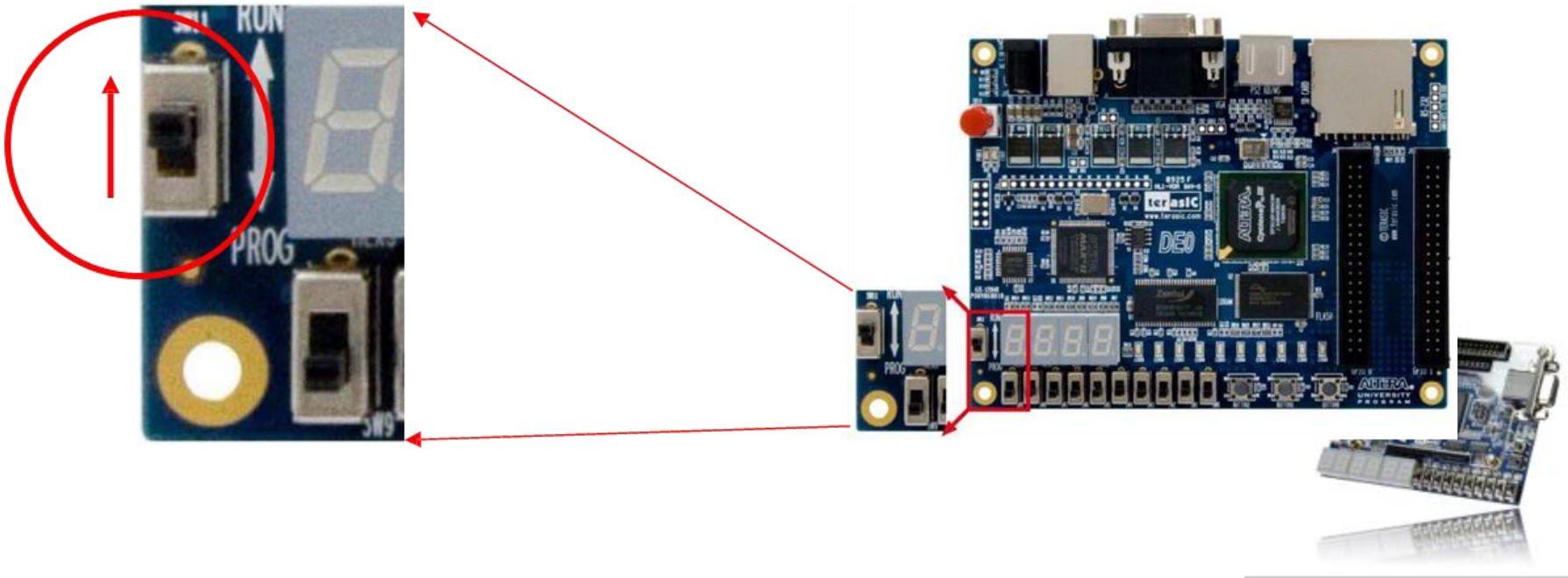
# 範例影片

- 作業：https://youtu.be/_wJ_RwZqcHg
- 加分：https://youtu.be/hdwyxrrdRck

# 模式選取

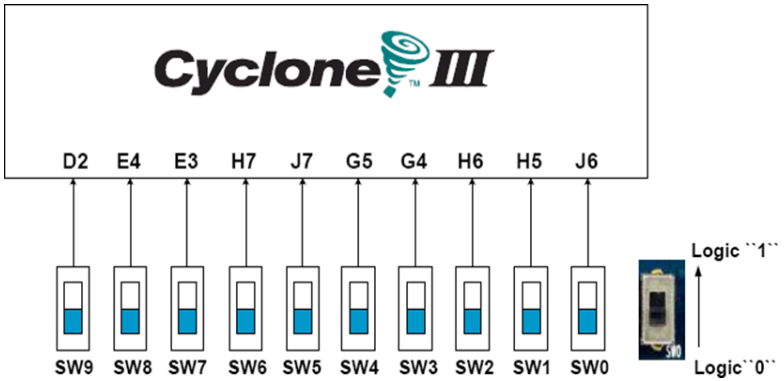
- Switch RUN 設定為 JTAG模式



# Switch 腳位

| Signal Name | FPGA Pin No. | Description |
|---|---|---|
| SW[0] | PIN_J6 | Slide Switch[0] |
| SW[1] | PIN_H5 | Slide Switch[1] |
| SW[2] | PIN_H6 | Slide Switch[2] |
| SW[3] | PIN_G4 | Slide Switch[3] |
| SW[4] | PIN_G5 | Slide Switch[4] |
| SW[5] | PIN_J7 | Slide Switch[5] |
| SW[6] | PIN_H7 | Slide Switch[6] |
| SW[7] | PIN_E3 | Slide Switch[7] |
| SW[8] | PIN_E4 | Slide Switch[8] |
| SW[9] | PIN_D2 | Slide Switch[9] |



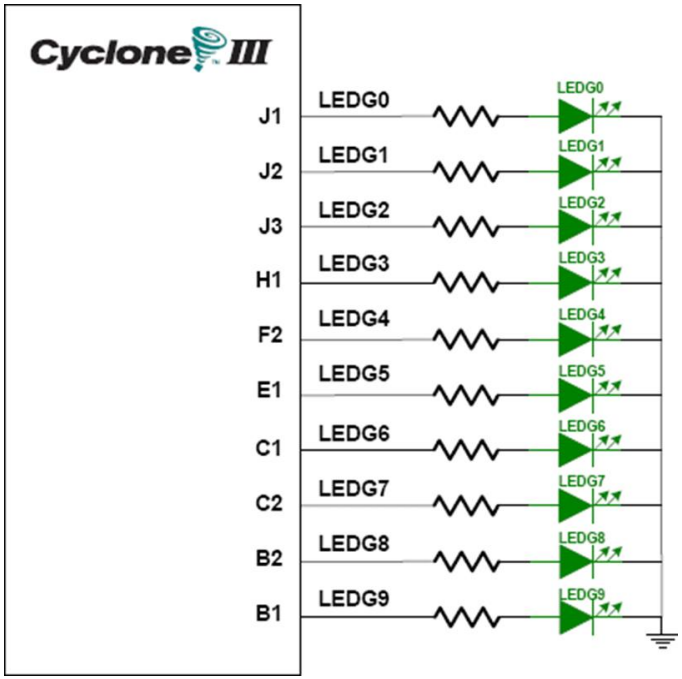

10 Slide switches (Sliders):

Up → Logic High

Down → Logic Low

# LED 腳位

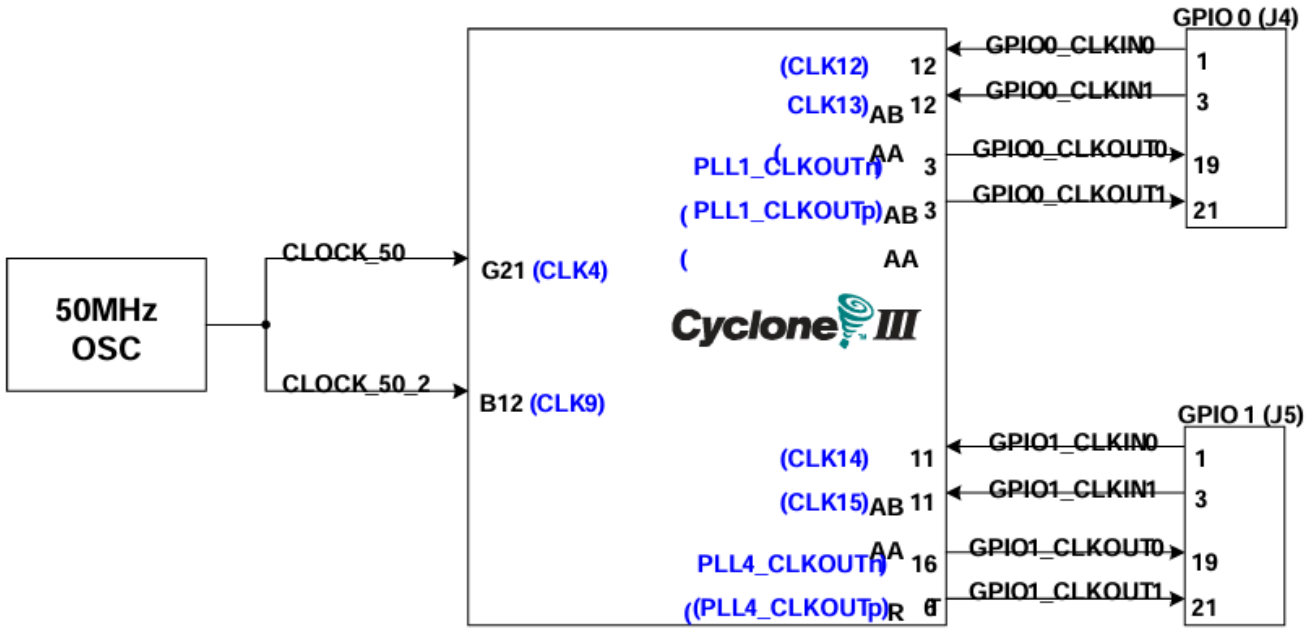
| Signal Name | FPGA Pin No. | Description |
|---|---|---|
| LEDG[0] | PIN_J1 | LED Green[0] |
| LEDG[1] | PIN_J2 | LED Green[1] |
| LEDG[2] | PIN_J3 | LED Green[2] |
| LEDG[3] | PIN_H1 | LED Green[3] |
| LEDG[4] | PIN_F2 | LED Green[4] |
| LEDG[5] | PIN_E1 | LED Green[5] |
| LEDG[6] | PIN_C1 | LED Green[6] |
| LEDG[7] | PIN_C2 | LED Green[7] |
| LEDG[8] | PIN_B2 | LED Green[8] |
| LEDG[9] | PIN_B1 | LED Green[9] |




10 LEDs
Output High → LED ON
Output Low → LED OFF

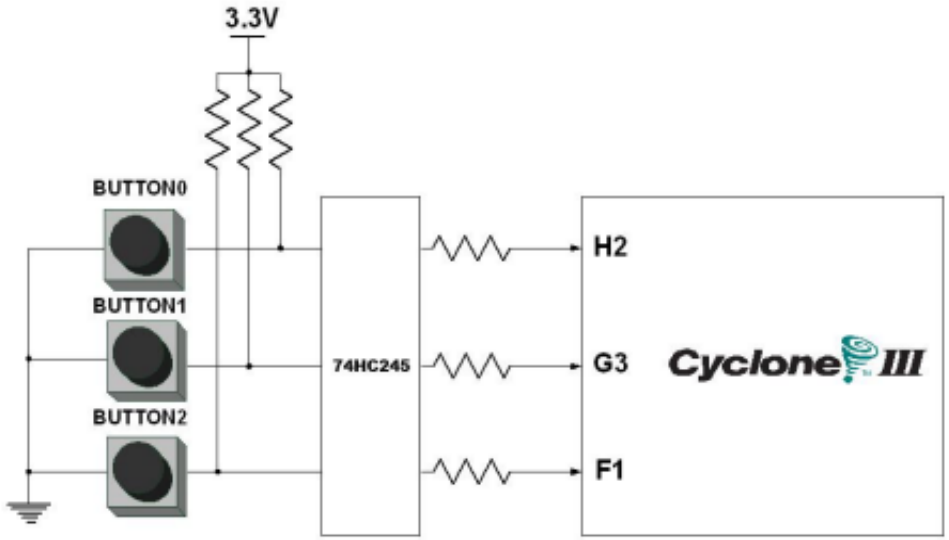
# Clock 腳位

| Signal Name | FPGA Pin No. | Description |
|---|---|---|
| CLOCK_50 | PIN_G21 | 50 MHz clock input |
| CLOCK_50_2 | PIN_B12 | 50 MHz clock input |




# Button 腳位

| Signal Name | FPGA Pin No. | Description |
|---|---|---|
| BUTTON [0] | PIN_ H2 | Pushbutton[0] |
| BUTTON [1] | PIN_ G3 | Pushbutton[1] |
| BUTTON [2] | PIN_ F1 | Pushbutton[2] |

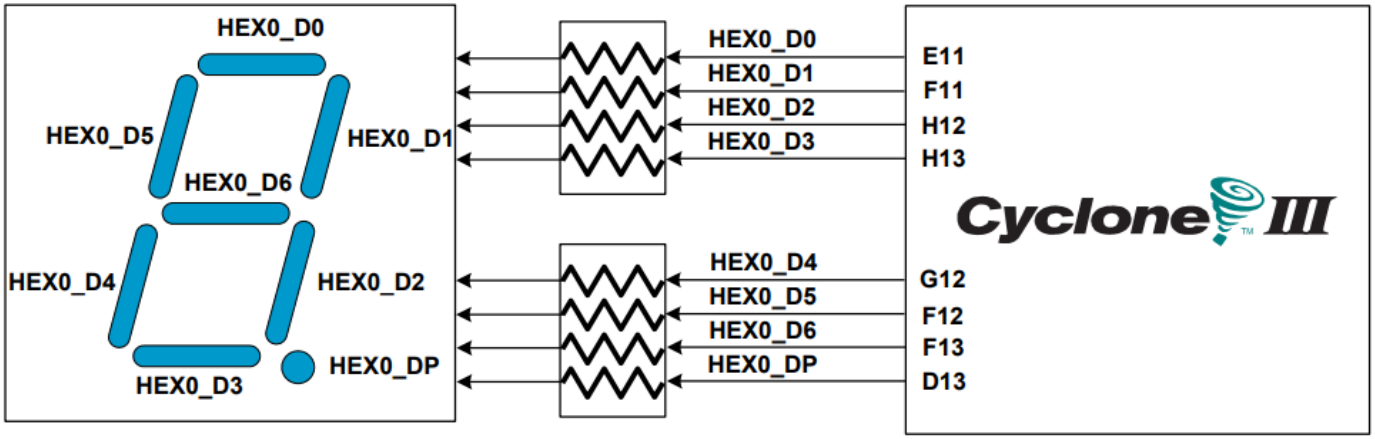



3 Pushbutton:

Not pressed → Logic High

Pressed → Logic Low

# 七段顯示器腳位




| Signal Name | FPGA Pin No. |
|---|---|
| HEX3_D[0] | PIN_B18 |
| HEX3_D[1] | PIN_F15 |
| HEX3_D[2] | PIN_A19 |
| HEX3_D[3] | PIN_B19 |
| HEX3_D[4] | PIN_C19 |
| HEX3_D[5] | PIN_D19 |
| HEX3_D[6] | PIN_G15 |
| HEX3_DP | PIN_G16 |

| Signal Name | FPGA Pin No. |
|---|---|
| HEX2_D[0] | PIN_D15 |
| HEX2_D[1] | PIN_A16 |
| HEX2_D[2] | PIN_B16 |
| HEX2_D[3] | PIN_E15 |
| HEX2_D[4] | PIN_A17 |
| HEX2_D[5] | PIN_B17 |
| HEX2_D[6] | PIN_F14 |
| HEX2_DP | PIN_A18 |

| Signal Name | FPGA Pin No. |
|---|---|
| HEX1_D[0] | PIN_A13 |
| HEX1_D[1] | PIN_B13 |
| HEX1_D[2] | PIN_C13 |
| HEX1_D[3] | PIN_A14 |
| HEX1_D[4] | PIN_B14 |
| HEX1_D[5] | PIN_E14 |
| HEX1_D[6] | PIN_A15 |
| HEX1_DP | PIN_B15 |

| Signal Name | FPGA Pin No. |
|---|---|
| HEX0_D[0] | PIN_E11 |
| HEX0_D[1] | PIN_F11 |
| HEX0_D[2] | PIN_H12 |
| HEX0_D[3] | PIN_H13 |
| HEX0_D[4] | PIN_G12 |
| HEX0_D[5] | PIN_F12 |
| HEX0_D[6] | PIN_F13 |
| HEX0_DP | PIN_D13 |