Model Based Formal Design for MVB System

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Outline

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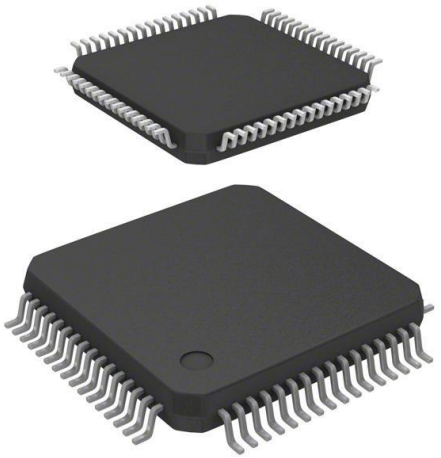
Background

There is a growing demand of computing resources due to the development of artificial intelligence.
CPU and GPU may not fulfill the requirements.
FPGA and ASIC are widely used to accelerate machine learning algorithms, IoT, and other data intensive tasks.



Bottom-up methodology

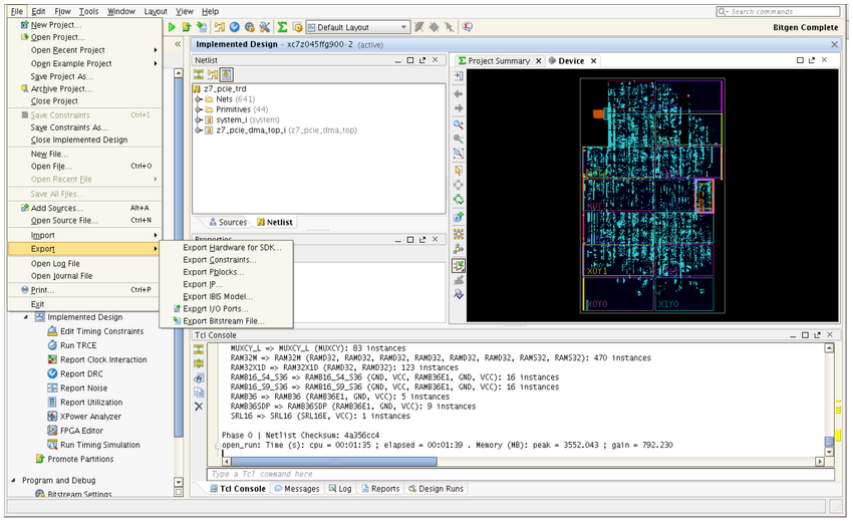
In traditional circuit development, the bottom-up methodology was first used. The design flow is based on basic electronic components, continue to function block components, and finally specify a whole system.

Weakness

- Hardware design must be understood by the designer.
- Developers can only test the design after getting the circuit.
- Hard to develop and maintain.
- ...

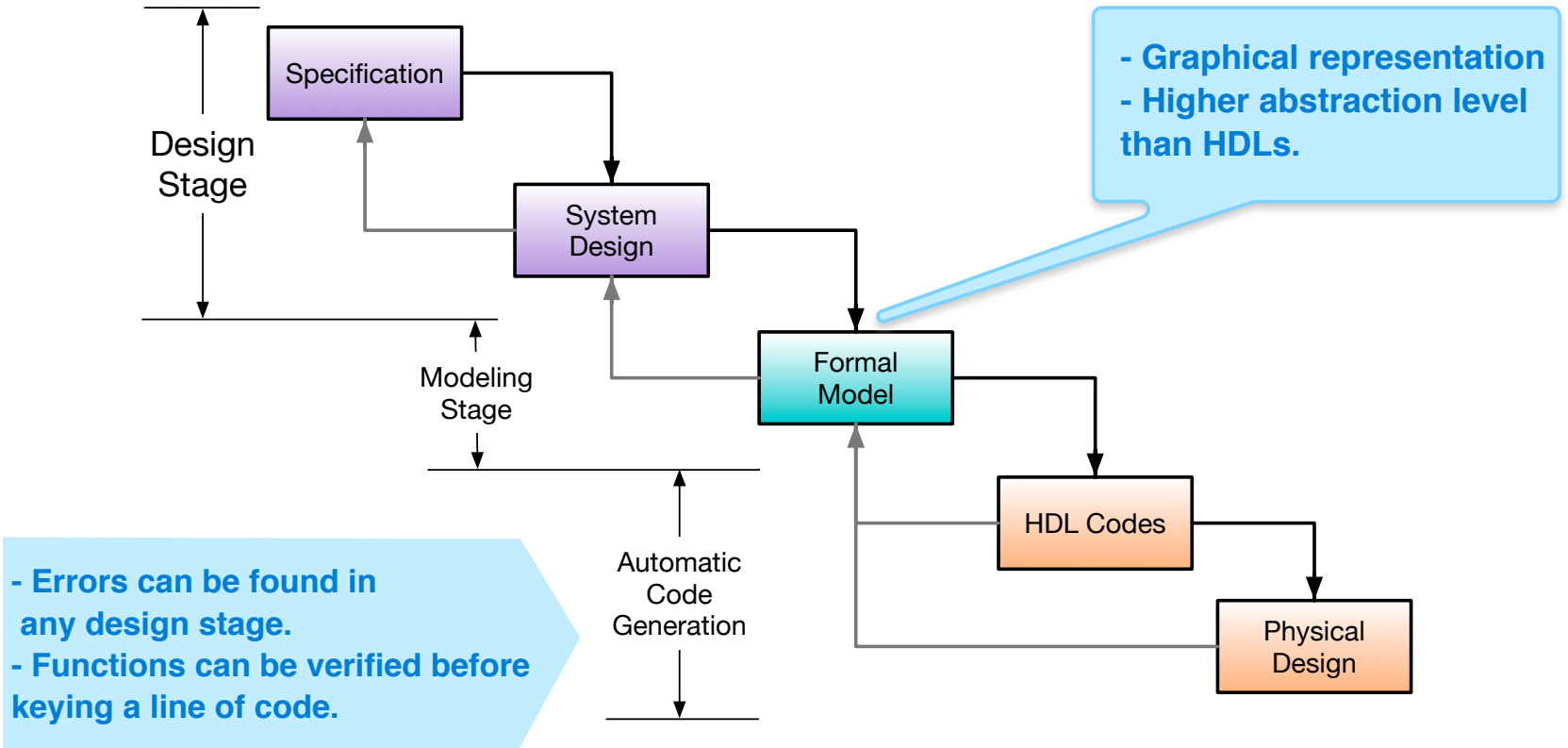
Top-down methodology

- HDLs are used to describe the system behavior.
- The behavior of the system can be verified before getting the real hardware.
- Synthesis tools can translate the design into hardware directly.
- Not good enough.



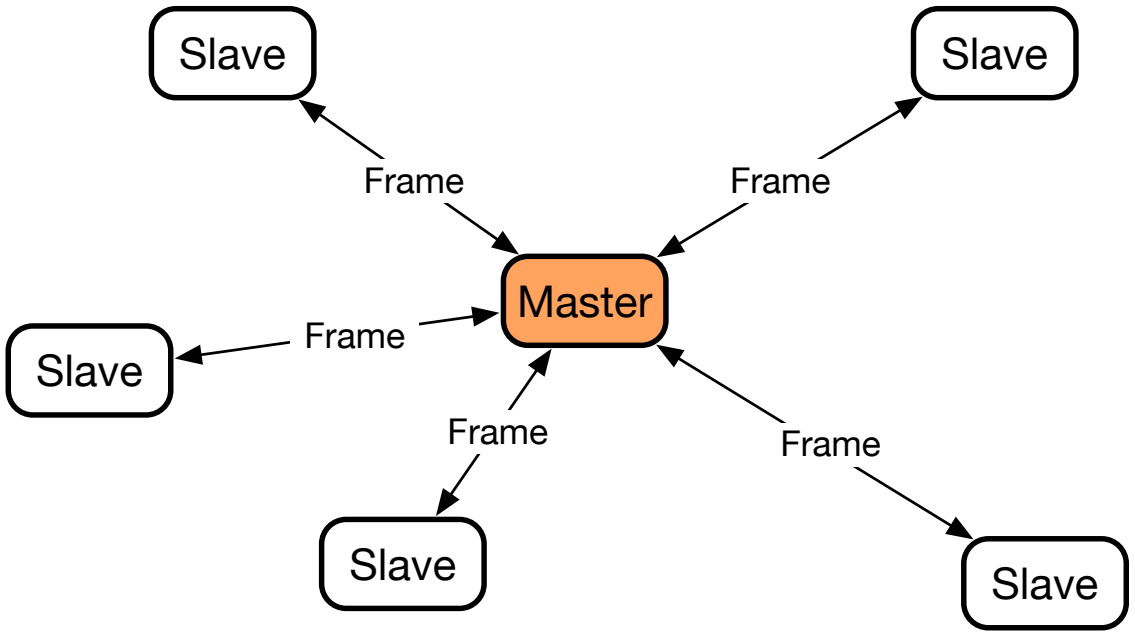
Getting hardware directly by synthesis tools(Xilinx ISE).

Formal modeling method



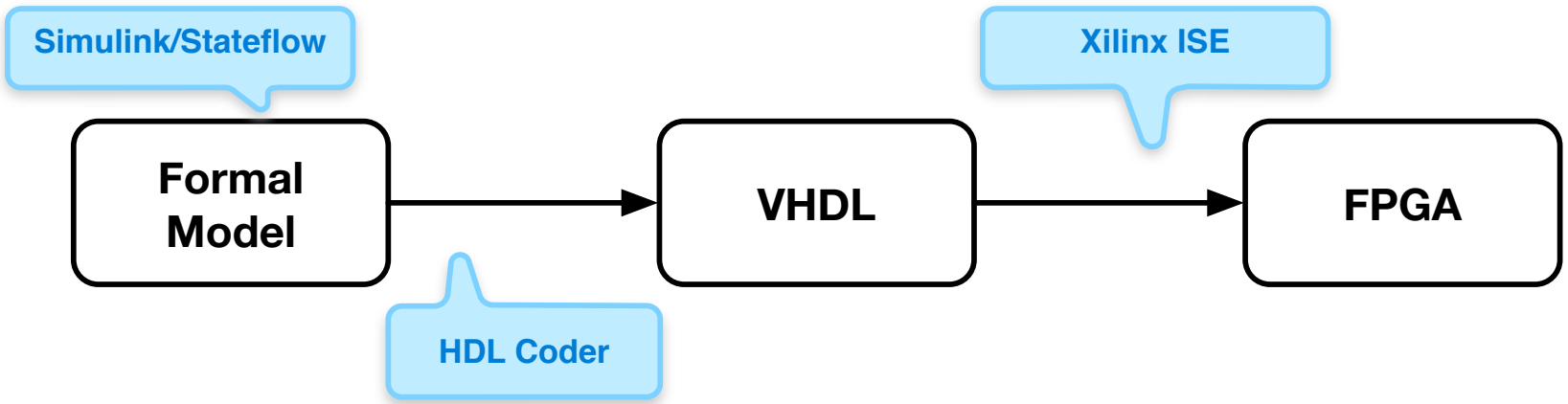
Multifunction Vehicle Bus

Multifunction Vehicle Bus (MVB) is a high-dependency field bus designed for railroad vehicle control systems.
Master-Slave architecture:



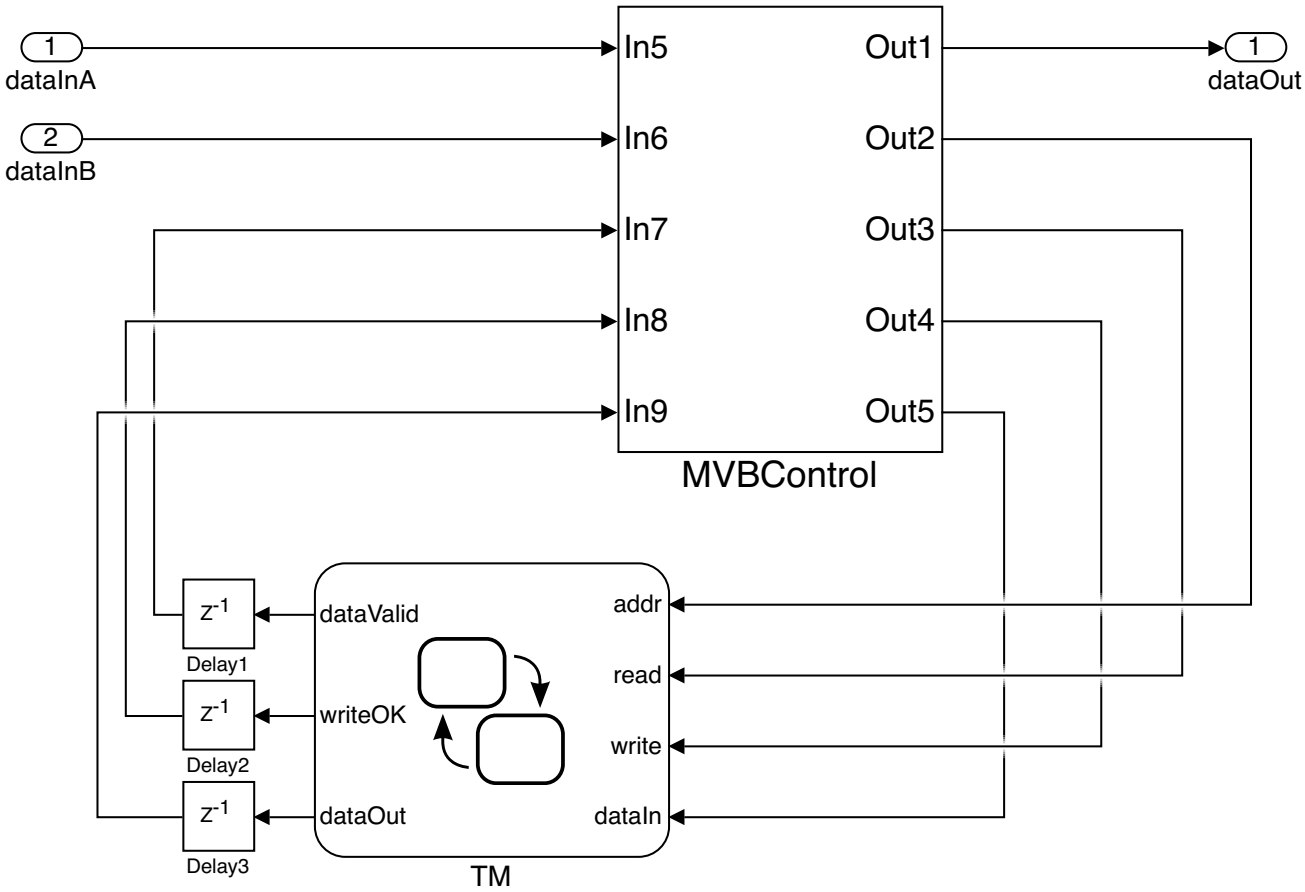
Multifunction Vehicle Bus

- MVB has been developed with HDLs(top-down methodology)
- Few investigations have been published regarding MVB development with formal modeling methods.
- This is the motivation for us to develop MVB with this novel method.

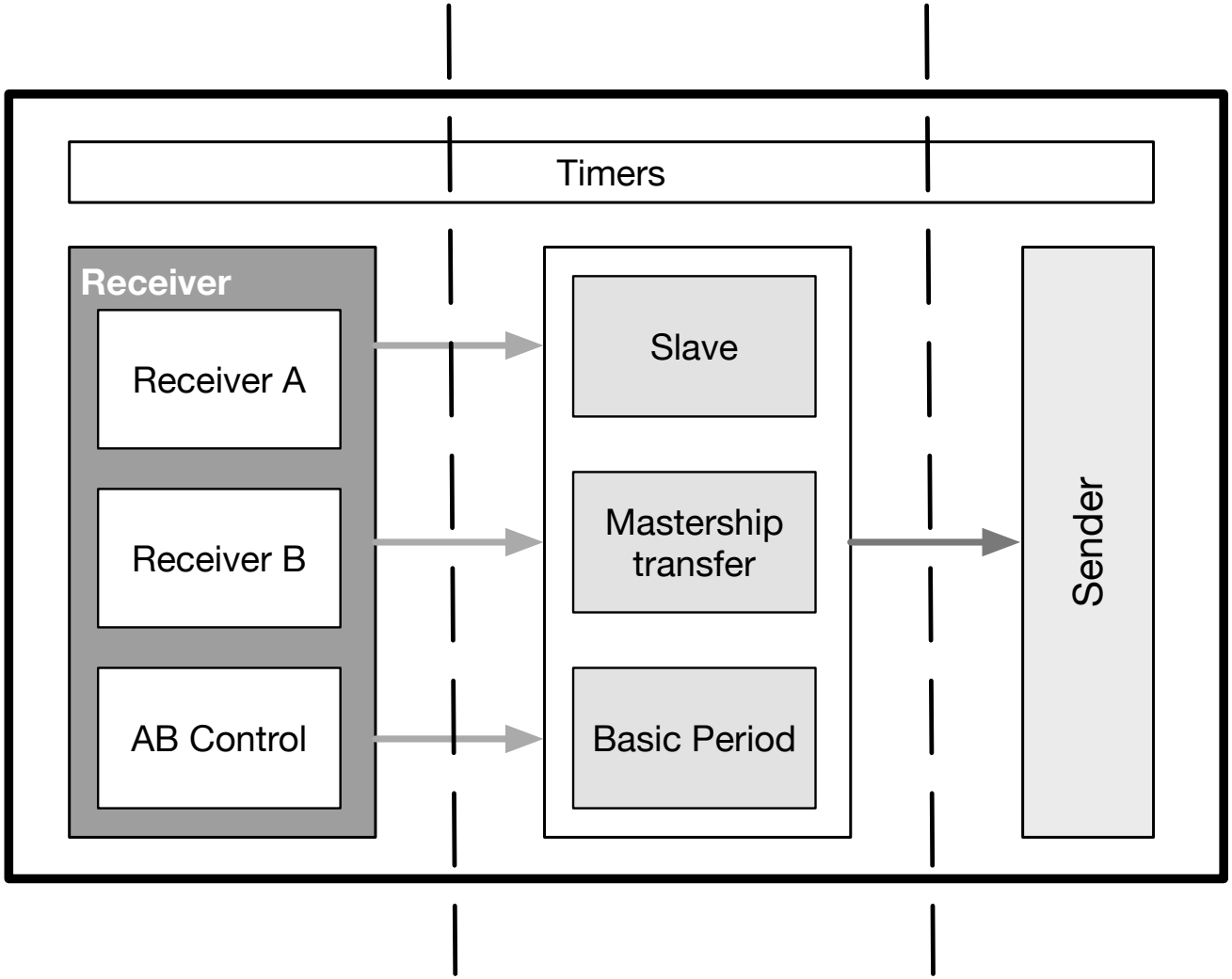


Contents

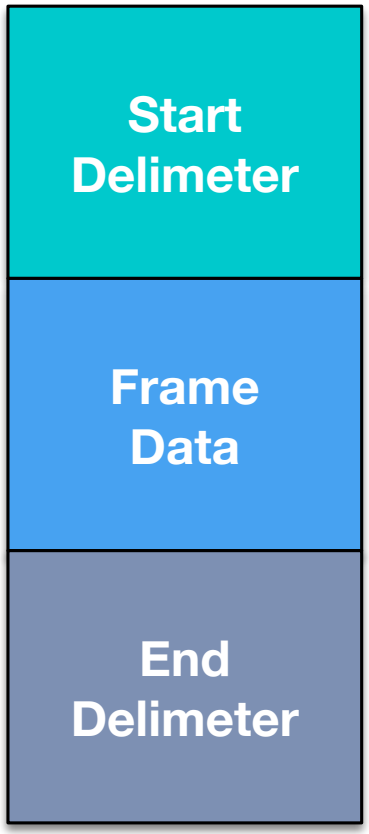
Device design

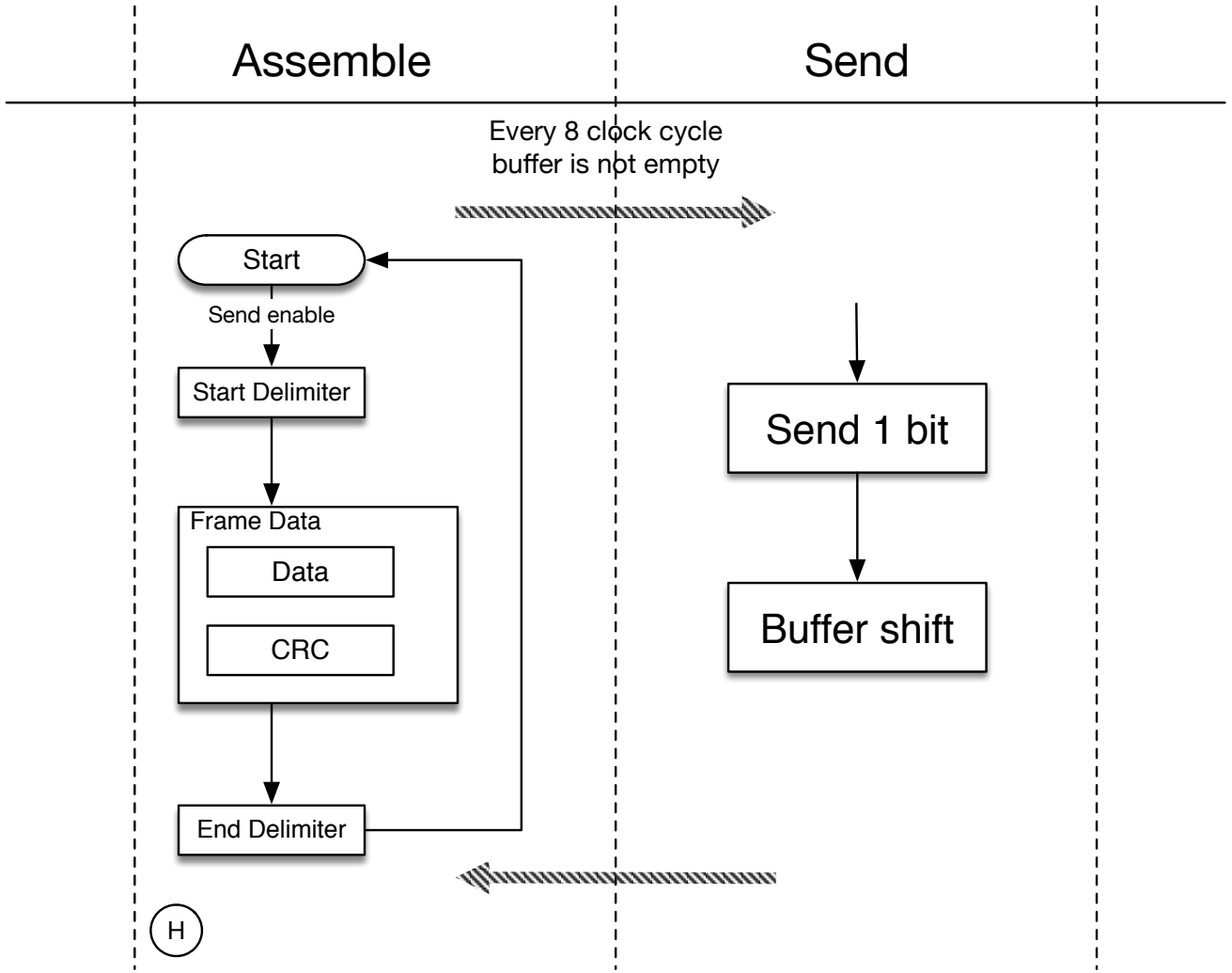


MVB Controller

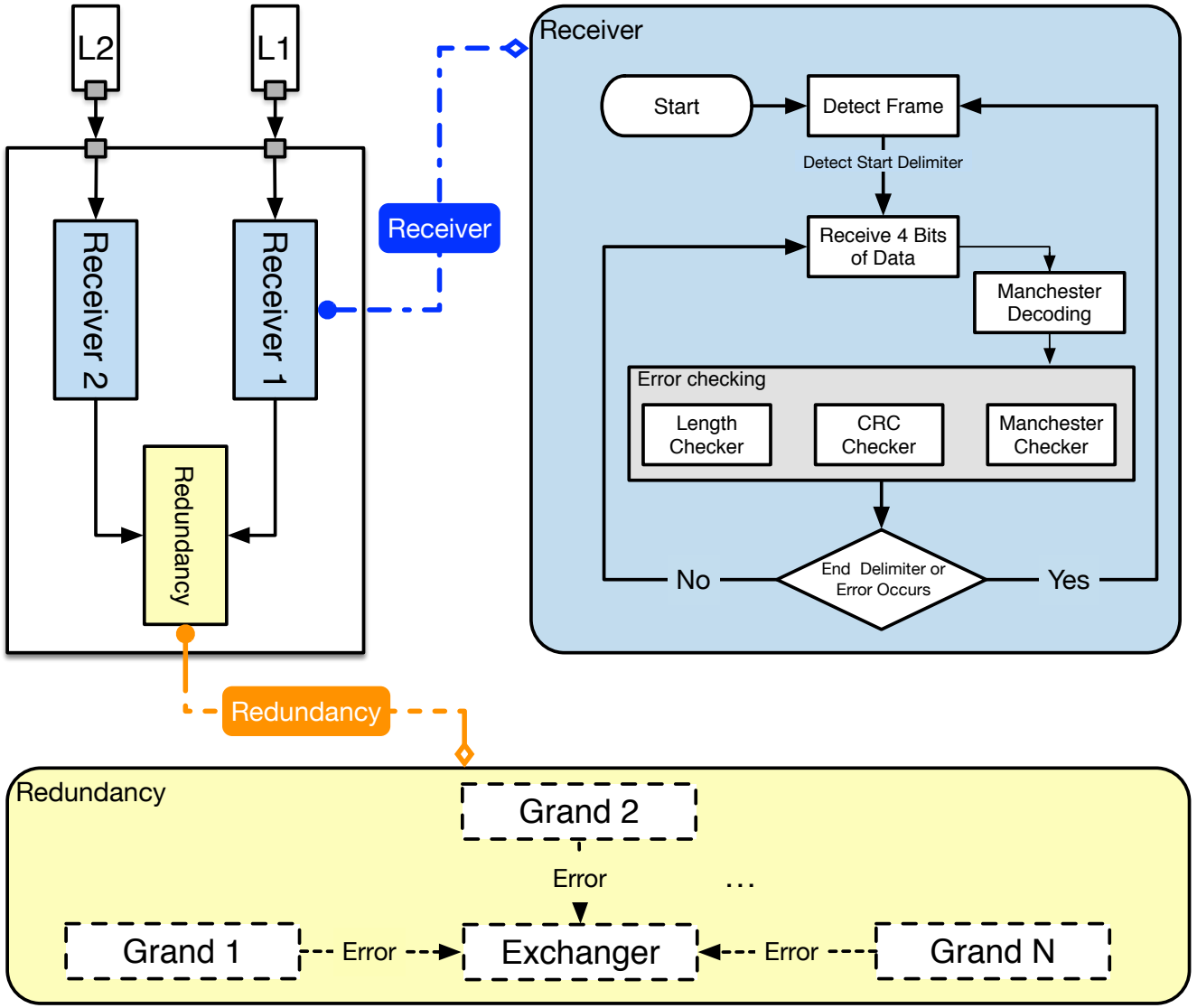


Sender module





Receiver module



Redundancy module

1. If no valid frame has been received from the Trusted_Line for T_switchover since the end of the last valid Master Frame or the last switchover;

2. If the receiver of the Observed_Line detects a valid frame and the receiver of the Trusted_Line detects no valid frame within T_skew_r;

3. If a valid frame has been received over the Trusted_Line, but the check sequence or the frame length is mistaken.

System design

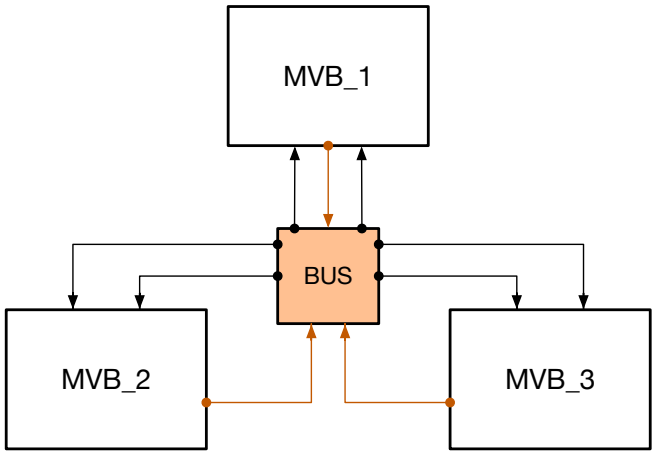


Figure 1: Testing environment

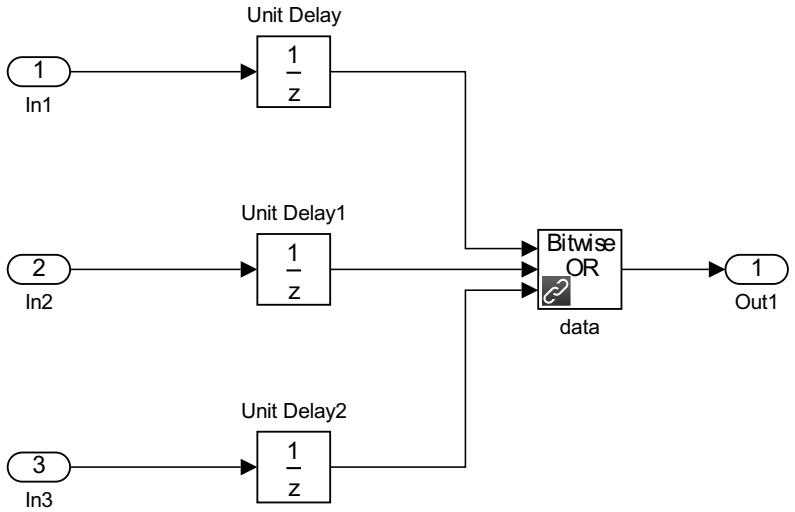


Figure 2: Bus module

Simulation

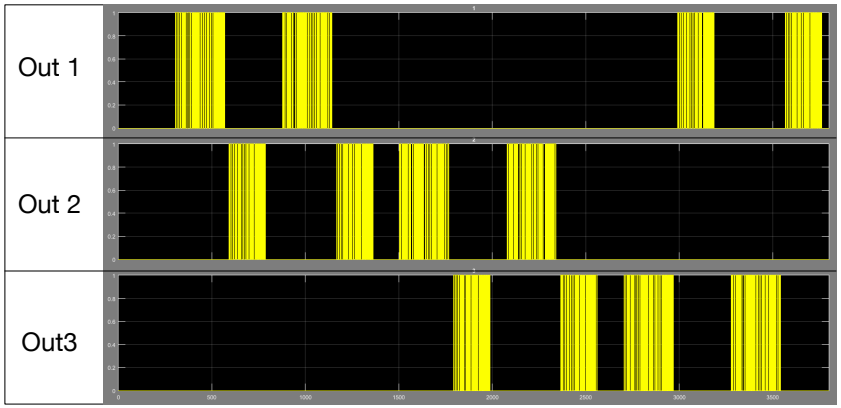


Figure 3: Simulation result of mastership transfer

We have tested the following functions:

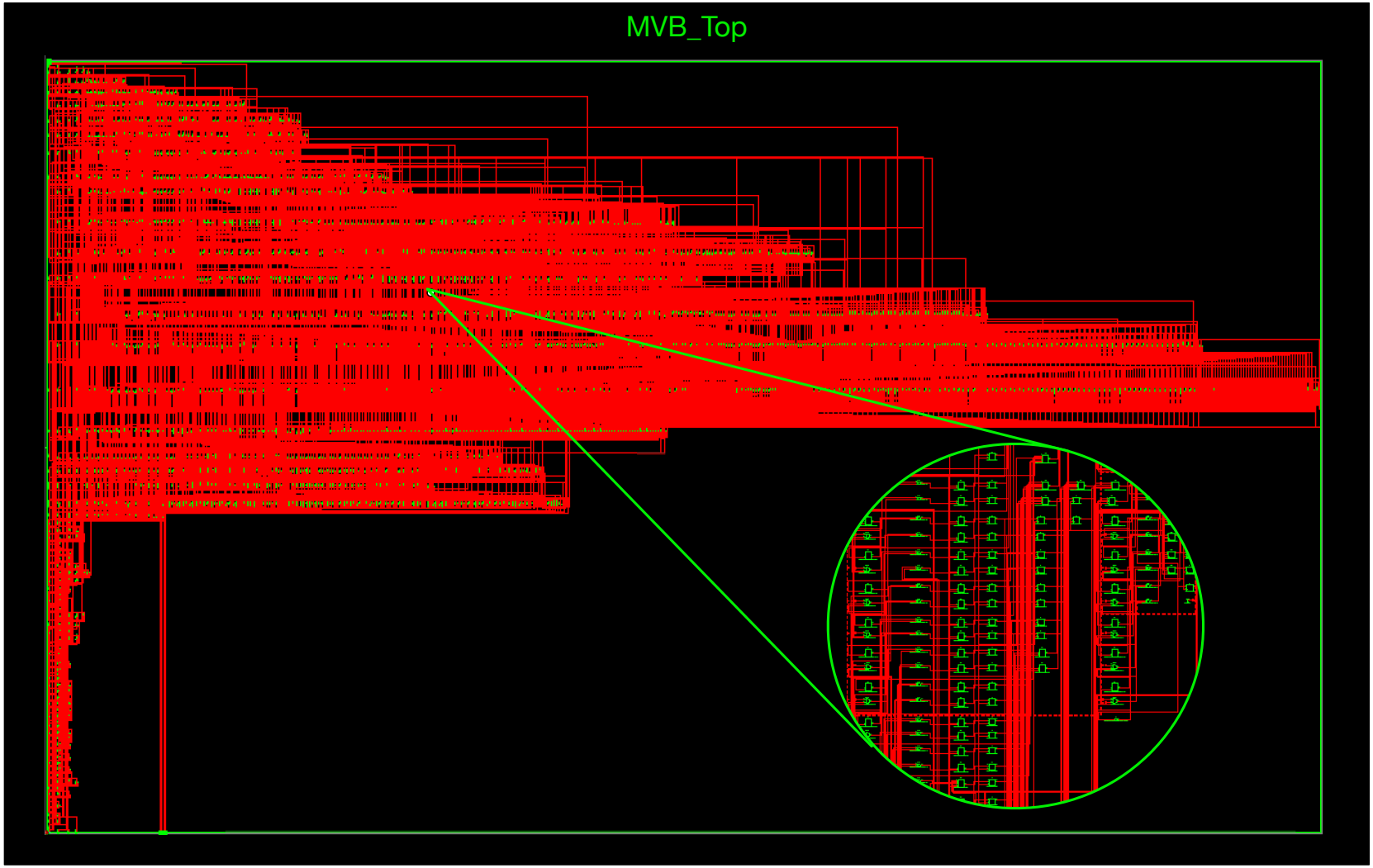
- Clock signal
- Mastership transfer
- Traffic memory
- Data transfer
- Base period
- ...

Constrains

After the model functions have been verified. We translated the model into VHDL codes. Limited by the circuit structure, some functions of formal model are not supported in circuit:

1. Do not call functions recursively.
2. Circling numbers can not be variable.
3. Do not use pointer and address operation.
4. Do not use events.
5. Use no history junctions in states with parallel (AND) decomposition.
6. Do not use Enumerated data, Simulink functions and so on.

Technology schematic



Procedural abstraction

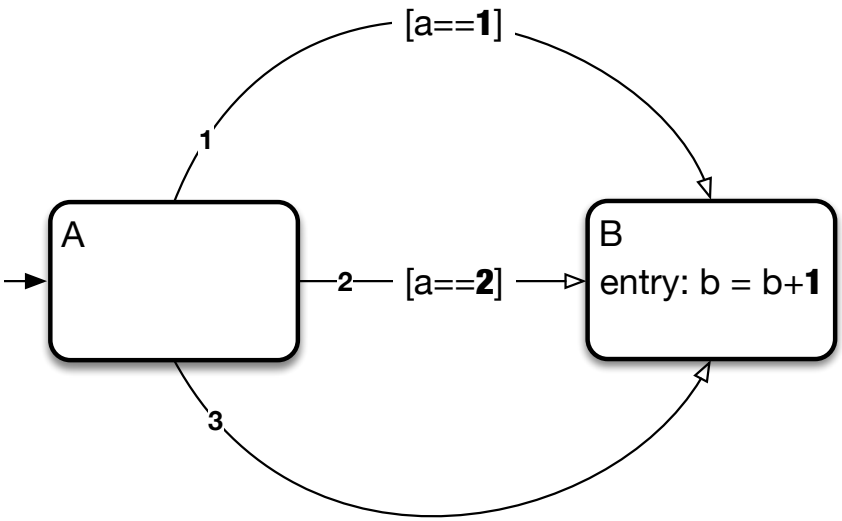


Figure 4: Entry action

```
1  case is_Chart is
2    when IN_A =>
3      if a = 1.0 then
4        is_Chart_next <= IN_B;
5        b_reg_next <= a + 1.0;
6      elsif a = 2.0 then
7        is_Chart_next <= IN_B;
8        b_reg_next <= a + 1.0;
9      else
10       is_Chart_next <= IN_B;
11       b_reg_next <= a + 1.0;
12     end if;
13   when others =>
14     null;
15 end case;
```

Figure 5: Generated code

Procedural abstraction

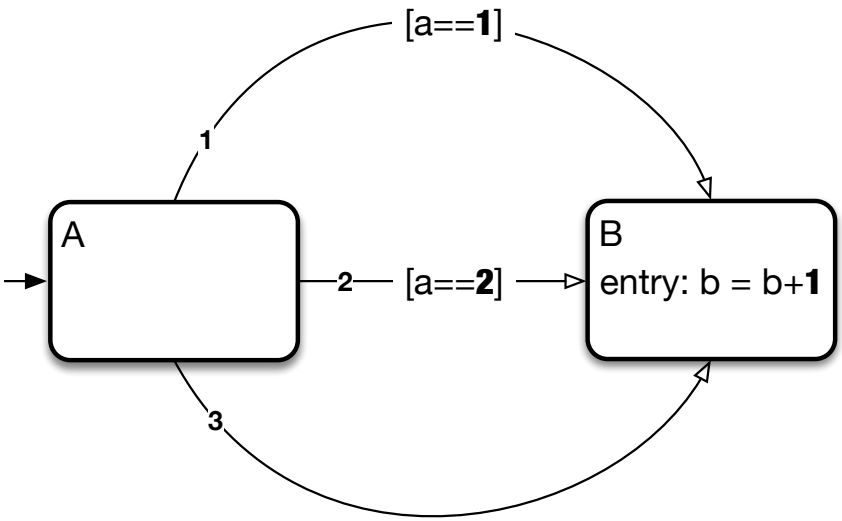


Figure 6: Entry action

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13   when others =>
14     null;
15 end case;
```

Figure 7: Generated code

Contents

Conclusion

Summary

We developed a complete MVB device with the novel formal modeling method.
Our work provides a novel method and a different vision for numeric circuit design.
Although this model based methodology would result in a lower performance, it can enhance the work efficiency.

Outlook

The generated code quality is not good enough. We will concentrate on improving the code quality.

Thank you!