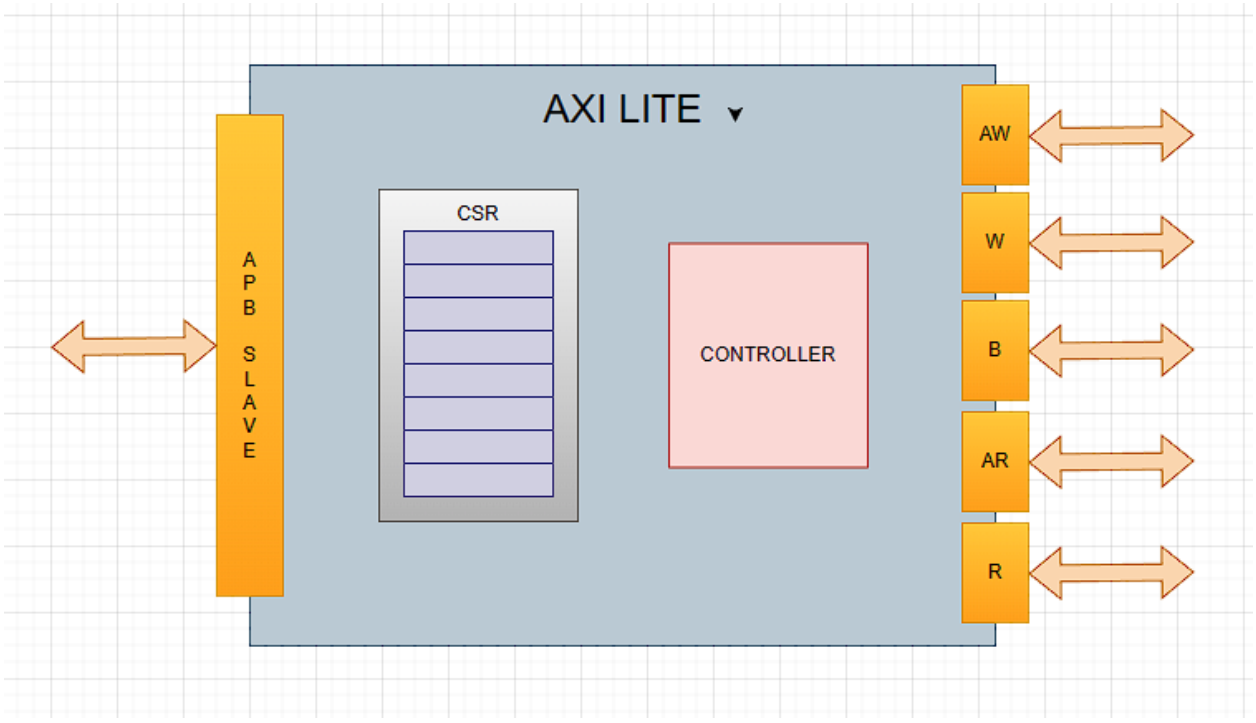
AXI-Lite Master Controller

Introduction:

This document explains how AXI-Lite Master Controller works.

Block Diagram:



Specifications:

- APB Slave interface for configuring CSR's.
- AXI4 Master interface to communicate with AXI4 supported devices.
- 32-bit address width.
- 32-bit data with.
- Interrupt support. To indicate error in transacion

CSR's Description:

CSR 1: Control CSR

Offset Value: 0x00

Reset Value: 0x00000000

Field Bits	Field Name	Description
0	start	This field indicates that all transfer related information is updated in CSR's and now transfer can be started.
6:1	bytes	This field indicates the number of bytes to be transferred in a transfer. As this is an AXI-Lite interface, the maximum allowed value for bytes is 4. If a value greater than 4 is set

		then it automatically resets it to 4 as it is the max allowed value.
7	read/write	This bit indicates whether the operation to be performed is read or write operation. ● 0 -> read operation ● 1 -> write operation
8	busy	Controller is busy is performing requested transaction
9	done	Transaction has been performed successfully. After each transaction it must be read. Reading the register resets this bit to '0'.
31:10	reserved	reserved

CSR 2: Address CSR
Offset Value: 0x01
Reset Value: 0x00000000

Field Bits	Field Name	Description
31:0	address	This field contains address on which read/write operation has to be performed by AXI Master

CSR 3: Write Data CSR
Offset Value: 0x10
Reset Value: 0x00000000

Field Bits	Field Name	Description
31:0	write data	This field contains data to be transferred to slave via AXI Write transaction

CSR 4: Read Data CSR
Offset Value: 0x10
Reset Value: 0x00000000

Field Bits	Field Name	Description
31:0	write data	This field contains data read from slave in AXI Read Transaction

Modes of Operation:

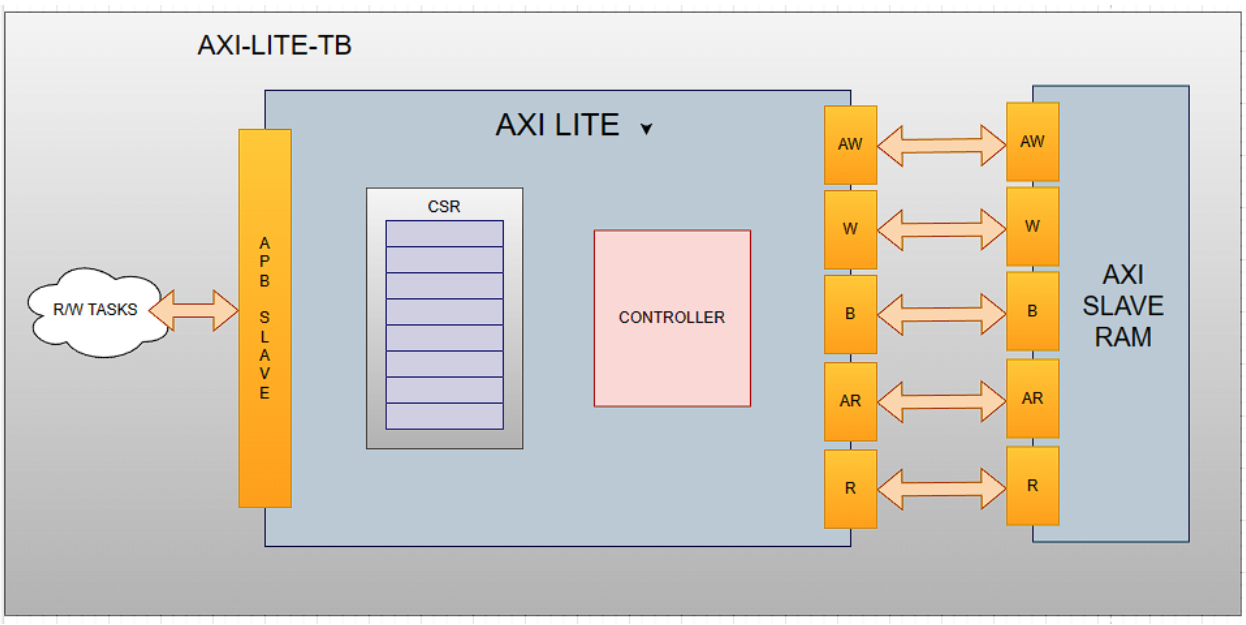
To initiate a write request from AXI Master, Controller can be configured as

- Write a valid address at “Address CSR (0x01)”.
- Write valid data at “Write Data CSR(0x01)”.
- Set the “read/write” bit of “Control CSR(0x00)” as 1 to indicate a write request.
- Set the “start” bit of “Control CSR(0x00)” as 1 to start the transaction.
- Wait for the “done” bit of “Control CSR(0x00)” to turn 1, indicating transfer completion.

To initiate a read request from AXI Master, Controller can be configured as

- Write a valid address at “Address CSR (0x01)”.
- Set the “read/write” bit of “Control CSR(0x00)” as 0 to indicate a read request.
- Set the “start” bit of “Control CSR(0x00)” as 1 to start the transaction.
- Wait for the “done” bit of “Control CSR(0x00)” to turn 1, indicating transfer completion.
- Read data from “Read Data CSR(0x20)”.

Testbench Architecture:



- Testbench consists of an AXI Lite Ram module that acts as slave and responds to read and write transactions initiated by master.
- The APB interface of Controller can be controlled by ‘write_apb’ and ‘read_apb’ tasks present in the testbench. These tasks mimics the apb protocol for read and write transfers on apb interface.
- There are two tasks
    - write_via_axi(input bit [31:0] addr, input [31:0] data);
    - read_via_axi(input bit [31:0] addr, output [31:0] data);

  To read and write data from AXI.

Waveform:

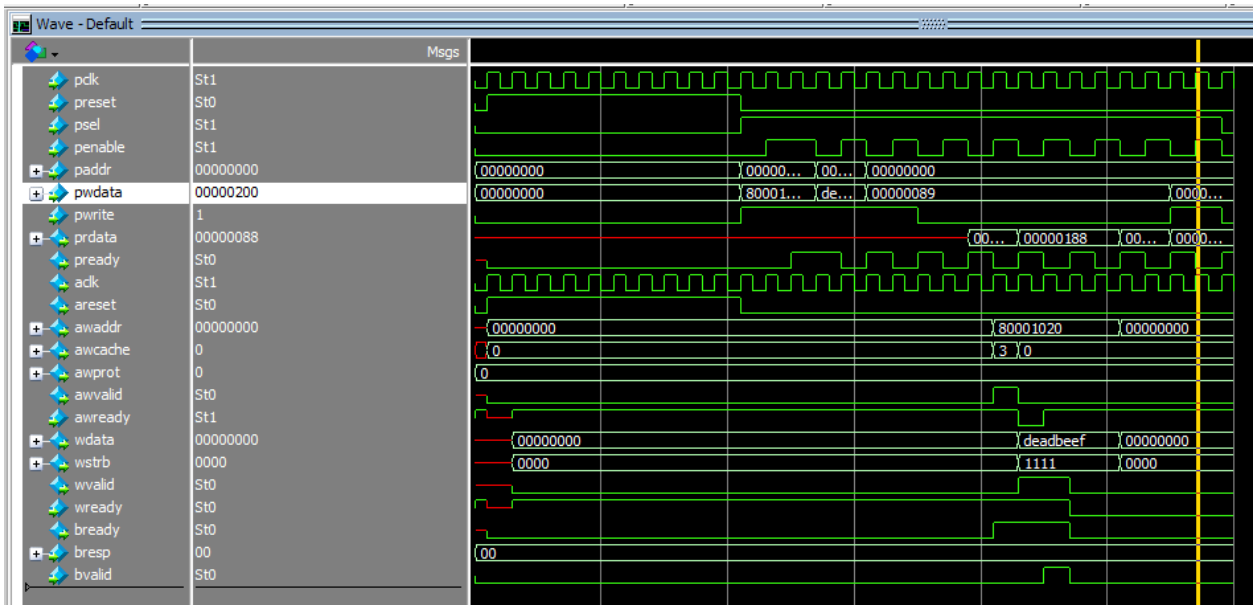


Image 1: AXI Write Transaction

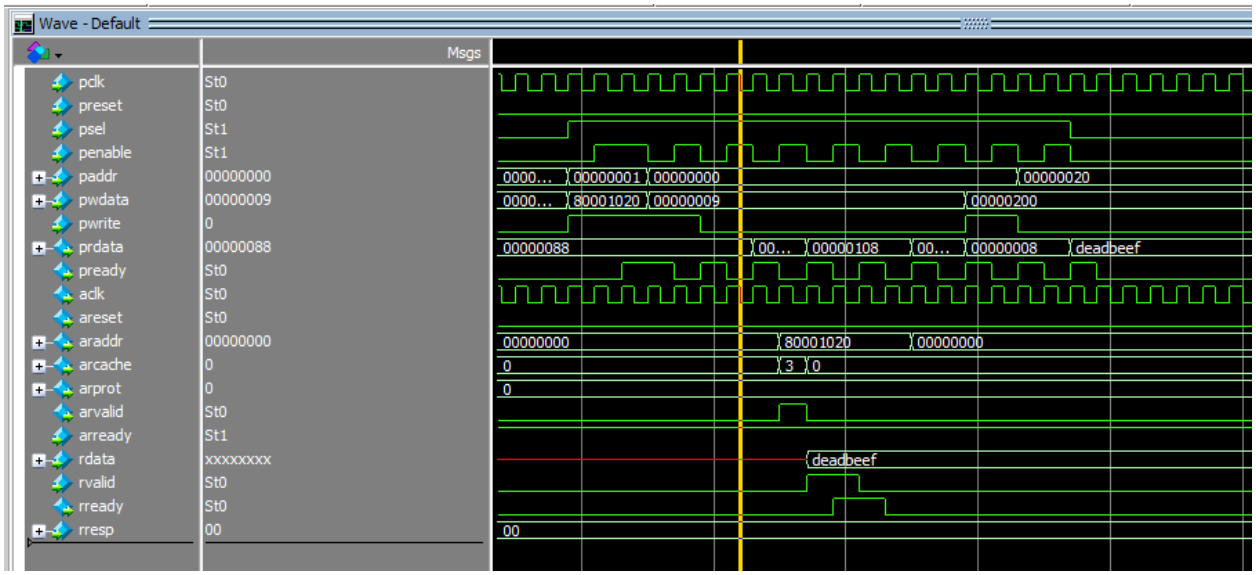


Image 2: AXI ReadTransaction

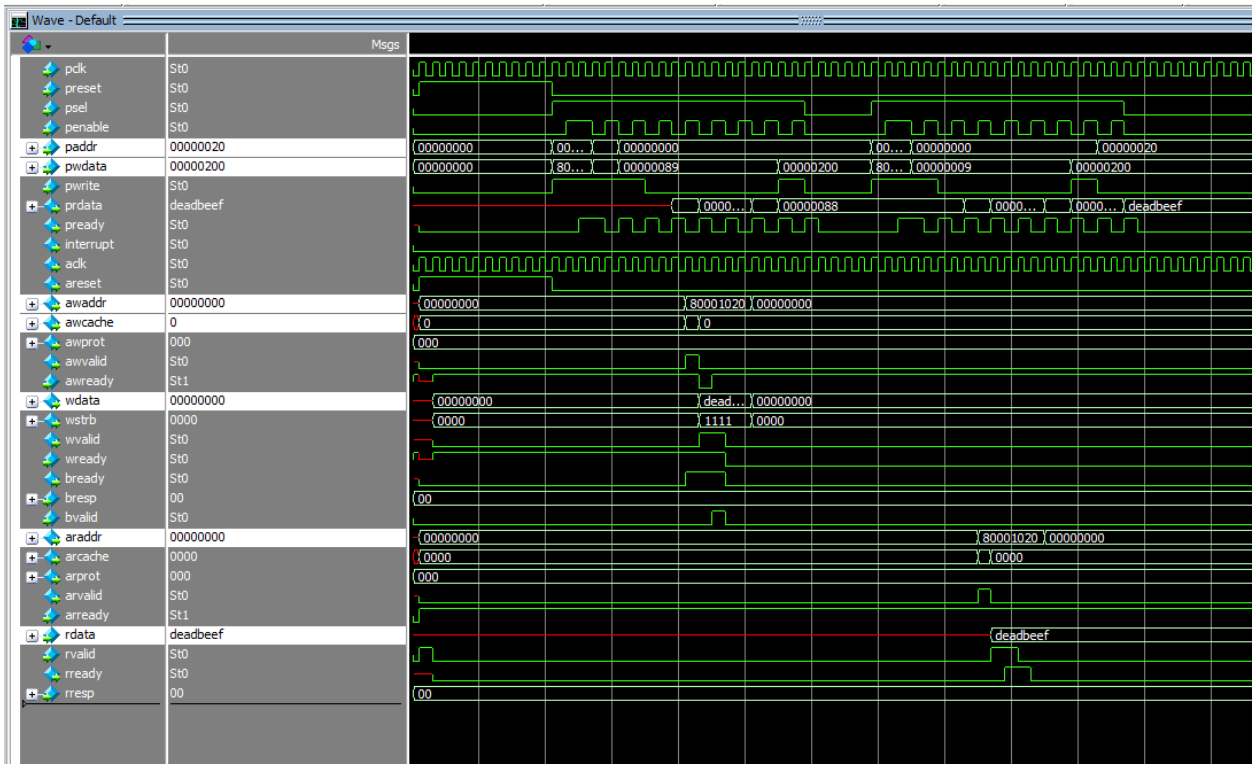


Image 3: AXI Write-ReadTransaction