\*\*\* Running vivado

with args -log mips\_final.vds -m64 -product Vivado -mode batch -messageDb vivado.pb -notrace -source mips\_final.tcl

WARNING: Default location for XILINX\_VIVADO\_HLS not found:

\*\*\*\*\*\* Vivado v2016.4 (64-bit)

\*\*\*\* SW Build 1756540 on Mon Jan 23 19:11:23 MST 2017

\*\*\*\* IP Build 1755317 on Mon Jan 23 20:30:07 MST 2017

\*\* Copyright 1986-2016 Xilinx, Inc. All Rights Reserved.

source mips\_final.tcl -notrace

Command: synth\_design -top mips\_final -part xc7a100tcsg324-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7a100t'

INFO: Launching helper process for spawning children vivado processes

INFO: Helper process launched with PID 10400

WARNING: [Synth 8-1849] concatenation with unsized literal; will interpret as 32 bits [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:163]

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Starting Synthesize : Time (s): cpu = 00:00:05 ; elapsed = 00:00:12 . Memory (MB): peak = 321.645 ; gain = 109.406

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INFO: [Synth 8-638] synthesizing module 'mips\_final' [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:23]

Parameter addALU bound to: 4'b0010

Parameter subALU bound to: 4'b0110

Parameter andALU bound to: 4'b0000

Parameter orALU bound to: 4'b0001

Parameter sltALU bound to: 4'b0111

Parameter norALU bound to: 4'b1100

Parameter lwOP bound to: 6'b100011

Parameter swOP bound to: 6'b101011

Parameter beqOP bound to: 6'b000100

Parameter bneOP bound to: 6'b000101

Parameter addiOP bound to: 6'b001000

Parameter andiOP bound to: 6'b001100

Parameter oriOP bound to: 6'b001101

Parameter jumpOP bound to: 6'b000010

Parameter jalOP bound to: 6'b000011

Parameter ROP bound to: 6'b000000

Parameter addFUNCT bound to: 6'b100000

Parameter subFUNCT bound to: 6'b100010

Parameter andFUNCT bound to: 6'b100100

Parameter orFUNCT bound to: 6'b100101

Parameter sltFUNCT bound to: 6'b101010

Parameter norFUNCT bound to: 6'b100111

Parameter jrFUNCT bound to: 6'b001000

INFO: [Synth 8-3876] $readmem data file 'final\_instruction\_memory.txt' is read successfully [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:94]

INFO: [Synth 8-3876] $readmem data file 'final\_data\_memory.txt' is read successfully [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:95]

INFO: [Synth 8-4471] merging register 'MemtoReg\_ID\_reg' into 'MemRead\_ID\_reg' [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:264]

INFO: [Synth 8-4471] merging register 'ID\_Rt\_reg[4:0]' into 'pass2\_reg[4:0]' [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:280]

INFO: [Synth 8-4471] merging register 'MemtoReg\_EX\_reg' into 'MemRead\_EX\_reg' [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:405]

INFO: [Synth 8-256] done synthesizing module 'mips\_final' (1#1) [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:23]

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Finished Synthesize : Time (s): cpu = 00:00:06 ; elapsed = 00:00:14 . Memory (MB): peak = 344.395 ; gain = 132.156

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Finished Constraint Validation : Time (s): cpu = 00:00:06 ; elapsed = 00:00:15 . Memory (MB): peak = 344.395 ; gain = 132.156

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Start Loading Part and Timing Information

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Loading part: xc7a100tcsg324-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:06 ; elapsed = 00:00:15 . Memory (MB): peak = 344.395 ; gain = 132.156

---------------------------------------------------------------------------------

INFO: [Device 21-403] Loading part xc7a100tcsg324-1

INFO: [Synth 8-5818] HDL ADVISOR - The operator resource <adder> is shared. To prevent sharing consider applying a KEEP on the output of the operator [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:362]

INFO: [Synth 8-5546] ROM "RF\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[0]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "branch" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "branchBNE" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "MemWrite0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "MemtoReg0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "arithmetic3" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "regDst0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5545] ROM "Zero0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "i\_mem" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[31]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[30]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[29]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[28]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[27]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[26]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[25]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[24]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[23]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[22]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[21]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[20]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[19]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[18]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[17]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[16]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[15]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[14]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[13]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[12]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[11]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[10]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[9]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[8]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[7]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[6]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[5]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[4]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[3]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[2]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[1]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "RF\_reg[0]" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "branch" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "branchBNE" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "MemWrite0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "MemtoReg0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "arithmetic3" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5546] ROM "regDst0" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5545] ROM "Zero0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-5546] ROM "i\_mem" won't be mapped to RAM because it is too sparse

INFO: [Synth 8-5544] ROM "forwardA0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "forwardB1" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "ALUOut0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "forwardC" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "PCSrc\_MEM0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "stallPipe" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "ALUSrc0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "jumpAddress\_ID" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "RegWrite0" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

INFO: [Synth 8-5544] ROM "ZeroExt" won't be mapped to Block RAM because address size (1) smaller than threshold (5)

---------------------------------------------------------------------------------

Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:07 ; elapsed = 00:00:15 . Memory (MB): peak = 390.594 ; gain = 178.355

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

No constraint files found.

---------------------------------------------------------------------------------

Start RTL Component Statistics

---------------------------------------------------------------------------------

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 3

3 Input 32 Bit Adders := 1

+---Registers :

32 Bit Registers := 45

5 Bit Registers := 9

4 Bit Registers := 1

2 Bit Registers := 3

1 Bit Registers := 18

+---RAMs :

32K Bit RAMs := 1

+---Muxes :

48 Input 32 Bit Muxes := 1

2 Input 32 Bit Muxes := 11

4 Input 32 Bit Muxes := 1

3 Input 32 Bit Muxes := 1

7 Input 32 Bit Muxes := 2

9 Input 9 Bit Muxes := 1

7 Input 7 Bit Muxes := 1

2 Input 5 Bit Muxes := 3

5 Input 5 Bit Muxes := 1

6 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 4

5 Input 4 Bit Muxes := 2

8 Input 3 Bit Muxes := 2

2 Input 3 Bit Muxes := 1

2 Input 2 Bit Muxes := 22

2 Input 1 Bit Muxes := 36

---------------------------------------------------------------------------------

Finished RTL Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

Hierarchical RTL Component report

Module mips\_final

Detailed RTL Component Info :

+---Adders :

2 Input 32 Bit Adders := 3

3 Input 32 Bit Adders := 1

+---Registers :

32 Bit Registers := 45

5 Bit Registers := 9

4 Bit Registers := 1

2 Bit Registers := 3

1 Bit Registers := 18

+---RAMs :

32K Bit RAMs := 1

+---Muxes :

48 Input 32 Bit Muxes := 1

2 Input 32 Bit Muxes := 11

4 Input 32 Bit Muxes := 1

3 Input 32 Bit Muxes := 1

7 Input 32 Bit Muxes := 2

9 Input 9 Bit Muxes := 1

7 Input 7 Bit Muxes := 1

2 Input 5 Bit Muxes := 3

5 Input 5 Bit Muxes := 1

6 Input 5 Bit Muxes := 1

2 Input 4 Bit Muxes := 4

5 Input 4 Bit Muxes := 2

8 Input 3 Bit Muxes := 2

2 Input 3 Bit Muxes := 1

2 Input 2 Bit Muxes := 22

2 Input 1 Bit Muxes := 36

---------------------------------------------------------------------------------

Finished RTL Hierarchical Component Statistics

---------------------------------------------------------------------------------

---------------------------------------------------------------------------------

Start Part Resource Summary

---------------------------------------------------------------------------------

Part Resources:

DSPs: 240 (col length:80)

BRAMs: 270 (col length: RAMB18 80 RAMB36 40)

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Finished Part Resource Summary

---------------------------------------------------------------------------------

No constraint files found.

---------------------------------------------------------------------------------

Start Cross Boundary and Area Optimization

---------------------------------------------------------------------------------

INFO: [Synth 8-5544] ROM "p\_0\_out0" won't be mapped to Block RAM because address size (2) smaller than threshold (5)

INFO: [Synth 8-5545] ROM "Zero0" won't be mapped to RAM because address size (32) is larger than maximum supported(25)

INFO: [Synth 8-3886] merging instance 'pass1\_reg[3]' (FDR) to 'jumpAddress\_ID\_reg[16]'

INFO: [Synth 8-3886] merging instance 'pass1\_reg[4]' (FDR) to 'jumpAddress\_ID\_reg[17]'

INFO: [Synth 8-3886] merging instance 'pass1\_reg[0]' (FDR) to 'jumpAddress\_ID\_reg[13]'

INFO: [Synth 8-3886] merging instance 'pass1\_reg[1]' (FDR) to 'jumpAddress\_ID\_reg[14]'

INFO: [Synth 8-3886] merging instance 'pass1\_reg[2]' (FDR) to 'jumpAddress\_ID\_reg[15]'

INFO: [Synth 8-3886] merging instance 'pc\_reg\_ID\_reg[28]' (FDR) to 'jumpAddress\_ID\_reg[28]'

INFO: [Synth 8-3886] merging instance 'pc\_reg\_ID\_reg[29]' (FDR) to 'jumpAddress\_ID\_reg[29]'

INFO: [Synth 8-3886] merging instance 'pc\_reg\_ID\_reg[30]' (FDR) to 'jumpAddress\_ID\_reg[30]'

INFO: [Synth 8-3886] merging instance 'pc\_reg\_ID\_reg[31]' (FDR) to 'jumpAddress\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[0]' (FDR) to 'jumpAddress\_ID\_reg[1]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\jumpAddress\_ID\_reg[1] )

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[2]' (FDR) to 'extend\_ID\_reg[0]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[3]' (FDR) to 'extend\_ID\_reg[1]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[4]' (FDR) to 'extend\_ID\_reg[2]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[5]' (FDR) to 'extend\_ID\_reg[3]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[6]' (FDR) to 'extend\_ID\_reg[4]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[7]' (FDR) to 'extend\_ID\_reg[5]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[8]' (FDR) to 'extend\_ID\_reg[6]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[9]' (FDR) to 'extend\_ID\_reg[7]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[10]' (FDR) to 'extend\_ID\_reg[8]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[11]' (FDR) to 'extend\_ID\_reg[9]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[12]' (FDR) to 'extend\_ID\_reg[10]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[13]' (FDR) to 'extend\_ID\_reg[11]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[14]' (FDR) to 'extend\_ID\_reg[12]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[15]' (FDR) to 'extend\_ID\_reg[13]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[16]' (FDR) to 'extend\_ID\_reg[14]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[17]' (FDR) to 'extend\_ID\_reg[15]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[18]' (FDR) to 'pass2\_reg[0]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[19]' (FDR) to 'pass2\_reg[1]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[20]' (FDR) to 'pass2\_reg[2]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[21]' (FDR) to 'pass2\_reg[3]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[22]' (FDR) to 'pass2\_reg[4]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[23]' (FDR) to 'ID\_Rs\_reg[0]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[24]' (FDR) to 'ID\_Rs\_reg[1]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[25]' (FDR) to 'ID\_Rs\_reg[2]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[26]' (FDR) to 'ID\_Rs\_reg[3]'

INFO: [Synth 8-3886] merging instance 'jumpAddress\_ID\_reg[27]' (FDR) to 'ID\_Rs\_reg[4]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\ALU\_Zero\_reg[1] )

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[16]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[17]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[18]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[19]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[20]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[21]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[22]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[23]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[24]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[25]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[26]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[27]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[28]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[29]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[30]' (FDR) to 'extend\_ID\_reg[31]'

INFO: [Synth 8-3886] merging instance 'instruction\_reg\_IF\_reg[6]' (FDE) to 'instruction\_reg\_IF\_reg[7]'

INFO: [Synth 8-3886] merging instance 'instruction\_reg\_IF\_reg[8]' (FDE) to 'instruction\_reg\_IF\_reg[9]'

INFO: [Synth 8-3886] merging instance 'instruction\_reg\_IF\_reg[9]' (FDE) to 'instruction\_reg\_IF\_reg[10]'

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\instruction\_reg\_IF\_reg[20] )

INFO: [Synth 8-3333] propagating constant 0 across sequential element (\EX\_Rt\_reg[4] )

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[6]' (FDR) to 'extend\_ID\_reg[7]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[8]' (FDR) to 'extend\_ID\_reg[10]'

INFO: [Synth 8-3886] merging instance 'extend\_ID\_reg[9]' (FDR) to 'extend\_ID\_reg[10]'

WARNING: [Synth 8-3332] Sequential element (instruction\_reg\_IF\_reg[20]) is unused and will be removed from module mips\_final.

WARNING: [Synth 8-3332] Sequential element (jumpAddress\_ID\_reg[1]) is unused and will be removed from module mips\_final.

WARNING: [Synth 8-3332] Sequential element (EX\_Rt\_reg[4]) is unused and will be removed from module mips\_final.

WARNING: [Synth 8-3332] Sequential element (ALU\_Zero\_reg[1]) is unused and will be removed from module mips\_final.

WARNING: [Synth 8-3332] Sequential element (pass2\_reg[4]) is unused and will be removed from module mips\_final.

---------------------------------------------------------------------------------

Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:24 . Memory (MB): peak = 629.613 ; gain = 417.375

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Start ROM, RAM, DSP and Shift Register Reporting

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Block RAM: Preliminary Mapping Report (see note below)

+------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|Module Name | RTL Object | PORT A (Depth x Width) | W | R | PORT B (Depth x Width) | W | R | Ports driving FF | RAMB18 | RAMB36 |

+------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

|mips\_final | d\_mem\_reg | 1 K x 32(READ\_FIRST) | W | | 1 K x 32(WRITE\_FIRST) | | R | Port A and B | 0 | 1 |

+------------+------------+------------------------+---+---+------------------------+---+---+------------------+--------+--------+

Note: The table above is a preliminary report that shows the Block RAMs at the current stage of the synthesis flow. Some Block RAMs may be reimplemented as non Block RAM primitives later in the synthesis flow. Multiple instantiated Block RAMs are reported only once.

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Finished ROM, RAM, DSP and Shift Register Reporting

---------------------------------------------------------------------------------

Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

+-+--------------+------------+----------+

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Start Timing Optimization

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No constraint files found.

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Finished Timing Optimization : Time (s): cpu = 00:00:14 ; elapsed = 00:00:24 . Memory (MB): peak = 629.613 ; gain = 417.375

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Technology Mapping

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INFO: [Synth 8-4480] The timing for the instance d\_mem\_reg (implemented as a block RAM) might be sub-optimal as no optional output register could be merged into the block ram. Providing additional output register may help in improving timing.

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Finished Technology Mapping : Time (s): cpu = 00:00:14 ; elapsed = 00:00:25 . Memory (MB): peak = 629.613 ; gain = 417.375

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Report RTL Partitions:

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| |RTL Partition |Replication |Instances |

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Report Check Netlist:

+------+------------------+-------+---------+-------+------------------+

| |Item |Errors |Warnings |Status |Description |

+------+------------------+-------+---------+-------+------------------+

|1 |multi\_driven\_nets | 0| 0|Passed |Multi driven nets |

+------+------------------+-------+---------+-------+------------------+

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Report RTL Partitions:

+-+--------------+------------+----------+

| |RTL Partition |Replication |Instances |

+-+--------------+------------+----------+

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

+-+--------------+----------+

+-+--------------+----------+

Report Cell Usage:

+------+---------+------+

| |Cell |Count |

+------+---------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 28|

|3 |LUT1 | 34|

|4 |LUT2 | 71|

|5 |LUT3 | 77|

|6 |LUT4 | 44|

|7 |LUT5 | 318|

|8 |LUT6 | 564|

|9 |MUXF7 | 193|

|10 |MUXF8 | 64|

|11 |RAMB36E1 | 1|

|12 |FDRE | 1411|

|13 |FDSE | 16|

|14 |IBUF | 1|

|15 |OBUF | 160|

+------+---------+------+

Report Instance Areas:

+------+---------+-------+------+

| |Instance |Module |Cells |

+------+---------+-------+------+

|1 |top | | 2983|

+------+---------+-------+------+

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Finished Writing Synthesis Report : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

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Synthesis finished with 0 errors, 0 critical warnings and 6 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:13 ; elapsed = 00:00:17 . Memory (MB): peak = 629.613 ; gain = 394.219

Synthesis Optimization Complete : Time (s): cpu = 00:00:15 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 417.375

INFO: [Project 1-571] Translating synthesized netlist

INFO: [Netlist 29-17] Analyzing 30 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

WARNING: [Netlist 29-101] Netlist 'mips\_final' is not ideal for floorplanning, since the cellview 'mips\_final' contains a large number of primitives. Please consider enabling hierarchy in synthesis if you want to do floorplanning.

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

INFO: [Common 17-83] Releasing license: Synthesis

172 Infos, 7 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:00:16 ; elapsed = 00:00:26 . Memory (MB): peak = 629.613 ; gain = 403.320

INFO: [Common 17-1381] The checkpoint 'J:/Documents/323\_lab9/323\_lab9.runs/synth\_1/mips\_final.dcp' has been generated.

report\_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.074 . Memory (MB): peak = 629.613 ; gain = 0.000

INFO: [Common 17-206] Exiting Vivado at Tue Apr 03 14:12:39 2018...