Vivado Simulator 2016.4

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Running: C:/Xilinx/Vivado/2016.4/bin/unwrapped/win64.o/xelab.exe -wto 9dc522be81a34fa39439e1c5f10c9e1d --debug typical --relax --mt 2 -L xil\_defaultlib -L unisims\_ver -L unimacro\_ver -L secureip --snapshot tb\_generic\_pipeline\_behav xil\_defaultlib.tb\_generic\_pipeline xil\_defaultlib.glbl -log elaborate.log

Using 2 slave threads.

Starting static elaboration

WARNING: [VRFC 10-526] concatenation with unsized literal; will interpret as 32 bits [J:/Documents/323\_lab9/323\_lab9.srcs/sources\_1/new/mips\_final.v:163]

Completed static elaboration

Starting simulation data flow analysis

Completed simulation data flow analysis

Time Resolution for simulation is 1ps

Compiling module xil\_defaultlib.mips\_final

Compiling module xil\_defaultlib.tb\_generic\_pipeline

Compiling module xil\_defaultlib.glbl

Built simulation snapshot tb\_generic\_pipeline\_behav