



**BANGLADESH UNIVERSITY OF PROFESSIONALS**

**FACULTY OF SCIENCE & TECHNOLOGY**

## **Lab Report**

**Report Title:** Design of a 4-bit ALU with Specified Functions

**Submitted by**

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**Section:** B

**Course Name:** Digital System Design

**Course Code:** CSE3204

**Date:** 27/04/2025

## **Report Title: Design of a 4-bit ALU with Specified Functions**

### **Functions:**

- ADD B to A
- ADD A and B with carry
- $A'B'$
- $A + B$  (logical OR)

### **a. Problem Definition**

In digital systems, an Arithmetic Logic Unit (ALU) is a vital component that performs both arithmetic and logic operations. This project aims to design and simulate a 4-bit ALU capable of executing four operations: addition of A and B, addition of A and B with a carry, bitwise OR operation ( $A + B$ ), and bitwise AND of the complemented inputs ( $A'B'$ ).

The selection of operations is controlled by a 2-bit selector input (S1, S0). The ALU takes two 4-bit inputs (A[3:0] and B[3:0]) and generates a 4-bit output depending on the selected operation. The design uses only basic logic gates (AND, OR, NOT) and standard ICs without employing any multiplexer structures, maintaining circuit transparency and clarity.

### **b. Design Procedure**

#### **1. Input Specification:**

Two 4-bit binary inputs: A[3:0] and B[3:0].

#### **2. Operation Selection (based on Select lines S1 and S0):**

- 00: ADD B to A
- 01: ADD A and B with external carry
- 10:  $A + B$  (bitwise OR)
- 11:  $A'B'$  (bitwise AND of complements)

#### **3. Component Selection:**

- 7482 (Dual 2-bit Full Adder ICs combined for 4-bit addition)
- 7408 (Quad 2-input AND gates)
- 7432 (Quad 2-input OR gates)
- 7404 (Hex Inverter gates)

#### 4. Design Strategy:

- Implement addition operations using 7482 ICs.
- Perform logical operations (OR and complemented AND) using basic gates.
- Design a manual selection circuit using AND-OR combinations to control output based on S1 and S0 without using multiplexers.

#### 5. Implementation and Testing:

- The circuit was designed and simulated in Proteus software.
- Various input combinations were tested to validate the correctness of each operation.

#### c. Truth Tables and Equations

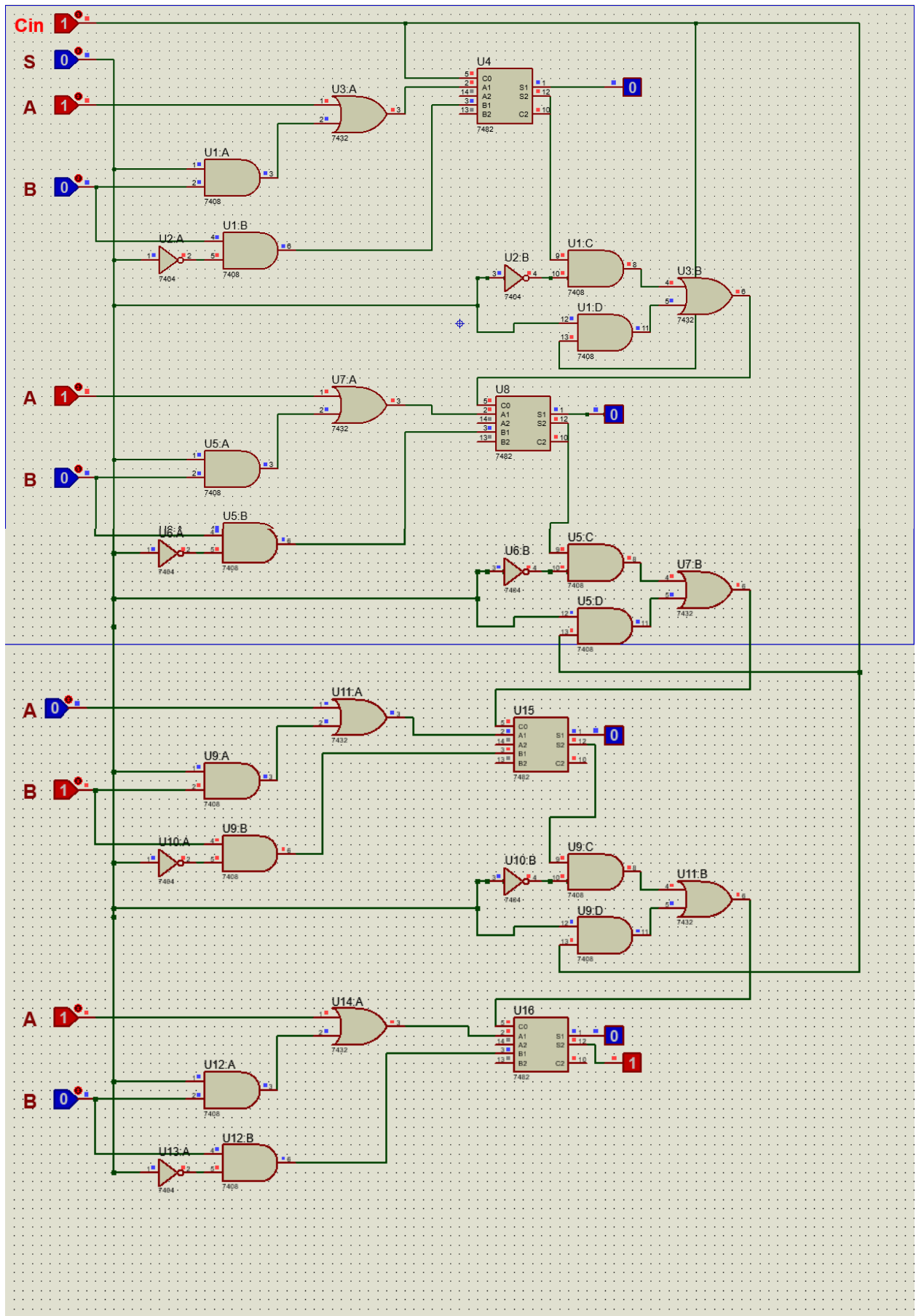
S	C <sub>in</sub>	X <sub>i</sub>	Y <sub>i</sub>	F
0	0	A <sub>i</sub>	B <sub>i</sub>	ADD A <sub>i</sub> , B <sub>i</sub>
0	1	A <sub>i</sub>	B <sub>i</sub>	ADC A <sub>i</sub> , B <sub>i</sub>
1	0	A <sub>i</sub> + B <sub>i</sub>	0	A <sub>i</sub> + B <sub>i</sub>
1	1	A <sub>i</sub> + B <sub>i</sub>	0	A <sub>i</sub> ' . B <sub>i</sub> '

$$X = A_i + SB_i$$

$$Y = S'B_i$$

$$C_{in} = S'C_{out} + SC_{in}$$

#### d. Simulation of 4-bit ALU in Proteus



### e. IC Descriptions

in the circuit we used total 14 AND gates, 7 OR gates & 7 Not gates. So required IC's:

IC Number	IC Name	Quantity Used	Description
7404	Hex Inverter	2	Simple addition without carry-in
7408	Quad 2-input AND	4	Addition with external carry input
7432	Quad 2-input OR	2	Bitwise OR operation
7482	Full Adder	4	Bitwise AND after complementing inputs

### Conclusion:

The project successfully demonstrates the design and simulation of a 4-bit ALU capable of performing essential arithmetic and logic operations using basic combinational logic elements. The design carefully avoids multiplexer use and achieves functionality purely through logic gates and standard ICs. The results obtained from Proteus simulation validate the correct functioning of the ALU for all combinations of inputs and operation select signals.