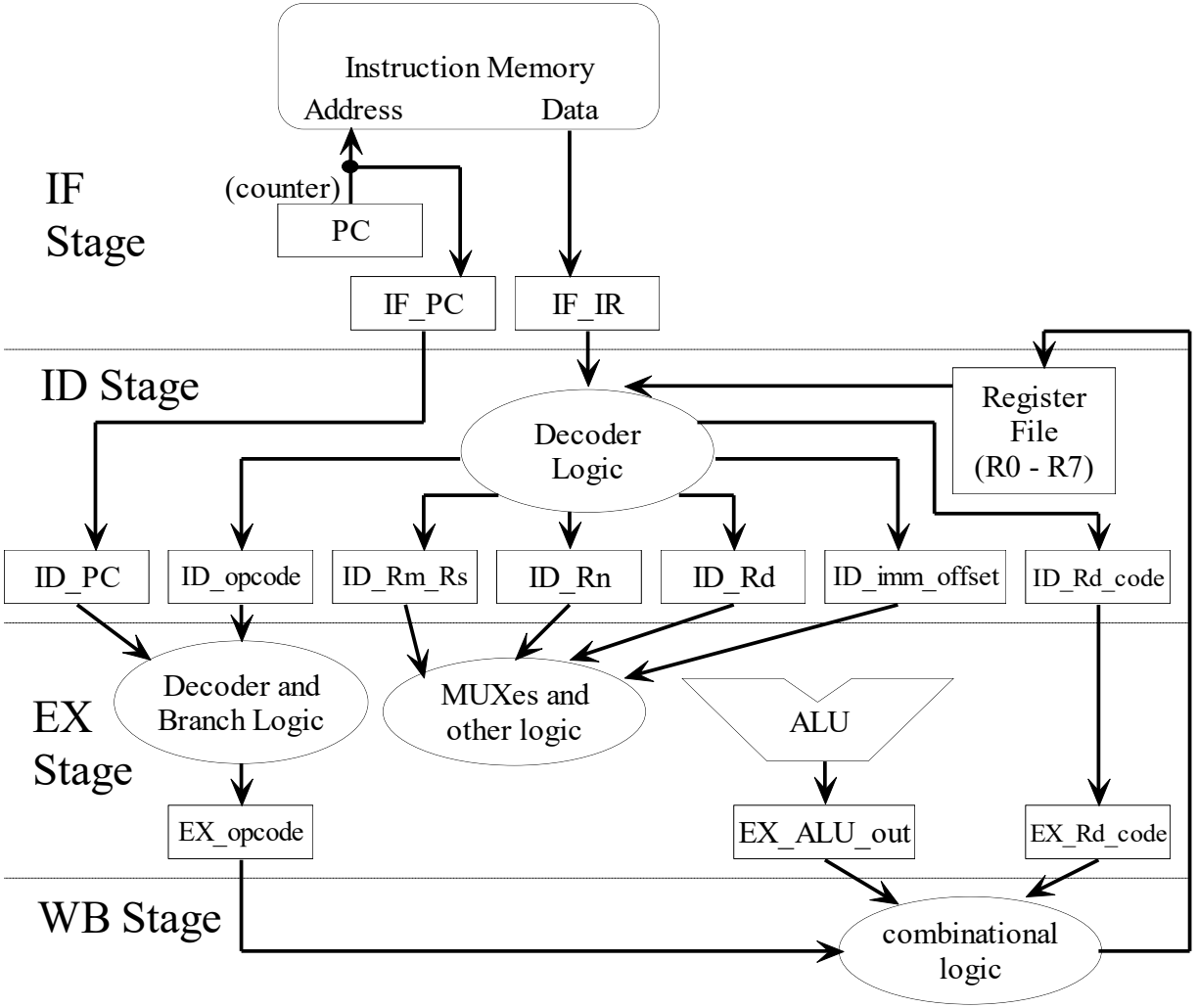
HDL HW3:
Pipelined THUMB CPU and Placement a nd Routing (P&R)

Outlines

- debug the THUMB RSIC CPU code
  - reset some signals
- synthesize THUMB 到 gatelevel，設為4個 pipeline stage
  - find critical path of each pipelined stage
- use prime time to measure power
- perform automatic placement-and-routing (APR) and mark the four pipelined stages in the layout view

THUMB Architecture

- 4 pipelined stages: IF, ID, EX, WB
  - refer to lecture 05 slides and given codes



One Pipelined Stage Per Module

- debug the given pipelined THUMB codes
  - both RTL codes and testbench are given
- modify the codes so that each pipelined stage is in a separate module
  - easy identification of critical path of each stage
- synthesize with three different constraints
  - area-optimized
  - delay-optimized
  - in-between
- find the delay of each pipelined stage
  - from Synopsys DC synthesis report
- measure delay and power using PrimeTime

summary table

- area, delay (each stage, and critical), power (DC and PT)
  - power from synthesis report, or
  - power measured using prime time

constraint	area	delay (DC)					power	
		1st	2nd	3rd	4th	Critical	DC	PT
Delay-opt						DC(PT)		
Area-opt								
In-between								

Placement and Routing

- perform automatic placement and routing (APR)
- mark the four pipelined stages in the layout view