

# **ADFP Cell-Based IC Physical Design and Verification with Innovus**

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# Outline

1. Pre-requirement
2. Assign Problem and Change Naming Rule Script
3. Design Import
4. Initial Step
5. Floor Plan
6. Power Plan
7. Power Route
8. Placement
9. CTS
10. Route
11. Post processing
12. Post Layout Simulation
13. HomeWork Requirment

# Pre-requirement

- ▶ Gate-Level netlist(Verilog)
- ▶ TestBench and Pattern
- ▶ SDC constraints
- ▶ Physical Library(ADFP製程LEF)
- ▶ Timing Library(ADFP製程LIB)
- ▶ Multi Mode Multi Corner MMMC.view.stylus

# 資料夾建立

/home/m123040031/TA/HDL\_HW3/ADFP/

Name	Size (KB)	Last modified	Owner
..			
ADFP_APR_script		2024-09-09...	m12304
APR		2024-09-23...	m12304
RTL		2024-09-11...	m12304
SYN		2024-09-11...	m12304
mmmc.view.stylus	2	2024-09-11...	m12304

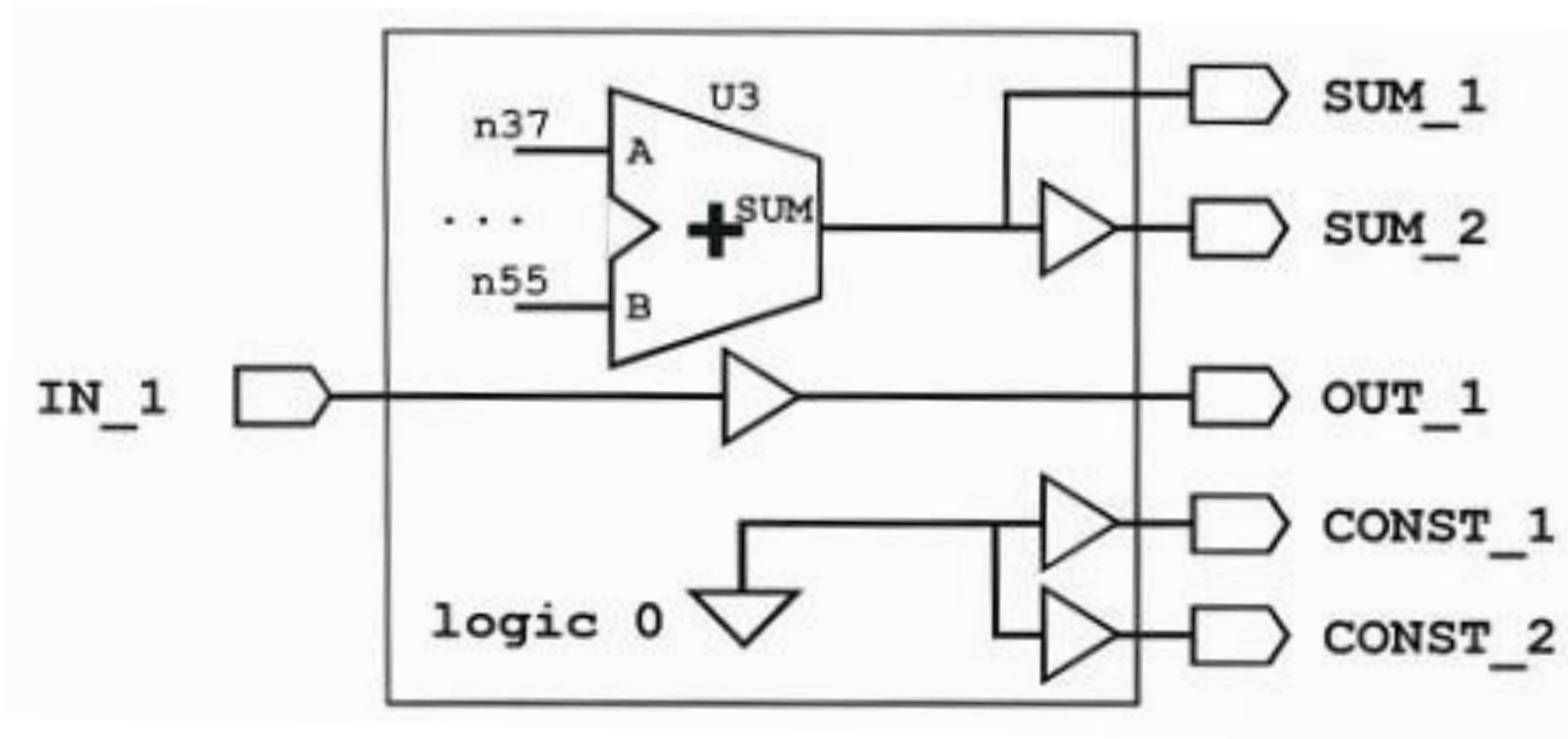


/home/m123040031/TA/HDL\_HW3/ADFP/APR/

Name	Size (KB)	Last modified	Owner
..			
.cadence		2024-09-11...	m12
db		2024-09-11...	m12
outputs		2024-09-11...	m12
timingReports		2024-09-11...	m12
.thumb_11868.slk.gz	594	2024-09-11...	m12
.thumb_37397.slk.gz	594	2024-09-11...	m12
innovus.cmd	24	2024-09-11...	m12

# Assign Problem and Change Naming Rule Script(1/2)

- ▶ The syntax of “assign” may cause problems in the LVS



- ▶ To ensure that your final netlist does not contain assign statements, separate the multiple port nets
- ▶ during compile. (一定要在合成前做以下指令在進行合成)
- ▶ `dc_shell > set_fix_multiple_port_nets -all -buffer_constants [get_designs *]`

# Assign Problem and Change Naming Rule Script(2/2)

- ▶ The wrong naming rules may cause problems in the LVS
- ▶ 在合成完後加入以下指令
- ▶ `set bus_inference_style {%s[%d]}`
- ▶ `set bus_naming_style {%s[%d]}`
- ▶ `set hdlout_internal_busses true`
- ▶ `change_names -hierarchy -rule verilog`
- ▶ `define_name_rules name_rule -allowed "A-Z a-z 0-9 _" -max_length 255 -type cell`
- ▶ `define_name_rules name_rule -allowed "A-Z a-z 0-9 _[]" -max_length 255 -type net`
- ▶ `define_name_rules name_rule -map {"\\*cell\\"*"cell"}`
- ▶ `define_name_rules name_rule -case_insensitive`
- ▶ `change_names -hierarchy -rules name_rule`

```
assign \A[19] = A[19];  
assign \A[18] = A[18];  
assign \A[17] = A[17];  
assign \A[16] = A[16];  
assign \A[15] = A[15];  
assign ABSVAL[19] = \A[19];  
assign ABSVAL[18] = \A[18];  
assign ABSVAL[17] = \A[17];  
assign ABSVAL[16] = \A[16];  
assign ABSVAL[15] = \A[15];
```



```
BUFX1 X37X( .I(A[19]), .Z(ABSVAL[19]) );  
BUFX1 X38X( .I(A[18]), .Z(ABSVAL[18]) );  
BUFX1 X39X( .I(A[17]), .Z(ABSVAL[17]) );  
BUFX1 X40X( .I(A[16]), .Z(ABSVAL[16]) );  
BUFX1 X41X( .I(A[15]), .Z(ABSVAL[15]) );
```

**Warning:** Verilog 'assign' or 'tran' statements are written out. (V0-4)

# SDC File

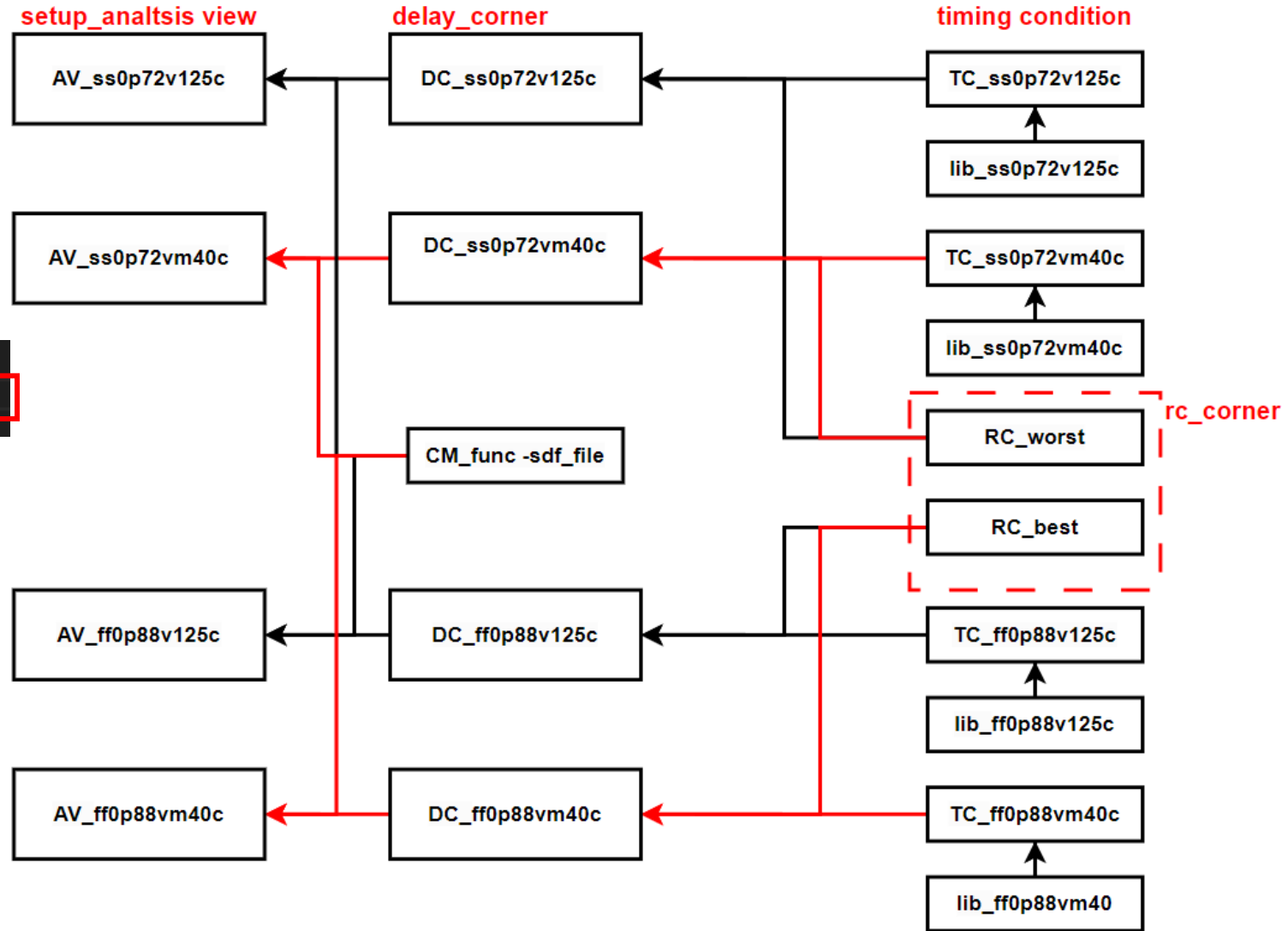
需要將這幾行註解

```
1 #####
2
3 # Created by write_sdc on Wed Sep 11 16:12:33 2024
4
5 #####
6 set sdc_version 2.1
7
8 #set_units -time ns -resistance kOhm -capacitance pF -voltage V -current mA
9 #set_operating_conditions -max ss0p72vm40c -max_library
10 #N16ADFP_StdCellss0p72vm40c_ccs\
11 #
12 #N16ADFP_StdCellff0p88v125c_ccs
13 #set_wire_load_mode top
14 #set_wire_load_model -name ZeroWireload -library N16ADFP_StdCellss0p72vm40c_ccs
15 #set_ideal_network [get_ports clk]
16 create_clock [get_ports clk] -period 2.5 -waveform {0 1.25}
17 set_clock_latency 0.2 [get_clocks clk]
18 set_clock_uncertainty 0.02 [get_clocks clk]
19 set_clock_transition -max -rise 0.1 [get_clocks clk]
20 set_clock_transition -max -fall 0.1 [get_clocks clk]
21 set_clock_transition -min -rise 0.1 [get_clocks clk]
22 set_clock_transition -min -fall 0.1 [get_clocks clk]
```

# Multi Mode Multi Corner MMMC.view.stylus

sdc\_file(XXX\_syn.sdc)

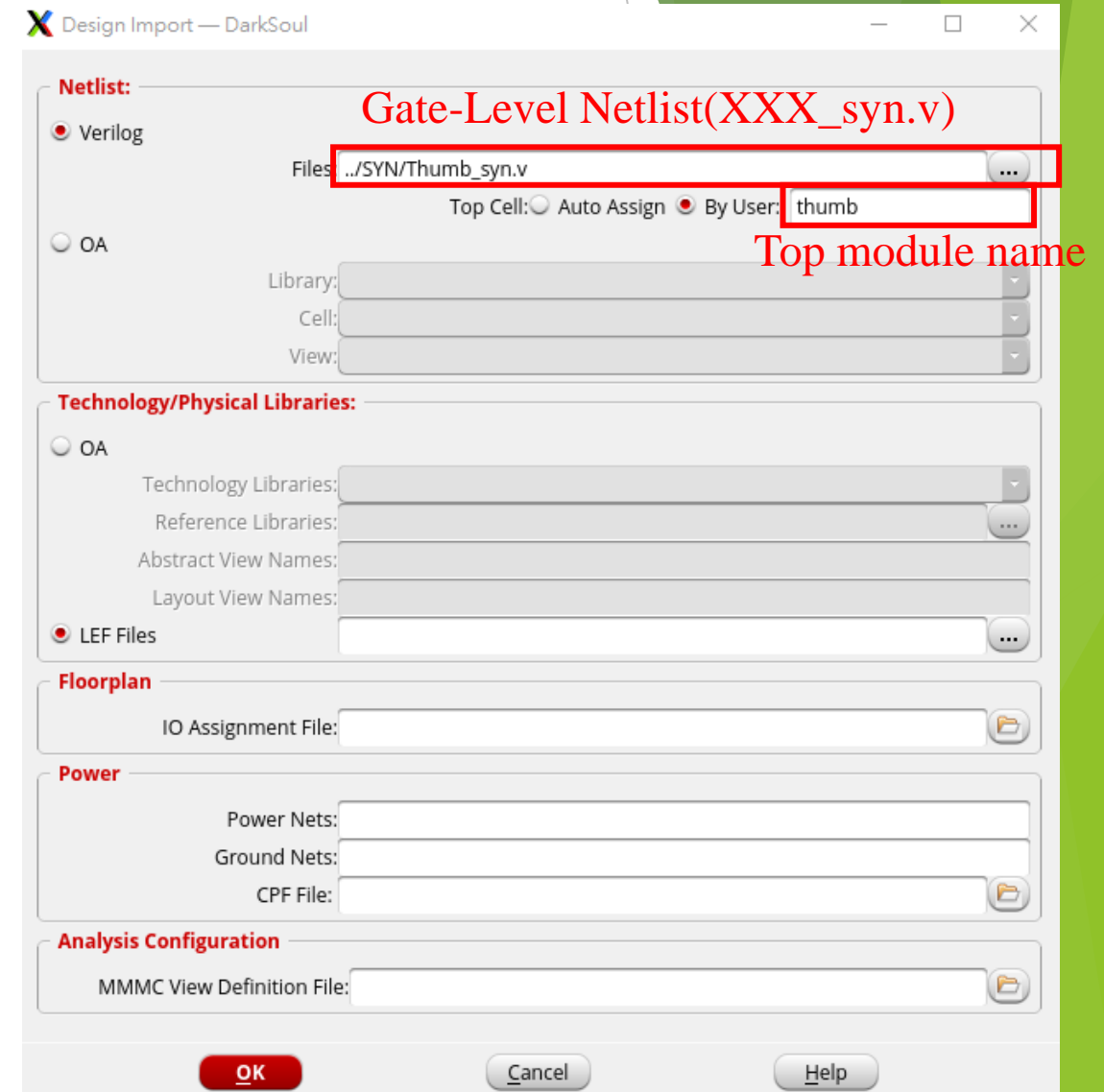
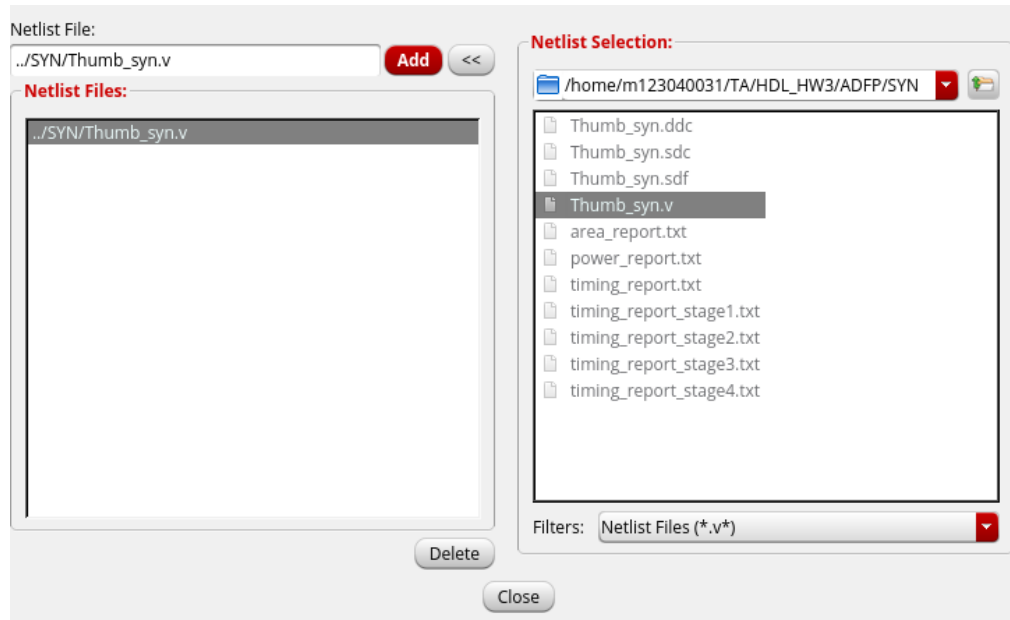
```
create_constraint mode -name CM func\  
-sdc_files /home/m123040031/TA/HDL_HW3/ADFP/SYN/Thumb_syn.sdc
```





# Design import(1/4)W

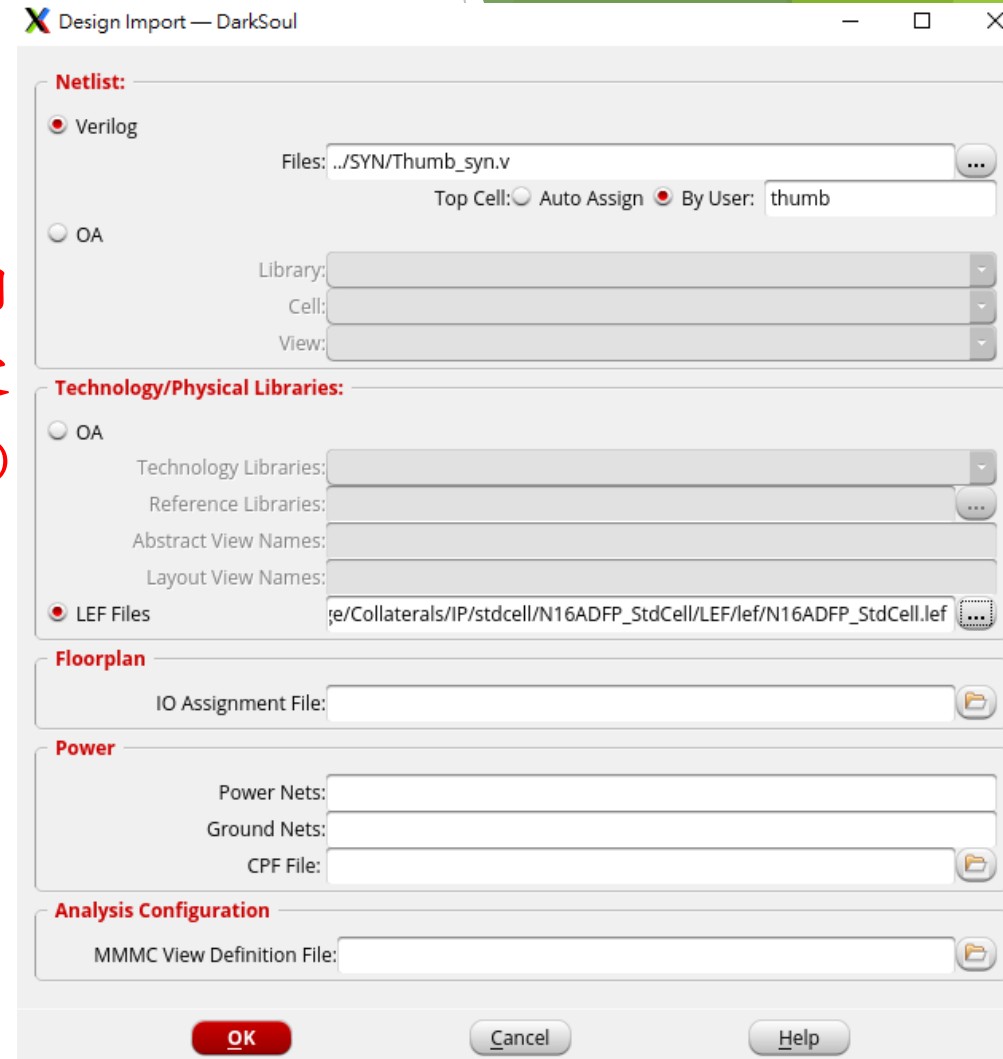
- ▶ **cd 進入APR資料夾**
- ▶ **Terminal 下輸入innovus -stylus**
- ▶ **1.File → Import Design → Netlist → Verilog → Files → ... →select your file and click Add**
- ▶ **2.Select By User,fill your\_design\_name**



# Design import(2/4)

- ▶ 3. Load process file
- ▶ LEF Files → ... → Filters: All Files(\*) → add lef files

註：製程的technology lef一定要放第一個，其餘的無順序之分，不同製程有不同的名字，如果不知道的話就一個一個試，錯誤的話最後設定完成後就會出現錯誤。（此範例為N16ADFP\_APR\_Innovus\_11M.10a.tlef）



/home/cad/CBDK/ADFP/Executable\_Package/Collaterals/Tech/APR/N16ADFP\_APR\_Innovus/N16ADFP\_APR\_Innovus\_11M.10a.tlef  
/home/cad/CBDK/ADFP/Executable\_Package/Collaterals/IP/stdcell/N16ADFP\_StdCell/LEF/lef/N16ADFP\_StdCell.lef

# Design import(3/4)

- ▶ 4.(Optional) IO Assignment File → add IO file
- ▶ 5.Power → Power Nets:VDD;Ground Nets:VSS

TSMC : VDD VSS  
UMC : VCC GND

Design Import — DarkSoul

**Netlist:**

☒ Verilog

Files: ../SYN/Thumb\_syn.v

Top Cell: ☐ Auto Assign ☒ By User: thumb

☐ OA

Library:

Cell:

View:

**Technology/Physical Libraries:**

☐ OA

Technology Libraries:

Reference Libraries:

Abstract View Names:

Layout View Names:

☒ LEF Files

../Collaterals/IP/stdcell/N16ADFP\_StdCell/LEF/lef/N16ADFP\_StdCell.lef

**Floorplan**

IO Assignment File:

**Power**

Power Nets: VDD

Ground Nets: VSS

CPF File:

**Analysis Configuration**

MMMC View Definition File:

OK Cancel Help

如果有IO配置檔就放

# Design import(4/4)

## ► 6. mmmc.view.stylus

Design Import — DarkSoul

**Netlist:**

☒ Verilog

Files:  ...

Top Cell: ☐ Auto Assign ☒ By User:

☐ OA

Library:

Cell:

View:

**Technology/Physical Libraries:**

☐ OA

Technology Libraries:

Reference Libraries:  ...

Abstract View Names:

Layout View Names:

☒ LEF Files

...

**Floorplan**

IO Assignment File:  ...

**Power**

Power Nets:

Ground Nets:

CPF File:  ...

**Analysis Configuration**

MMMC View Definition File:  ...

**mmmc.view.stylus**

OK Cancel Help

# Initial Step(1/3)

## 1.Connect global power

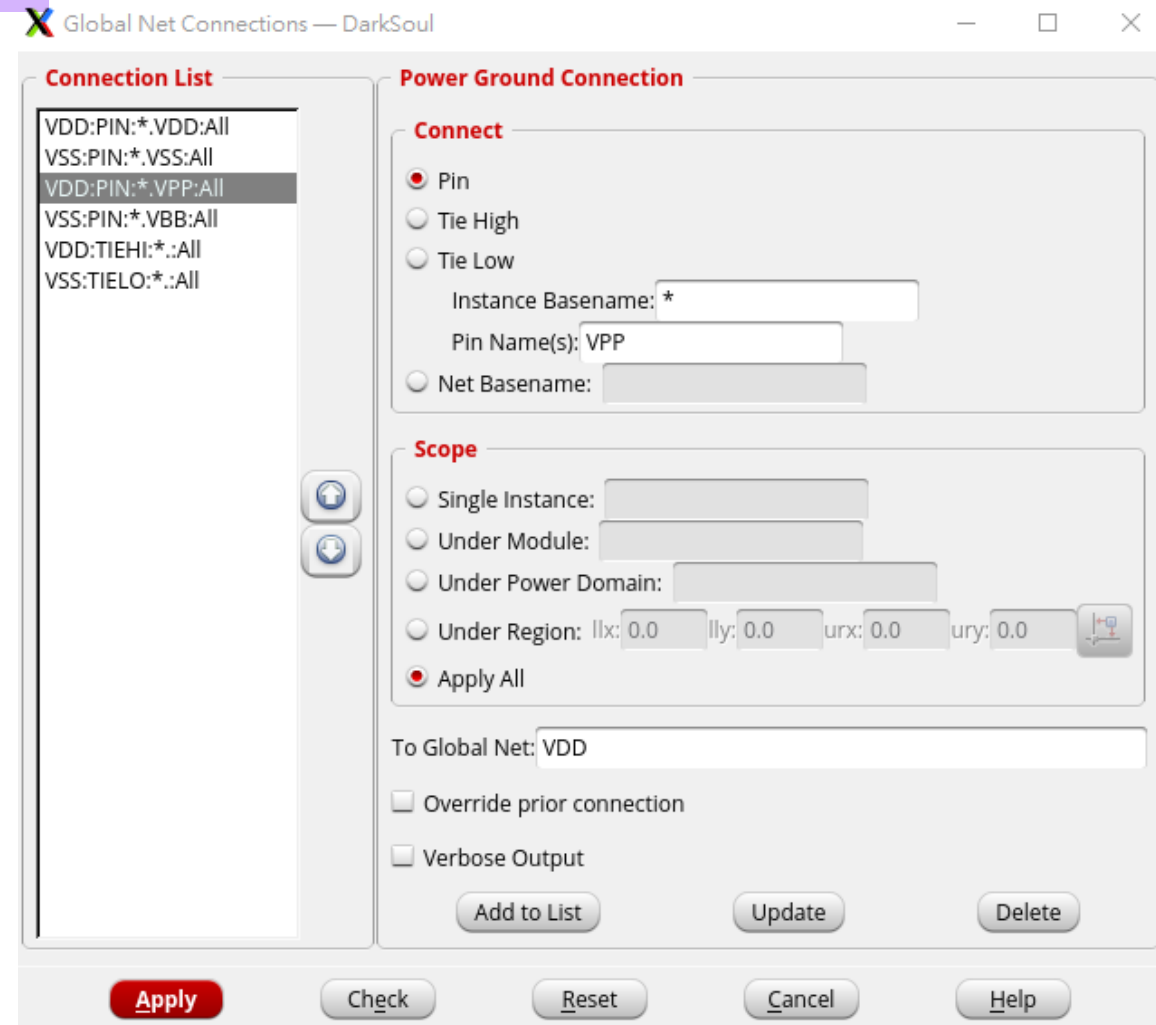
**Power → Connect Global Nets → Connect:Pin → Pin Name(s): VDD;  
Scope:Apply All; To Global Net: VDD → Add to List → Do it again but  
change VDD to VSS**

**Power → Connect Global Nets → Connect:Pin → Pin Name(s): VPP;  
Scope:Apply All; To Global Net: VDD → Add to List**

**Power → Connect Global Nets → Connect:Pin → Pin Name(s): VBB;  
Scope:Apply All; To Global Net: VSS → Add to List**

**Power → Connect Global Nets → Connect:Tie High → Scope:Apply All;  
To Global Net: VDD → Add to List**

**Power → Connect Global Nets → Connect:Tie Low → Scope:Apply All;  
To Global Net: VSS → Add to List → Apply → Check → Close**



# Initial Step(2/3)

▶ **innovus** > source -quiet ADFP\_APR\_script/config.tcl

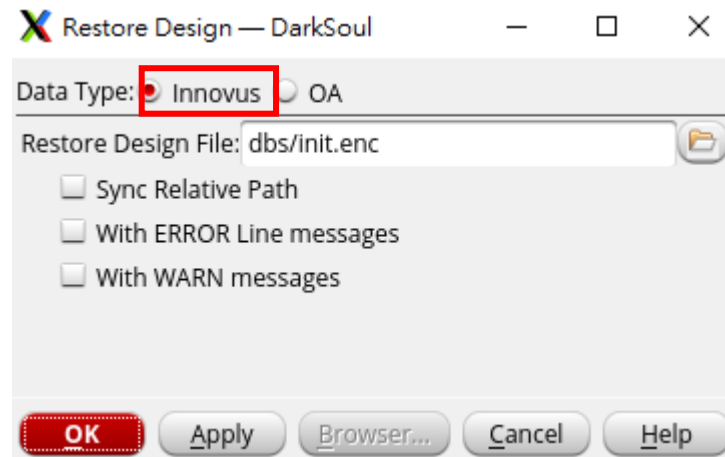
▶ **innovus** > source ADFP\_APR\_script/config\_cts.tcl

▶ **Save Design**

File → Save Design

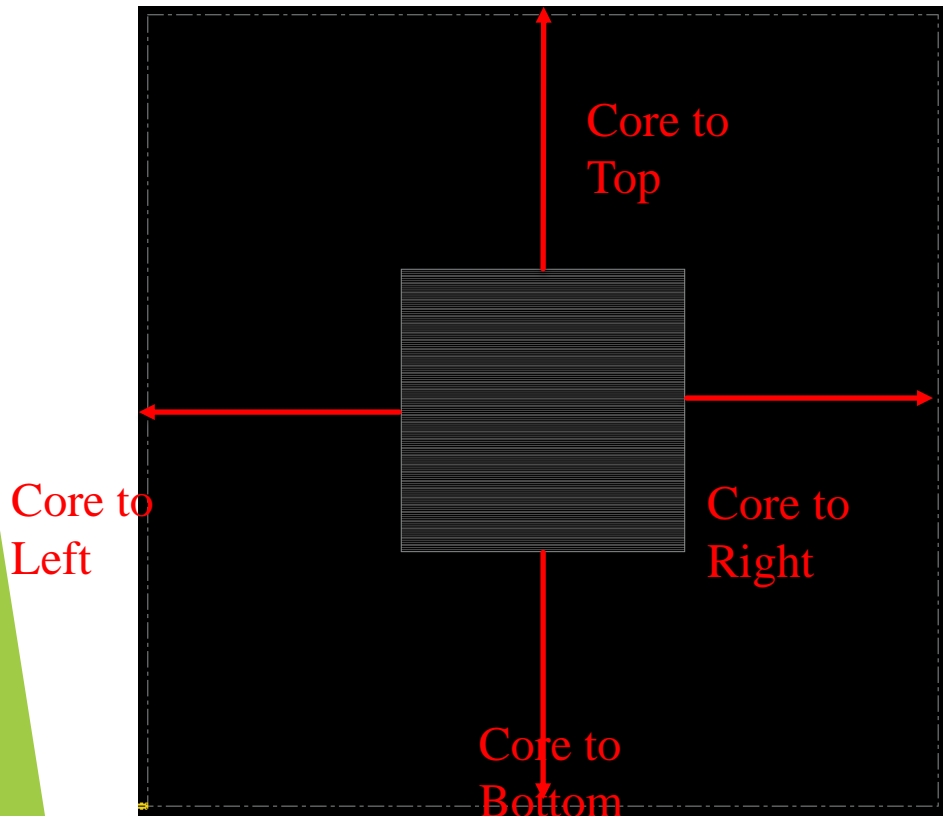
▶ **Restore Design**

File → Restore Design



# Initial Step(3/3)

- ▶ 3. Decide the overview of your design.
- ▶ Floorplan → Specify Floorplan... → ...
- ▶ Ratio (H/W):1 ; Core Utilization:0.7 ; (建議0.6-0.8)
- ▶ Core to Left:80; Core to Right:80; Core to Top:80; Core to Bottom:80;



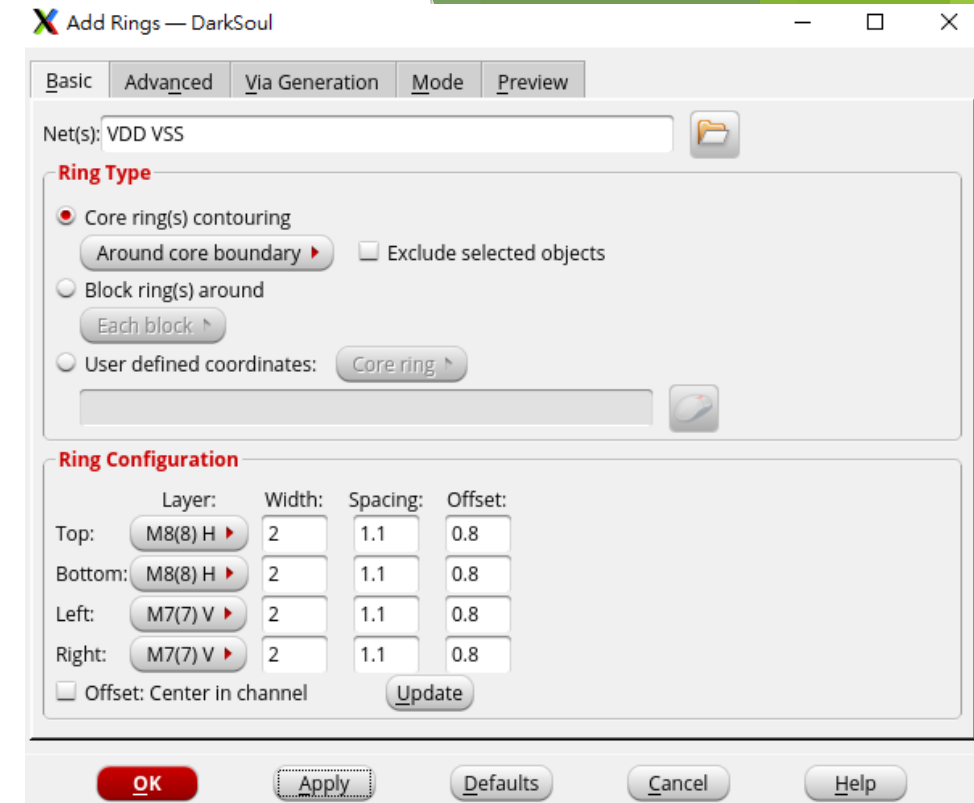
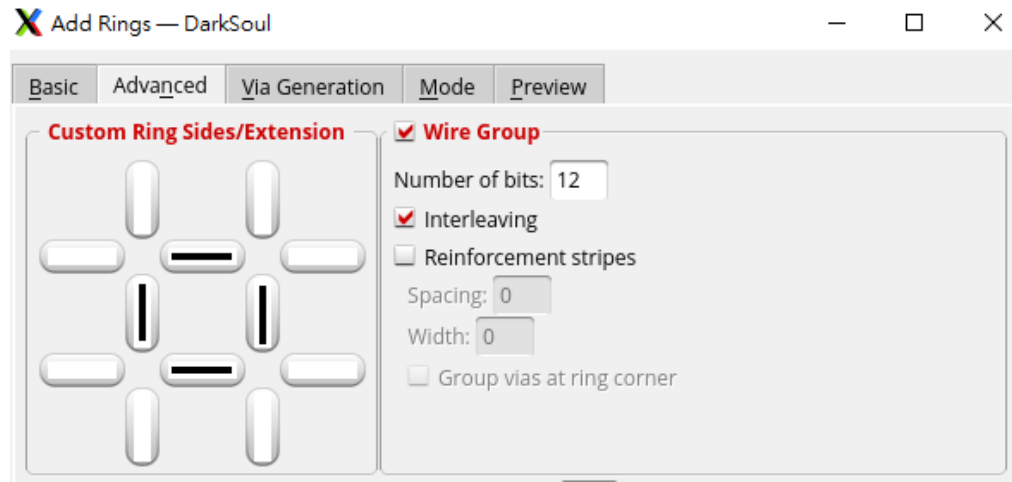
Density of your design



註：如果有PAD的話要調整適當的距離，如果Core跟PAD太接近，在後面接Power Ring及Route後，有可能會DRC錯誤

# PowerPlan(1/9)

- ▶ 1. **innovus** > source ADFP\_APR\_script/pns.tcl
- ▶ 2. Create Power Ring ---- To give Power to chip
- ▶ 3. Power → Power Planning → Add Rings → Basic
  - Nets: VDD VSS
  - In Ring Configuration, change Top & Bottom to METAL8, Left & Right to METAL7;
  - Set Width to 2 and Spacing to 1.1
- ▶ 4. Change to Advanced
  - Select Wire Group, set Numbers of Bits to 12
  - Select Interleaving

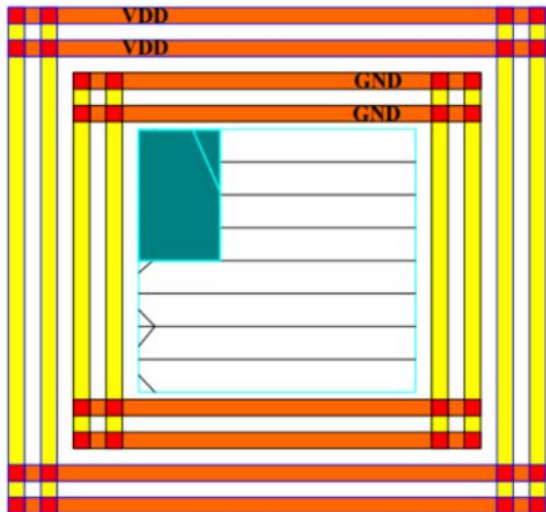




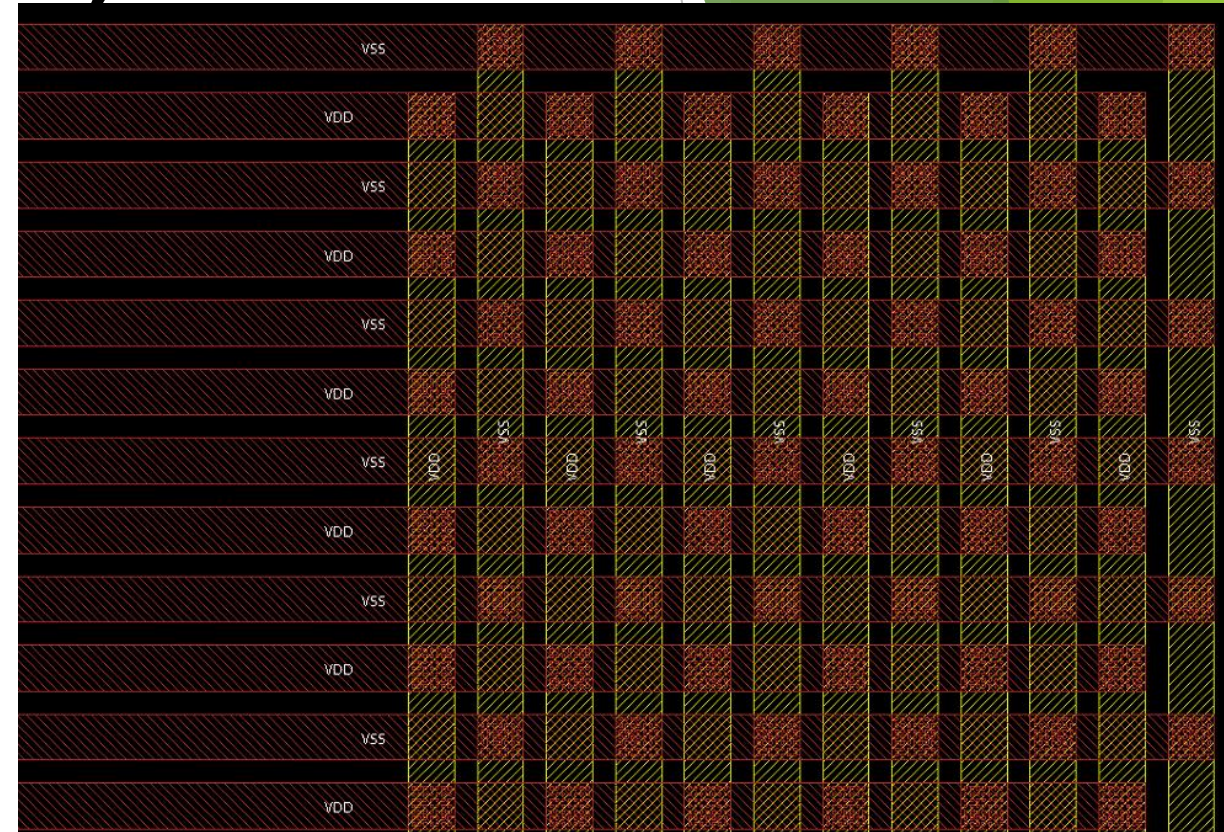
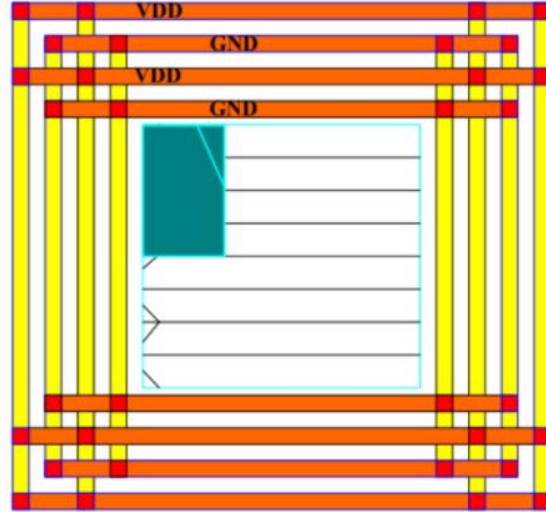
# PowerPlan(2/9)

## ► What's Interleaving?

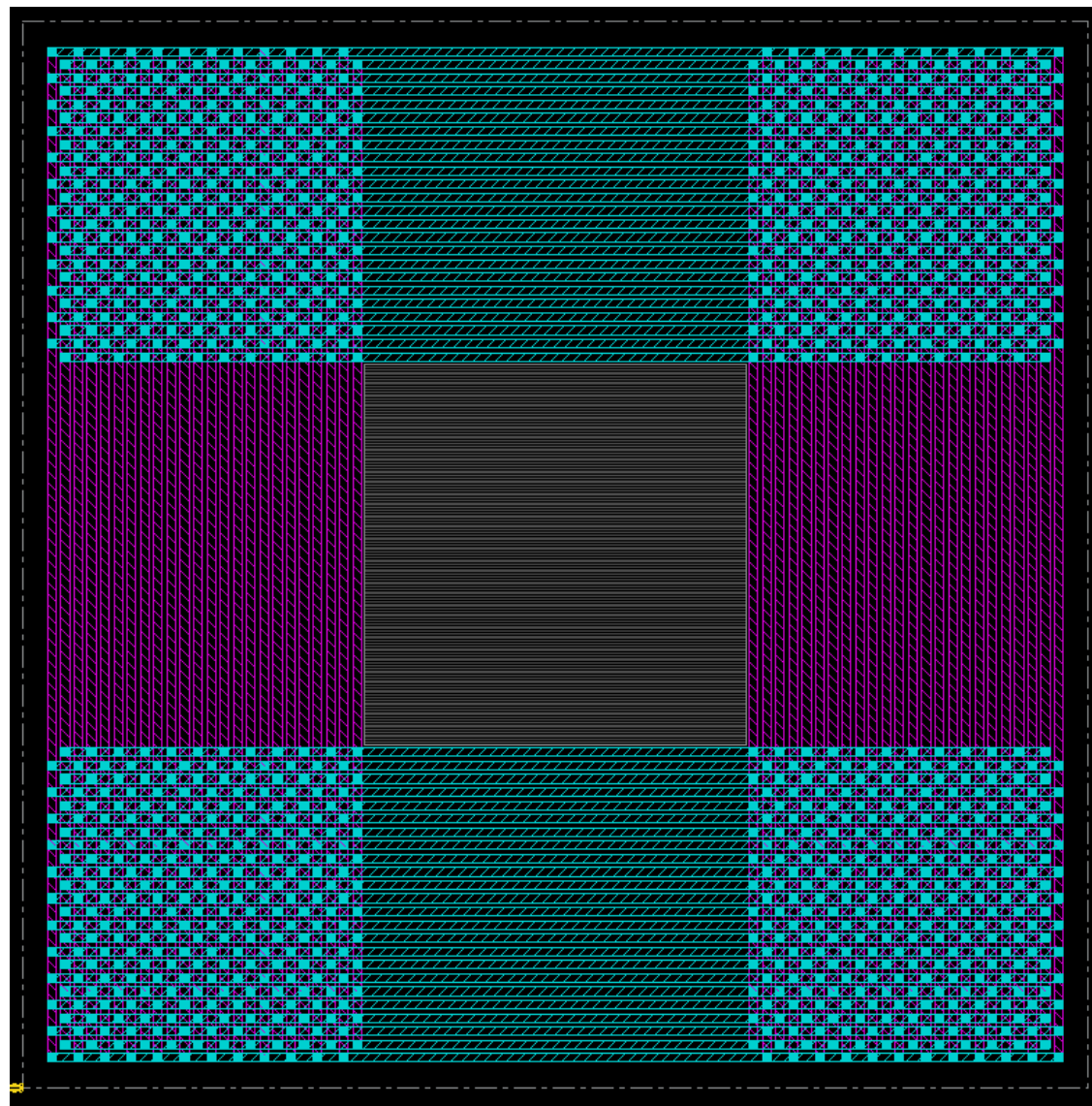
- ✓ Use wire group
- no interleaving
- ✓ number of bits = 2



- ✓ Use wire group
- ✓ interleaving
- ✓ number of bits = 2



# PowerPlan(3/9)



# PowerPlan(4/9)

5. Create Power Ring ---- To give Power to chip

6. Power → Power Planning → Add Rings → Basic

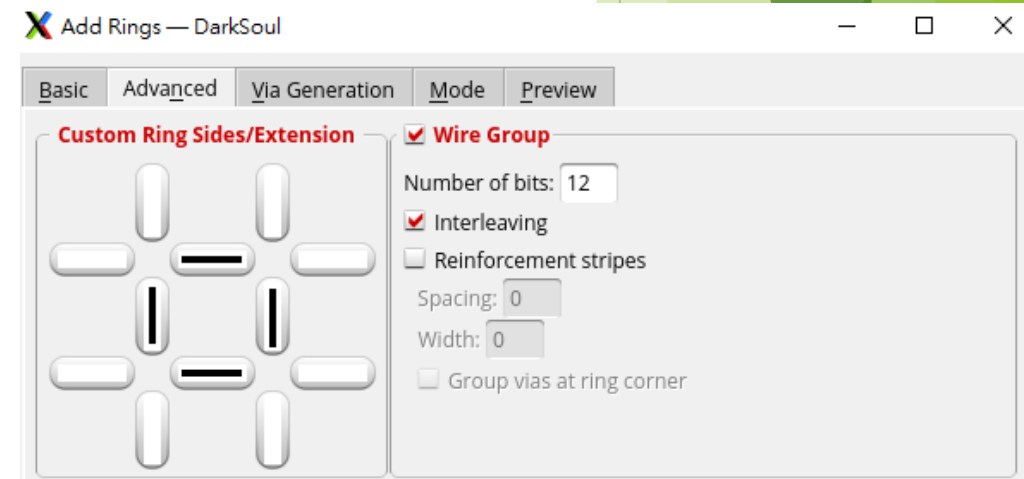
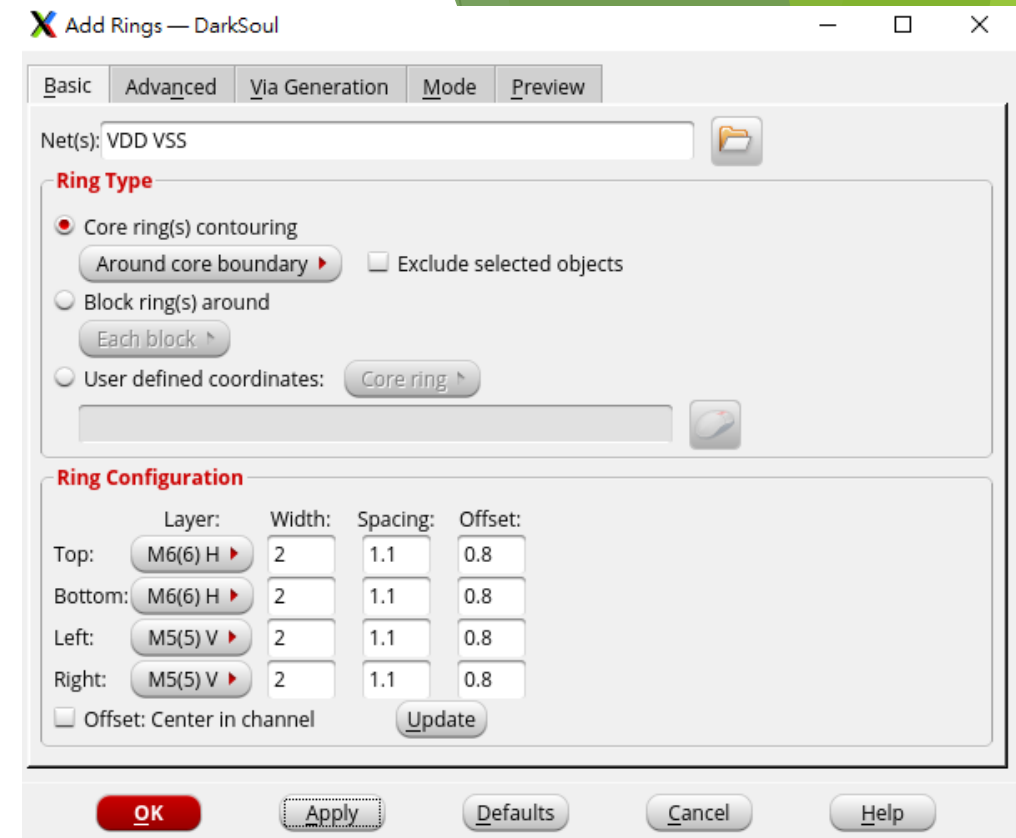
- Nets: VDD VSS
- In Ring Configuration, change Top & Bottom to **METAL6**, Left & Right to **METAL5**;
- Set Width to 2 and Spacing to 1.1

7. Change to Advanced

- Select Wire Group, set Numbers of Bits to 12
- Select Interleaving

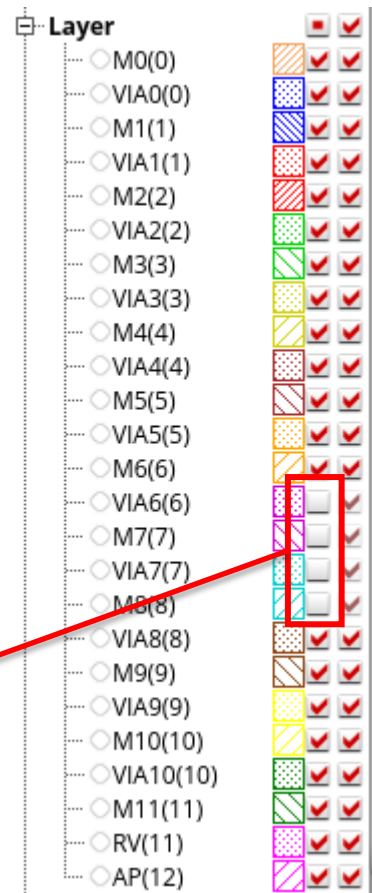
8. **innovus** > edit\_trim\_routes -nets {VDD VSS} -layer {M8 M7 M6 M5}

會把Power Ring 多餘的部分切掉

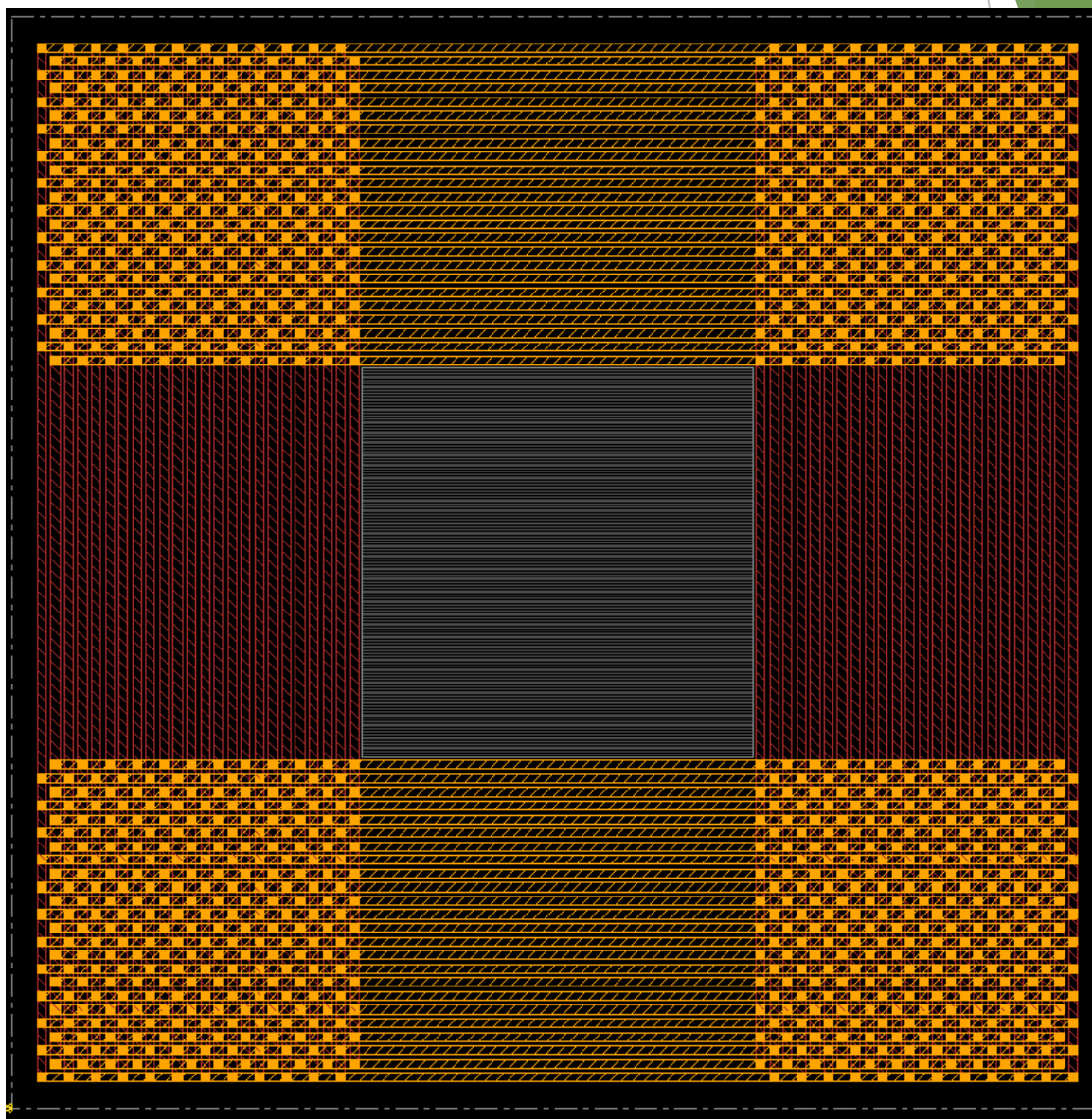




# PowerPlan(5/9)



把這4層勾選掉才能看到M5, M6



# PowerPlan(6/9)

## 8. Add stripe

- The deeper part of your design may not have enough power from power ring, so you need to add stripe to boost the voltage.
- Vertical stripe is recommended.

## 9. Power → Power Planning → Add Stripe → Basic

- Nets: VDD VSS
- Layers: METAL9 and select Vertical;
- Set Width to 1.8 and Spacing to 1.8
- In Set Pattern, select Set-to-set distance and input 7.2
- Select Relative from core or selected area
- Start: 1.8

The screenshot shows the 'Add Stripes' dialog box in the DarkSoul software. The 'Basic' tab is selected, and the configuration is as follows:

- Set Configuration:**
  - Net(s): VDD VSS
  - Layer: M9(9)
  - Directions: ☒ Vertical ☐ Horizontal
  - Width: 1.8
  - Spacing: 1.8
  - Update button
- Set Pattern:**
  - ☒ Set-to-set distance: 7.2
  - ☐ Number of sets: 1
  - ☐ Bumps: Over
  - ☐ Over P/G pins: Pin layer: Top pin layer, Pin Width:
  - ☐ Master name:
  - ☐ Selected blocks
  - ☒ All blocks
  - ☐ Over Physical Pins: Pin layer: Top pin layer, Pin Width:
- Stripe Boundary:**
  - ☒ Core ring
  - ☐ Pad ring: Outer
  - ☐ All domains
  - ☐ Design boundary
  - ☒ Create pins
  - ☐ Each selected block/domain/fence
  - ☐ Specify rectangular area: X1: , Y1: , X2: , Y2:
  - ☐ Specify rectilinear area:
- First/Last Stripe:**
  - Start from: ☒ Left ☐ Right ☐ Top ☐ Bottom
  - ☒ Relative from core or selected area: Start: 1.8, Stop:
  - ☐ Absolute: Start: , Stop:

Buttons at the bottom: OK, Apply, Defaults, Cancel, Help.

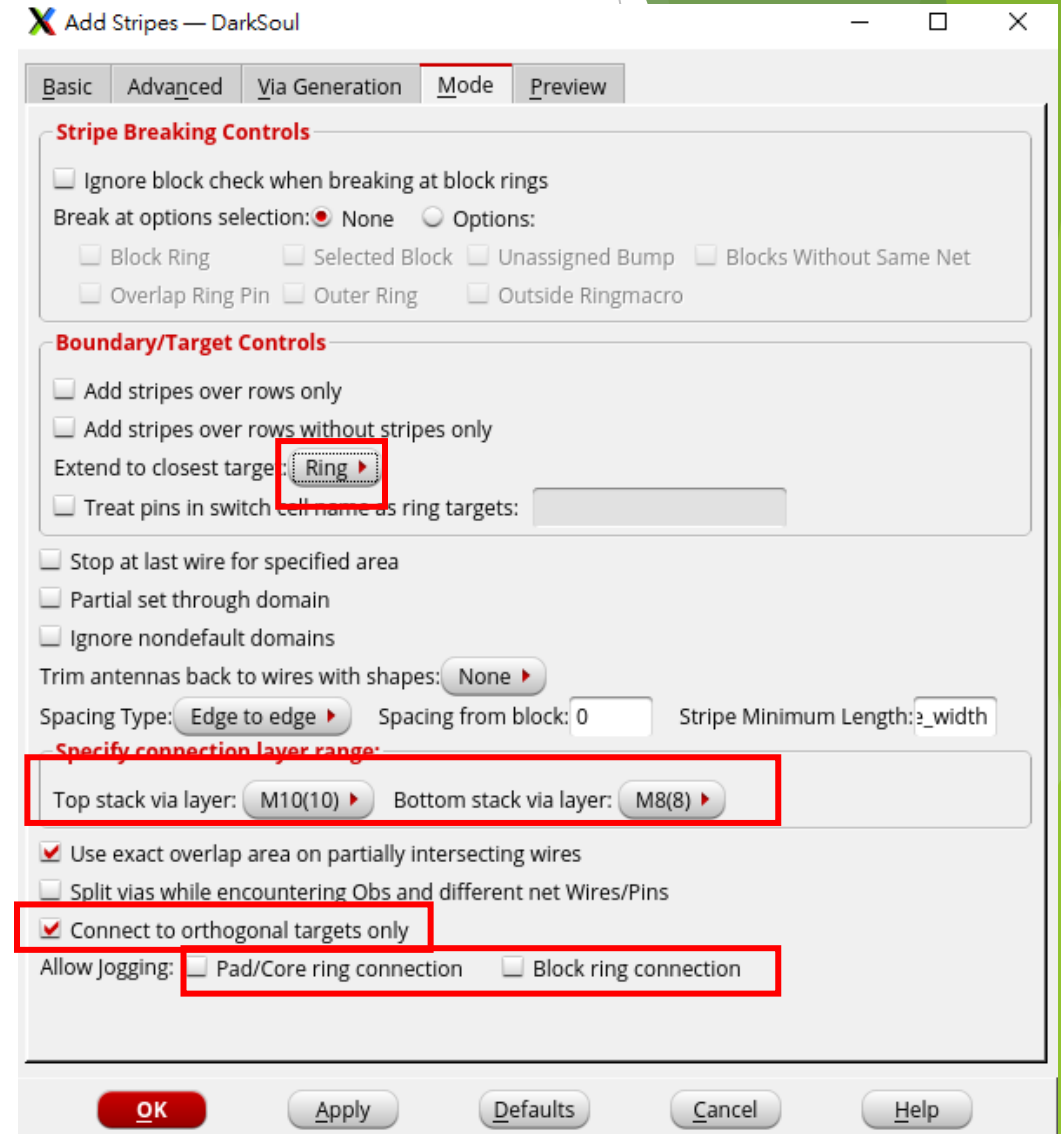
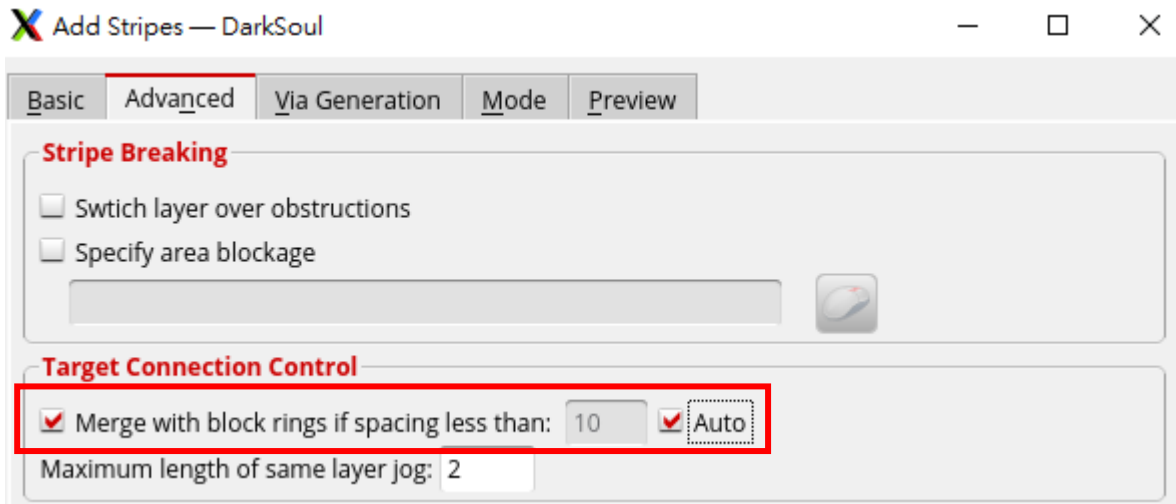
# PowerPlan(7/9)

## 10. Change to Advanced Page

- Choose Merge with block ring if spacing less then : 10
- Choose Auto

## 11. Change to Mode

- Extend to closest target: Ring
- Top Stack via layer: METAL10 Bottom Stack via layer: METAL8
- Choose Connect to orthogonal targets only
- un-choose Pad/Core ring connection & Block ring connection



# PowerPlan(8/9)

Net	Metal layer	dir	width	space	set to set	start	Top stack via	Bottom stack via	Snap to Routing grid
VDD VSS	M9	V	1.8	1.8	7.2	1.8	M10	M8	
VDD	M8	H	0.864	0	2.88	0	M9	M7	Half_Grid
VSS	M8	H	0.864	0	2.88	1.44	M9	M7	Half_Grid
VDD	M7	V	0.24	0	7.2	7.2	M8	M6	Grid
VSS	M7	V	0.24	0	7.2	3.6	M8	M6	Grid
VDD	M6	H	0.24	0	7.2	0	M7	M5	Grid
VSS	M6	H	0.24	0	7.2	3.6	M7	M5	Grid
VDD	M5	V	0.24	0	7.2	0	M6	M4	Grid
VSS	M5	V	0.24	0	7.2	3.6	M6	M4	Grid

Add Stripes — DarkSoul

Basic Advanced Via Generation Mode Preview

**Stripe Breaking**

☐ Switch layer over obstructions

☐ Specify area blockage

**Target Connection Control**

☒ Merge with block rings if spacing less than: 10 ☒ Auto

Maximum length of same layer jog: 2

**Layer Control for Target Connections**

Pad/Core rings Bottom limit: M1(1) Top limit: AP(12)

Block rings/Over obstructions Bottom limit: M1(1) Top limit: AP(12)

☐ **Wire Group**

☐ Interleaving Number of bits:

Snap wire center to routing grid: Half\_Grid

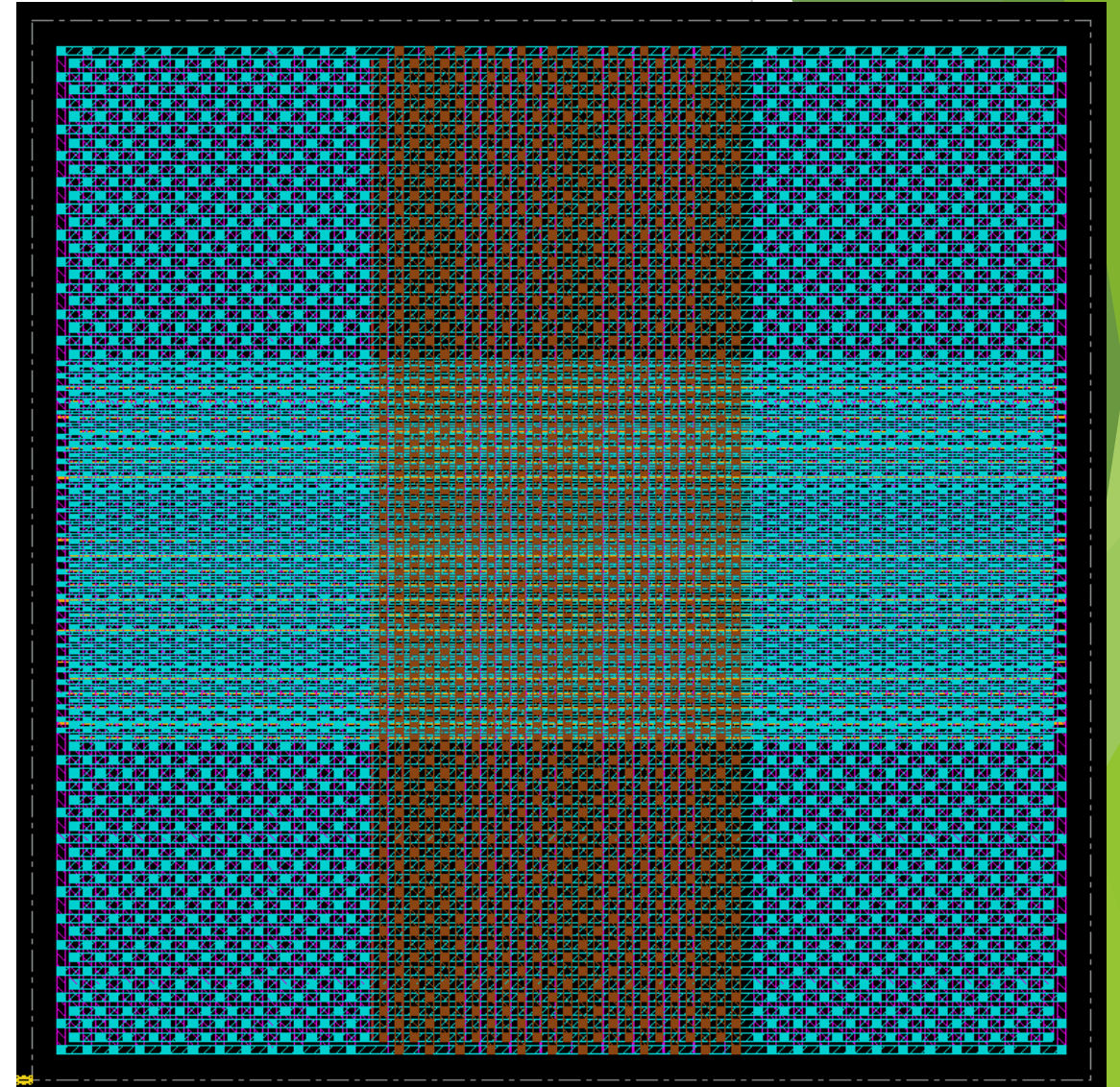
OK Apply Defaults Cancel Help



# PowerPlan(9/9)

## 12. Check → CheckDRC... → OK

```
VERIFY DRC ..... Sub-Area: {194.432 222.208 222.208 248.736} 80 of 81  
VERIFY DRC ..... Sub-Area : 80 complete 0 Viols.  
VERIFY DRC ..... Sub-Area: {222.208 222.208 248.940 248.736} 81 of 81  
VERIFY DRC ..... Sub-Area : 81 complete 0 Viols.  
Verification Complete : 0 Viols.
```





# Power Route(1/8)

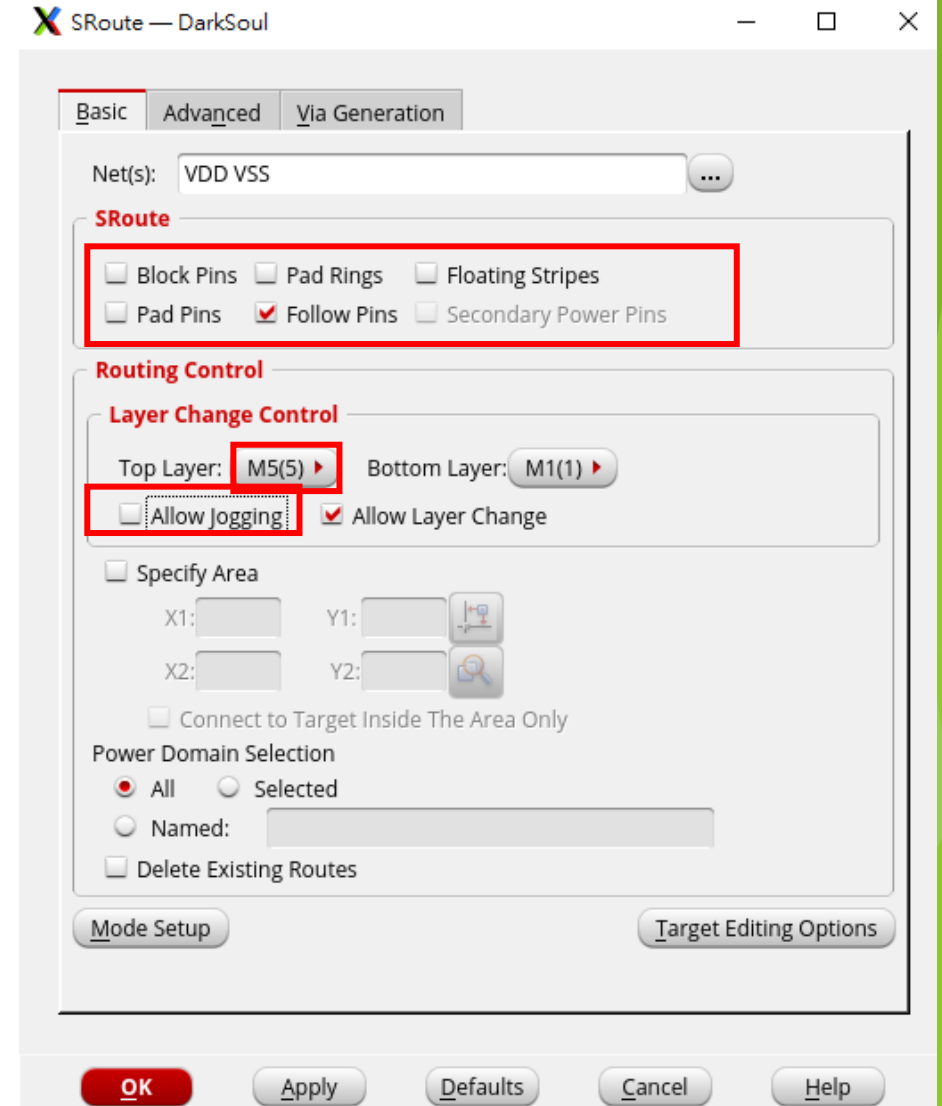
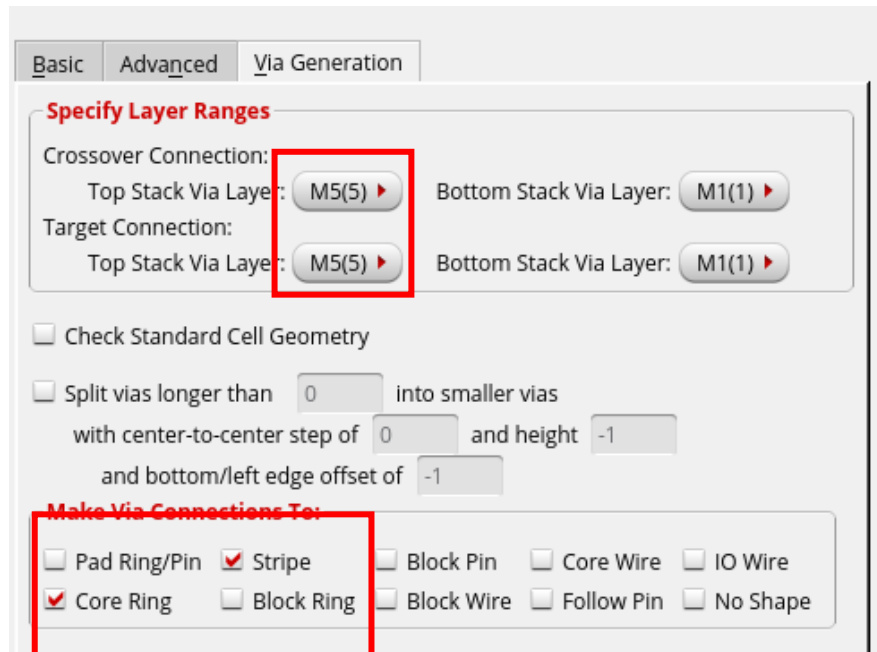
What's power route? ---- Connect all cell to power ring

1. Route → Special Route → Basic

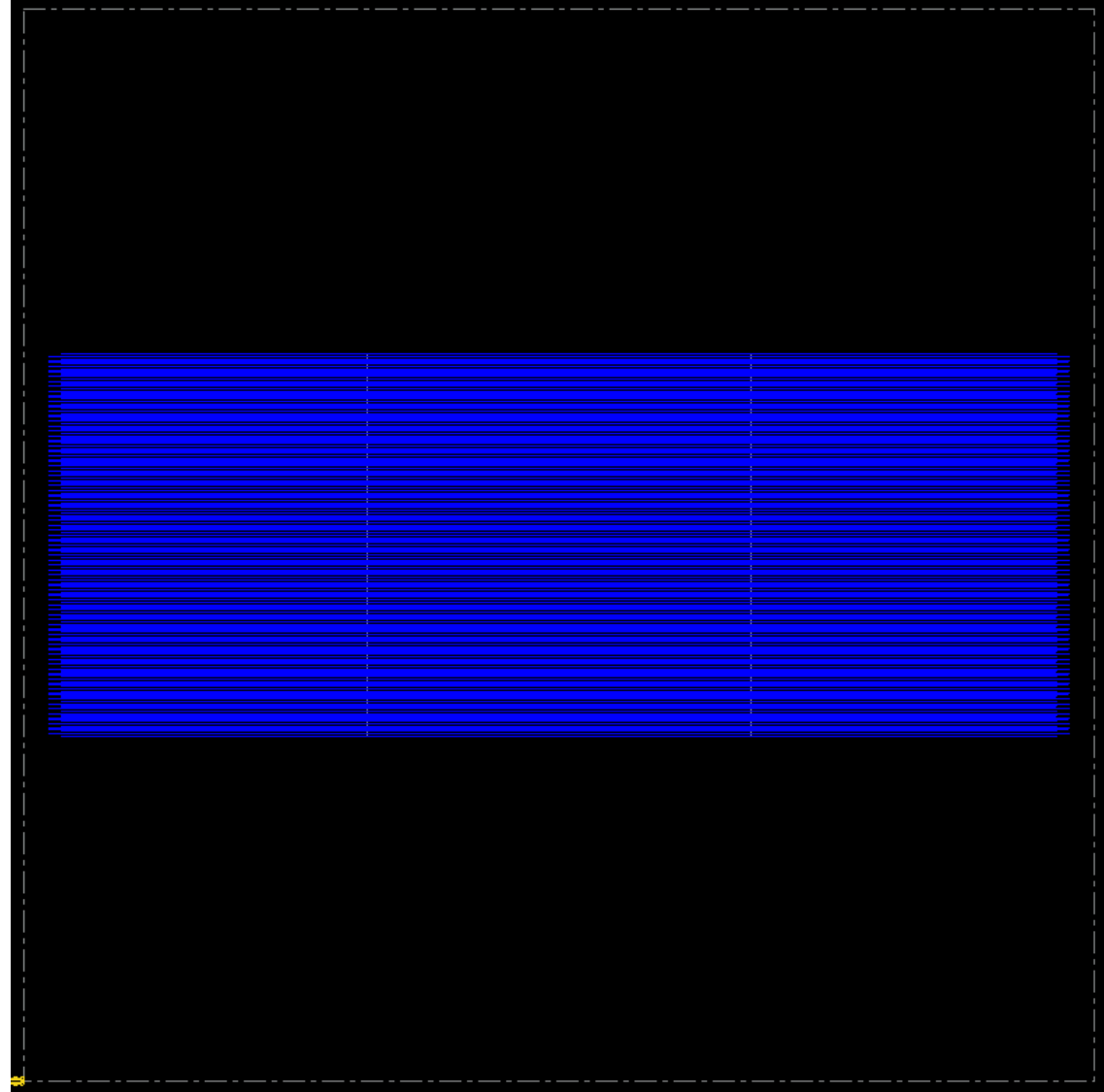
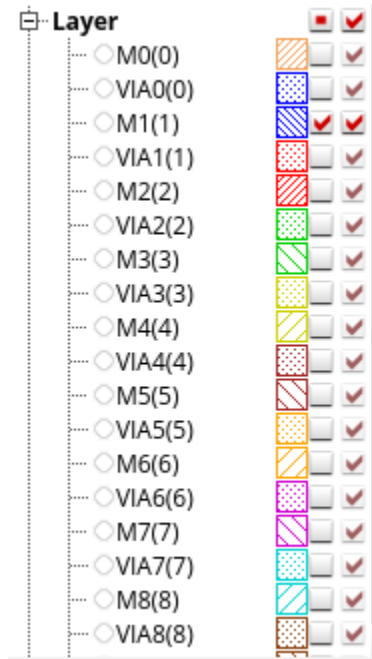
- Net(s): VDD VSS
- In SRoute, only select Follow pins
- un-choose Allow jogging

2. Change to Via Generation

- In Make Via Connection To, select Core Ring & Stripe
- Crossover Connection: Top Stack Via Layer: METAL5

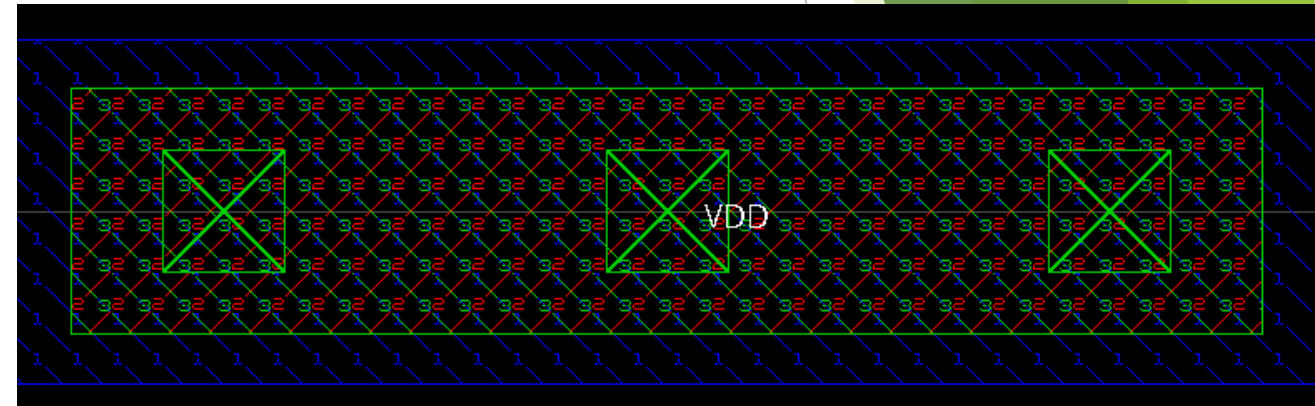
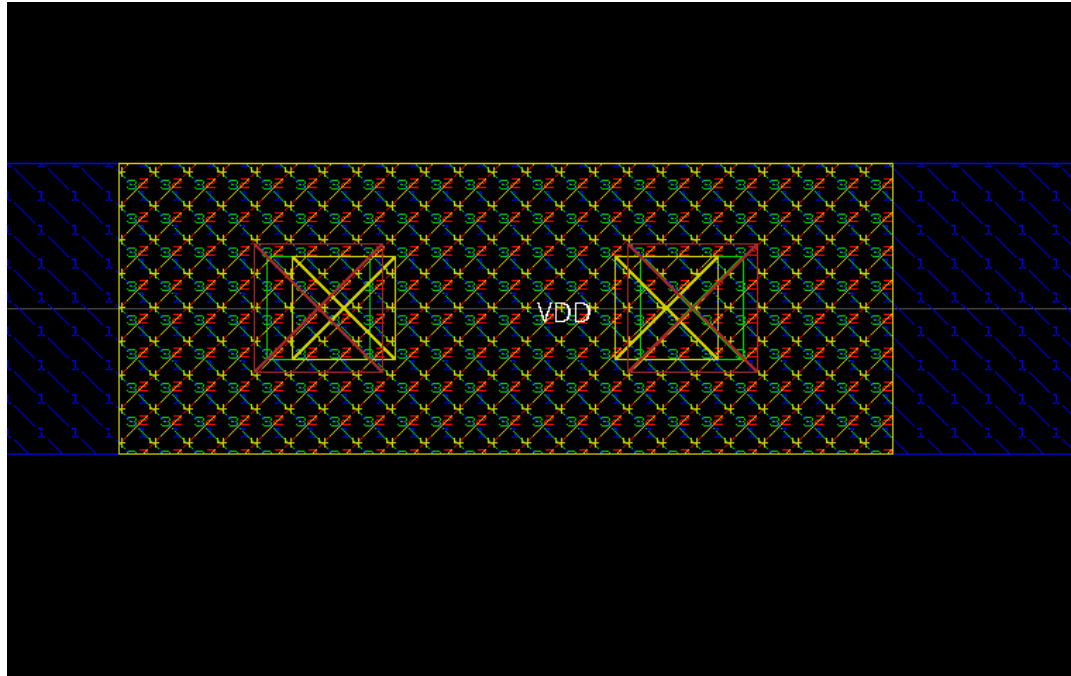


# Power Route(2/8)



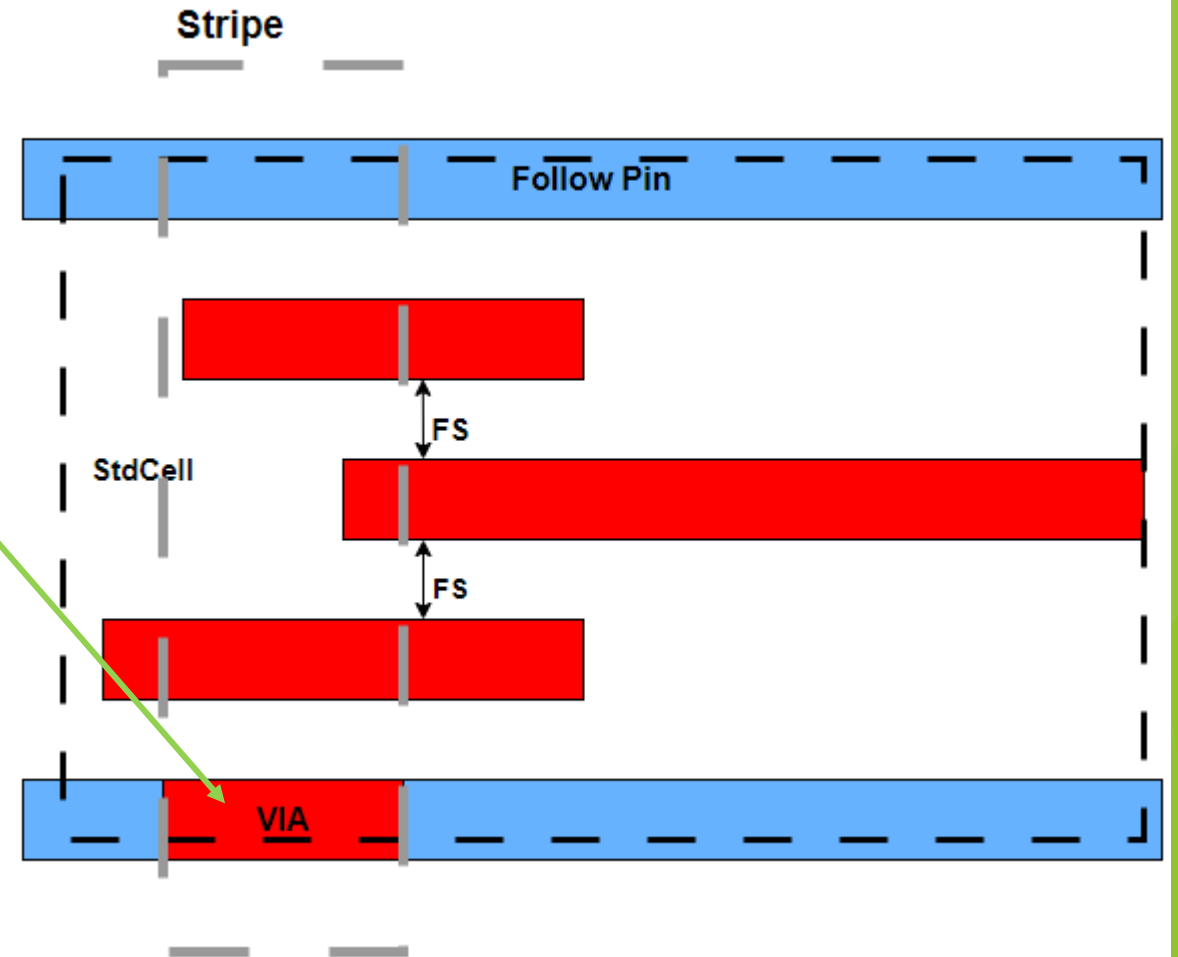
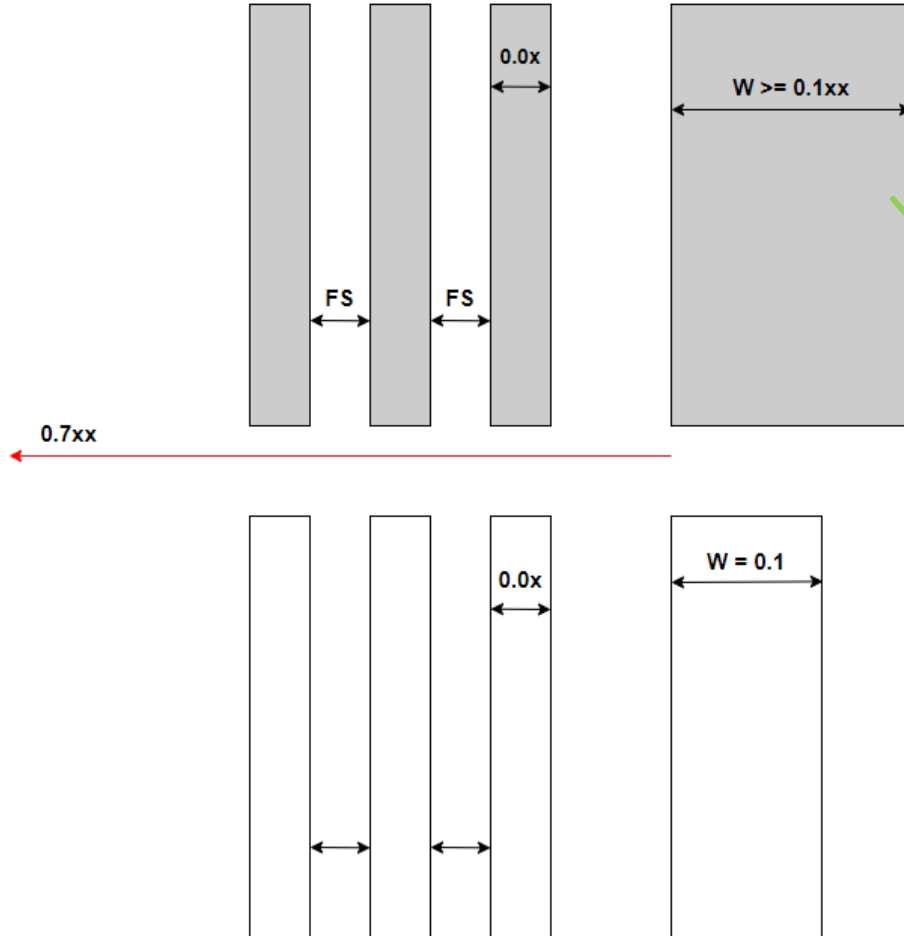
# Power Route(3/8)

3. **innovus** > source ADFP\_APR\_script/shrink\_via.tcl



# Power Route(4/8)

## ► Mxa Forbidden Spacing



# Power Route(5/8)

## 4. Power → Power Planning → Add Stripe → Basic

- Nets: VSS
- Layers: METAL2 and select Horizontal;
- Set Width to 0.064 and Spacing to 0
- In Set Pattern, select Set-to-set distance and input 1.152
- Select Relative from core or selected area
- Start: 0.544

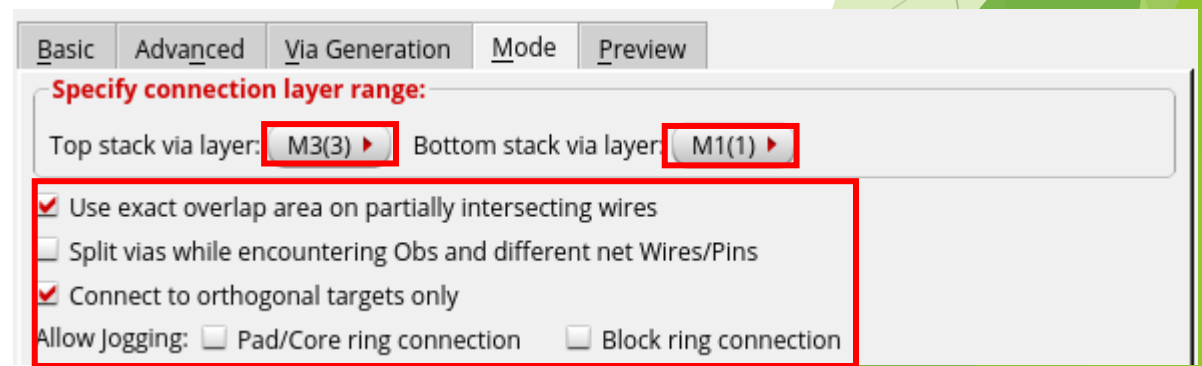
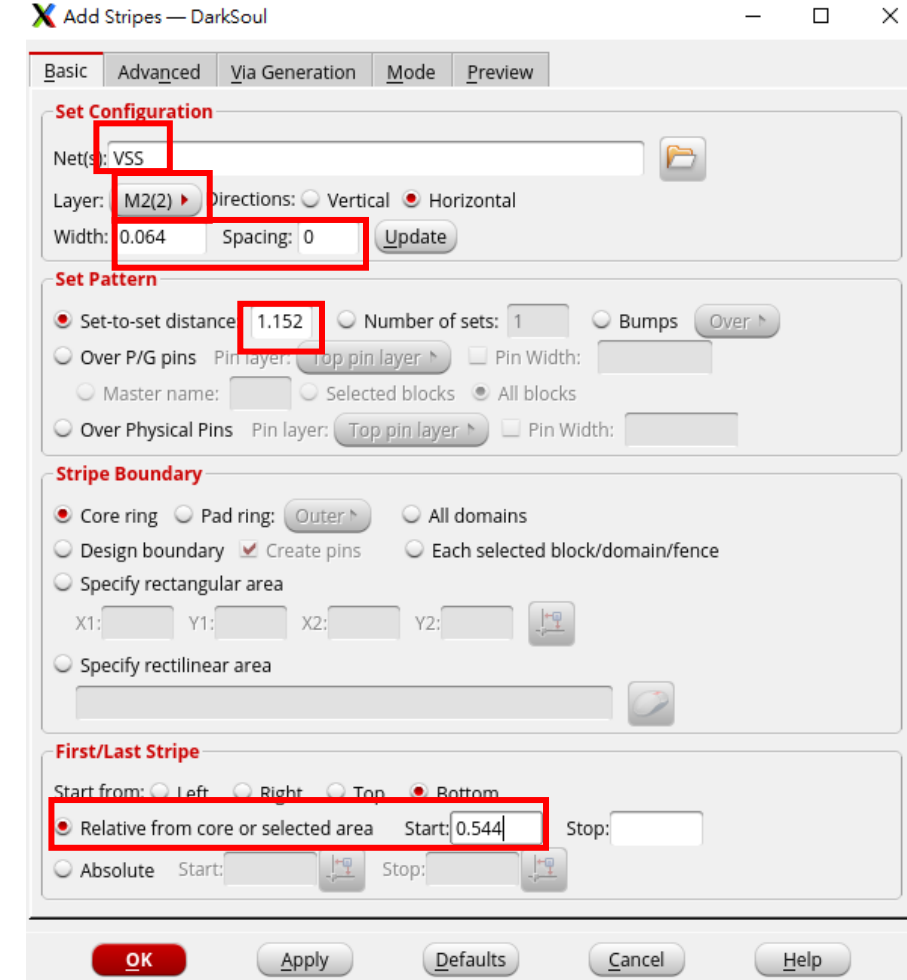
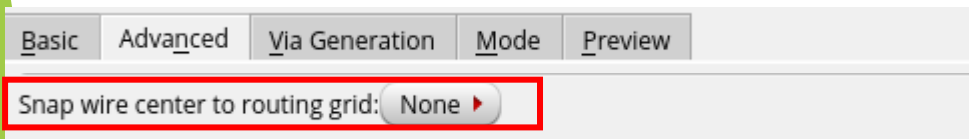
## 5. Change to Advanced Page

- Snap wire center to routing grid : select “None”

## 6. Change to Mode

- Extend to closest target: Ring
- Top Stack via layer: METAL3 Bottom Stack via layer: METAL1
- un-choose Pad/Core ring connection & Block ring connection

## 7. Click Apply



# Power Route(6/8)

## 8. Change VSS to VDD

- Nets: VDD
- Start: -0.032

## 9. Click Apply

Add Stripes — DarkSoul

Basic Advanced Via Generation Mode Preview

**Set Configuration**

Net(s): VDD

Layer: M2(2) Directions: ☐ Vertical ☒ Horizontal

Width: 0.064 Spacing: 0 Update

**Set Pattern**

☒ Set-to-set distance: 1.152 ☐ Number of sets: 1 ☐ Bumps Over

☐ Over P/G pins Pin layer: Top pin layer ☐ Pin Width:

☐ Master name:  ☐ Selected blocks ☒ All blocks

☐ Over Physical Pins Pin layer: Top pin layer ☐ Pin Width:

**Stripe Boundary**

☒ Core ring ☐ Pad ring: Outer ☐ All domains

☐ Design boundary ☒ Create pins ☐ Each selected block/domain/fence

☐ Specify rectangular area

X1:  Y1:  X2:  Y2:

☐ Specify rectilinear area

**First/Last Stripe**

Start from: ☐ Left ☐ Right ☐ Top ☒ Bottom

☒ Relative from core or selected area Start: -0.032 Stop:

☐ Absolute Start:  Stop:

OK Apply Defaults Cancel Help

# Power Route(7/8)

## 10. Check → Check Connectivity...

- Net Type: Special Only
- Nets: VDD VSS
- In Check, un-choose DanglingWire (Antenna)

There should not have any violation and X on the screen.

```
***** End: VERIFY CONNECTIVITY *****  
Verification Complete : 0 Viols. 0 Wrngs.  
(CPU Time: 0:00:00.1 MEM: 0.000M)
```

Verify Connectivity — DarkSoul

**Net Type**

☐ All  
☐ Regular Only  
☒ Special Only

**Nets**

☐ All  
☐ Selected  
☒ Named: VDD VSS

**Check**

<input checked="" type="checkbox"/> Open	<input checked="" type="checkbox"/> UnConnected Pin	<input checked="" type="checkbox"/> Unrouted Net
<input type="checkbox"/> Connectivity Loop	<input type="checkbox"/> DanglingWire (Antenna)	<input checked="" type="checkbox"/> Weakly Connected Pin
<input type="checkbox"/> Geometry Loop	<input type="checkbox"/> Geometry Connectivity	<input type="checkbox"/> Keep Previous Results
<input type="checkbox"/> Divide Power Net	<input checked="" type="checkbox"/> Soft PG Connect	<input type="checkbox"/> Raw Violations Mark
<input type="checkbox"/> Use new open Vio	<input type="checkbox"/> Remove old open Vio	<input type="checkbox"/> Use Virtual Connection
<input type="checkbox"/> TSV Die Abstract File		

Verify Connectivity Report: thumb.conn.rpt

**Report Limits**

Error: 1000  
Warning: 50

Set Multiple CPU...

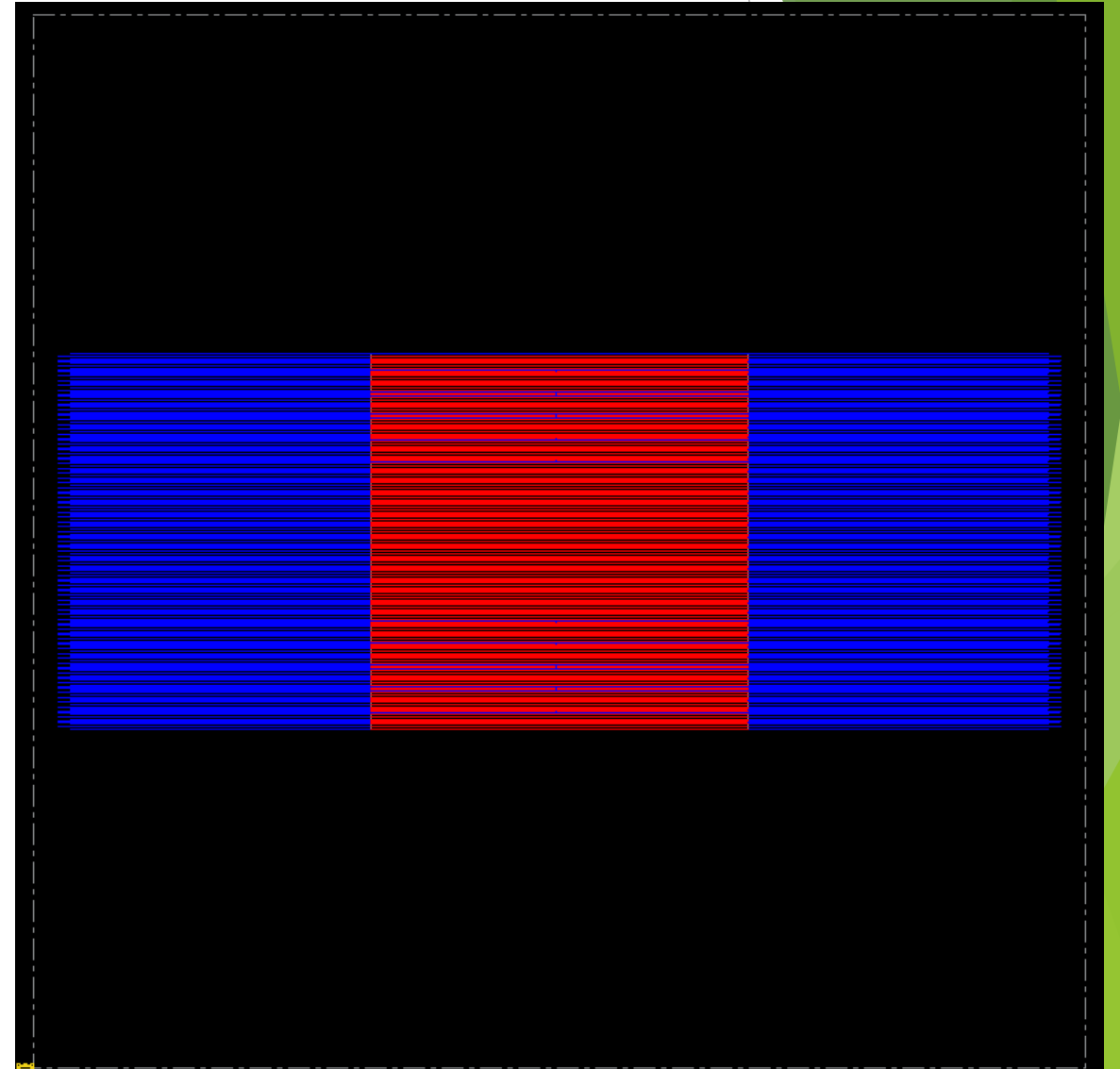
OK Apply Cancel Help

# Power Route(8/8)

12. Check → CheckDRC... → OK

```
VERIFY DRC ..... Sub-Area : 80 complete 0 Viols.  
VERIFY DRC ..... Sub-Area: {222.208 222.208 248.940 248.736} 81 of 81  
VERIFY DRC ..... Sub-Area : 81 complete 0 Viols.  
Verification Complete : 0 Viols.
```

Layer			
M0(0)			<input checked="" type="checkbox"/>
VIA0(0)			<input checked="" type="checkbox"/>
M1(1)			<input checked="" type="checkbox"/>
VIA1(1)			<input checked="" type="checkbox"/>
M2(2)			<input checked="" type="checkbox"/>
VIA2(2)			<input checked="" type="checkbox"/>
M3(3)			<input checked="" type="checkbox"/>
VIA3(3)			<input checked="" type="checkbox"/>
M4(4)			<input checked="" type="checkbox"/>
VIA4(4)			<input checked="" type="checkbox"/>
M5(5)			<input checked="" type="checkbox"/>
VIA5(5)			<input checked="" type="checkbox"/>
M6(6)			<input checked="" type="checkbox"/>
VIA6(6)			<input checked="" type="checkbox"/>
M7(7)			<input checked="" type="checkbox"/>
VIA7(7)			<input checked="" type="checkbox"/>
M8(8)			<input checked="" type="checkbox"/>
VIA8(8)			<input checked="" type="checkbox"/>
M9(9)			<input checked="" type="checkbox"/>
VIA9(9)			<input checked="" type="checkbox"/>
M10(10)			<input checked="" type="checkbox"/>
VIA10(10)			<input checked="" type="checkbox"/>
M11(11)			<input checked="" type="checkbox"/>
RV(11)			<input checked="" type="checkbox"/>

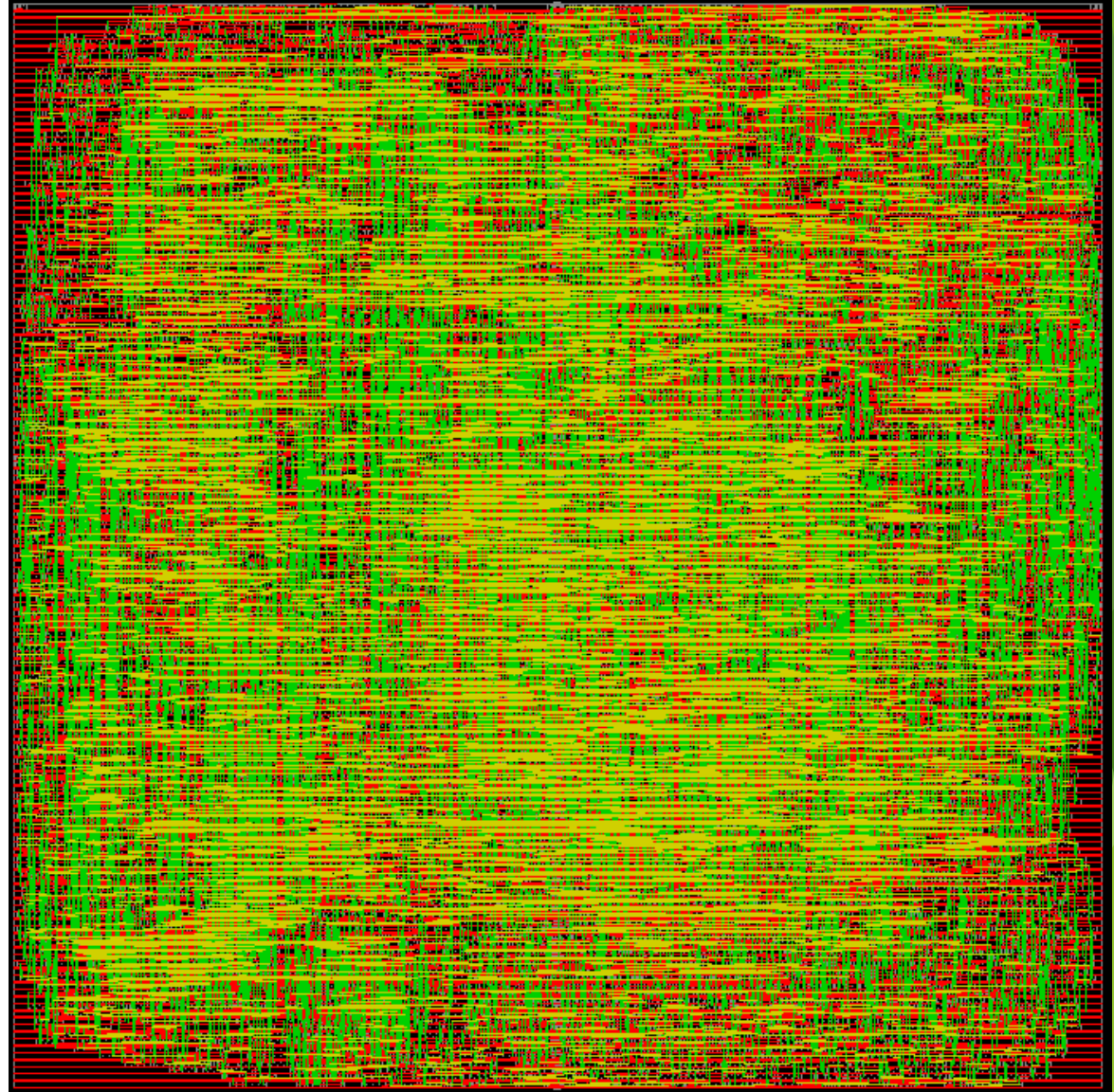




# Placement(1/3)

1. **innovus** > source ADFP\_APR\_script/add\_well\_taps.tcl
2. Place → Place Standard Cell → Click OK
3. Place → Check Placement → Click Ok

```
Begin checking placement ... (start mem=4451.4M, init mem=4451.4M)
*info: Placed = 13587          (Fixed = 78)
*info: Unplaced = 0
```



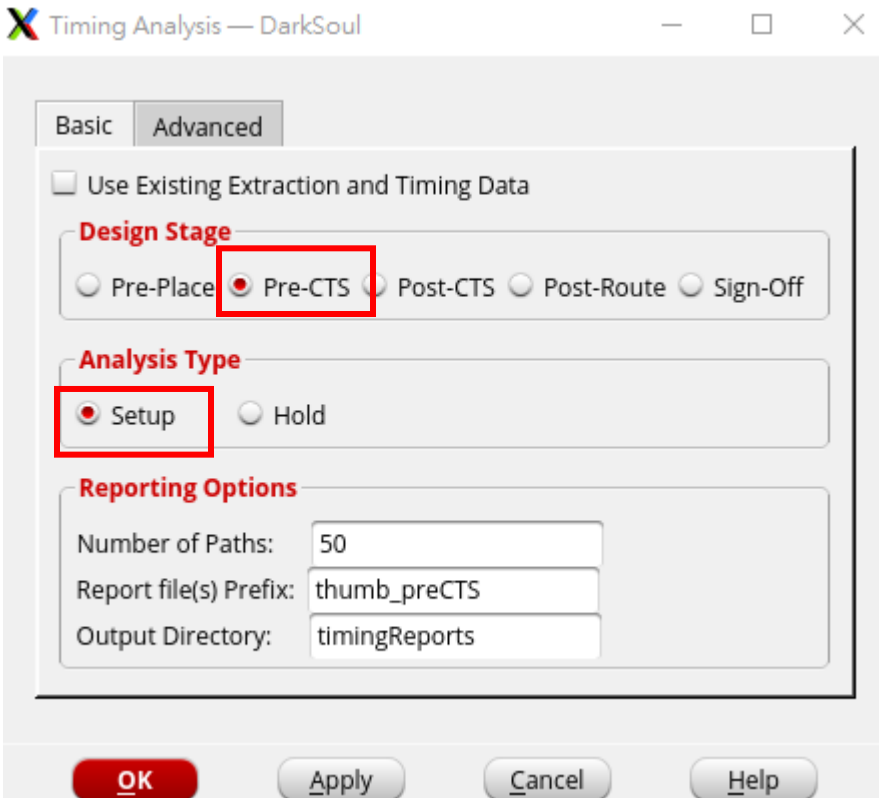
# Placement(2/3)

## ► 4. Timing → Report Timing

- Design Stage : Choose Pre-CTS

-Analysis Type : Choose Setup

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	-1.009	-1.009	0.154	0.456	N/A	0.000
TNS (ns):	164.026	164.026	0.000	0.000	N/A	0.000
Violating Paths:	339	339	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0



The image shows a screenshot of the 'Timing Analysis' dialog box in the DarkSoul software. The 'Basic' tab is selected. The 'Use Existing Extraction and Timing Data' checkbox is unchecked. Under 'Design Stage', the 'Pre-CTS' radio button is selected and highlighted with a red box. Under 'Analysis Type', the 'Setup' radio button is selected and highlighted with a red box. Under 'Reporting Options', the 'Number of Paths' is set to 50, 'Report file(s) Prefix' is 'thumb\_preCTS', and 'Output Directory' is 'timingReports'. At the bottom, there are buttons for 'OK', 'Apply', 'Cancel', and 'Help'.

Timing Analysis — DarkSoul

Basic Advanced

☐ Use Existing Extraction and Timing Data

**Design Stage**

☐ Pre-Place ☒ Pre-CTS ☐ Post-CTS ☐ Post-Route ☐ Sign-Off

**Analysis Type**

☒ Setup ☐ Hold

**Reporting Options**

Number of Paths: 50

Report file(s) Prefix: thumb\_preCTS

Output Directory: timingReports

OK Apply Cancel Help

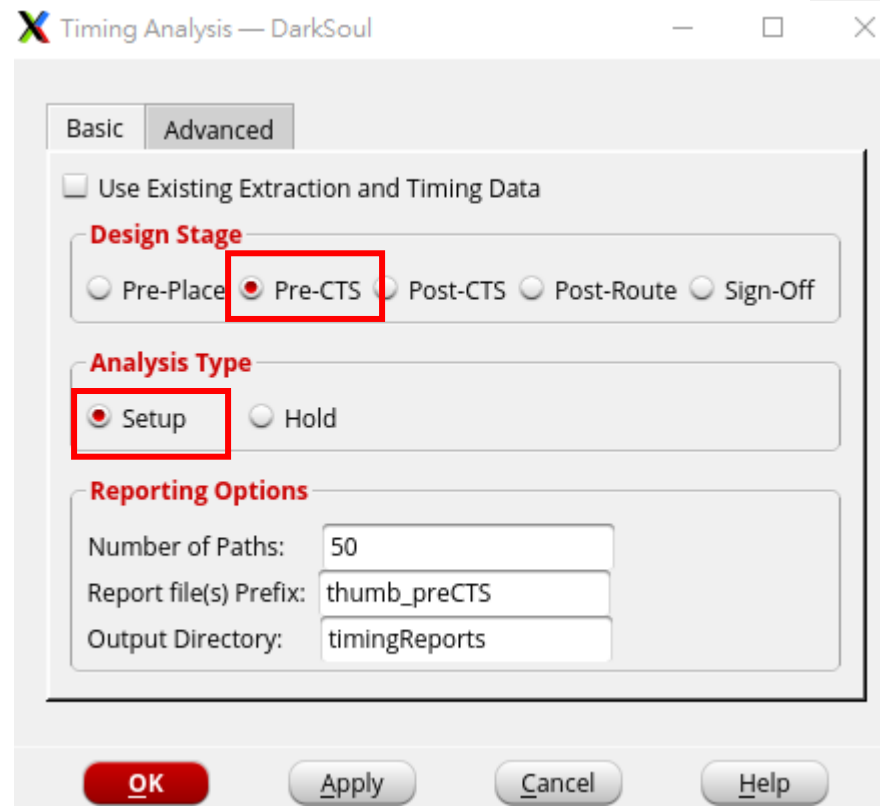
# Placement(3/3)

## 5. ECO → Optimize Design

- Design Stage : Choose Pre-CTS
- Optimization Type : Choose Max Fanout

## 6. Timing → Report Timing

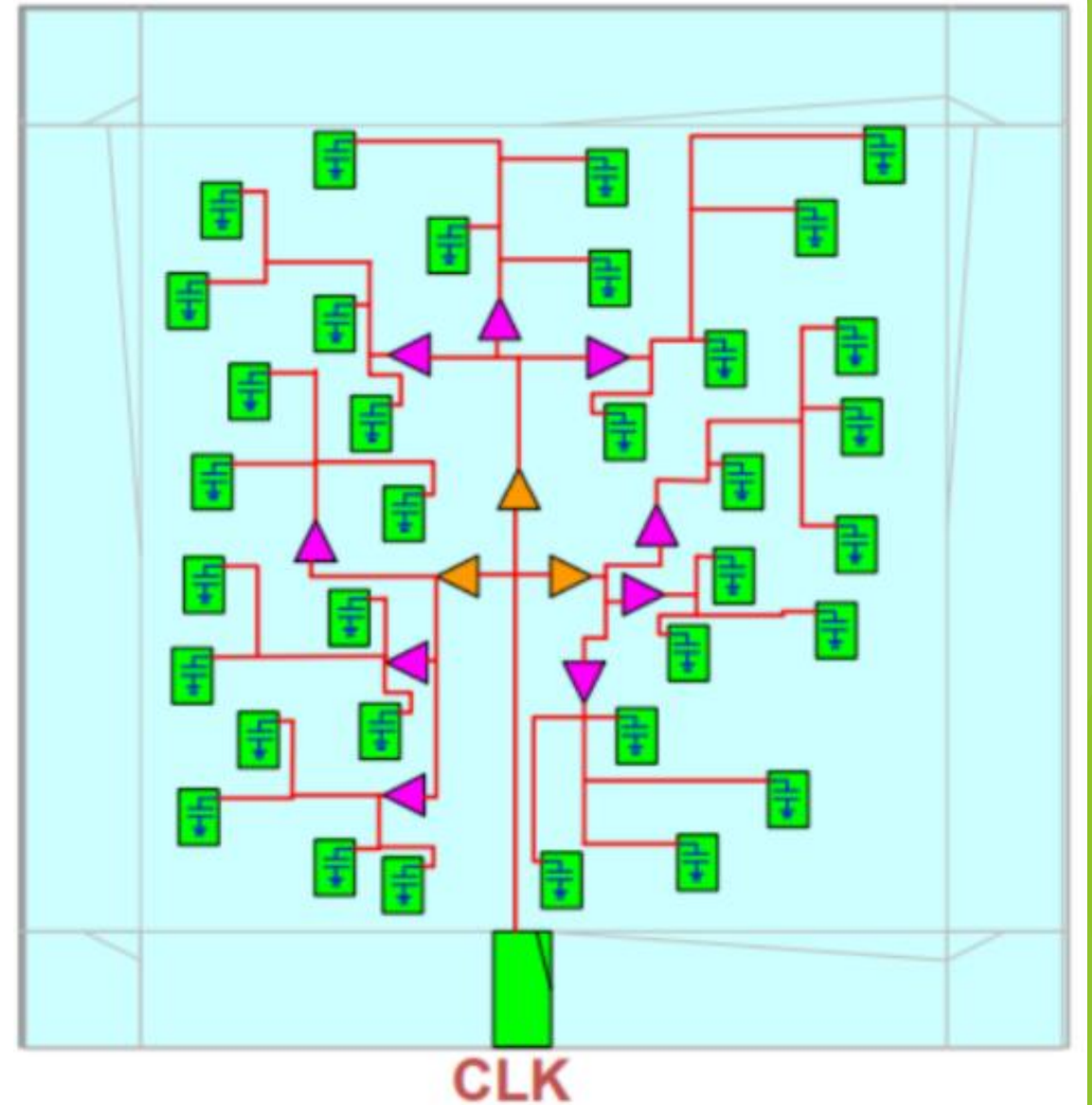
- Design Stage : Choose Pre-CTS
- Analysis Type : Choose Setup



# CTS(1/6)

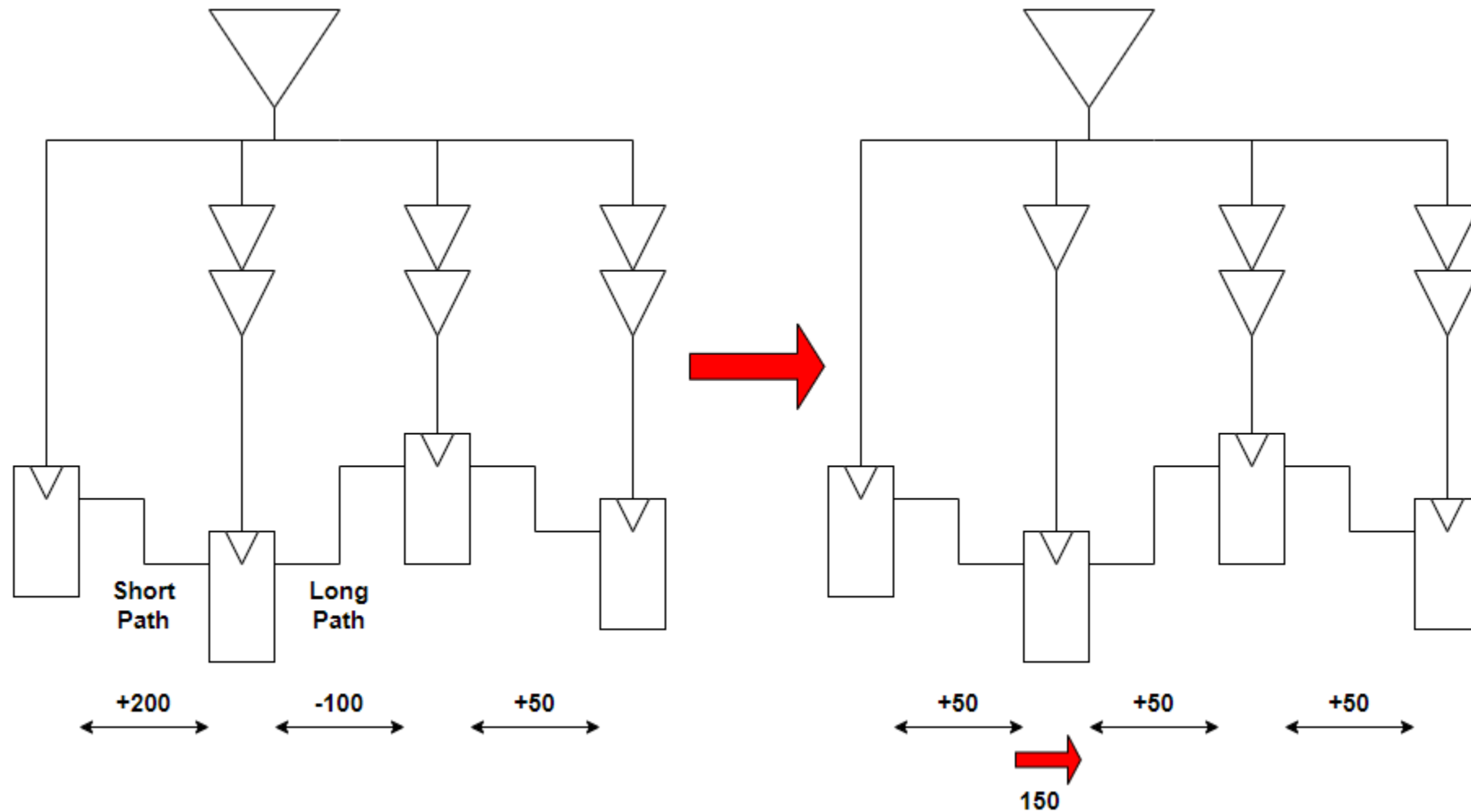
► Clock Tree Synthesis(CTS), To solve Clock problem:

- Heavy clock net loading
- Long clock insertion delay
- Clock skew
- Skew across clocks
- Clock to signal coupling effect
- Clock is power hungry



# CTS(2/6)

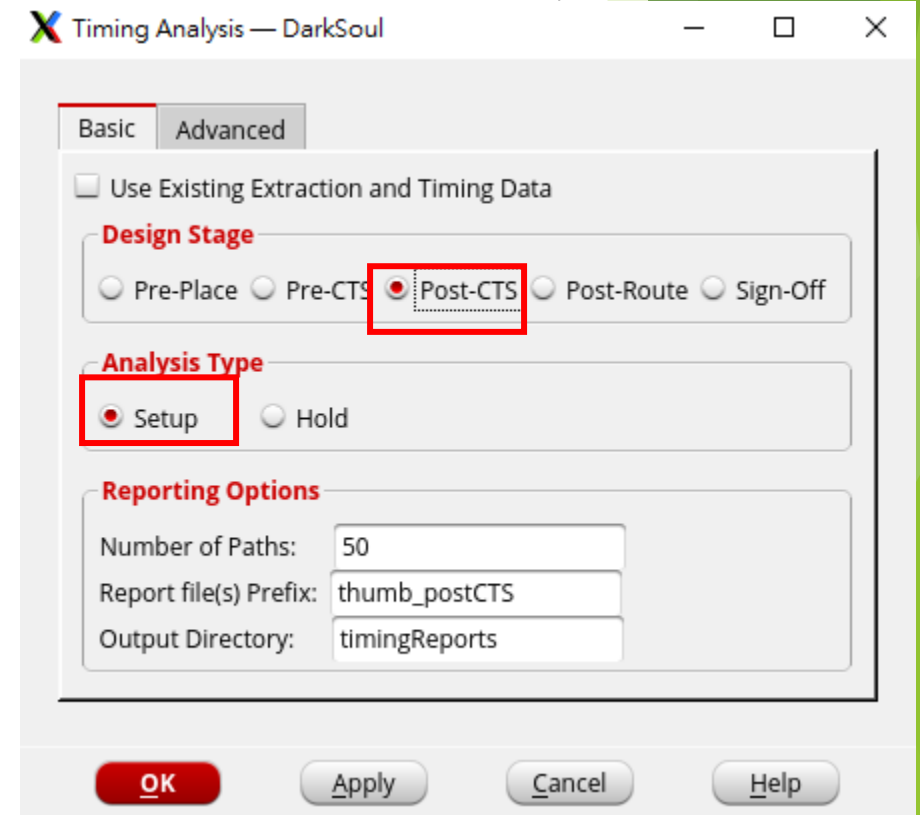
## ► Clock Concurrent Optimization



# CTS(3/6)

- ▶ 1. **innovus** > set\_interactive\_constraint\_modes [all\_constraint\_modes]
- ▶ 2. **innovus** > reset\_clock\_latency [all\_clocks]
- ▶ 3. **innovus** > ccopt\_design
- ▶ 4. Timing → Report Timing
  - Design Stage : Choose Post-CTS
  - Analysis Type : Choose Setup

Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.001	0.001	0.297	0.413	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1349	734	1006	66	N/A	0





# CTS(4/6)

- 5. Timing → Report Timing
  - Design Stage : Choose Post-CTS
  - Analysis Type : Choose hold

Timing Analysis — DarkSoul

Basic Advanced

☐ Use Existing Extraction and Timing Data

**Design Stage**

☐ Pre-Place ☐ Pre-CTS ☒ Post-CTS ☐ Post-Route ☐ Sign-Off

**Analysis Type**

☐ Setup ☒ Hold

**Reporting Options**

Number of Paths: 50

Report file(s) Prefix: thumb\_postCTS

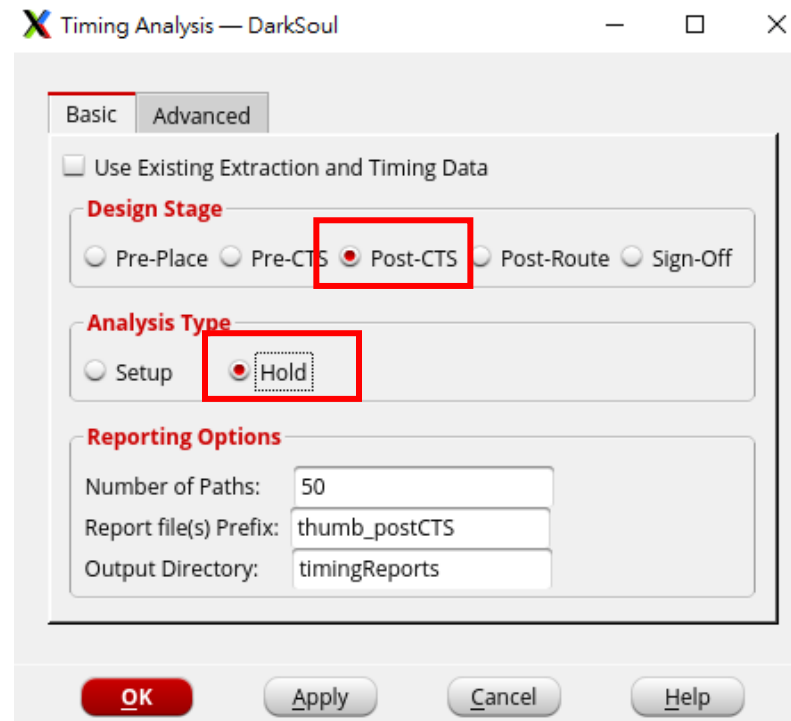
Output Directory: timingReports

OK Apply Cancel Help

Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	-0.061	0.027	-0.061	0.041	N/A	0.000
TNS (ns):	-28.644	0.000	-28.644	0.000	N/A	0.000
Violating Paths:	724	0	724	0	N/A	0
All Paths:	1349	734	1006	66	N/A	0

# CTS(5/6)

- ▶ 6. ECO → Optimize Design
  - Design Stage : Choose Post-CTS
  - Optimization Type : Choose Hold
  - Optimization Type : Choose Max Fanout
- ▶ 7. Timing → Report Timing
  - Design Stage : Choose Post-CTS
  - Analysis Type : Choose Hold

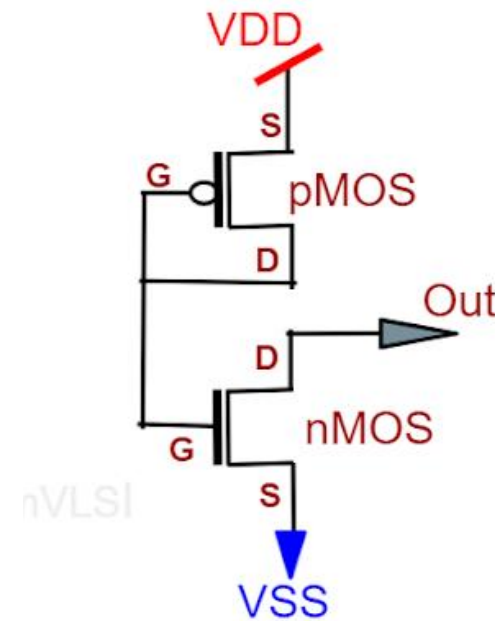
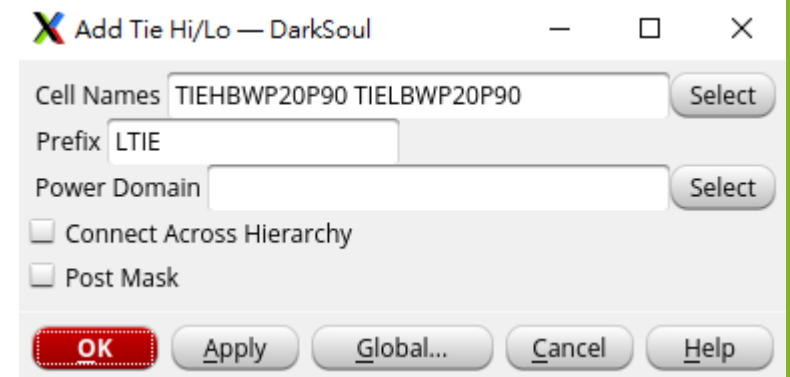
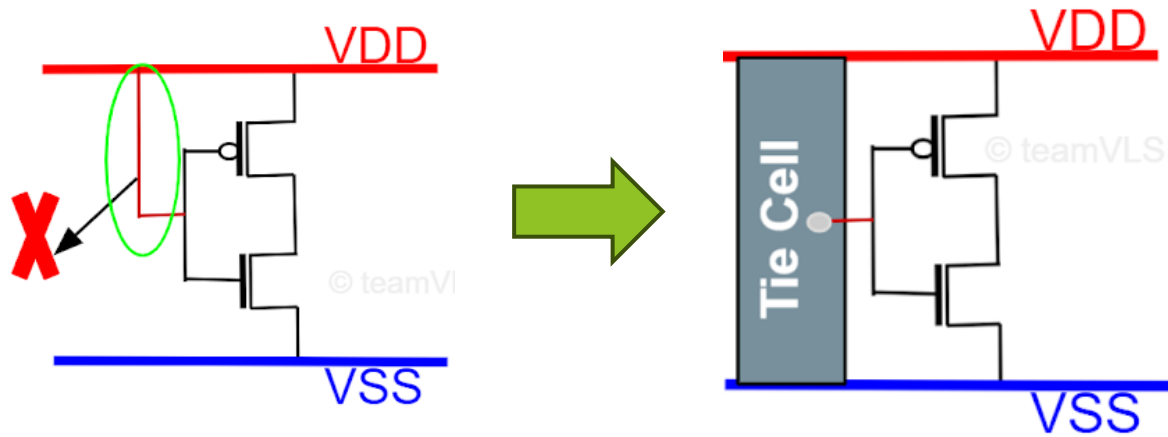




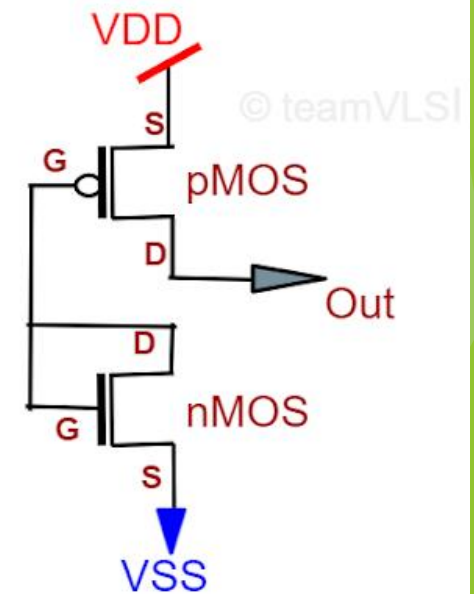
# CTS(6/6)

## ► 8. Add Tie HI / LO cell

- Place → Tie HI / LO → Add



Tie-low Cell

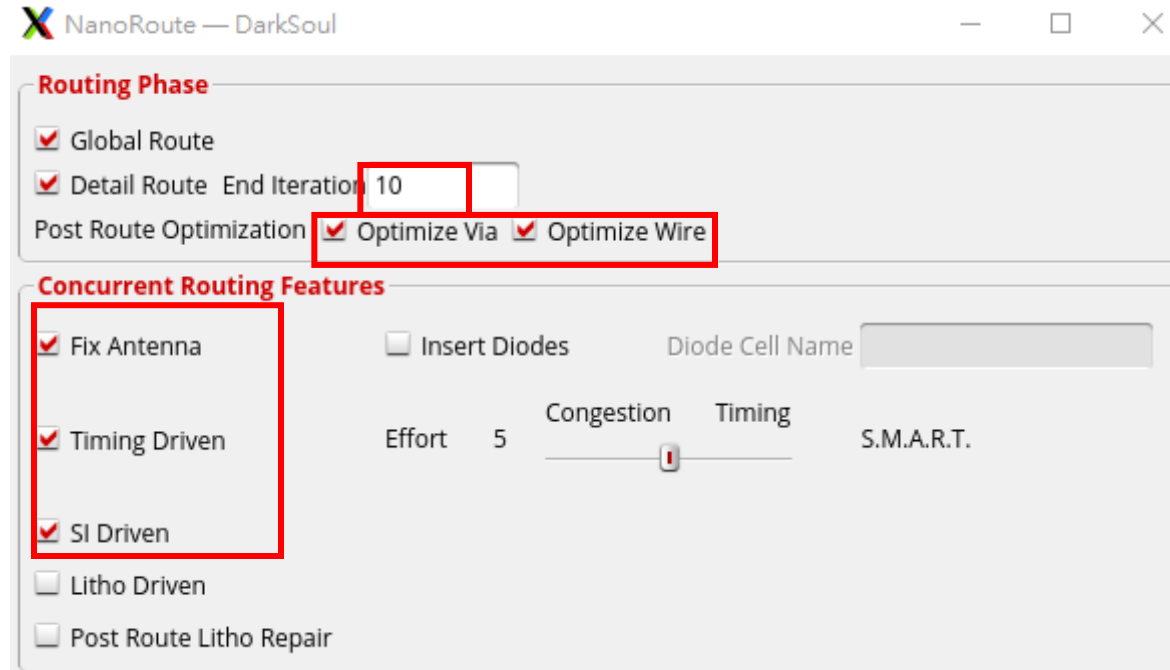


Tie-high Cell

# Route(1/5)

## ► 1. Start routing:

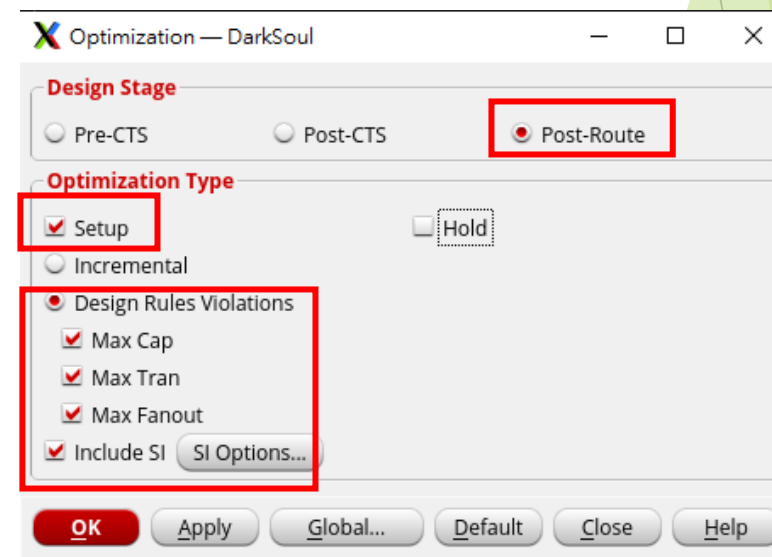
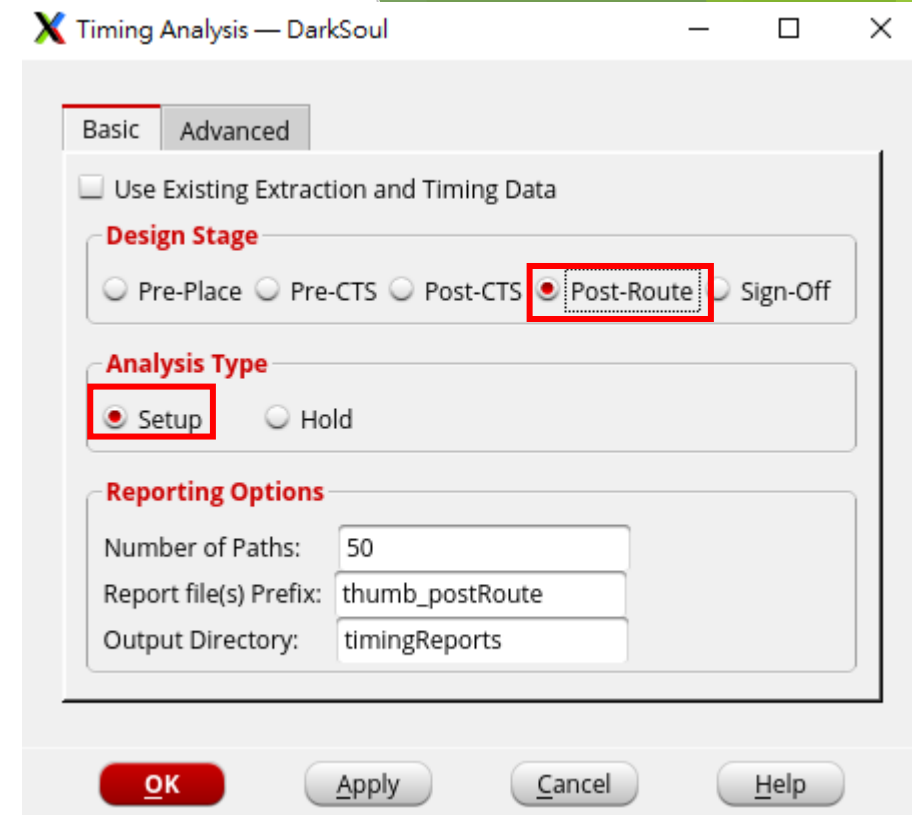
- Route → NanoRoute → Route
- Detail Route End Iteration :10
- In Routing Phase, select Optimize Via & Optimize Wire
- In Concurrent Routing Features, select Fix Antenna, Timing Driven, SI Driven
- Click OK



# Route(2/5)

- ▶ 2. **innovus** > set\_db delaycal\_enable\_si true
- ▶ 3. Timing → Report Timing
  - Design Stage : Choose Post-Route
  - Analysis Type : Choose Setup
- ▶ 4. ECO → Optimize Design
  - Design Stage : Choose Post-Route
  - Optimization Type : Choose Setup
  - Click OK

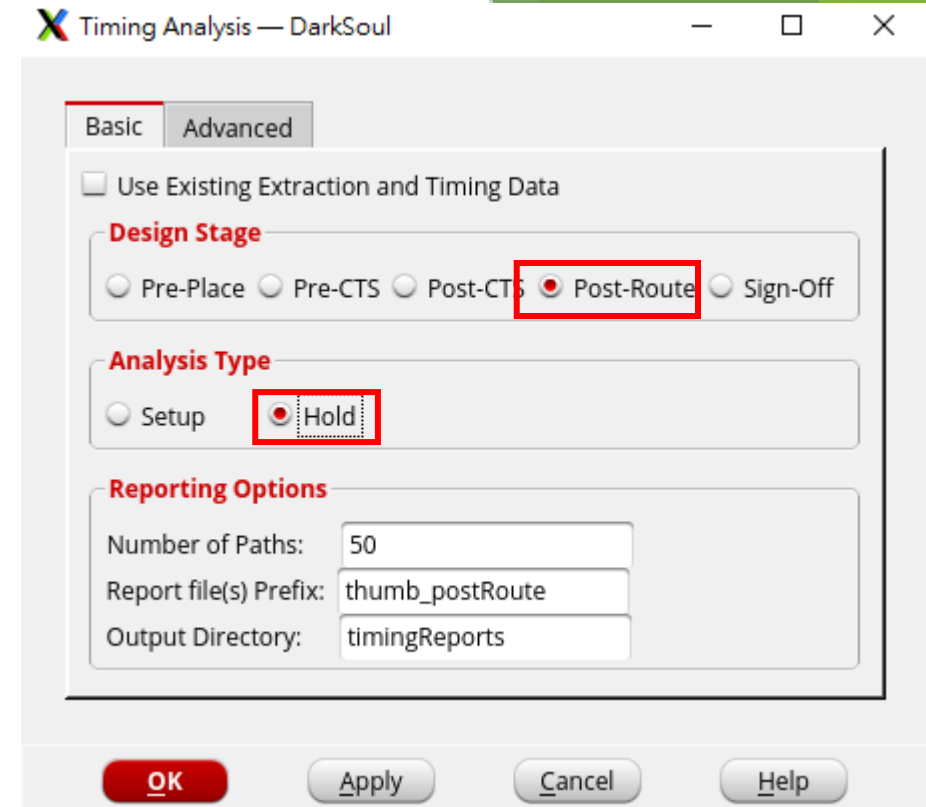
Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.398	0.746	0.398	2.303	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0



# Route(3/5)

- 5. Timing → Report Timing
  - Design Stage : Choose Post-Route
  - Analysis Type : Choose Hold
- 6. ECO → Optimize Design
  - Design Stage : Choose Post-Route
  - Optimization Type : Choose Hold
  - Click OK

Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.004	0.004	0.034	0.086	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0



Timing Analysis — DarkSoul

Basic Advanced

☐ Use Existing Extraction and Timing Data

**Design Stage**

☐ Pre-Place ☐ Pre-CTS ☐ Post-CTS ☒ Post-Route ☐ Sign-Off

**Analysis Type**

☐ Setup ☒ Hold

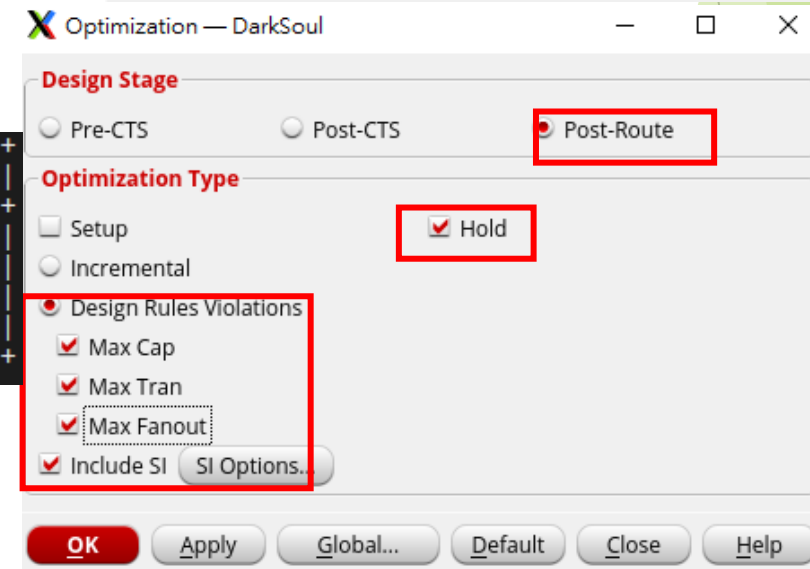
**Reporting Options**

Number of Paths: 50

Report file(s) Prefix: thumb\_postRoute

Output Directory: timingReports

OK Apply Cancel Help



Optimization — DarkSoul

**Design Stage**

☐ Pre-CTS ☐ Post-CTS ☒ Post-Route

**Optimization Type**

☐ Setup ☒ Hold

☒ Design Rules Violations

☒ Max Cap

☒ Max Tran

☒ Max Fanout

☒ Include SI SI Options...

OK Apply Global... Default Close Help

# Route(4/5)

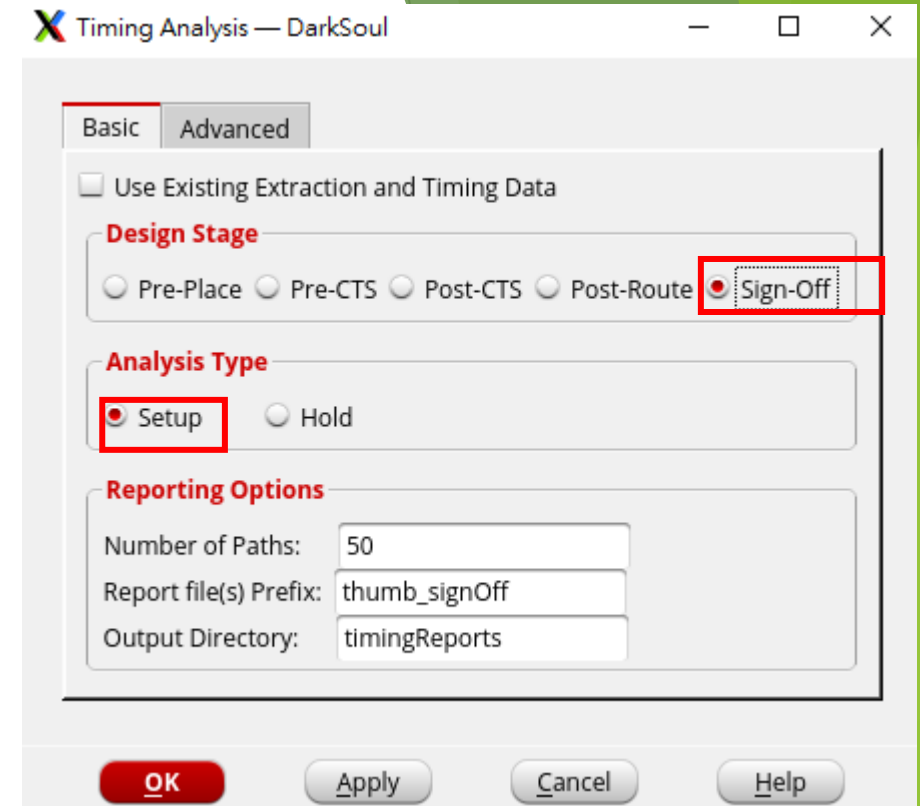
## ► 7. Timing → Report Timing

-Design Stage : Choose Sign-Off

-Analysis Type : Choose Setup

## ► 8. **innovus** > set\_multi\_cpu\_usage -remote\_host 8

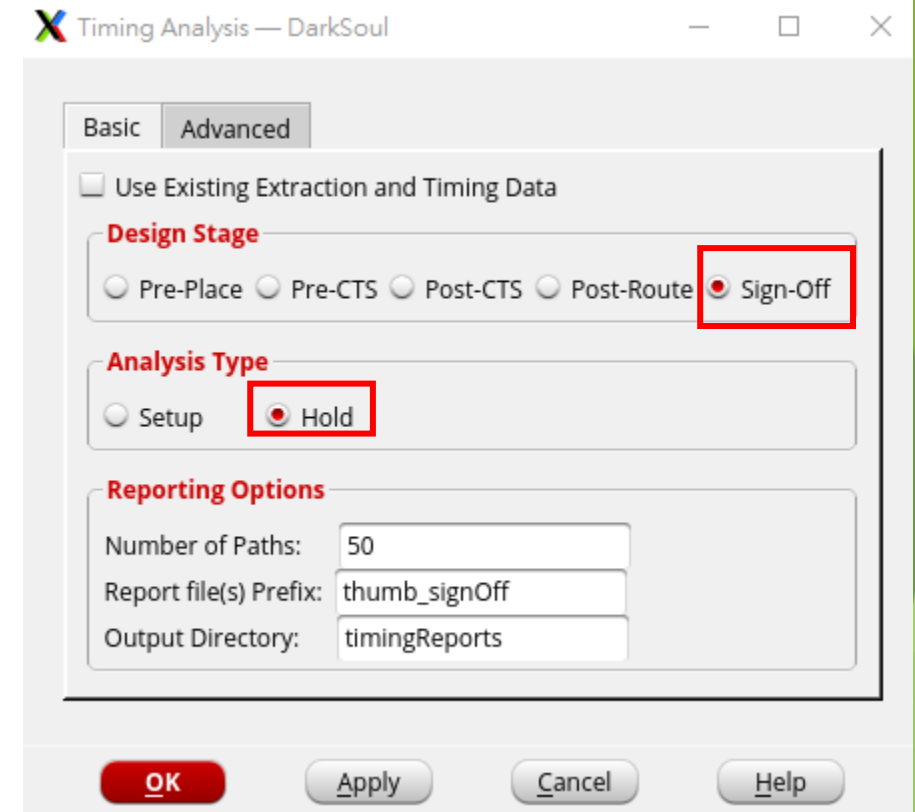
**innovus** > opt\_signoff -setup



Setup mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.730	0.730	1.319	2.302	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0

# Route(5/5)

- ▶ 9. Timing → Report Timing
  - Design Stage : Choose Sign-Off
  - Analysis Type : Choose Hold
- ▶ 10. **innovus** > set\_multi\_cpu\_usage -remote\_host 8  
**innovus** > opt\_signoff -hold

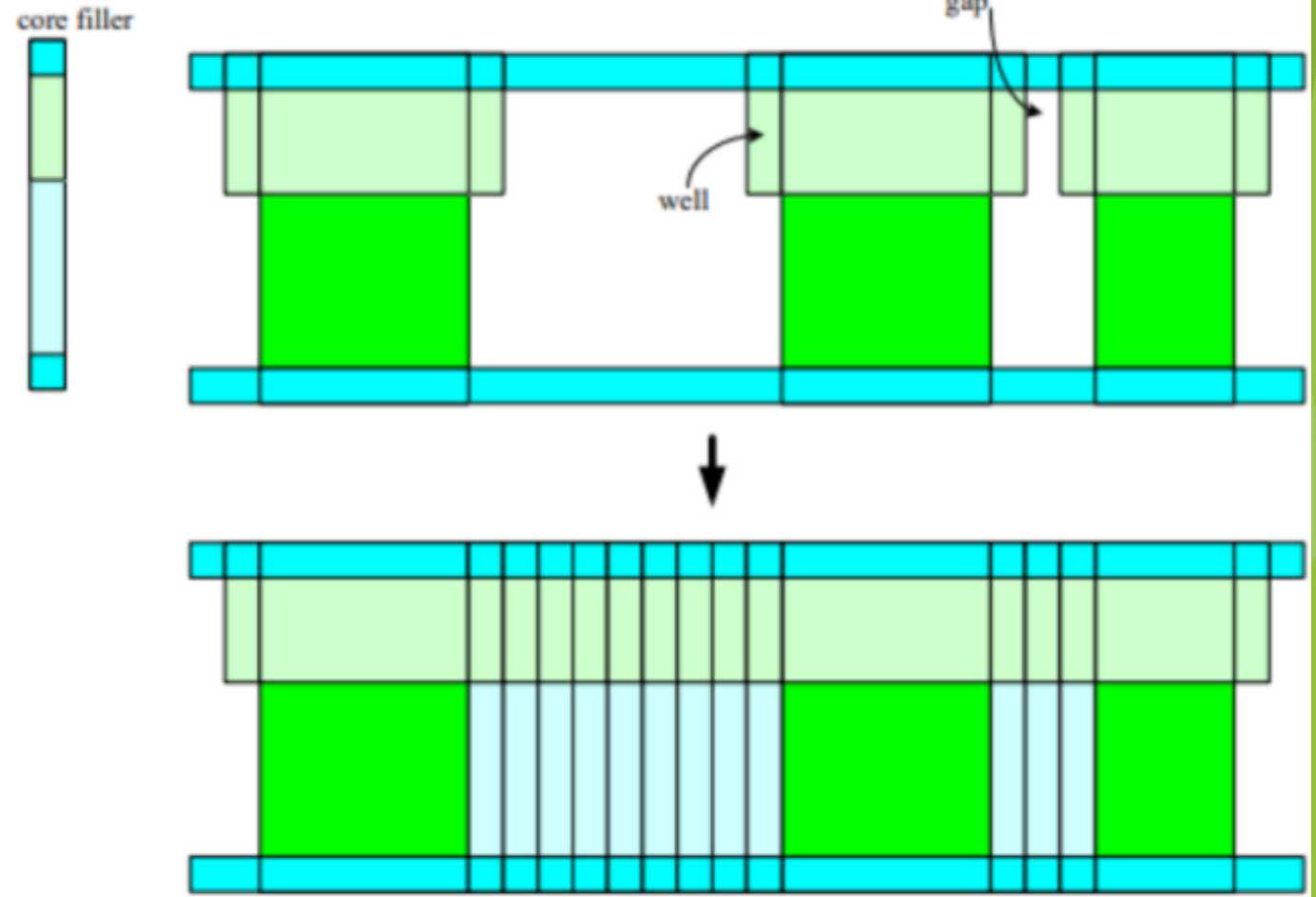


Hold mode	all	reg2reg	in2reg	reg2out	in2out	default
WNS (ns):	0.008	0.008	0.018	0.090	N/A	0.000
TNS (ns):	0.000	0.000	0.000	0.000	N/A	0.000
Violating Paths:	0	0	0	0	N/A	0
All Paths:	1351	735	1007	66	N/A	0

# Post processing(1/5)

## ► 1. Add Core Filler

- To fill the gap between cells.
- Start from wider filler to narrow filler



# Post processing(2/5)

## ► 2. Add Core Filler:

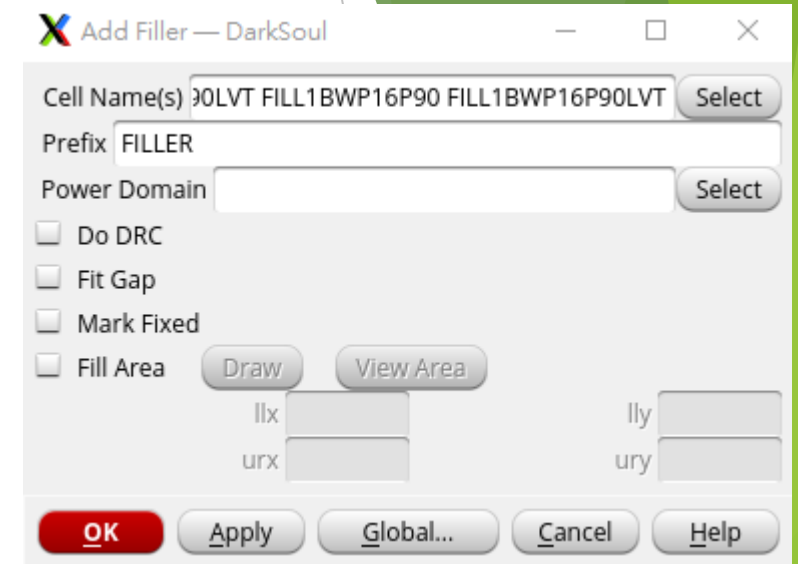
- **innovus** > get\_db add\_fillers\_cells
- Place → Physical Cells → Add Filler → Click OK

## ► 3. Add VIA1 between M1 and M2

- **innovus** > source ADFP\_APR\_script/post\_via\_drop.tcl

## ► 4. Check DRC

- **innovus** > set\_db check\_drc\_limit 10000
- **innovus** > check\_drc
- **innovus** > source ADFP\_APR\_script/fix\_manual\_via12.tcl

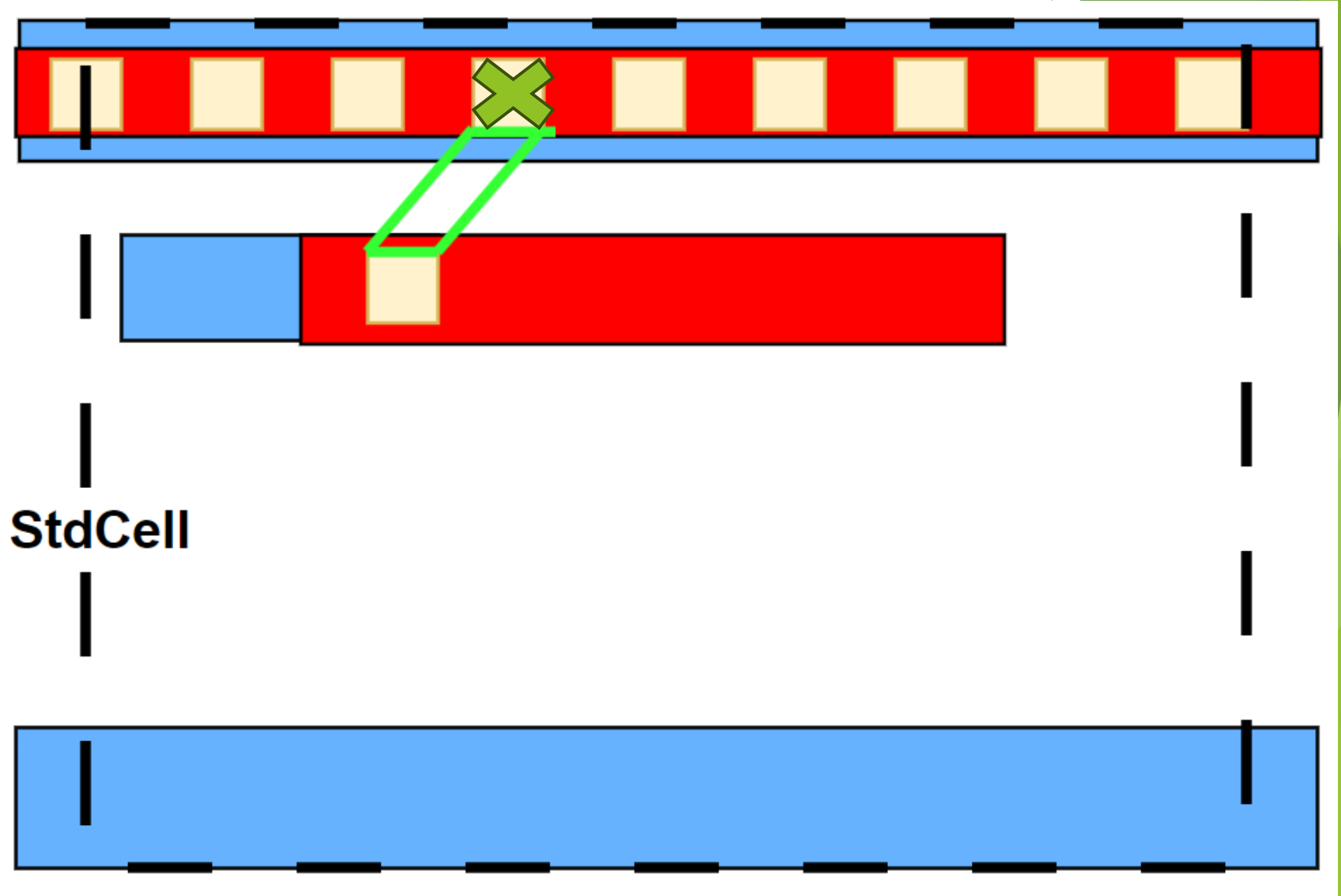


```
VERIFY DRC ..... Thread : 2 finished.  
VERIFY DRC ..... Sub-Area: {0.000 187.488 27.280 214.272} 64 of 81 Thread : 6  
VERIFY DRC ..... Thread : 6 finished.  
VERIFY DRC ..... Sub-Area: {54.560 187.488 81.840 214.272} 66 of 81 Thread : 7  
VERIFY DRC ..... Thread : 7 finished.  
VERIFY DRC ..... Sub-Area: {218.240 187.488 241.380 214.272} 72 of 81 Thread : 0  
VERIFY DRC ..... Thread : 0 finished.  
VERIFY DRC ..... Sub-Area: {163.680 187.488 190.960 214.272} 70 of 81 Thread : 4  
VERIFY DRC ..... Thread : 4 finished.  
  
Verification Complete : 3 Viols
```



# Post processing(3/5)

fix\_manual\_via12.tcl



# Post processing(4/5)

- ▶ 5. Check → CheckDRC... → OK
- ▶ 6. Check → Check Connectivity
  - Net Type → Choose Regular Only
  - Net → All
  - Check → un-choose DanglingWire(Antenna)
- ▶ 7. Finish Design
  - **innovus** > source ADFP\_APR\_script/write\_netlist.tcl
  - **innovus** > source ADFP\_APR\_script/write\_sdf.tcl
  - **innovus** > source /ADFP\_APR\_script/write\_stream.tcl

```
VERIFY DRC ..... Thread : 4 finished.  
VERIFY DRC ..... Thread : 6 finished.  
VERIFY DRC ..... Sub-Area: {190.960 187.488 218.240 214.272} 71 of 81 Thread : 3  
VERIFY DRC ..... Thread : 3 finished.  
  
Verification Complete : 0 Viols  
  
*** End Verify DRC (CPU: 0:01:18 ELAPSED TIME: 14.00 MEM: 8.0M) ***
```

**Verify Connectivity** — DarkSoul

**Net Type**

- ☐ All
- ☒ Regular Only
- ☐ Special Only

**Nets**

- ☐ All
- ☐ Selected
- ☒ Named: VDD VSS

**Check**

- ☒ Open
- ☒ UnConnected Pin
- ☒ Unrouted Net
- ☐ Connectivity Loop
- ☐ DanglingWire (Antenna)
- ☒ Weakly Connected Pin
- ☐ Geometry Loop
- ☐ Geometry Connectivity
- ☐ Keep Previous Results
- ☐ Divide Power Net
- ☒ Soft PG Connect
- ☐ Raw Violations Mark
- ☐ Use new open Vio
- ☐ Remove old open Vio
- ☐ Use Virtual Connection
- ☐ TSV Die Abstract File

Verify Connectivity Report: FMA\_pipe.conn.rpt

**Report Limits**

Error: 1000  
Warning: 50

Set Multiple CPU...

OK Apply Cancel Help

# Post processing(5/5)

## write\_netlist.tcl

```
Delete_empty_hinsts

write_netlist outputs/FMA_pipe_pr.v
set TAP_CELL_LIST [get_db [get_db base_cells TAP_*] .name]
set BOUNDARY_CELL_LIST [get_db [get_db base_cells BOUNDARY_*] .name]
set DECAP_CELL_LIST [get_db [get_db base_cells DCAP_*] .name]
set PVDD_CELL_LIST [get_db [get_db base_cells PVDD_*] .name]
set FILLER_CELL_LIST [get_db [get_db base_cells FILL_*] .name]
set PFILLER_CELL_LIST [get_db [get_db base_cells PFILL_*] .name]
set PCORNER_CELL_LIST [get_db [get_db base_cells PCORNER_*] .name]
write_netlist -include_pg_ports -include_phys_cells "$TAP_CELL_LIST $BOUNDARY_CELL_LIST $DECAP_CELL_LIST $PVDD_CELL_LIST $FILLER_CELL_LIST $PFILLER_CELL_LIST $PCORNER_CELL_LIST" outputs/FMA_pipe_pg.v
```

## write\_sdf.tcl

```
write_sdf outputs/FMA_pipe_ff0p88v125c.sdf -max_view AV_func_ff0p88v125c
write_sdf outputs/FMA_pipe_ss0p72vm40c.sdf -max_view AV_func_ss0p72vm40c
```

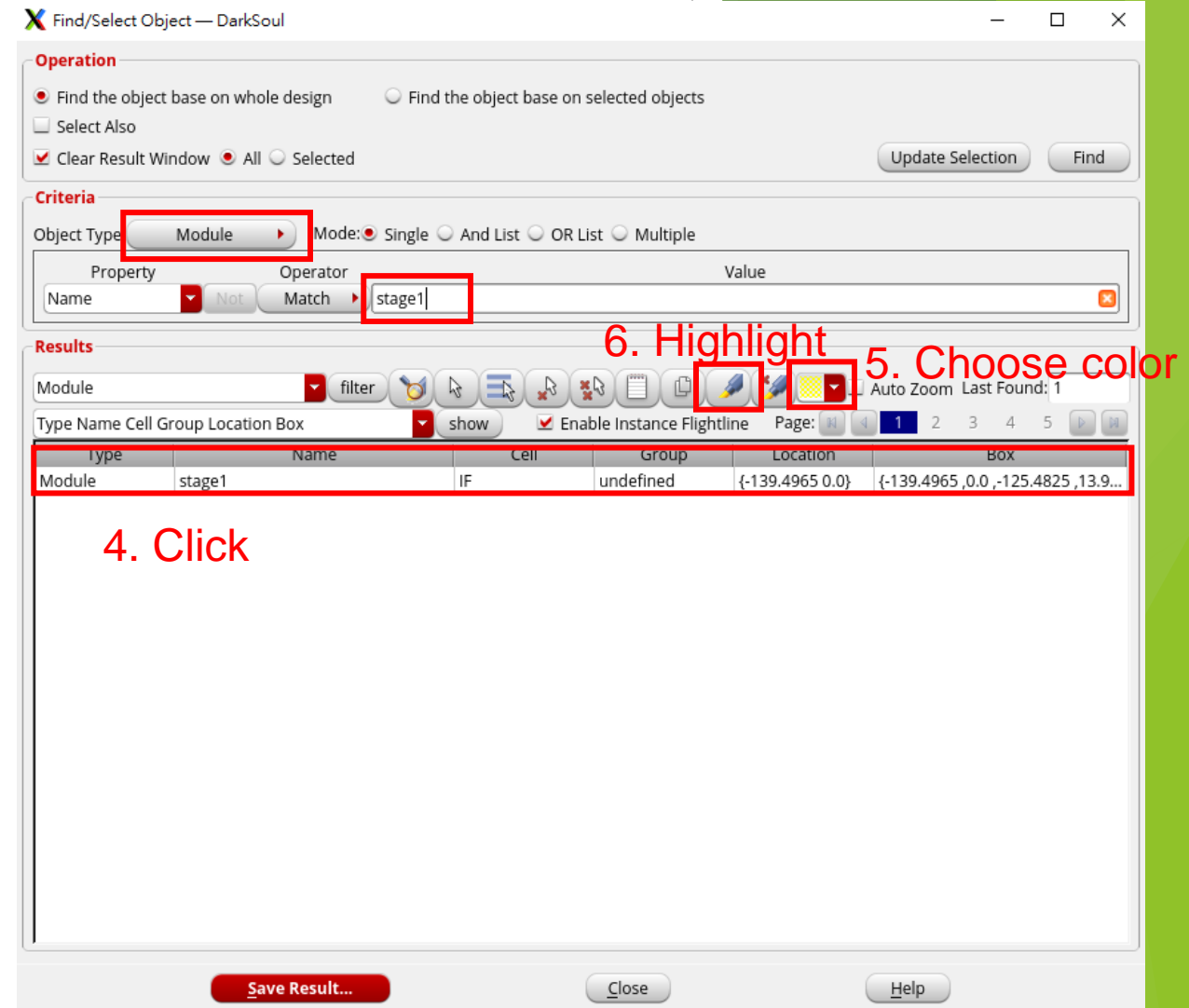
## write\_stream.tcl

```
write_stream outputs/FMA_pipe.gds -map_file stream_out_map -lib_name DesignLib \
    -merge { \
        /home/cad/CBDK/ADFP/Executable_Package/Collaterals/IP/stdcell/N16ADFP_StdCell/GDS/N16ADFP_StdCell.gds \
    } \
    -uniquify_cell_names -unit 1000 -mode all -report_file write_stream.log

#create_pin_text -cells thumb label_loc.txt
```

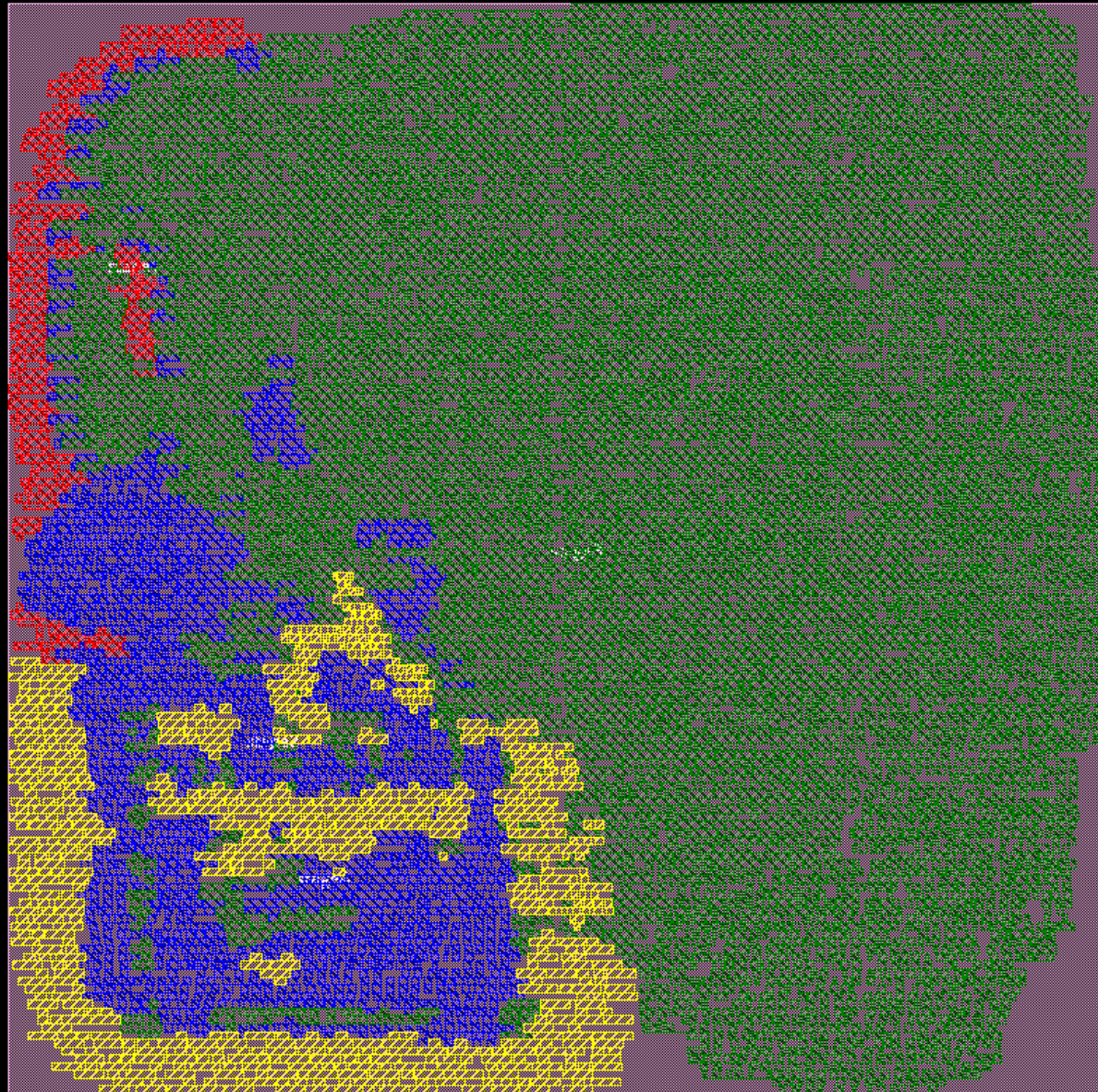
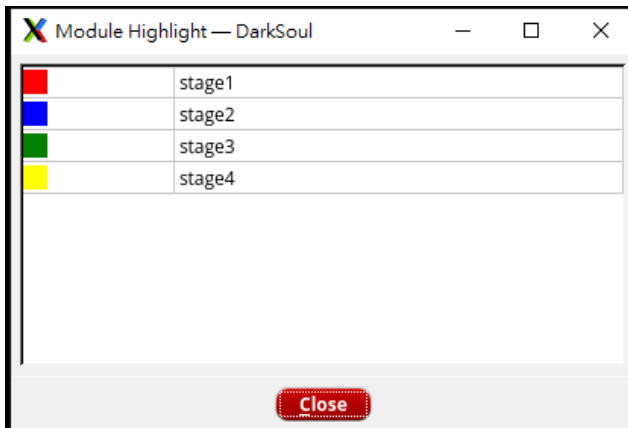
# Highlight module(1/3)

- ▶ 1. ctrl +f
- ▶ 2. Select Module
- ▶ 3. Type **stage1** → Enter



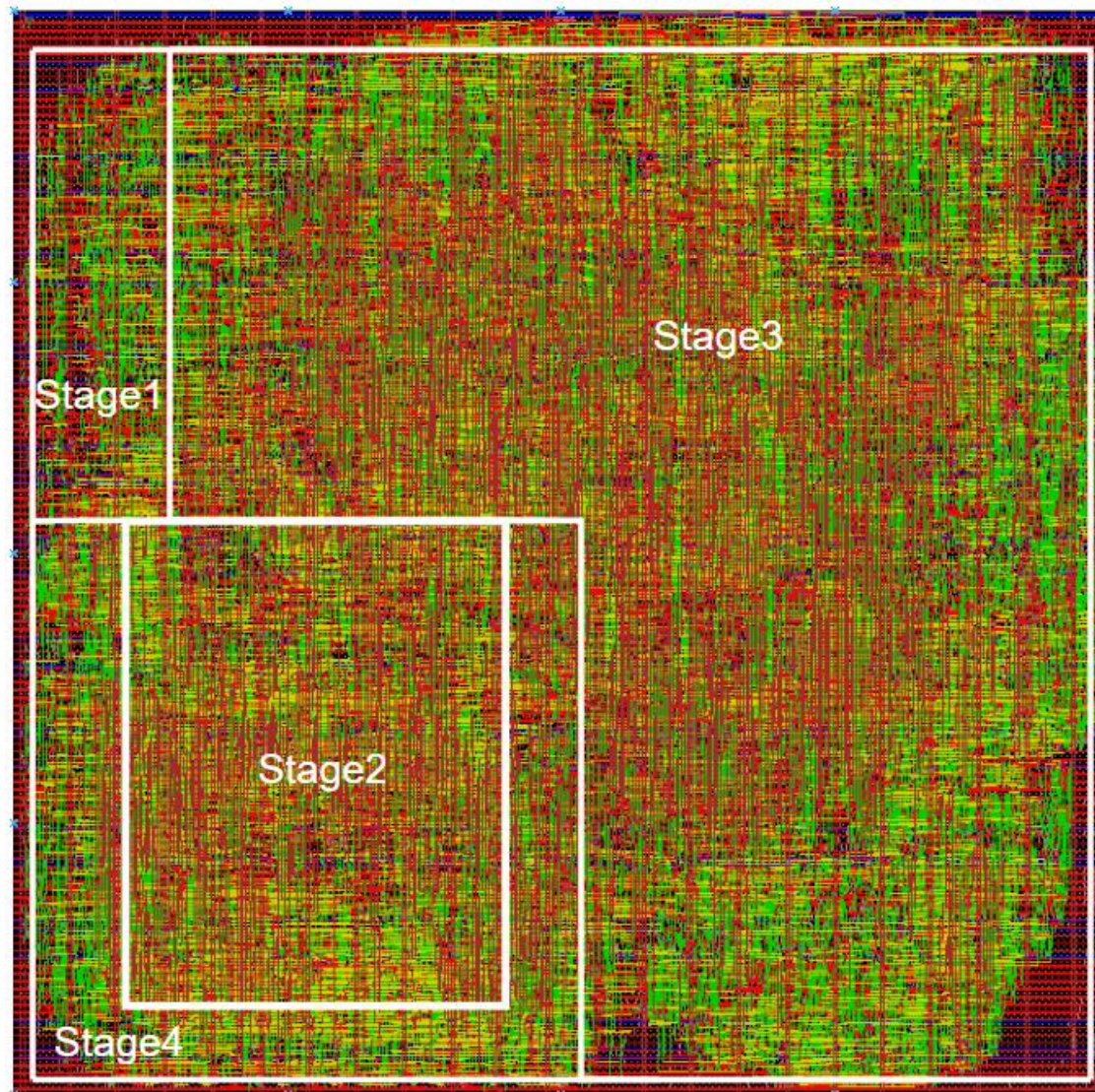


# Highlight module(2/3)





# Highlight module(3/3)



The background features abstract, overlapping green geometric shapes, primarily triangles and polygons, in various shades of green, creating a modern, layered effect on the right side of the slide.

# Thank you