FPGA ARCHITECTURE SCHEMATIC

English – v1.0

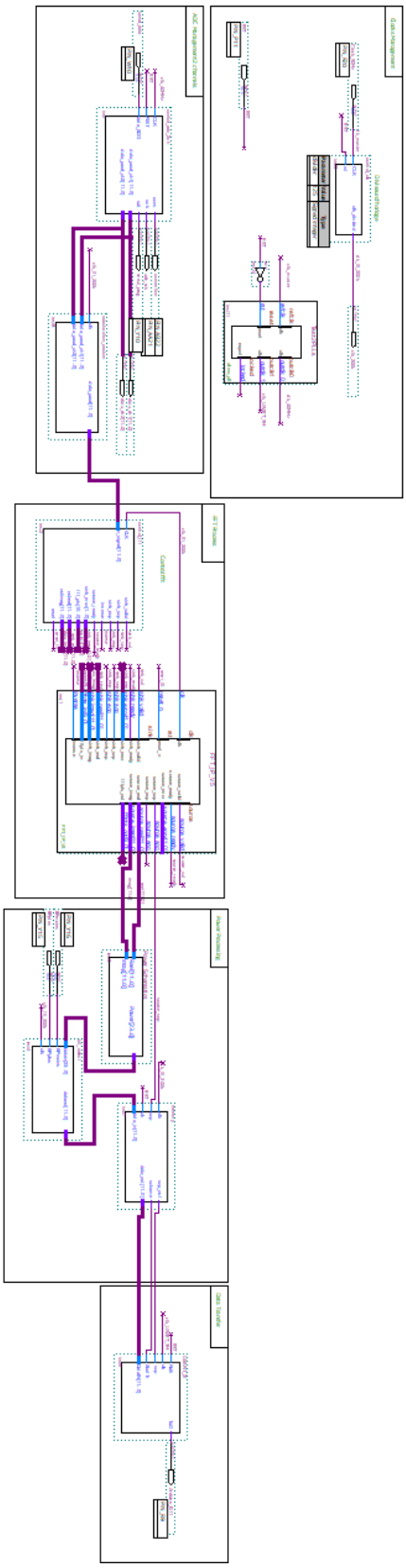
Abstract

This document presents an overview of the FPGA design implemented in Intel Quartus. Since the complete project files cannot be shared due to proprietary IP content, only a visual capture of the Quartus design is provided. The image illustrates the top-level architecture and interconnections between the main logic blocks used in the OCTAVie system, including acquisition, FFT processing, and communication modules. This overview aims to give readers a clear understanding of the FPGA design structure while respecting intellectual property constraints.

L. Durieux

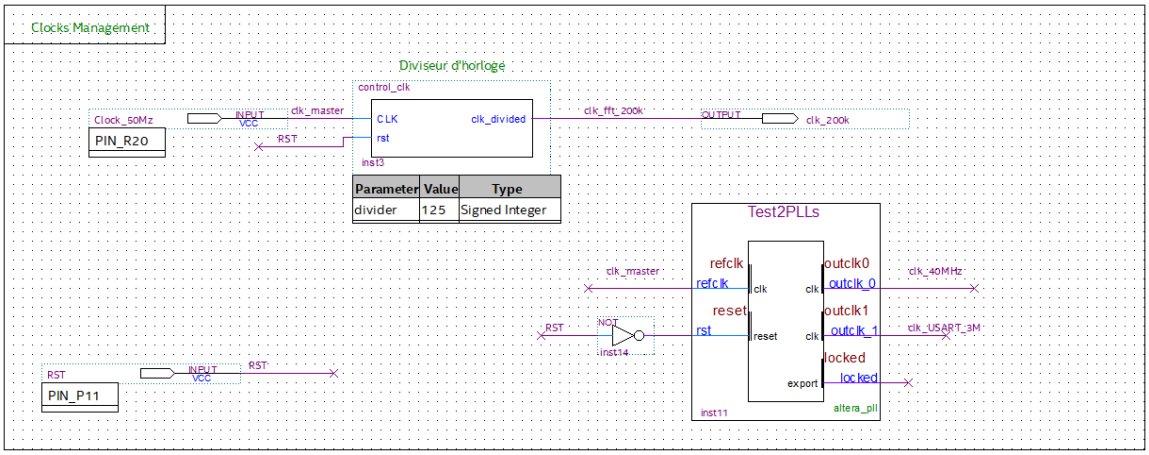
Table of Contents

Section 1 — FPGA Quartus schematic full view

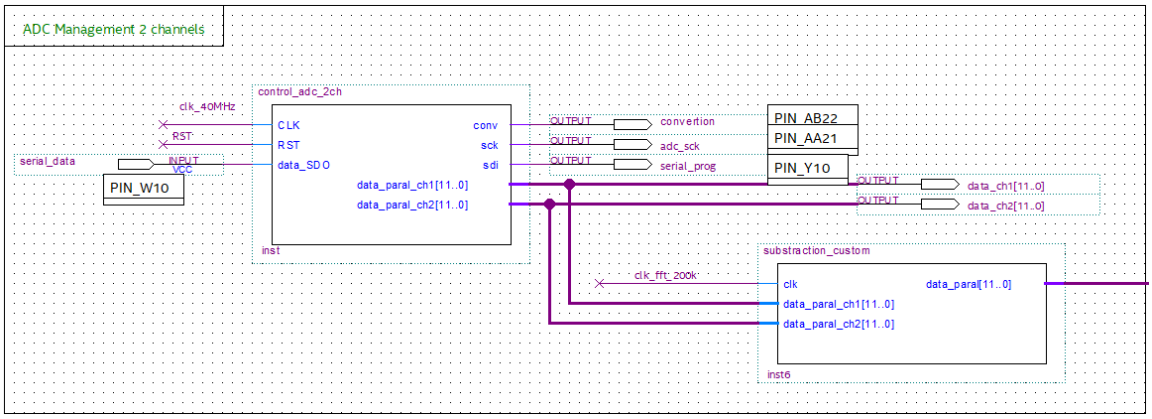


Section 2 – Details on the subblocks

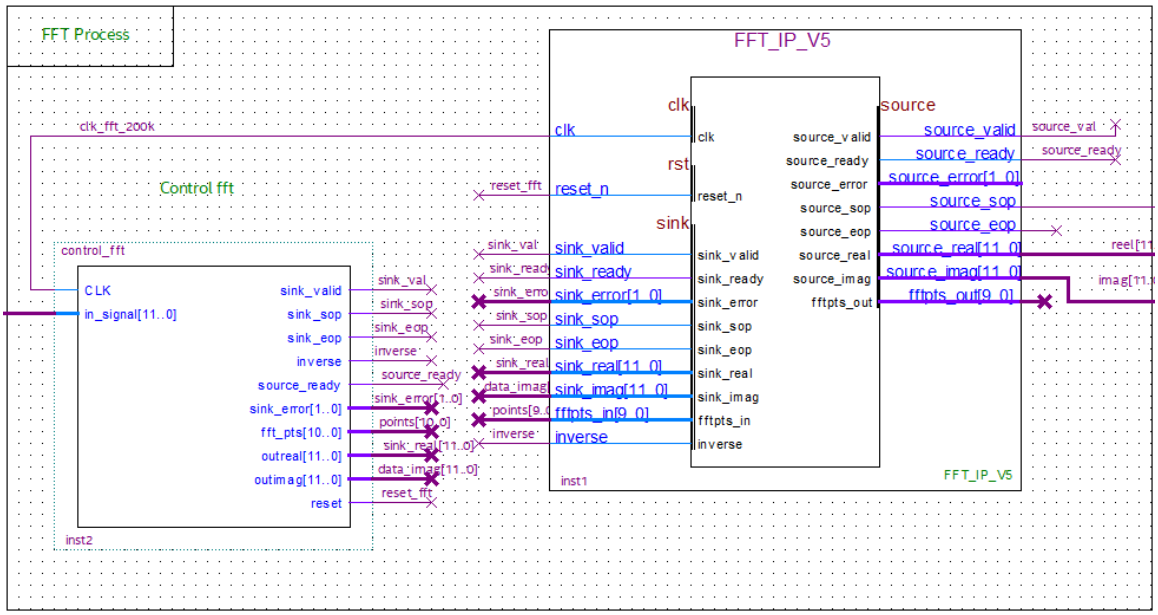
Clocks management



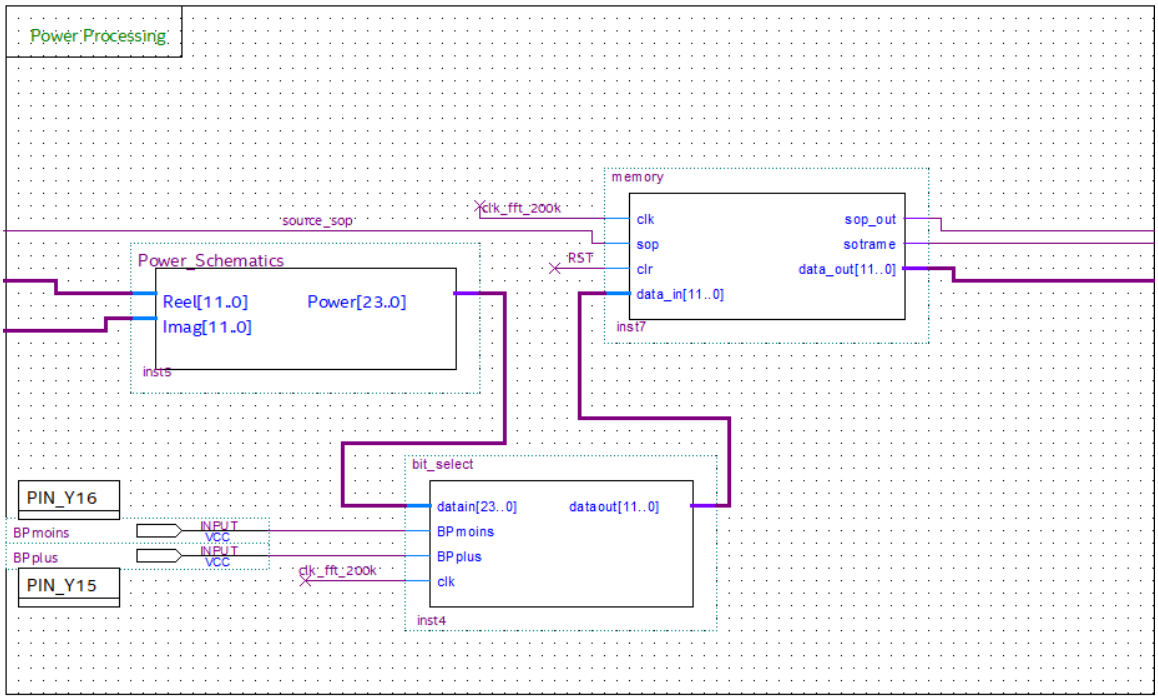
ADC management 2channels



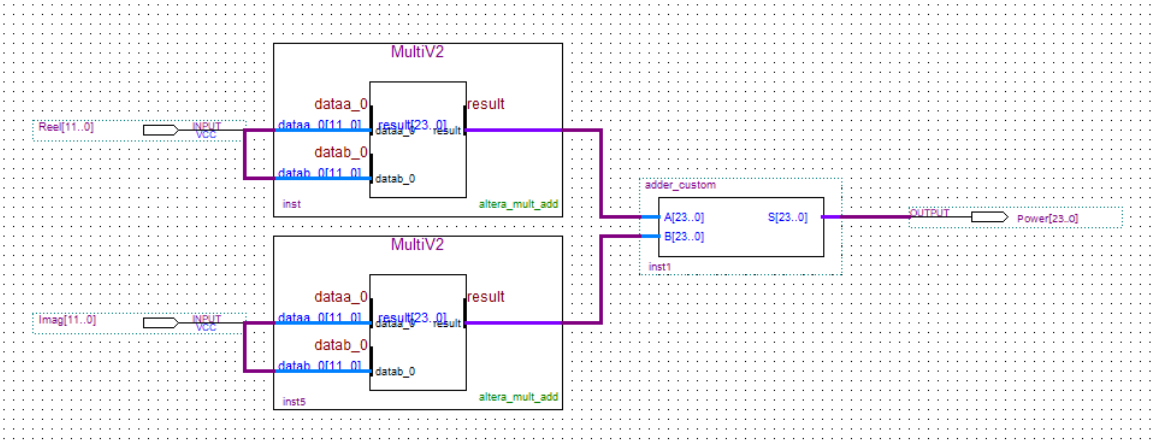
FFT Process



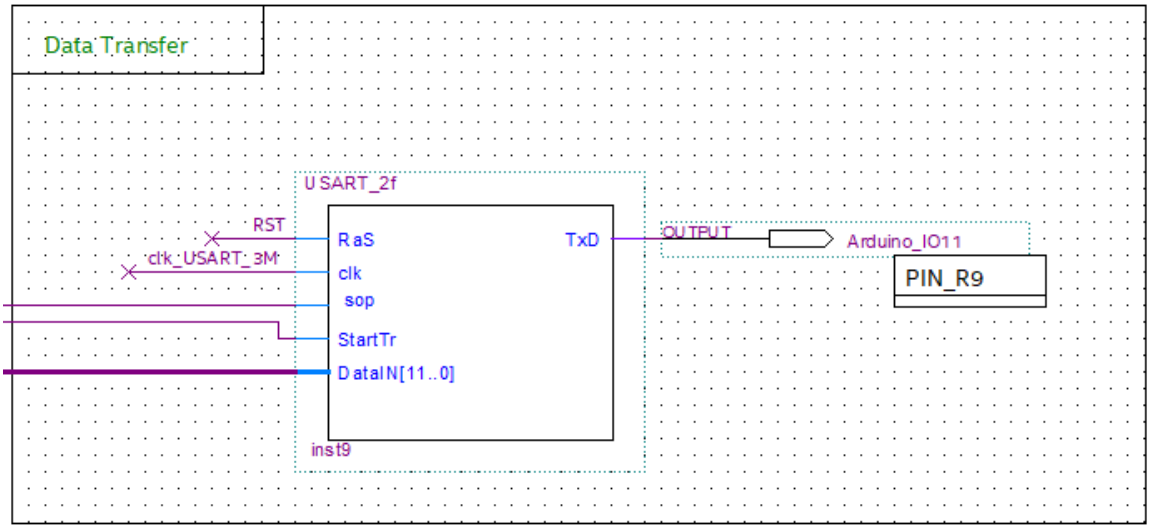
Power processing



Inside Power Schematics:



Data Transfer



Section 3 – list of the available modules

- **adder_custom.vhd**

Performs a simple 24-bit unsigned addition between two input vectors. Used for internal arithmetic operations such as sample accumulation or amplitude scaling.

- **bit_select.vhd**

Implements a dynamic bit-window selector controlled by two push buttons. Allows the user to manually choose a 12-bit slice within a 24-bit signal, useful for debugging or signal inspection.

- **control_adc_2ch.vhd**

Controls a two-channel ADC via a bit-banged SPI protocol. Manages conversion timing, serial data readout, and channel configuration for alternating acquisition between channel 1 and channel 2.

- **control_clk.vhd**

A simple clock divider generating a lower-frequency clock from the main 50 MHz input. Used to derive timing signals for slower subsystems such as the ADC interface or FFT logic.

- **control_fft.vhd**

Generates the control interface for an FFT IP core (start, end, valid, and reset).
Feeds the FFT block with real input samples, handles SOP/EOP markers, and produces a short reset pulse during startup.

- **memory.vhd**

Implements a 256×12-bit synchronous RAM buffer with simultaneous write and read operations. Used to temporarily store and replay sample data, synchronized with a "start of packet" (SOP) trigger.

- **substraction_custom.vhd**

Performs a signed subtraction between two 12-bit input channels. Used to compute differential signals (e.g., between ADC channels) before FFT processing.

- **USART_2f.vhd**

Custom two-frame UART transmitter that serializes 12-bit data over two consecutive UART-like frames. Each frame includes start, data, and stop bits, plus embedded SOP flag bits for synchronization.

What is not included are the blocks IP of INTEL Namely:

- MultiV2
- FFT_IP_V5
- Test2PLLs

To be able to redo the full schematic you need to buy these blocks. Note that, to simply program the FPGA with the current version without modifying the function, you can simply use bitstream.

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Versioning

AUTHORS	VERSION	DATE	COMMENT
L. DURIEUX	V1.0	29.10.2025	Document first release
F. STOCK		01.11.2025	Review