Shape

Description automatically generated with medium confidenceText

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Graphical user interface, text, application

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L. Durieux

Abstract

This document presents an overview of the FPGA design implemented in Intel Quartus. Since the complete project files cannot be shared due to proprietary IP content, only a visual capture of the Quartus design is provided. The image illustrates the top-level architecture and interconnections between the main logic blocks used in the OCTAVie system, including acquisition, FFT processing, and communication modules. This overview aims to give readers a clear understanding of the FPGA design structure while respecting intellectual property constraints.

FPGA architecture schematic

English – v1.0

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# Section 1 — FPGA Quartus schematic

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# Versioning

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