Shape

Description automatically generated with medium confidenceText

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Graphical user interface, text, application

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L. Durieux

Abstract

This document details the FPGA pinout configuration used in the OCTAVie system. It provides a clear mapping between the logical FPGA signals and their corresponding physical pins, as defined in the Quartus project. The pinout includes connections for external interfaces such as ADC inputs, SPI, UART, GPIO, and clock sources, ensuring proper communication between the FPGA and the peripheral boards. This reference is essential for hardware integration, debugging, and firmware development, allowing consistent alignment between schematic design, PCB layout, and HDL implementation.

FPGA Pinout

English – v1.0

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# Section 1 — FPGA Pinout

To completed

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# Versioning

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| Authors | Version | Date | Comment |
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