1. Clk
2. Input: clk, written, 32_pins(rd_addr[]), 32_pins(data_in[]), 32_pins(wr_addr[]) | Output: 32_pins(data_out[]), FIFO_MEM_BLK
3. No undriven nets
4. No multiply instantiated designs
5. No need to uniquify any design as there is no multiply-instantiated design/hierarchy
6. no unconstrained endpoints
7. WNS: -0.6 TNS: -116.9
8. No DRCs violated
9. 11 levels of logic
10. 5 hierarchical cell count
11. The critical path typically traverses all levels of the project hierarchy
12. Approx. 13%
13. WNS: 0.53 TNS: 100.4 (Both WNS and TNS reduced when a max delay timing derate range of 5%-15% is set)
14. No DRCs violated
15. The WNS is different because when we use timing derate, we set bounds, this allows for a reduction in the negative slack
16. 1.6 clock speed because we previously achieved 0.53 WNS. This will result in WNS: 0 and TNS: 0, with no DRCs violated