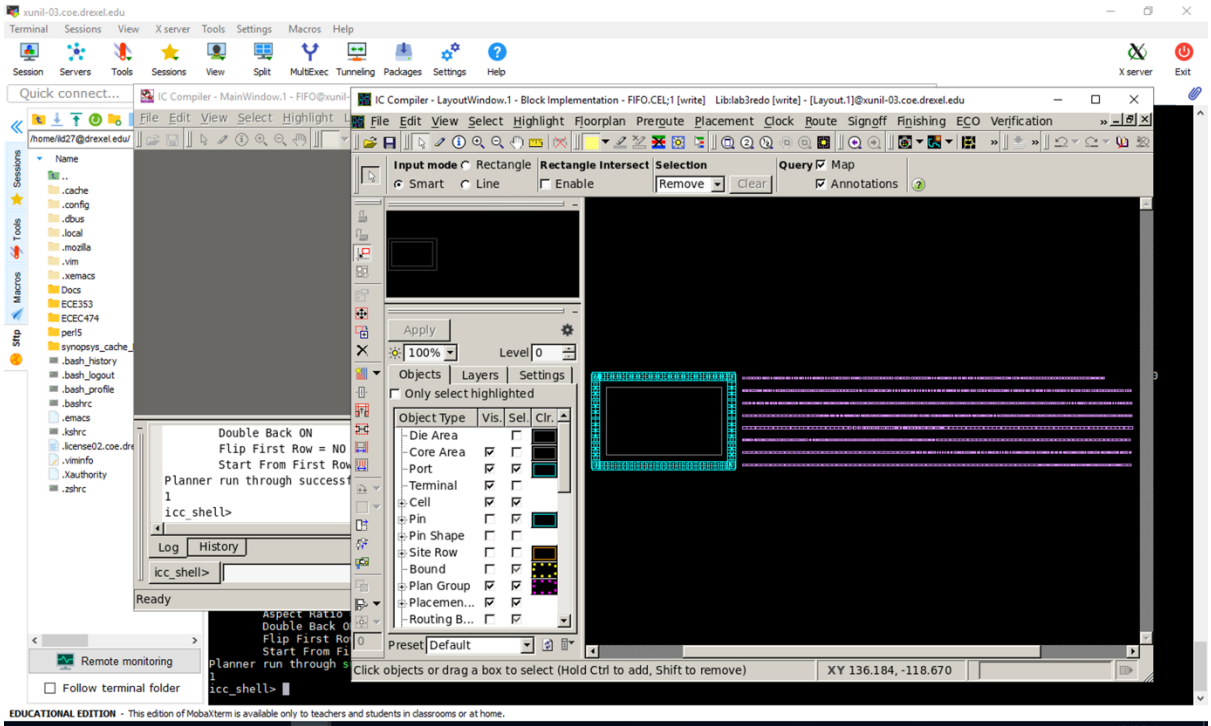
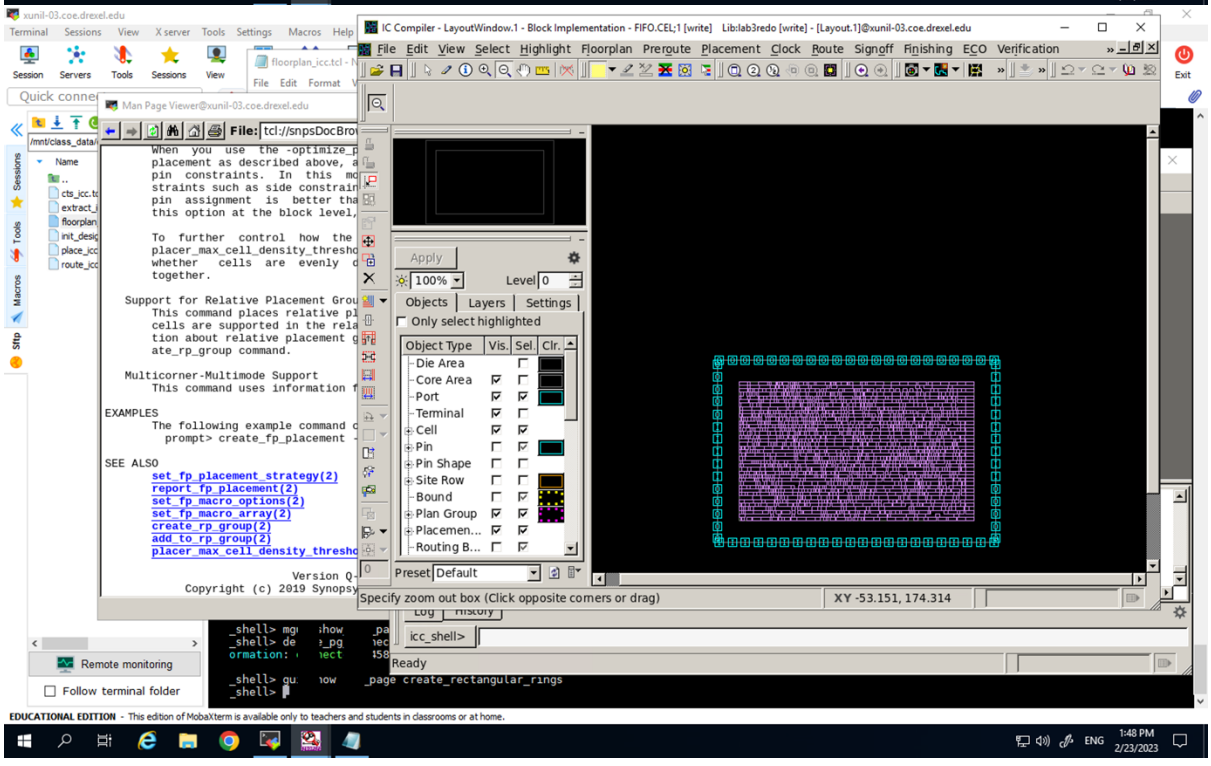
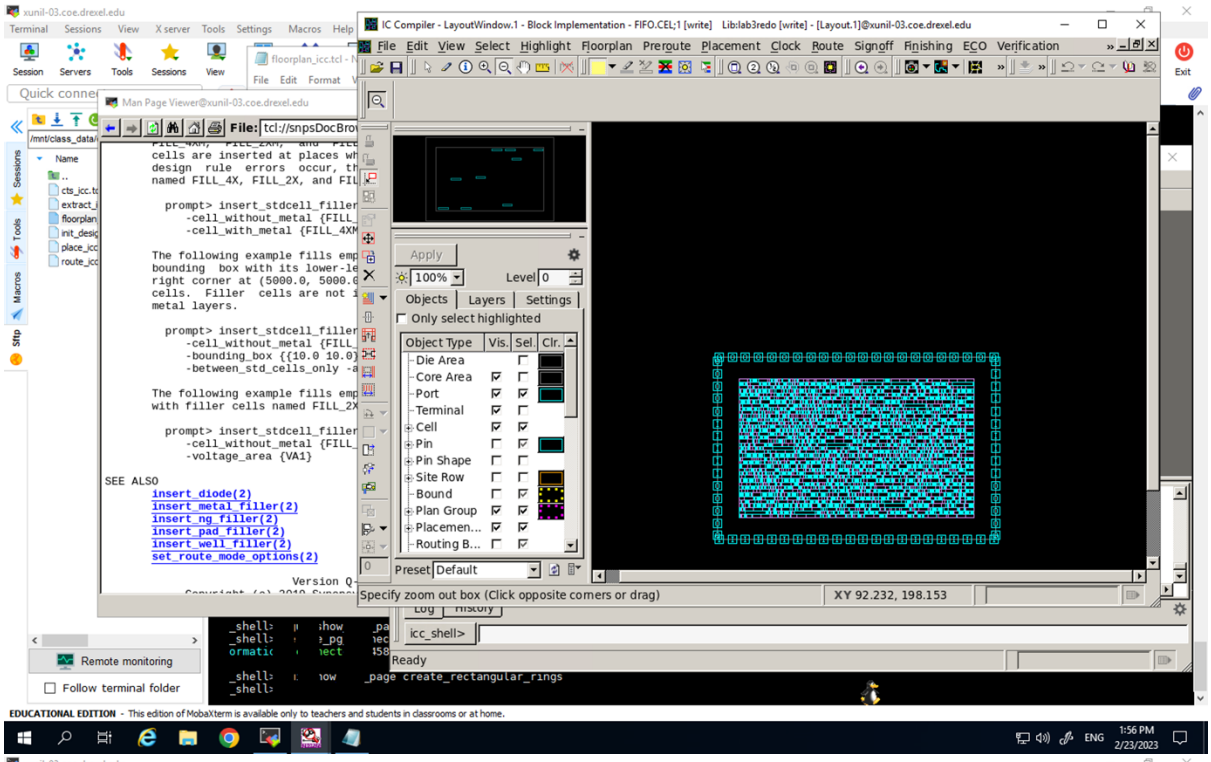
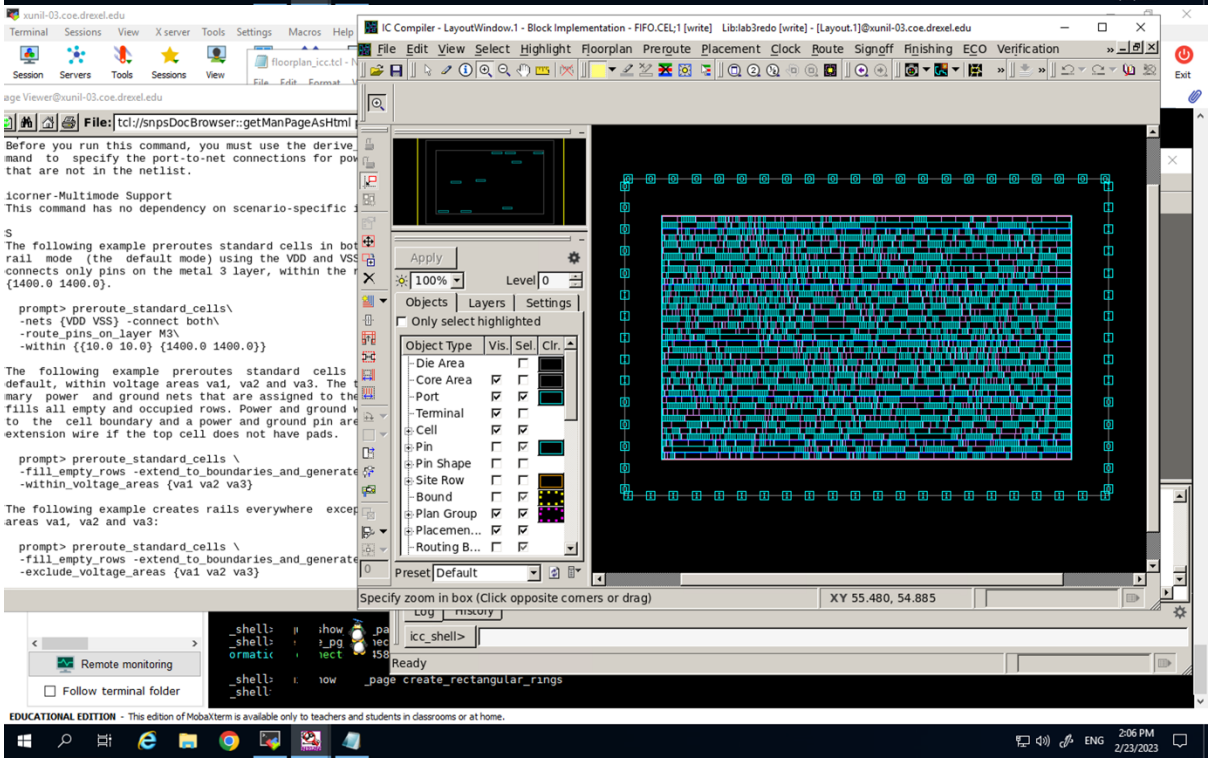
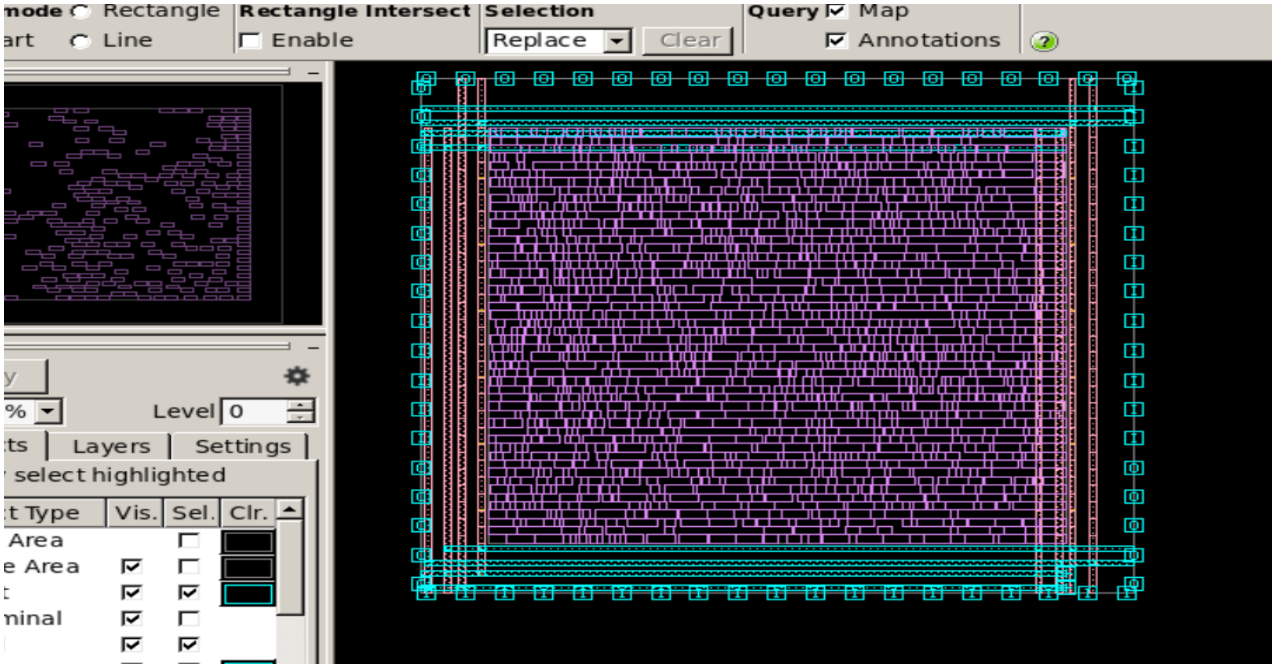

IC Compiler - LayoutWindow.1 - Block Implementation - FIFO.CEL;1 [write] Lib:lab3redo [write] - [Layout.1]@xunil-03.coe.drexel.edu
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
XY 136.184, -118.670
Ready
12:43 PM
2/23/2023


IC Compiler - LayoutWindow.1 - Block Implementation - FIFO.CEL;1 [write] Lib:lab3redo [write] - [Layout.1]@xunil-03.coe.drexel.edu
Specify zoom out box (Click opposite corners or drag)
XY -53.151, 174.314
Ready
1:48 PM
2/23/2023


IC Compiler - LayoutWindow.1 - Block Implementation - FIFO.CEL;1 [write] Lib:lab3redo [write] - [Layout.1]@xunil-03.coe.drexel.edu
Specify zoom out box (Click opposite corners or drag)
XY 92.232, 198.153
icc_shell>
Ready
Remote monitoring
Follow terminal folder
EDUCATIONAL EDITION - This edition of MobaXterm is available only to teachers and students in classrooms or at home.


IC Compiler - LayoutWindow.1 - Block Implementation - FIFO.CEL;1 [write] Lib:lab3redo [write] - [Layout.1]@xunil-03.coe.drexel.edu
Specify zoom in box (Click opposite corners or drag)
XY 55.480, 54.885
icc_shell>
Ready
Remote monitoring
Follow terminal folder
EDUCATIONAL EDITION - This edition of MobaXterm is available only to teachers and students in classrooms or at home.




```
Total wirelength: 20849.65
Number of 100x100 tracks cell density regions: 25
Number of low (< 10%) cell density regions: 0 (0.000%)
Number of high (> 200%) cell density regions: 0 (0.000%)
Maximum cell density: 64.37% (at 52 51 66 65)
Checking hard macro to hard macro overlaps ...
Number of hard macro to hard macro overlaps: 0
Checking hard macro to std cell overlaps ...
Number of hard macro to std cell overlaps: 0
Checking plan group to plan group overlaps ...
Number of plan group to plan group overlaps: 0
Number of TL cells overlapping PG: 0
Number of cells violating core area: 0
Total number of cells violating plan group or core area: 0
```

Floorplan Creation:
The first set of screenshots show the floorplan of the design with a core utilization of 60% and an aspect ratio of 0.6. The IO to core margin is set to 10µm on all sides. The floorplan shows the core area where the actual design will be placed, surrounded by a margin where IOs and other external connections can be placed. The aspect ratio of 0.6 means that the height of the core is 60% of its width.

Power and Ground Connection:
The second set of screenshots shows the power and ground connections of the design. The IC Compiler command 'derive pg connection' is used to connect the VDD and VSS pins to their respective power and ground nets. This step is essential for ensuring proper power distribution to the design.

Power Ring Creation:
The third set of screenshots shows the power and ground rings that have been created for VDD and VSS. Metal layer M6 is used for the top and bottom segments of the ring, while metal layer M7 is used for the left and right segments. Power straps of width 3µm have also been added. The power and ground rings are essential for ensuring proper power distribution to the design.

Coarse Placement and Power Network Creation:
The fourth set of screenshots shows the placement of hard macros and leaf cells in the design. This is a coarse placement that is done during floor planning. The IC Compiler command 'create fp placement' is used to insert filler cells into the empty spaces of the design. The filler cells are standard cells that do not affect the functionality of the design. Next, the fifth shows the power network that has been created for the design. The IC Compiler command 'preroute standard cells' is used to connect the power and ground pins in the standard cells to the power and ground rings created earlier. This step is essential for ensuring proper power distribution to the design.

Floorplan Reports:
The final set of screenshots shows the floorplan reports for any violations. The IC Compiler command 'report fp placement' is used to generate these reports. The reports show any violations that may have occurred during the floor planning process, such as overlap between cells or placement outside of the design's boundary.

Overall, the design flow with minimalistic design constraints involves creating a floorplan, connecting power and ground pins, creating power and ground rings, performing coarse placement, creating a power network, and checking for violations. These steps are essential for ensuring proper power distribution and placement of the design's components.