Design (Period 2)	Operating condition	Wire load model	Area	Power (uW)	WNS	TNS	Cell count	No. of violating paths
s386.v	ss0p95v125c	ForQA	43.9	2.0713	12.45	149.68	6	13
s9234.v	ss0p95v125c	ForQA	806	28.5	175.32	3636.44	211	217
s15850.v	ss0p95v125c	ForQA	1568.4	40.2	477.08	126431.48	534	640
s35932.v	ss0p95v125c	ForQA	5605.87	327.62	133492.12	228019184	1728	2048
s1238.v	ss0p95v125c	ForQA	150.09	6.243	13.97	330.38	18	32
dff.v	ss0p95v125c	ForQA	0.91187	1.189e-02	0.06	0.11	0	2

Design (Period 10)	Area	Power (uW)	WNS	TNS	Cell count	No. of violating paths
s386.v	43.9	0.4143	4.45	45.68	6	13
s9234.v	806	5.7091	167.32	2629.68	211	96
s15850.v	1568.4	8.0471	469.08	122464.84	534	640
s35932.v	5605.87	65.52	133484.12	228005040	1728	1760
s1238.v	150.09	1.248	5.97	104.68	18	24
dff.v	0.91187	2.378e-03	0	0	0	0

Observations:

Comparing the two design periods, we can observe the following:

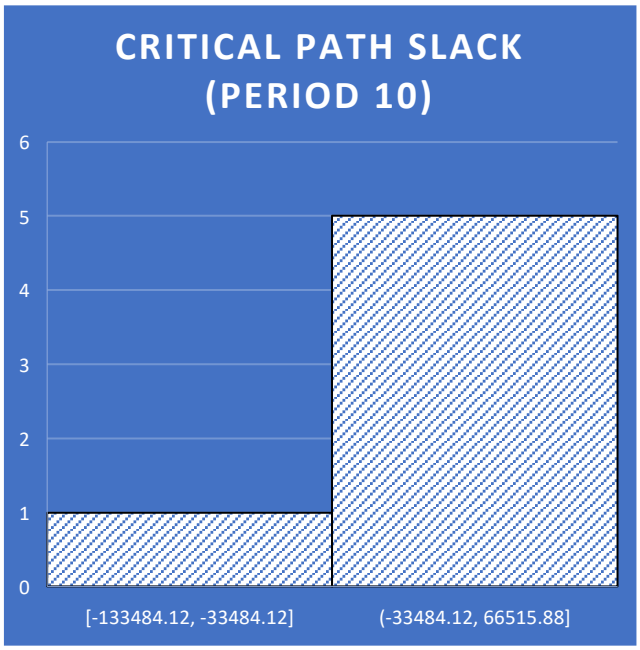
- Power: The power consumption of all the designs has reduced significantly in Period 10 compared to Period 2. The power reduction varies from 80% to 99%.
- Performance: The Worst Negative Slack (WNS) has reduced in Period 10 compared to Period 2 for all the designs except for s1238.v. The Total Negative Slack (TNS) has also reduced for all designs, except s35932.v.
- Area: The area of all designs remained constant between the two design periods.
- Violations: There are fewer violating paths in Period 10 compared to Period 2 for all designs, except for s9234.v and s35932.v.

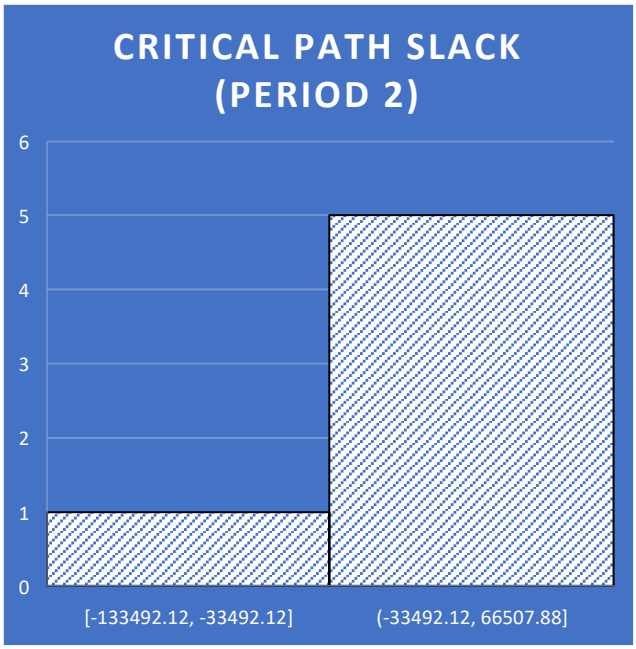
Reasons for violations:

- WNS violations occur when the timing path has a negative slack, indicating that the path does not meet the timing requirements. This can occur due to various reasons such as poor clock distribution, large combinational logic, etc.
- TNS violations occur when the total negative slack of the design is greater than the clock period, indicating that the design may not meet the timing requirements. This can occur due to the same reasons as WNS violations.
- Violations in Period 2 could have been due to larger combinational logic and poor clock distribution. In Period 10, the logic may have been optimized to reduce the number of violations.
- The violation in s9234.v in Period 10 could be due to a change in the design that may have increased the critical path delay.
- The increase in the number of violating paths in s35932.v in Period 10 could be due to a design change that may have increased the complexity of the design.

Overall, the power consumption of the designs has reduced significantly in Period 10, while the performance has improved slightly. The number of violating paths has reduced for most designs, indicating that the design has been optimized for better timing performance.

Design	Critical path slack (Period 10)	Critical path slack (Period 2)
s386.v	-4.45	-12.45
s9234.v	-167.32	-175.32
s15850.v	-469.08	-477.08
s35932.v	-133484.12	-133492.12
s1238.v	-5.97	-13.97
dff.v	7.94	-0.06





DC ASSIGNMENT SCRIPT

```
dc_shell –tcl |& tee logs/dc_shell
define_design_lib WORK -path ./work
analyze -f verilog [list src_assignment/[file name]]
elaborate [file name]
link
write -hier -f ddc -output [file name].sdc
lappend search_path ../src/
define_design_lib WORK -path "work"
## Define the library location
set link_library [ list /mnt/class_data/ecec574-w2019/PDKs/SAED32nm/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p95v125c.db /mnt/class_data/ecec574-w2019/PDKs/SAED32nm/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p95v25c.db /mnt/class_data/ecec574-w2019/PDKs/SAED32nm/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p95vn40c.db]
set target_library [ list /mnt/class_data/ecec574-w2019/PDKs/SAED32nm/lib/stdcell_rvt/db_ccs/saed32rvt_ss0p95v25c.db ]
## Create Constraints
create_clock clk -name ideal_clock11 -period 2 (for 500MHZ)   10 (for 100MHZ)
set_input_delay 2 [ remove_from_collection [all_inputs] clk ] -clock ideal_clock12
set_output_delay 2 [all_outputs ] -clock ideal_clock12
set_clock_uncertainty 0.05 [get_clocks ideal_clock12]
set_clock_latency 0.4 [get_clocks ideal_clock12]
set_clock_transition 0.1 [get_clocks ideal_clock12]
set_max_area 0
set_load 0.3 [ all_outputs ]
##output reports to terminal
report_area
report_power
report_qor
```