PRACTICE 4

Assembly and evaluation of sequential systems.

1.- Objetives:

The aim of this module is to familiarize students with sequential systems starting from simple (a bistable) to get the design and implementation of a counter.

2.- Previous concepts. (Notes of theory and Floyd chapters 8 and 9).

Bistable JK.
Frequency divider.
555 Timer.
Asynchronous and synchronous counters.

3.- Materials Required

Specification Sheets characteristics of integrated practice.
555 Timer.
Integrated 74LS76 (2 JK flip-flops each).
BCD-seven segment decoder (74LS47).
7-segment display (7750).
8 resistors 330Ω
Integrated with gates: calculate the required in the previous study.
Resistors. Calculate the necessary in the previous study.
Variable resistance. Deduct margins in the previous study.
Capacitor 100 nF.
LEDs.
Connection wires.
Insert Board.

4.- Procedure

Answer questions from the previous study (paragraph 6) and provide a copy of the same in the first lab session. Retain other copy for mounting the circuit.
This is required to attend the next session of the laboratory.

5.- PRACTICE DEVELOPEMENT

The practice is divided in two parts

5.1 First part: 555 timer and JK Bistable

Connect the timer 555 with the capacitor and the resistors required to obtain at the output a frequency of approximately 2 Hz and a duty cycle greater than 50%. This documentation use the 555 in operation ASTABLE configuration (data sheet of 555 and Floyd p. 448). Use the variable resistor to set the frequency.

Study modes of operation of the JK flip-flops summarized in features table of 74LS76 (first pages of the specification sheets).

Connect the timer 555 and two JK flip-flops in the appropriate operation mode for performing a frequency divider that produces signals of 1 Hz and 0.5 Hz from a signal of 2 Hz.
The three signals must be displayed in LEDs.

For this design, decide which of the possible configurations of 74LS76 should be used.

5.2 Second part:. Decades up counter

Taking advantage of the frequency divider design of the previous section, make an up counter decades (0-9) using the clock and the JK flip-flop needed.

Connect the output of the counter to the decoder BCD-to-seven segment display to see your account which must also be performed at a frequency of approximately 1 Hz.

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6- PREVIOUS STUDY.

Apellidos, Nombre: _____Grupo:_____

Use the datasheets.
Give a copy of these pages to the teacher in the first practice session

First Part 6.1

Calculate resistors to get a 2 Hz frequency signal at the output of 555.

Use the relationships of the application sheets (page 11). (From Floyd 448)

Draw below the 2Hz clock signal (at least 7 cycles) and the outputs Q1 and Q2 of the two JK flip-flops in a timing diagram that shows what should do the frequency divider.

CIRCUIT DESIGN. Draw the layout of devices and connections. Identify the signs previously drawn

Second Part 6.2

How do you get the counter starts at 3 and stops at 9?

CIRCUIT DESIGN. Draw the layout of devices and connections (do not forget the 555).