PIC32MM0256GPM064 FAMILY

32-Bit Flash Microcontroller with MIPS32® microAptiv™ UC Core, Low Power and USB

Operating Conditions

- 2.0V to 3.6V, -40ºC to +85ºC, DC to 25 MHz

Low-Power Modes

- Low-Power modes:
  - Idle – CPU off, peripherals run from system clock
  - Sleep – CPU and peripherals off:
    - Fast wake-up Sleep with retention
    - Low-power Sleep with retention
- 0.65 µA Sleep current for RAM Retention Regulator mode and 5 µA for Regulator Standby mode
- On-Chip 1.8V Voltage Regulator (VREG)
- On-Chip Ultra Low-Power Retention Regulator

High-Performance 32-Bit RISC CPU

- microAptiv™ UC 32-Bit Core with 5-Stage Pipeline
- microMIPS™ Instruction Set for 35% Smaller Code and 98% Performance compared to MIPS32 Instructions
- 1.53 DMIPS/MHz (37 DMIPS) (Dhrystone 2.1) Performance
- 3.17 CoreMark®/MHz (79 CoreMark) Performance
- 16-Bit/32-Bit Wide Instructions with 32-Bit Wide Data Path
- Two Sets of 32 Core Register Files (32-bit) to Reduce Interrupt Latency
- Single-Cycle 32x16 Multiply and Two-Cycle 32x32 Multiply
- 64-Bit, Zero Wait State Flash with ECC to Maximize Endurance/Retention

Microcontroller Features

- Up to 256K Flash Memory
  - 20,000 Erase/Write Cycle Endurance
  - 20 Years Minimum Data Retention
  - Self-Programmable under Software Control
- Up to 32K SRAM Memory
- Multiple Interrupt Vectors with Individually Programmable Priority
- Fail-Safe Clock Monitor mode
- Configurable Watchdog Timer with On-Chip, Low-Power RC Oscillator
- Programmable Code Protection
- Selectable Oscillator Options Including:
  - High-precision, 8 MHz (FRC) internal RC oscillator – 2x/3x/4x/6x/12x/24x PLL, which can be clocked from FRC or the Primary Oscillator
  - Primary high-speed, crystal/resonator oscillator or external clock

Peripheral Features

- USB 2.0 Compliant Full-Speed and Low-Speed Device, Host and On-The-Go (OTG) Controller:
  - Dedicated DMA
  - Device mode operation from FRC oscillator; no crystal oscillator required
- Atomic Set, Clear and Invert Operation on Select Peripheral Registers
- High-Current Sink/Source
- Independent, Low-Power 32 kHz Timer Oscillator
- Three 4-Wire SPI modules:
  - 16-byte FIFO
  - Variable width
  - I^2S mode
- Three I^2C Master and Slave w/Address Masking and IPMI Support
- Three Enhanced Addressable UARTs:
  - RS-232, RS-485 and LIN/J2602 support
  - IrDA® with on-chip hardware encoder and decoder
- External Edge and Level Change Interrupt on All Ports
- Hardware Real-Time Clock and Calendar (RTCC)
- Up to 24 Peripheral Pin Select (PPS) Remappable Pins
- 21 Total 16-Bit Timers:
  - Three dedicated 16-bit timers/counters
  - Two can be concatenated to form a 32-bit timer
  - Two additional 16-bit timers in each MCCP and SCCP module, totaling 18
- Capture/Compare/PWM/Timer modules:
  - Two 16-bit timers or one 32-bit timer in each module
  - PWM resolution down to 21 ns
  - Three Multiple Output (MCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Six PWM outputs
    - Programmable dead time
    - Auto-shutdown
  - Six Single Output (SCCP) modules:
    - Flexible configuration as PWM, input capture, output compare or timers
    - Single PWM output
- Reference Clock Output (REFO)
- Four Configurable Logic Cells (CLC) with Internal Connections to Select Peripherals and PPS
- 4-Channel Hardware DMA with Automatic Data Size Detection and CRC Engine

Debug Features

- Two Programming and Debugging Interfaces:
  - 2-wire ICSP™ interface with non-intrusive access and real-time data exchange with application
  - 4-wire MIPS® standard Enhanced JTAG interface
- IEEE Standard 1149.2 Compatible (JTAG) Boundary Scan

Analog Features

- Three Analog Comparators with Input Multiplexing
- Programmable High/Low-Voltage Detect (HLVD)
- 5-Bit Comparator Voltage Reference DAC with Pin Output
- Up to 24-Channel, Software-Selectable 10/12-Bit SAR Analog-to-Digital Converter (ADC):
  - 12-bit 200K samples/second conversion rate (single Sample-and-Hold)
  - 10-bit 300k samples/second conversion rate (single Sample-and-Hold)
  - Sleep mode operation
  - Low-voltage boost for input
  - Band gap reference input feature
  - Windowed threshold compare feature
  - Auto-scan feature
- Brown-out Reset (BOR)

TABLE 1: PIC32MM0256GPM064 FAMILY DEVICES

Device	Pins	Program Memory (Kbytes)	Data Memory (Kbytes)	General Purpose I/O/PPS	16-Bit Timers Maximum	PWM Outputs Maximum	Remappable Peripherals						10/12-Bit ADC (External Channels)	Comparators	CRC	RTCC	I^2C	USB	Packages
							Dedicated 16-Bit Timers	UART(1)/LIN/J2602	MCCP(4)	SCCP(3)	CLC	SPI(2)/I^2S							
PIC32MM0064GPM028	28	64	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0128GPM028	28	128	16	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0256GPM028	28	256	32	21/18	21	18	3	3	3	6	4	3	12	3	Yes	Yes	3	Yes	SSOP/QFN/ UQFN
PIC32MM0064GPM036	36/40	64	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0128GPM036	36/40	128	16	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0256GPM036	36/40	256	32	27/20	21	20	3	3	3	6	4	3	15	3	Yes	Yes	3	Yes	VQFN/UQFN
PIC32MM0064GPM048	48	64	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0128GPM048	48	128	16	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0256GPM048	48	256	32	38/24	21	24	3	3	3	6	4	3	17	3	Yes	Yes	3	Yes	UQFN/TQFP
PIC32MM0064GPM064	64	64	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0128GPM064	64	128	16	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP
PIC32MM0256GPM064	64	256	32	52/24	21	24	3	3	3	6	4	3	20	3	Yes	Yes	3	Yes	QFN/TQFP

Note 1: UART1 has assigned pins. UART2 and UART3 are remappable.

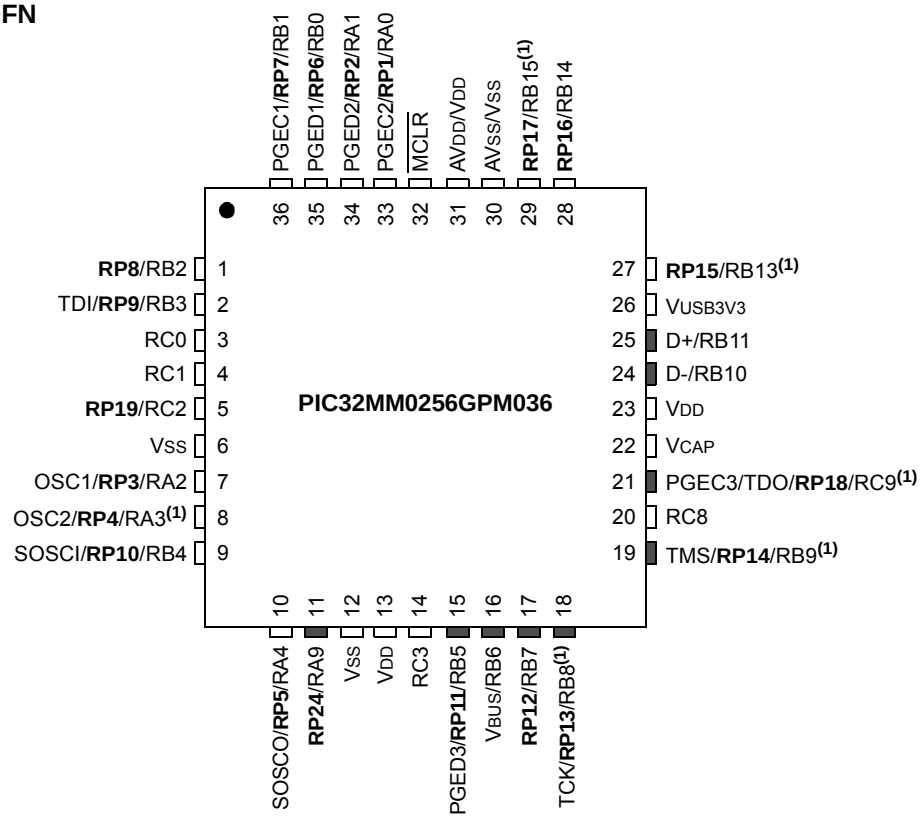
2: SPI1 and SPI3 have assigned pins. SPI2 is remappable.

3: SCCP can be configured as a PWM with 1 output, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

4: MCCP can be configured as a PWM with up to 6 outputs, input capture, output compare, 2 x 16-bit timers or 1 x 32-bit timer.

Pin Diagrams (Continued)

36-Pin QFN



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

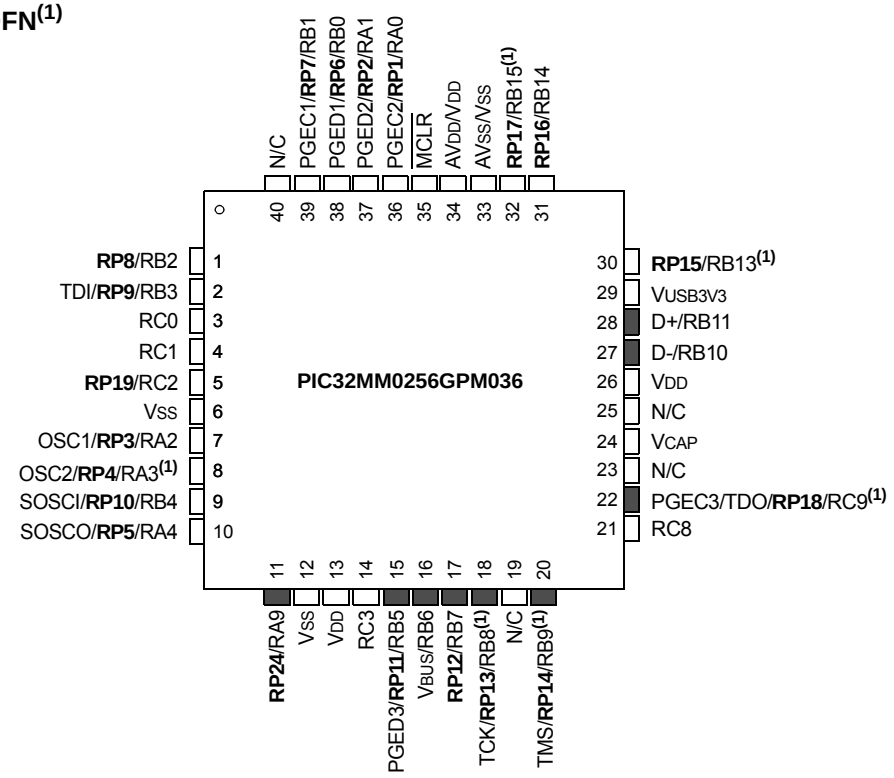
TABLE 4: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 36-PIN QFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	19	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/U1RTS/U1BCLK/SDO1/OCM1B/INT2/RB9(1)
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	20	AN14/LVDIN/C2INC/RC8
3	AN12/C2IND/T2CK/T2G/RC0	21	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/SDO3/RC9(1)
4	AN13/T3CK/T3G/RC1	22	VCAP
5	**RP19**/OCM2A/RC2	23	VDD
6	VSS	24	D-/RB10
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	25	D+/RB11
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	26	VUSB3V3
9	SOSCI/AN7/**RP10**/OCM3C/RB4	27	AN8/**RP15**/SCL3/SCK3/RB13(1)
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	28	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
11	**RP24**/OCM3A/RA9	29	AN10/C3INA/REFCLKO/**RP17**/U1RX/SS1/FSYNC1/OCM2B/INT0/RB15(1)
12	VSS	30	AVSS/VSS
13	VDD	31	AVDD/VDD
14	RC3	32	MCLR
15	PGED3/**RP11**/ASDA1(2)/USBID/SS3/FSYNC3/OCM3E/RB5	33	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
16	VBUS/RB6	34	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
17	**RP12**/SDA3/SDI3/OCM3F/RB7	35	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
18	TCK/**RP13**/SCL1/U1CTS/SCK1/OCM1A/RB8(1)	36	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

40-Pin UQFN(1)



Legend: Shaded pins are up to 5V tolerant.
Note 1: High drive strength pin.

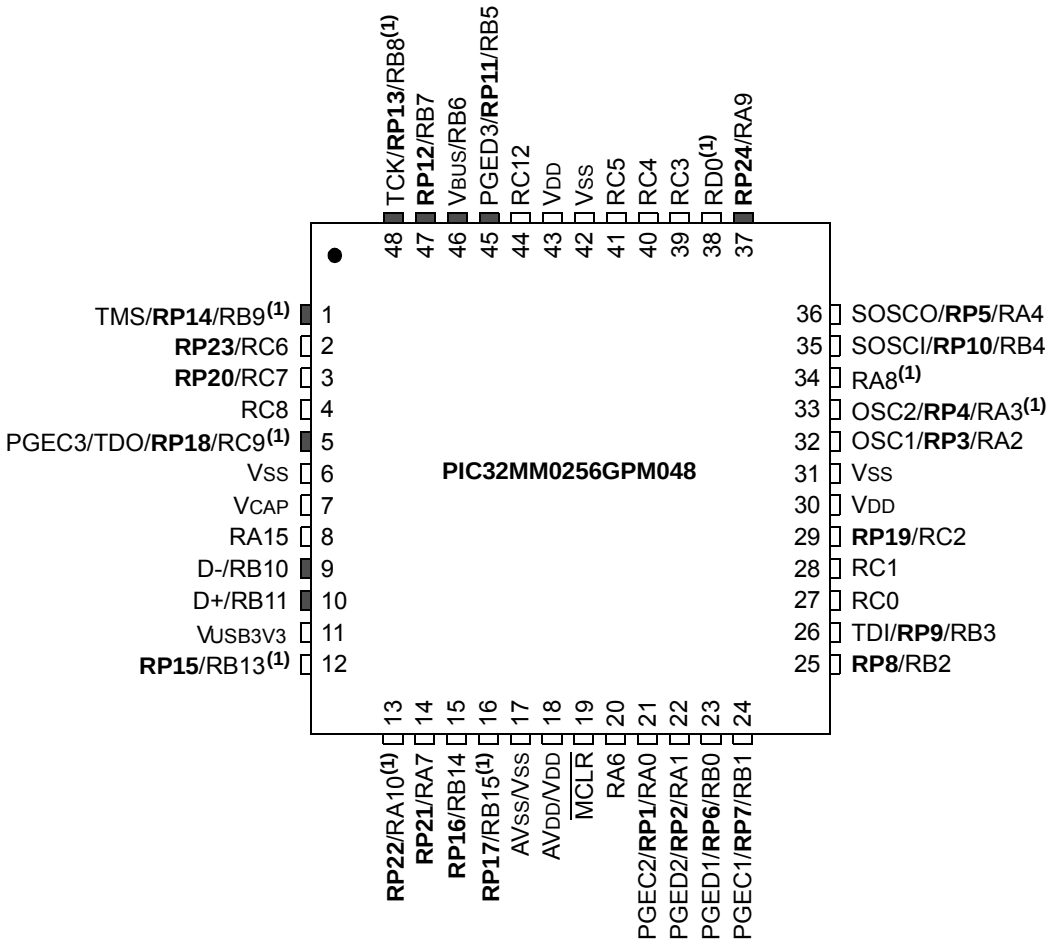
TABLE 5: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 40-PIN UQFN DEVICES

Pin	Function	Pin	Function
1	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2	21	AN14/LVDIN/C2INC/RC8
2	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3	22	PGEC3/TDO/**RP18**/ASCL1(2)/SDO3/USBOEN/RC9(1)
3	AN12/C2IND/T2CK/T2G/RC0	23	N/C
4	AN13/T3CK/T3G/RC1	24	VCAP
5	**RP19**/OCM2A/RC2	25	N/C
6	VSS	26	VDD
7	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2	27	D-/RB10
8	OSC2/CLKO/AN6/C3IND/**RP4**/OCM1D/RA3(1)	28	D+/RB11
9	SOSCI/AN7/**RP10**/OCM3C/RB4	29	VUSB3V3
10	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4	30	AN8/**RP15**/SCL3/SCK3/RB13(1)
11	**RP24**/OCM3A/RA9	31	CVREF/AN9/C3INB/**RP16**/RTCC/U1TX/VBUSON/SDI1/OCM3B/INT1/RB14
12	VSS	32	AN10/C3INA/REFCLKO/**RP17**/U1RX/$\overline{SS1}$/FSYNC1/OCM2B/INT0/RB15(1)
13	VDD	33	AVSS/VSS
14	RC3	34	AVDD/VDD
15	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{SS3}$/FSYNC3/OCM3E/RB5	35	$\overline{MCLR}$
16	VBUS/RB6	36	PGEC2/VREF+/CVREF+/AN0/**RP1**/OCM1E/INT3/RA0
17	**RP12**/SDA3/SDI3/OCM3F/RB7	37	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1
18	TCK/**RP13**/SCL1/$\overline{U1CTS}$/SCK1/OCM1A/RB8(1)	38	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0
19	N/C	39	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1
20	TMS/REFCLKI/**RP14**/SDA1/T1CK/T1G/$\overline{U1RTS}$/U1BCLK/SDO1/OCM1B/INT2/RB9(1)	40	N/C

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

Pin Diagrams (Continued)

48-Pin UQFN, TQFP(1)



Legend: Shaded pins are up to 5V tolerant.

Note 1: High drive strength pin.

TABLE 6: COMPLETE PIN FUNCTION DESCRIPTIONS FOR 48-PIN UQFN/TQFP DEVICES

Pin	Function	Pin	Function
1	TMS/**RP14**/SDA1/OCM1B/INT2/RB9(1)	25	AN4/C1INB/**RP8**/SDA2/OCM2E/RB2
2	**RP23**/RC6	26	TDI/AN11/C1INA/**RP9**/SCL2/OCM2F/RB3
3	**RP20**/RC7	27	AN12/C2IND/T2CK/T2G/RC0
4	AN14/LVDIN/C2INC/RC8	28	AN13/T3CK/T3G/RC1
5	PGEC3/TDO/**RP18**/ASCL1(2)/USBOEN/RC9(1)	29	**RP19**/OCM2A/RC2
6	VSS	30	VDD
7	VCAP	31	VSS
8	RTCC/RA15	32	OSC1/CLKI/AN5/**RP3**/OCM1C/RA2
9	D-/RB10	33	OSC2/CLKO/AN6/C3IND/**RP4**/RA3(1)
10	D+/RB11	34	SDO3/RA8(1)
11	VUSB3V3	35	SOSCI/AN7/**RP10**/OCM3C/RB4
12	AN8/**RP15**/SCL3/RB13(1)	36	SOSCO/SCLKI/**RP5**/PWRLCLK/OCM3D/RA4
13	**RP22**/SCK3/RA10(1)	37	**RP24**/OCM3A/RA9
14	**RP21**/SDI3/RA7	38	REFCLKI/T1CK/T1G/$\overline{\text{U1RTS}}$/U1BCLK/SDO1/RD0(1)
15	CVREF/AN9/C3INB/**RP16**/VBUSON/SDI1/OCM3B/INT1/RB14	39	OCM2B/RC3
16	AN10/C3INA/REFCLKO/**RP17**/$\overline{\text{SS1}}$/FSYNC1/INT0/RB15(1)	40	OCM1E/INT3/RC4
17	AVSS/VSS	41	AN15/OCM1D/RC5
18	AVDD/VDD	42	VSS
19	$\overline{\text{MCLR}}$	43	VDD
20	AN19/U1RX/RA6	44	U1TX/RC12
21	PGEC2/VREF+/CVREF+/AN0/**RP1**/RA0	45	PGED3/**RP11**/ASDA1(2)/USBID/$\overline{\text{SS3}}$/FSYNC3/OCM3E/RB5
22	PGED2/VREF-/AN1/**RP2**/OCM1F/RA1	46	VBUS/RB6
23	PGED1/AN2/C1IND/C2INB/C3INC/**RP6**/OCM2C/RB0	47	**RP12**/SDA3/OCM3F/RB7
24	PGEC1/AN3/C1INC/C2INA/**RP7**/OCM2D/RB1	48	TCK/**RP13**/SCL1/$\overline{\text{U1CTS}}$/SCK1/OCM1A/RB8(1)

Note 1: High drive strength pin.
2: Alternate pin assignments for I2C1 as determined by the I2C1SEL Configuration bit.

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Referenced Sources

This device data sheet is based on the following individual sections of the *"PIC32 Family Reference Manual"*. These documents should be considered as the general reference for the operation of a particular module or device feature.

Note: To access the documents listed below, browse the documentation section of the Microchip web site (www.microchip.com).

- **Section 1. "Introduction"** (DS60001127)
- **Section 5. "Flash Programming"** (DS60001121)
- **Section 7. "Resets"** (DS60001118)
- **Section 8. "Interrupts"** (DS61108)
- **Section 10. "Power-Saving Modes"** (DS60001130)
- **Section 12. "I/O Ports"** (DS60001120)
- **Section 14. "Timers"** (DS60001105)
- **Section 19. "Comparator"** (DS60001110)
- **Section 20. "Comparator Voltage Reference"** (DS61109)
- **Section 21. "UART"** (DS61107)
- **Section 23. "Serial Peripheral Interface (SPI)"** (DS61106)
- **Section 24. "Inter-Integrated Circuit™ (I^2C™)"** (DS61116)
- **Section 25. "12-Bit Analog-to-Digital Converter (ADC) with Threshold Detect"** (DS60001359)
- **Section 27. "USB On-The-Go (OTG)"** (DS61126)
- **Section 28. "RTCC with Timestamp"** (DS60001362)
- **Section 30. "Capture/Compare/PWM/Timer (MCCP and SCCP)"** (DS60001381)
- **Section 31. "DMA Controller"** (DS60001117)
- **Section 33. "Programming and Diagnostics"** (DS61129)
- **Section 36. "Configurable Logic Cell"** (DS60001363)
- **Section 48. "Memory Organization and Permissions"** (DS60001214)
- **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192)
- **Section 59. "Oscillators with DCO"** (DS60001329)
- **Section 62. "Dual Watchdog Timer"** (DS60001365)

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

This data sheet contains device-specific information for the PIC32MM0256GPM064 family devices.

Figure 1-1 illustrates a general block diagram of the core and peripheral modules in the PIC32MM0256GPM064 family of devices.

Table 1-1 lists the pinout I/O descriptions for the pins shown in the device pin tables.

FIGURE 1-1: PIC32MM0256GPM064 FAMILY BLOCK DIAGRAM

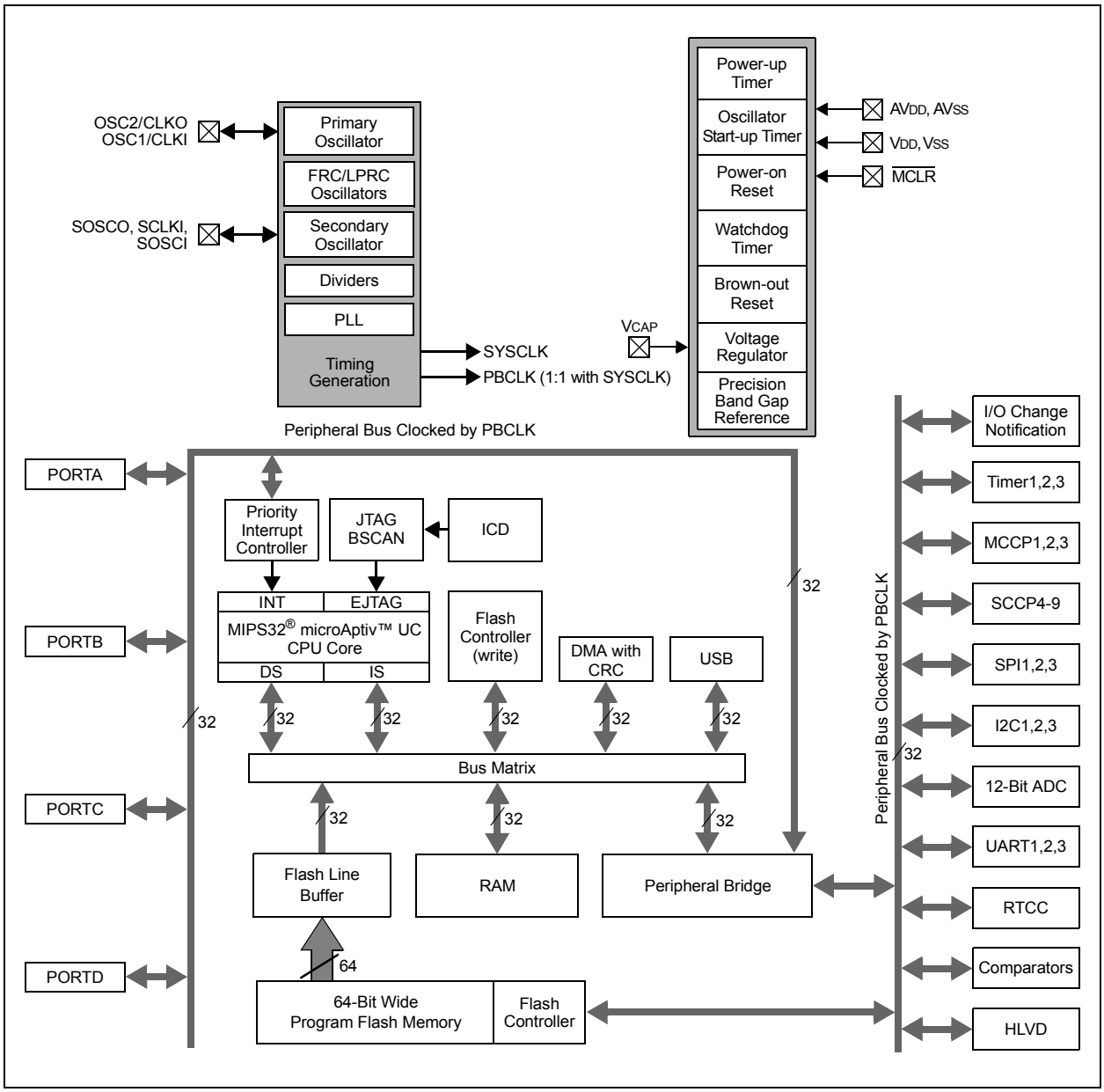


TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
AN0	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter input channels
AN1	3	28	34	37	22	12	I	ANA	
AN2	4	1	35	38	23	13	I	ANA	
AN3	5	2	36	39	24	14	I	ANA	
AN4	6	3	1	1	25	15	I	ANA	
AN5	9	6	7	7	32	25	I	ANA	
AN6	10	7	8	8	33	26	I	ANA	
AN7	11	8	9	9	35	28	I	ANA	
AN8	24	21	27	30	12	63	I	ANA	
AN9	25	22	28	31	15	2	I	ANA	
AN10	26	23	29	32	16	3	I	ANA	
AN11	7	4	2	2	26	16	I	ANA	
AN12	—	—	3	3	27	19	I	ANA	
AN13	—	—	4	4	28	20	I	ANA	
AN14	—	—	20	21	4	52	I	ANA	
AN15	—	—	—	—	41	37	I	ANA	
AN16	—	—	—	—	—	6	I	ANA	
AN17	—	—	—	—	—	7	I	ANA	
AN18	—	—	—	—	—	8	I	ANA	
AN19	—	—	—	—	—	10	I	ANA	
AV_{DD}	28	25	31	34	18	5	P	—	Analog modules power supply
AV_{SS}	27	24	30	33	17	4	P	—	Analog modules ground
C1INA	7	4	2	2	26	16	I	ANA	Comparator 1 Input A
C1INB	6	3	1	1	25	15	I	ANA	Comparator 1 Input B
C1INC	5	2	36	39	24	14	I	ANA	Comparator 1 Input C
C1IND	4	1	35	38	23	13	I	ANA	Comparator 1 Input D
C2INA	5	2	36	39	24	14	I	ANA	Comparator 2 Input A
C2INB	4	1	35	38	23	13	I	ANA	Comparator 2 Input B
C2INC	—	—	20	21	4	52	I	ANA	Comparator 2 Input C
C2IND	—	—	3	3	27	19	I	ANA	Comparator 2 Input D
C3INA	26	23	29	32	16	3	I	ANA	Comparator 3 Input A
C3INB	25	22	28	31	15	2	I	ANA	Comparator 3 Input B
C3INC	4	1	35	38	23	13	I	ANA	Comparator 3 Input C
C3IND	10	7	8	8	33	26	I	ANA	Comparator 3 Input D
CLKI	9	6	7	7	32	25	I	ST	External Clock source input (EC mode)
CLKO	10	7	8	8	33	26	O	DIG	System clock output
CV_{REF}	25	22	28	31	15	2	O	ANA	Comparator voltage reference output
$CV_{REF}+$	2	27	33	36	21	11	I	ANA	Positive comparator voltage reference input
D+	22	19	25	28	10	61	I/O	—	USB transceiver differential plus line
D-	21	18	24	27	9	60	I/O	—	USB transceiver differential minus line
FSYNC1	26	23	29	32	16	32	I/O	ST/DIG	SPI1 frame signal input or output
FSYNC3	14	11	15	15	45	22	I/O	ST/DIG	SPI3 frame signal input or output

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
INT0	26	23	29	32	16	32	I	ST	External Interrupt 0
INT1	25	22	28	31	15	31	I	ST	External Interrupt 1
INT2	18	15	19	20	1	49	I	ST	External Interrupt 2
INT3	2	27	33	36	40	36	I	ST	External Interrupt 3
LVDIN	24	21	20	21	4	52	I	ANA	High/Low-Voltage Detect input
$\overline{\text{MCLR}}$	1	26	32	35	19	9	I	ST	Master Clear (device Reset)
OCM1A	17	14	18	18	48	7	O	DIG	MCCP1 Output A
OCM1B	18	15	19	20	1	53	O	DIG	MCCP1 Output B
OCM1C	9	6	7	7	32	25	O	DIG	MCCP1 Output C
OCM1D	10	7	8	8	41	37	O	DIG	MCCP1 Output D
OCM1E	2	27	33	36	40	36	O	DIG	MCCP1 Output E
OCM1F	3	28	34	37	22	12	O	DIG	MCCP1 Output F
OCM2A	19	16	5	5	29	21	O	DIG	MCCP2 Output A
OCM2B	26	23	29	32	39	35	O	DIG	MCCP2 Output B
OCM2C	4	1	35	38	23	13	O	DIG	MCCP2 Output C
OCM2D	5	2	36	39	24	14	O	DIG	MCCP2 Output D
OCM2E	6	3	1	1	25	15	O	DIG	MCCP2 Output E
OCM2F	7	4	2	2	26	16	O	DIG	MCCP2 Output F
OCM3A	24	21	11	11	37	54	O	DIG	MCCP3 Output A
OCM3B	25	22	28	31	15	33	O	DIG	MCCP3 Output B
OCM3C	11	8	9	9	35	59	O	DIG	MCCP3 Output C
OCM3D	12	9	10	10	36	41	O	DIG	MCCP3 Output D
OCM3E	14	11	15	15	45	42	O	DIG	MCCP3 Output E
OCM3F	16	13	17	17	47	45	O	DIG	MCCP3 Output F
OSC1	9	6	7	7	32	25	—	—	Primary Oscillator crystal
OSC2	10	7	8	8	33	26	—	—	Primary Oscillator crystal
PGEC1	5	2	36	39	24	14	I	ST	ICSP™ Port 1 programming clock input
PGEC2	2	27	33	36	21	11	I	ST	ICSP Port 2 programming clock input
PGEC3	19	16	21	22	5	55	I	ST	ICSP Port 3 programming clock input
PGED1	4	1	35	38	23	13	I/O	ST/DIG	ICSP Port 1 programming data
PGED2	3	28	34	37	22	12	I/O	ST/DIG	ICSP Port 2 programming data
PGED3	14	11	15	15	45	43	I/O	ST/DIG	ICSP Port 3 programming data
PWRLCLK	12	9	10	10	36	29	I	ST	Real-Time Clock 50/60 Hz clock input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RA0	2	27	33	36	21	11	I/O	ST/DIG	PORTA digital I/Os
RA1	3	28	34	37	22	12	I/O	ST/DIG	
RA2	9	6	7	7	32	25	I/O	ST/DIG	
RA3	10	7	8	8	33	26	I/O	ST/DIG	
RA4	12	9	10	10	36	29	I/O	ST/DIG	
RA5	—	—	—	—	—	54	I/O	ST/DIG	
RA6	—	—	—	—	20	10	I/O	ST/DIG	
RA7	—	—	—	—	14	1	I/O	ST/DIG	
RA8	—	—	—	—	34	27	I/O	ST/DIG	
RA9	—	—	11	11	37	30	I/O	ST/DIG	
RA10	—	—	—	—	13	64	I/O	ST/DIG	
RA11	—	—	—	—	—	8	I/O	ST/DIG	
RA12	—	—	—	—	—	7	I/O	ST/DIG	
RA13	—	—	—	—	—	6	I/O	ST/DIG	
RA14	—	—	—	—	—	59	I/O	ST/DIG	
RA15	—	—	—	—	8	58	I/O	ST/DIG	
RB0	4	1	35	38	23	13	I/O	ST/DIG	PORTB digital I/Os
RB1	5	2	36	39	24	14	I/O	ST/DIG	
RB2	6	3	1	1	25	15	I/O	ST/DIG	
RB3	7	4	2	2	26	16	I/O	ST/DIG	
RB4	11	8	9	9	35	28	I/O	ST/DIG	
RB5	14	11	15	15	45	43	I/O	ST/DIG	
RB6	15	12	16	16	46	44	I/O	ST/DIG	
RB7	16	13	17	17	47	46	I/O	ST/DIG	
RB8	17	14	18	18	48	48	I/O	ST/DIG	
RB9	18	15	19	20	1	49	I/O	ST/DIG	
RB10	21	18	24	27	9	60	I/O	ST/DIG	
RB11	22	19	25	28	10	61	I/O	ST/DIG	
RB13	24	21	27	30	12	63	I/O	ST/DIG	
RB14	25	22	28	31	15	2	I/O	ST/DIG	
RB15	26	23	29	32	16	3	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RC0	—	—	3	3	27	19	I/O	ST/DIG	PORTC digital I/Os
RC1	—	—	4	4	28	20	I/O	ST/DIG	
RC2	—	—	5	5	29	21	I/O	ST/DIG	
RC3	—	—	14	14	39	35	I/O	ST/DIG	
RC4	—	—	—	—	40	36	I/O	ST/DIG	
RC5	—	—	—	—	41	37	I/O	ST/DIG	
RC6	—	—	—	—	2	50	I/O	ST/DIG	
RC7	—	—	—	—	3	51	I/O	ST/DIG	
RC8	—	—	20	21	4	52	I/O	ST/DIG	
RC9	19	16	21	22	5	55	I/O	ST/DIG	
RC10	—	—	—	—	—	45	I/O	ST/DIG	
RC11	—	—	—	—	—	22	I/O	ST/DIG	
RC12	—	—	—	—	44	40	I/O	ST/DIG	
RC13	—	—	—	—	—	47	I/O	ST/DIG	
RC14	—	—	—	—	—	41	I/O	ST/DIG	
RC15	—	—	—	—	—	42	I/O	ST/DIG	
RD0	—	—	—	—	38	34	I/O	ST/DIG	PORTD digital I/Os
RD1	—	—	—	—	—	53	I/O	ST/DIG	
RD2	—	—	—	—	—	32	I/O	ST/DIG	
RD3	—	—	—	—	—	33	I/O	ST/DIG	
RD4	—	—	—	—	—	31	I/O	ST/DIG	
REFCLKI	18	15	19	20	38	34	I	ST	External reference clock input
REFCLKO	26	23	29	32	16	3	O	ST	External reference clock output
RP1	2	27	33	36	21	11	I/O	ST/DIG	Remappable peripherals (input or output)
RP2	3	28	34	37	22	12	I/O	ST/DIG	
RP3	9	6	7	7	32	25	I/O	ST/DIG	
RP4	10	7	8	8	33	26	I/O	ST/DIG	
RP5	12	9	10	10	36	29	I/O	ST/DIG	
RP6	4	1	35	38	23	13	I/O	ST/DIG	
RP7	5	2	36	39	24	14	I/O	ST/DIG	
RP8	6	3	1	1	25	15	I/O	ST/DIG	
RP9	7	4	2	2	26	16	I/O	ST/DIG	
RP10	11	8	9	9	35	28	I/O	ST/DIG	
RP11	14	11	15	15	45	43	I/O	ST/DIG	
RP12	16	13	17	17	47	46	I/O	ST/DIG	
RP13	17	14	18	18	48	48	I/O	ST/DIG	
RP14	18	15	19	20	1	49	I/O	ST/DIG	
RP15	24	21	27	30	12	63	I/O	ST/DIG	
RP16	25	22	28	31	15	2	I/O	ST/DIG	
RP17	26	23	29	32	16	3	I/O	ST/DIG	
RP18	19	16	21	22	5	55	I/O	ST/DIG	
RP19	—	—	5	5	29	21	I/O	ST/DIG	
RP20	—	—	—	—	3	51	I/O	ST/DIG	

Legend: ST = Schmitt Trigger input buffer; I2C = I^2C/SMBus input buffer; DIG = Digital input/output; ANA = Analog level input/output; P = Power

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
RP21	—	—	—	—	14	1	I/O	ST/DIG	Remappable peripherals (input or output)
RP22	—	—	—	—	13	64	I/O	ST/DIG	
RP23	—	—	—	—	2	50	I/O	ST/DIG	
RP24	—	—	11	11	37	30	I/O	ST/DIG	
RTCC	25	22	28	31	8	58	O	DIG	Real-Time Clock/Calendar alarm/seconds output
SCK1	17	14	18	18	48	47	I/O	ST/DIG	SPI1 clock (input or output)
SCK3	24	21	27	30	13	64	I/O	ST/DIG	SPI3 clock (input or output)
SCL1	17	14	18	18	48	48	I/O	I2C	I2C1 synchronous serial clock input/output
ASCL1	19	16	21	22	5	55	I/O	I2C	Alternate I2C1 synchronous serial clock input/ output
SCL2	7	4	2	2	26	16	I/O	I2C	I2C2 synchronous serial clock input/output
SCL3	24	21	27	30	12	63	I/O	I2C	I2C3 synchronous serial clock input/output
SCLKI	12	9	10	10	36	29	I	ST	Secondary Oscillator digital clock input
SDA1	18	15	19	20	1	49	I/O	I2C	I2C1 data input/output
ASDA1	14	11	15	15	45	43	I/O	I2C	Alternate I2C1 data input/output
SDA2	6	3	1	1	25	15	I/O	I2C	I2C2 data input/output
SDA3	16	13	17	17	47	46	I/O	I2C	I2C3 data input/output
SDI1	25	22	28	31	15	31	I	ST	SPI1 data input
SDI3	16	13	17	17	14	1	I	ST	SPI3 data input
SDO1	18	15	19	20	38	34	O	DIG	SPI1 data output
SDO3	19	16	21	22	34	27	O	DIG	SPI3 data output
SOSCI	11	8	9	9	35	28	—	—	Secondary Oscillator crystal
SOSCO	12	9	10	10	36	29	—	—	Secondary Oscillator crystal
$\overline{SS1}$	26	23	29	32	16	32	I	ST	SPI1 slave select input
$\overline{SS3}$	14	11	15	15	45	22	I	ST	SPI3 slave select input
T1CK	18	15	19	20	38	34	I	ST	Timer1 external clock input
T2CK	18	15	3	3	27	19	I	ST	Timer2 external clock input
T3CK	19	16	4	4	28	20	I	ST	Timer3 external clock input
T1G	18	15	19	20	38	34	I	ST	Timer1 clock gate input
T2G	18	15	3	3	27	19	I	ST	Timer2 clock gate input
T3G	19	16	4	4	28	20	I	ST	Timer3 clock gate input
TCK	17	14	18	18	48	48	I	ST	JTAG clock input
TDI	7	4	2	2	26	16	I	ST	JTAG data input
TDO	19	16	21	22	5	55	O	DIG	JTAG data output
TMS	18	15	19	20	1	49	I	ST	JTAG mode select input

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

TABLE 1-1: PIC32MM0256GPM064 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Name	Pin Number						Pin Type	Buffer Type	Description
	28-Pin SSOP	28-Pin QFN/ UQFN	36-Pin QFN	40-Pin UQFN	48-Pin QFN/ TQFP	64-Pin QFN/ TQFP			
U1BCLK	18	15	19	20	38	34	O	DIG	UART1 IrDA® 16x baud clock output
$\overline{\text{U1CTS}}$	17	14	18	18	48	6	I	ST	UART1 Clear-to-Send
$\overline{\text{U1RTS}}$	18	15	19	20	38	34	O	DIG	UART1 Ready-to-Send
U1RX	26	23	29	32	20	10	I	ST	UART1 receive data input
U1TX	25	22	28	31	44	40	O	DIG	UART1 transmit data output
USBID	14	11	15	15	45	43	I	ST	USB OTG ID (OTG mode only)
USBOEN	19	16	21	22	5	55	O	—	USB transceiver output enable flag
VBUSON	25	22	28	31	15	2	O	—	USB host and On-The-Go (OTG) bus power control output
VBUS	15	12	16	16	46	44	P	—	USB VBUS connection (5V nominal)
VUSB3V3	23	20	26	29	11	62	P	—	USB transceiver power input (3.3V nominal)
VCAP	20	17	22	24	7	56	P	—	Core voltage regulator filter capacitor connection
VDD	13,28	10,25	13,23,31	13,26, 34	18,30, 43	17,23, 39,57	P	—	Digital modules power supply
VREF-	3	28	34	37	22	12	I	ANA	Analog-to-Digital Converter negative reference
VREF+	2	27	33	36	21	11	I	ANA	Analog-to-Digital Converter positive reference
VSS	8,27	5,24	6,12,30	6,12,33	6,17,31, 42	18,24, 38	P	—	Digital modules ground

Legend: ST = Schmitt Trigger input buffer DIG = Digital input/output P = Power
I2C = I^2C/SMBus input buffer ANA = Analog level input/output

2.0 GUIDELINES FOR GETTING STARTED WITH 32-BIT MICROCONTROLLERS

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

2.1 Basic Connection Requirements

Getting started with the PIC32MM0256GPM064 family of 32-bit Microcontrollers (MCUs) requires attention to a minimal set of device pin connections before proceeding with development. The following is a list of pin names, which must always be connected:

- All VDD and VSS pins (see **Section 2.2 "Decoupling Capacitors"**)
- All AVDD and AVSS pins, even if the ADC module is not used (see **Section 2.2 "Decoupling Capacitors"**)
- $\overline{\text{MCLR}}$ pin (see **Section 2.3 "Master Clear (MCLR) Pin"**)
- VCAP pin (see **Section 2.4 "Voltage Regulator Pin (VCAP)"**)
- PGECx/PGEDx pins, used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes (see **Section 2.5 "ICSP Pins"**)
- OSC1 and OSC2 pins, when external oscillator source is used (see **Section 2.7 "External Oscillator Pins"**)
- VUSB3V3 pin, this pin must be powered for USB operation (see **Section 18.4 "Powering the USB Transceiver"**)

The following pin(s) may be required as well:

VREF+/VREF- pins, used when external voltage reference for the ADC module is implemented.

Note: The AVDD and AVSS pins must be connected, regardless of ADC use and the ADC voltage reference source.

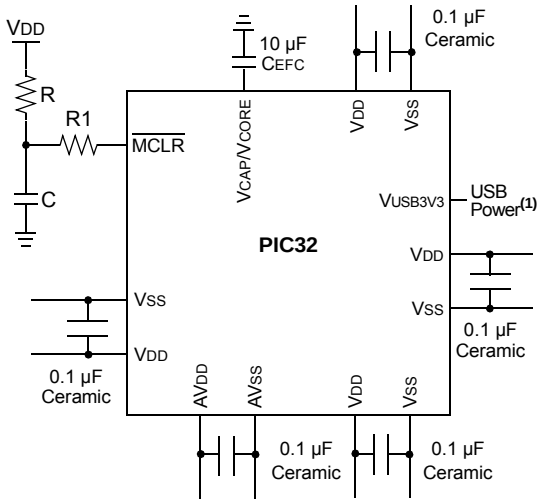
2.2 Decoupling Capacitors

The use of decoupling capacitors on power supply pins, such as VDD, VSS, AVDD and AVSS, is required. See Figure 2-1.

Consider the following criteria when using decoupling capacitors:

- **Value and type of capacitor:** A value of 0.1 µF (100 nF), 10-20V is recommended. The capacitor should be a low Equivalent Series Resistance (low-ESR) capacitor and have resonance frequency in the range of 20 MHz and higher. It is further recommended that ceramic capacitors be used.
- **Placement on the printed circuit board:** The decoupling capacitors should be placed as close to the pins as possible. It is recommended that the capacitors be placed on the same side of the board as the device. If space is constricted, the capacitor can be placed on another layer on the PCB using a via; however, ensure that the trace length from the pin to the capacitor is within one-quarter inch (6 mm) in length.
- **Handling high-frequency noise:** If the board is experiencing high-frequency noise, upward of tens of MHz, add a second ceramic-type capacitor in parallel to the above described decoupling capacitor. The value of the second capacitor can be in the range of 0.01 µF to 0.001 µF. Place this second capacitor next to the primary decoupling capacitor. In high-speed circuit designs, consider implementing a decade pair of capacitances, as close to the power and ground pins as possible. For example, 0.1 µF in parallel with 0.001 µF.
- **Maximizing performance:** On the board layout from the power supply circuit, run the power and return traces to the decoupling capacitors first, and then to the device pins. This ensures that the decoupling capacitors are first in the power chain. Equally important is to keep the trace length between the capacitor and the power pins to a minimum, thereby reducing PCB track inductance.

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: Refer to **Section 18.4 "Powering the USB Transceiver"** for requirements of this pin.

2.2.1 BULK CAPACITORS

The use of a bulk capacitor is recommended to improve power supply stability. Typical values range from 4.7 µF to 47 µF. This capacitor should be located as close to the device as possible.

2.3 Master Clear (MCLR) Pin

The MCLR pin provides for two specific device functions:

- Device Reset
- Device Programming and Debugging

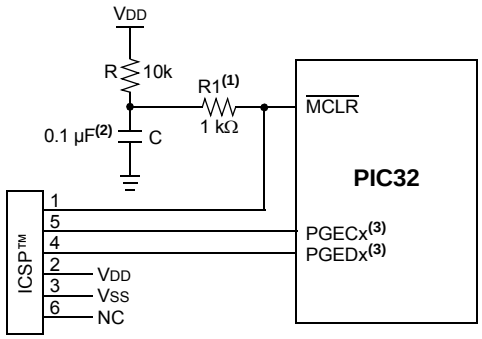
Pulling The MCLR pin low generates a device Reset. Figure 2-2 illustrates a typical MCLR circuit. During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

Note: When MCLR is used to wake the device from Retention Sleep, a POR Reset will occur.

For example, as illustrated in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components illustrated in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS(1,2,3)



Note 1: 470Ω ≤ R1 ≤ 1 kΩ will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown, due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met without interfering with the debugger/programmer tools.

2: The capacitor can be sized to prevent unintentional Resets from brief glitches or to extend the device Reset period during POR.

3: No pull-ups or bypass capacitors are allowed on active debug/program PGECx/PGEDx pins.

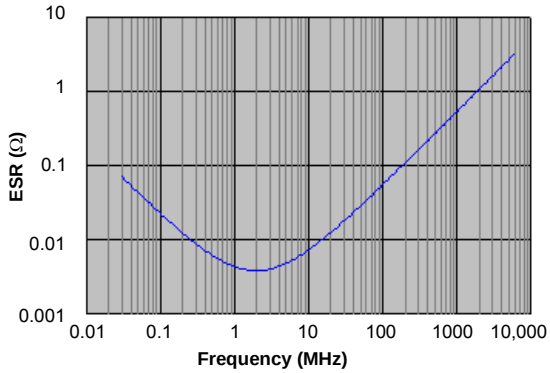
2.4 Voltage Regulator Pin (VCAP)

A low-ESR (< 5Ω) capacitor is required on the VCAP pin to stabilize the output voltage of the on-chip voltage regulator. The VCAP pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specification can be used.

The placement of this capacitor should be close to VCAP. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 29.0 "Electrical Characteristics"** for additional information.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

FIGURE 2-3: FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at +25°C, 0V DC bias.

TABLE 2-1: SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to +125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to +85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to +125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to +85ºC
Murata	GRM319R61C106KE15D	10 µF	±10%	16V	-55 to +85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface-mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

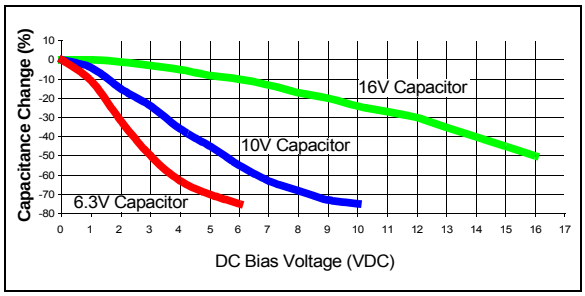
Typical low-cost, 10 μF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R) or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 μF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal regulator.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

Typical DC bias voltage vs. capacitance graph for X7R type capacitors is shown in Figure 2-4.

FIGURE 2-4: DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. The minimum DC rating for the ceramic capacitor on VCAP is 16V. Suggested capacitors are shown in Table 2-1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for In-Circuit Serial Programming™ (ICSP™) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Input Voltage High (VIH) and Input Voltage Low (VIL) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® ICD 3 or MPLAB REAL ICE™ In-Circuit Emulator.

For more information on MPLAB® ICD 3 and REAL ICE connection requirements, refer to the following documents that are available from the Microchip web site.

- *"Using MPLAB® ICD 3"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" (*DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 JTAG

The TMS, TDO, TDI and TCK pins are used for testing and debugging according to the Joint Test Action Group (JTAG) standard. It is recommended to keep the trace length between the JTAG connector, and the JTAG pins on the device, as short as possible. If the JTAG connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the TMS, TDO, TDI and TCK pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits, and pin Input Voltage High (V_{IH}) and Input Voltage Low (V_{IL}) requirements.

2.7 External Oscillator Pins

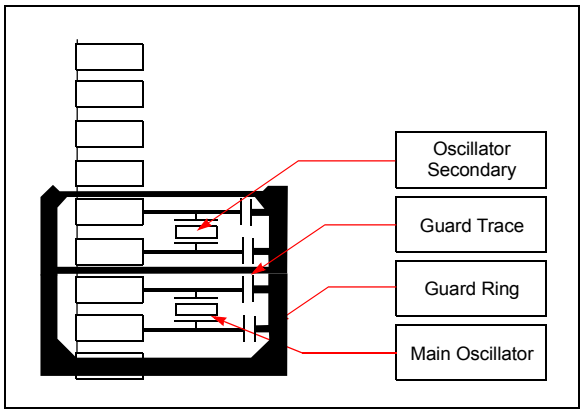
This family of devices has options for two external oscillators: a high-frequency Primary Oscillator and a low-frequency Secondary Oscillator (refer to **Section 9.0 "Oscillator Configuration"** for details).

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is illustrated in Figure 2-5.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site: (www.microchip.com).

- AN826, *"Crystal Oscillator Basics and Crystal Selection for rfPIC™ and PICmicro® Devices"*
- AN849, *"Basic PICmicro® Oscillator Design"*
- AN943, *"Practical PICmicro® Oscillator Analysis and Design"*
- AN949, *"Making Your Oscillator Work"*

FIGURE 2-5: SUGGESTED OSCILLATOR CIRCUIT PLACEMENT



2.8 Unused I/Os

To minimize power consumption, unused I/O pins should not be allowed to float as inputs. They can be configured as outputs and driven to a logic low or logic high state.

Alternatively, inputs can be reserved by ensuring the pin is always configured as an input and externally connecting the pin to V_{SS} or V_{DD}. A current-limiting resistor may be used to create this connection if there is any risk of inadvertently configuring the pin as an output with the logic output state opposite of the chosen power rail.

3.0 CPU

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 50. "CPU for Devices with MIPS32® microAptiv™ and M-Class Cores"** (DS60001192) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). MIPS32® microAptiv™ UC microprocessor core resources are available at: www.imgtec.com. The information in this data sheet supersedes the information in the FRM.

The MIPS32® microAptiv™ UC microprocessor core is the heart of the PIC32MM0256GPM064 family devices. The CPU fetches instructions, decodes each instruction, fetches source operands, executes each instruction and writes the results of the instruction execution to the proper destinations.

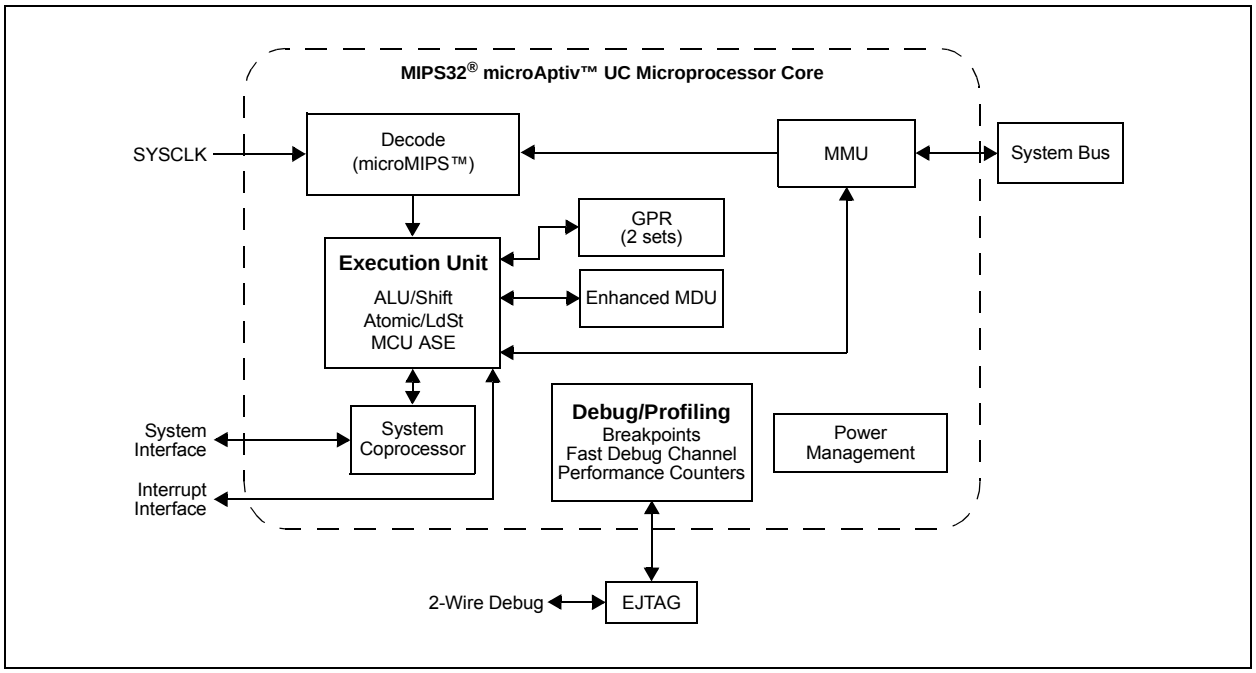
3.1 Features

The PIC32MM0256GPM064 family processor core key features include:

- 5-Stage Pipeline
- 32-Bit Address and Data Paths
- MIPS32 Enhanced Architecture:
  - Multiply-add and multiply-subtract instructions.
  - Targeted multiply instruction.
  - Zero and one detect instructions.
  - `WAIT` instruction.
  - Conditional move instructions.
  - Vectored interrupts.
  - Atomic interrupt enable/disable.
  - One GPR shadow set to minimize latency of interrupts.
  - Bit field manipulation instructions.
- microMIPS™ Instruction Set:
  - microMIPS allows improving the code size density over MIPS32, while maintaining MIPS32 performance.
  - microMIPS supports all MIPS32 instructions (except for branch-likely instructions) with new optimized 32-bit encoding. Frequent MIPS32 instructions are available as 16-bit instructions.
  - Added seventeen new and thirty-five MIPS32® corresponding, commonly used instructions in 16-bit opcode format.
  - Stack Pointer implicit in instruction.
  - MIPS32 assembly and ABI compatible.
- Memory Management Unit with Simple Fixed Mapping Translation (FMT) Mechanism
- Multiply/Divide Unit (MDU):
  - Configurable using high-performance multiplier array.
  - Maximum issue rate of one 32x16 multiply per clock.
  - Maximum issue rate of one 32x32 multiply every other clock.
  - Early-in iterative divide. Minimum 11 and maximum 33 clock latency (dividend (rs) sign extension dependent).
- Power Control:
  - No minimum frequency: 0 MHz.
  - Power-Down mode (triggered by `WAIT` instruction).
- EJTAG Debug/Profiling:
  - CPU control with start, stop and single stepping.
  - Software breakpoints via the `SDBBP` instruction.
  - Simple hardware breakpoints on virtual addresses, 4 instruction and 2 data breakpoints.
  - PC and/or load/store address sampling for profiling.
  - Performance counters.
  - Supports Fast Debug Channel (FDC).

A block diagram of the PIC32MM0256GPM064 family processor core is shown in Figure 3-1.

FIGURE 3-1: PIC32MM0256GPM064 FAMILY MICROPROCESSOR CORE BLOCK DIAGRAM



3.2 Architecture Overview

The MIPS32® microAptiv™ UC microprocessor core in the PIC32MM0256GPM064 family devices contains several logic blocks, working together in parallel, providing an efficient high-performance computing engine. The following blocks are included with the core:

- Execution Unit
- General Purpose Register (GPR)
- Multiply/Divide Unit (MDU)
- System Control Coprocessor (CP0)
- Memory Management Unit (MMU)
- Power Management
- microMIPS Instructions Decoder
- Enhanced JTAG (EJTAG) Controller

3.2.1 EXECUTION UNIT

The processor core execution unit implements a load/store architecture with single-cycle ALU operations (logical, shift, add, subtract) and an autonomous Multiply/Divide Unit (MDU). The core contains thirty-two 32-bit General Purpose Registers (GPRs) used for integer operations and address calculation. One additional register file shadow set (containing thirty-two registers) is added to minimize context switching overhead during interrupt/exception processing. The register file consists of two read ports and one write port, and is fully bypassed to minimize operation latency in the pipeline.

The execution unit includes:

- 32-bit adder used for calculating the data address
- Address unit for calculating the next instruction address
- Logic for branch determination and branch target address calculation
- Load aligner
- Bypass multiplexers used to avoid Stalls when executing instruction streams where data producing instructions are followed closely by consumers for their results
- Leading zero/one detect unit for implementing the `CLZ` and `CLO` instructions
- Arithmetic Logic Unit (ALU) for performing arithmetic and bitwise logical operations
- Shifter and store aligner

3.2.2 MULTIPLY/DIVIDE UNIT (MDU)

The microAptiv UC core includes a Multiply/Divide Unit (MDU) that contains a separate pipeline for multiply and divide operations. This pipeline operates in parallel with the Integer Unit (IU) pipeline and does not stall when the IU pipeline stalls. This allows the long-running MDU operations to be partially masked by system Stalls and/or other Integer Unit instructions.

The high-performance MDU consists of a 32x16 booth recoded multiplier, Result/Accumulation registers (HI and LO), a divide state machine, and the necessary multiplexers and control logic. The first number shown (‘32’ of 32x16) represents the rs operand. The second number (‘16’ of 32x16) represents the rt operand. The microAptiv UC core only checks the value of the rt operand to determine how many times the operation must pass through the multiplier. The 16x16 and 32x16 operations pass through the multiplier once. A 32x32 operation passes through the multiplier twice.

The MDU supports execution of one 16x16 or 32x16 multiply operation every clock cycle; 32x32 multiply operations can be issued every other clock cycle. Appropriate interlocks are implemented to stall the issuance of back-to-back, 32x32 multiply operations. The multiply operand size is automatically determined by logic built into the MDU. Divide operations are implemented with a simple 1-bit-per-clock iterative algorithm. An early-in detection checks the sign extension of the dividend (rs) operand. If rs is 8 bits wide, 23 iterations are skipped. For a 16-bit wide rs, 15 iterations are skipped, and for a 24-bit wide rs, 7 iterations are skipped. Any attempt to issue a subsequent MDU instruction while a divide is still active causes an IU pipeline Stall until the divide operation has completed.

Table 3-1 lists the repeat rate (peak issue rate of cycles until the operation can be re-issued), and latency (number of cycles until a result is available) for the microAptiv UC core multiply and divide instructions. The approximate latency and repeat rates are listed in terms of pipeline clocks.

TABLE 3-1: MULTIPLY/DIVIDE UNIT LATENCIES AND REPEAT RATES

Opcode	Operand Size (mul *rt*) (div *rs*)	Latency	Repeat Rate
`MULT/MULTU`, `MADD/MADDU`, `MSUB/MSUBU`	16 bits	1	1
	32 bits	2	2
`MUL` (GPR destination)	16 bits	2	1
	32 bits	3	2
`DIV/DIVU`	8 bits	12	11
	16 bits	19	18
	24 bits	26	25
	32 bits	33	32

The MIPS® architecture defines that the result of a multiply or divide operation be placed in the HI and LO registers. Using the Move-From-HI (MFHI) and Move-From-LO (MFLO) instructions, these values can be transferred to the general purpose register file.

In addition to the HI/LO targeted operations, the MIPS architecture also defines a Multiply instruction, MUL, which places the least significant results in the primary register file instead of the HI/LO register pair. By avoiding the explicit MFLO instruction, required when using the LO register, and by supporting multiple destination registers, the throughput of multiply-intensive operations is increased.

Two other instructions, Multiply-Add (MADD) and Multiply-Subtract (MSUB), are used to perform the multiply-accumulate and multiply-subtract operations. The MADD instruction multiplies two numbers and then adds the product to the current contents of the HI and LO registers. Similarly, the MSUB instruction multiplies two operands and then subtracts the product from the HI and LO registers. The MADD and MSUB operations are commonly used in DSP algorithms.

3.2.3 SYSTEM CONTROL COPROCESSOR (CP0)

In the MIPS architecture, CP0 is responsible for the virtual-to-physical address translation, the exception control system, the processor's diagnostics capability, the operating modes (Kernel, User and Debug) and whether interrupts are enabled or disabled. These configuration options and other system information are available by accessing the CP0 registers listed in Table 3-2.

3.3 Power Management

The processor core offers a number of power management features, including low-power design, active power management and Power-Down modes of operation. The core is a static design that supports slowing or halting of the clocks, which reduces system power consumption during Idle periods.

The mechanism for invoking Power-Down mode is implemented through execution of the WAIT instruction, used to initiate Sleep or Idle. The majority of the power consumed by the processor core is in the clock tree and clocking registers. The PIC32MM family makes extensive use of local gated clocks to reduce this dynamic power consumption.

3.4 EJTAG Debug Support

The microAptiv UC core has an Enhanced JTAG (EJTAG) interface for use in the software debug. In addition to the standard mode of operation, the microAptiv UC core provides a Debug mode that is entered after a debug exception (derived from a hardware breakpoint, single-step exception, etc.) is taken and continues until a Debug Exception Return (DERET) instruction is executed. During this time, the processor executes the debug exception handler routine.

The EJTAG interface operates through the Test Access Port (TAP), a serial communication port used for transferring test data in and out of the microAptiv UC core. In addition to the standard JTAG instructions, special instructions defined in the EJTAG specification specify which registers are selected and how they are used.

3.5 MIPS32® microAptiv™ UC Core Configuration

Register 3-1 through Register 3-4 show the default configuration of the microAptiv UC core, which is included on PIC32MM0256GPM064 family devices.

REGISTER 3-1: CONFIG: CONFIGURATION REGISTER; CP0 REGISTER 16, SELECT 0

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	R/W-0	R/W-1	R/W-0	R/W-0	R/W-1	R/W-0	r-0
	—	K23<2:0>			KU<2:0>(1)			—
23:16	r-0	R-0	R-1	R-0	r-0	r-0	r-0	R-1
	—	UDI	SB	MDU	—	—	—	DS
15:8	R-0	R-0	R-0	R-0	R-0	R-1	R-0	R-1
	BE	AT<1:0>		AR<2:0>			MT<2:1>	
7:0	R-1	r-0	r-0	r-0	r-0	R/W-0	R/W-1	R/W-0
	MT<0>	—	—	—	—	K0<2:0>		

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the CONFIG1 register

bit 30-28 **K23<2:0>:** Cacheability of the kseg2 and kseg3 Segments bits
010 = Cache is not implemented

bit 27-25 **KU<2:0>:** Cacheability of the kuseg and useg Segments bits(1)
010 = Cache is not implemented

bit 24-23 **Reserved:** Must be written as zeros; returns zeros on reads

bit 22 **UDI:** User-Defined bit
0 = CorExtend user-defined instructions are not implemented

bit 21 **SB:** SimpleBE bit
1 = Only Simple Byte Enables are allowed on the internal bus interface

bit 20 **MDU:** Multiply/Divide Unit bit
0 = Fast, high-performance MDU

bit 19-17 **Reserved:** Must be written as zeros; returns zeros on reads

bit 16 **DS:** Dual SRAM Interface bit
1 = Dual instruction/data SRAM interface

bit 15 **BE:** Endian Mode bit
0 = Little-endian

bit 14-13 **AT<1:0>:** Architecture Type bits
00 = MIPS32®

bit 12-10 **AR<2:0>:** Architecture Revision Level bits
001 = MIPS32 Release 2

bit 9-7 **MT<2:0>:** MMU Type bits
011 = Fixed mapping

bit 6-3 **Reserved:** Must be written as zeros; returns zeros on reads

bit 2-0 **K0<2:0>:** kseg0 Coherency Algorithm bits
010 = Cache is not implemented

Note 1: The KU<2:0> bits are not usable as this device does not support User mode.

REGISTER 3-2: CONFIG1: CONFIGURATION REGISTER 1; CP0 REGISTER 16, SELECT 1

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-1	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	R-1	R-0	R-0	R-1	R-0
	—	—	—	PC	WR	CA	EP	FP

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired to '1' to indicate the presence of the CONFIG2 register

bit 30-5 **Unimplemented:** Read as '0'

bit 4 **PC:** Performance Counter bit
1 = The processor core contains performance counters

bit 3 **WR:** Watch Register Presence bit
0 = No Watch registers are present

bit 2 **CA:** Code Compression Implemented bit
0 = No MIPS16e® are present

bit 1 **EP:** EJTAG Present bit
1 = Core implements EJTAG

bit 0 **FP:** Floating Point Unit bit
0 = Floating point unit is not implemented

REGISTER 3-3: CONFIG3: CONFIGURATION REGISTER 3; CP0 REGISTER 16, SELECT 3

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	r-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	R-0	R-1	R-0	R-0	R-0	R-1	R-1
	—	IPLW<1:0>		MMAR<2:0>			MCU	ISAONEXC
15:8	R-0	R-1	R-1	R-1	U-0	U-0	U-0	R-0
	ISA<1:0>		ULRI	RXI	—	—	—	ITL
7:0	U-0	R-1	R-1	R-0	R-1	U-0	U-0	R-0
	—	VEIC	VINT	SP	CDMM	—	—	TL

Legend:	r = Reserved bit	y = Value set from Configuration bits on POR
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 31 **Reserved:** This bit is hardwired as '0'

bit 30-23 **Unimplemented:** Read as '0'

bit 22-21 **IPLW<1:0>:** Width of the Status IPL and Cause RIPL bits
01 = IPL and RIPL bits are 8 bits in width

bit 20-18 **MMAR<2:0>:** microMIPS™ Architecture Revision Level bits
000 = Release 1

bit 17 **MCU:** MIPS® MCU ASE Implemented bit
1 = MCU ASE is implemented

bit 16 **ISAONEXC:** ISA on Exception bit
1 = microMIPS is used on entrance to an exception vector

bit 15-14 **ISA<1:0>:** Instruction Set Availability bits
01 = Only microMIPS is implemented

bit 13 **ULRI:** UserLocal Register Implemented bit
1 = UserLocal Coprocessor 0 register is implemented

bit 12 **RXI:** RIE and XIE Implemented in PageGrain bit
1 = RIE and XIE bits are implemented

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **ITL:** Indicates that iFlowtrace™ Hardware is Present bit
0 = The iFlowtrace hardware is not implemented in the core

bit 7 **Unimplemented:** Read as '0'

bit 6 **VEIC:** External Vector Interrupt Controller bit
1 = Support for an external interrupt controller is implemented.

bit 5 **VINT:** Vector Interrupt bit
1 = Vector interrupts are implemented

bit 4 **SP:** Small Page bit
0 = 4-Kbyte page size

bit 3 **CDMM:** Common Device Memory Map bit
1 = CDMM is implemented

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TL:** Trace Logic bit
0 = Trace logic is not implemented

REGISTER 3-4: CONFIG5: CONFIGURATION REGISTER 5; CP0 REGISTER 16, SELECT 5

Bit Range	Bit 31/23/15/7	Bit 30/22/14/6	Bit 29/21/13/5	Bit 28/20/12/4	Bit 27/19/11/3	Bit 26/18/10/2	Bit 25/17/9/1	Bit 24/16/8/0
31:24	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
23:16	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
15:8	U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
	—	—	—	—	—	—	—	—
7:0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	R-1
	—	—	—	—	—	—	—	NF

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 31-1 **Unimplemented:** Read as '0'

bit 0 **NF:** Nested Fault bit

1 = Nested Fault feature is implemented

4.0 MEMORY ORGANIZATION

PIC32MM microcontrollers provide 4 GBytes of unified virtual memory address space. All memory regions, including program memory, data memory, SFRs and Configuration registers, reside in this address space at their respective unique addresses. The data memory can be made executable, allowing the CPU to execute code from data memory.

Key features include:

- 32-Bit Native Data Width
- Separate Boot Flash Memory (BFM) for Protected Code
- Robust Bus Exception Handling to Intercept Runaway Code
- Simple Memory Mapping with Fixed Mapping Translation (FMT) Unit

The PIC32MM0256GPM064 family devices implement two address spaces: virtual and physical. All hardware resources, such as program memory, data memory and peripherals, are located at their respective physical addresses. Virtual addresses are exclusively used by the CPU to fetch and execute instructions. Physical addresses are used by peripherals, such as Flash controllers, that access memory independently of the CPU.

The virtual address space is divided into two segments of 512 Mbytes each, labeled kseg0 and kseg1. The Program Flash Memory (PFM) and Data RAM Memory (DRM) are accessible from either kseg0 or kseg1, while the Boot Flash Memory (BFM) and peripheral SFRs are accessible only from kseg1.

The Fixed Mapping Translation (FMT) unit translates the memory segments into corresponding physical address regions. Figure 4-1 through Figure 4-3 illustrate the fixed mapping scheme, implemented by the PIC32MM0256GPM064 family core, between the virtual and physical address space.

The mapping of the memory segments depends on the CPU error level, set by the ERL bit in the CPU STATUS register. Error level is set (ERL = 1) by the CPU on a Reset, Soft Reset or Non-Maskable Interrupt (NMI). In this mode, the CPU can access memory by the physical address. This mode is provided for compatibility with other MIPS processor cores that use a TLB-based MMU. The C start-up code clears the ERL bit to zero, so that when application software starts up, it sees the proper virtual to physical memory mapping.

4.1 Alternate Configuration Bits Space

Every Configuration Word has an associated Alternate Word (designated by the letter A as the first letter in the name of the word). During device start-up, Primary Words are read, and if uncorrectable ECC errors are found, the BCFGERR (RCON<27>) flag is set and Alternate Words are used. If uncorrectable ECC errors are found in Primary and Alternate Words, the BCFGFAIL (RCON<26>) flag is set, and the default configuration is used. The Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. The Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768.

4.2 Bus Matrix (BMX)

The BMX is a switch fabric that connects the system bus initiators (Flash controller, CPU instruction, CPU data, system DMA and USB) to bus targets (RAM, Flash and peripherals without integrated DMA). All data and instructions are transferred through this bus. Only one initiator can connect to a given target at a time. Multiple initiators can be active at one time provided each one has a separate target. Multiple priority modes (Round Robin, Fixed CPU Highest and Fixed CPU Lowest) are available to allow the priority to be tailored to the application needs. Mode 0 is a Fixed Priority mode with the CPU having the highest priority (refer to Table 4-1). For most applications, this mode should be sufficient; however, it is possible for the CPU to generate sufficient bus traffic to 'starve' the other initiators attempting to access Flash memory, preventing them from performing transfers in the required time limit. If this 'starvation' occurs, the Round Robin or CPU Lowest mode should be chosen.

Mode 1 is a Fixed Priority mode with the CPU having the lowest priority (refer to Table 4-1). This mode can reduce the latency of DMA transfers because the DMA engines have a higher priority than the CPU.

Mode 2 is a Round Robin or Rotating Priority mode. The initiator's priority for each target rotates with every access. This ensures, not that the initiator is starved, but the latency for accesses changes with every access; this makes the latency variable.

The Arbitration mode is selected by the BMXARB<1:0> bits (CFGCON<25:24>).

Note:	The CPU has two initiators: one for data and the other for instructions. In all Arbitration modes, the CPU data initiator has higher priority than the CPU instruction initiator.

TABLE 4-1: FIXED MODES ORDER OF PRIORITY

Mode 1	Mode 0
CPU Lowest	**CPU Highest**
Highest Priority	
Flash Controller	Flash Controller
DMA	CPU
USB	USB
CPU	DMA
Lowest Priority	

Note: The Arbitration mode chosen only has an effect on system performance when a contention for a target occurs.

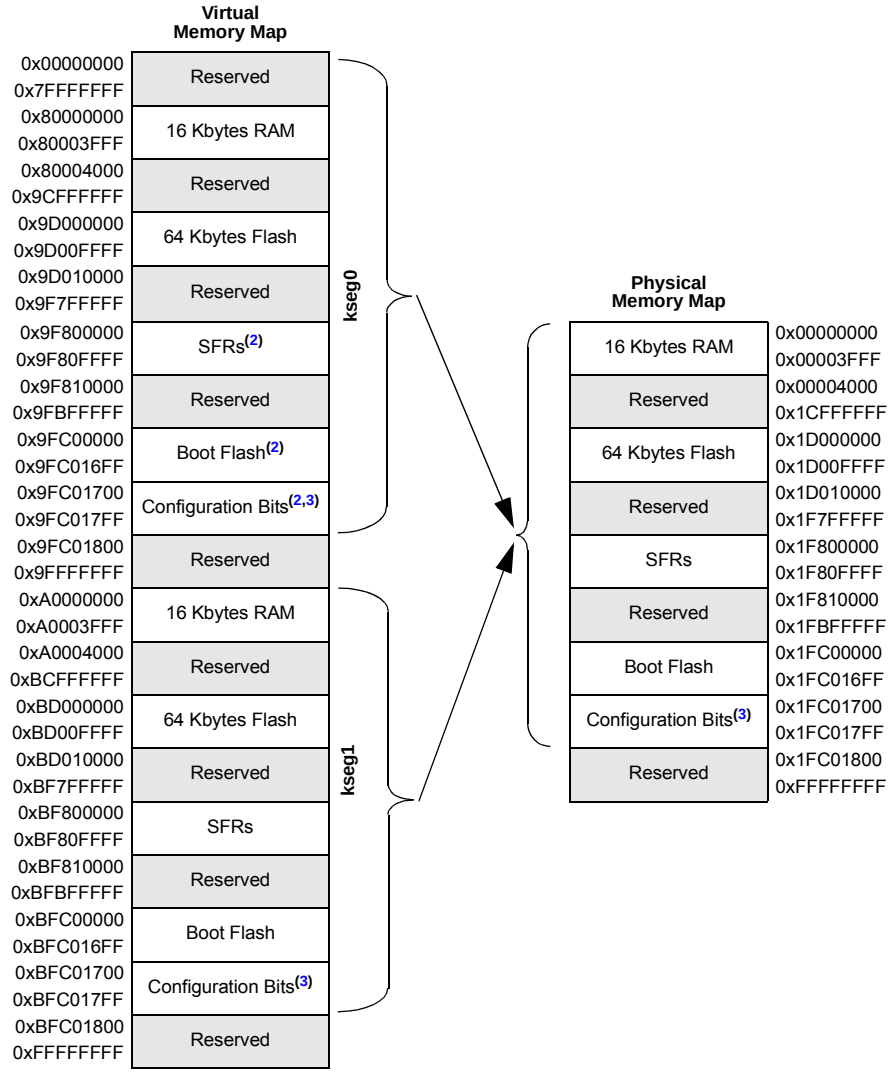
The Flash controller, when programming memory, always has the highest priority regardless of the priority mode setting.

Refer to **Section 48. "Memory Organization and Permissions"** (DS60001214) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32) for more information regarding Bus Matrix operation.

4.3 Flash Line Buffer

The Flash line buffer is a buffer that resides between the Bus Matrix and the Flash memory. When a Flash fetch is generated, an aligned double word (64 bits) is read. This is then placed in the Flash line buffer. If the next initiator requested address's data is contained in the Flash line buffer, it is read directly without requiring another Flash fetch; if it is not in the Flash line buffer, a Flash fetch is generated.

FIGURE 4-1: MEMORY MAP FOR DEVICES WITH 64 Kbytes OF PROGRAM MEMORY(1)

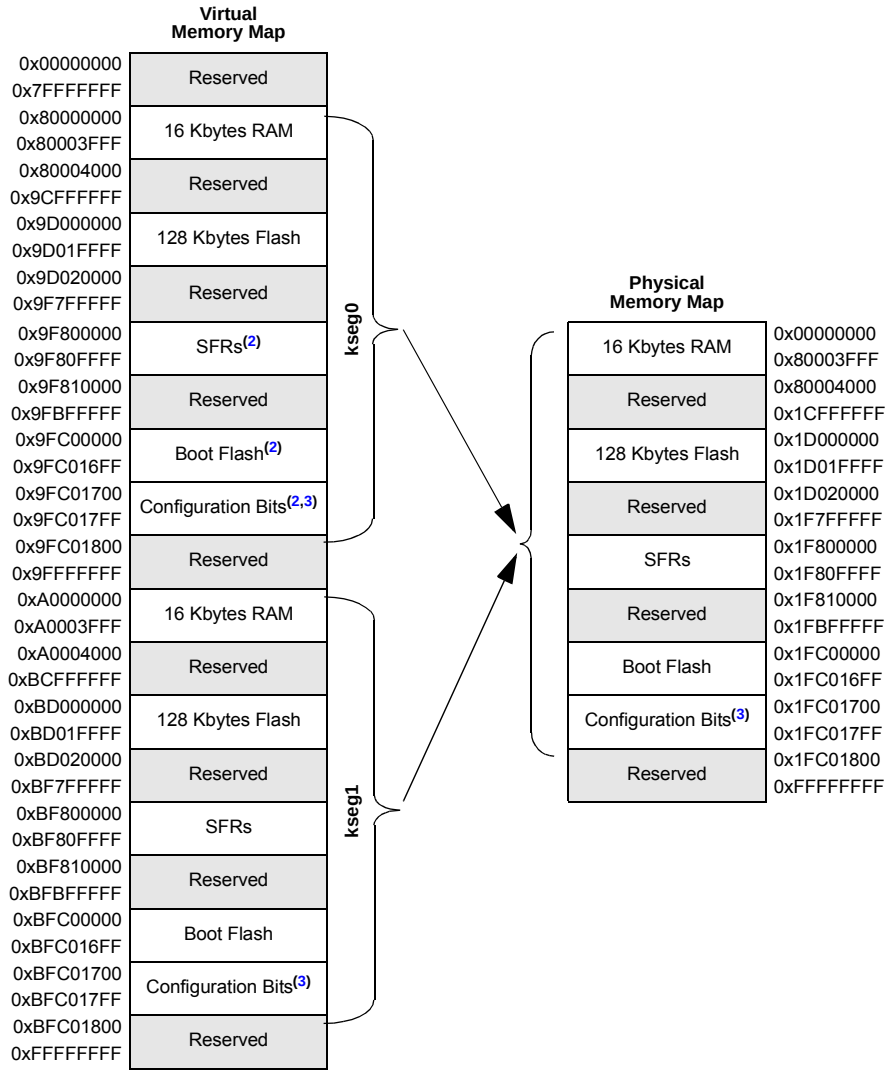


Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

FIGURE 4-2: MEMORY MAP FOR DEVICES WITH 128 Kbytes OF PROGRAM MEMORY(1)



Note 1: Memory areas are not shown to scale.

2: This region should be accessed from kseg1 space only.

3: Primary Configuration bits' area is located at the address range, from 0x1FC01780 to 0x1FC017E8. Alternate Configuration bits' area is located at the address range, from 0x1FC01700 to 0x1FC01768. Refer to **Section 4.1 "Alternate Configuration Bits Space"** for more information.

5.0 FLASH PROGRAM MEMORY

Note: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32). The information in this data sheet supersedes the information in the FRM.

PIC32MM0256GPM064 family devices contain an internal Flash program memory for executing user code. The program and Boot Flash can be write-protected. The erase page size is 512 32-bit words. The program row size is 64 32-bit words. The memory can be programmed by rows or by two 32-bit words, called double-words.

Note: Double-words must be 64-bit aligned.

The devices implement a 6-bit Error Correcting Code (ECC). The memory control block contains a logic to write and read ECC bits to and from the Flash memory. The Flash is programmed at the same time as the corresponding ECC bits. The ECC provides improved resistance to Flash errors. The ECC single-bit error generates an interrupt and can be transparently corrected. The ECC double-bit error results in a bus error exception.

There are three methods by which the user can program this memory:

- Run-Time Self-Programming (RTSP)
- EJTAG Programming
- In-Circuit Serial Programming™ (ICSP™)

RTSP is performed by software executing from either Flash or RAM memory. Information about RTSP techniques is described in **Section 5. "Flash Programming"** (DS60001121) in the *"PIC32 Family Reference Manual"*. EJTAG programming is performed using the JTAG port of the device. ICSP programming requires fewer connections than for EJTAG programming. The EJTAG and ICSP methods are described in the *"PIC32 Flash Programming Specification"* (DS60001145), which is available for download from the Microchip web site.

5.1 Flash Controller Registers Write Protection

The NVMPWP and NVMBWP registers, and the WR bit in the NVMCON register are protected (locked) from an accidental write. Each time a special unlock sequence is required to modify the content of these registers or bits. To unlock, the following steps should be done:

1. Disable interrupts prior to the unlock sequence.
2. Execute the system unlock sequence by writing the key values of 0xAA996655 and 0x556699AA to the NVMKEY register.
3. Write the new value to the required bits.
4. Re-enable interrupts.
5. Relock the system.

Refer to Example 5-1.

EXAMPLE 5-1:

```
// unlock sequence
NVMKEY = AA996655;
NVMKEY = 556699AA;


// relock
NVMKEY = 0;
```

8.0 DIRECT MEMORY ACCESS (DMA) CONTROLLER

Note 1: This data sheet summarizes the features of the PIC32MM0256GPM064 family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **Section 31. "DMA Controller"** (DS60001117) in the *"PIC32 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com/PIC32).

The Direct Memory Access (DMA) Controller is a bus master module useful for data transfers between peripherals and memory without CPU intervention. The source and destination of a DMA transfer can be any of the memory-mapped modules, that do not have a dedicated DMA, existent in the PIC32 (such as SPI, UART, PMP, etc.) or the memory itself.

The following are some of the key features of the DMA Controller module:

- Four Identical Channels, Each Featuring:
  - Auto-Increment Source and Destination Address registers
  - Source and Destination Pointers
  - Memory to memory and memory to peripheral transfers
- Automatic Word Size Detection:
  - Transfer granularity, down to byte level
  - Bytes need not be word-aligned at source and destination
- Fixed Priority Channel Arbitration
- Flexible DMA Channel Operating modes:
  - Manual (software) or automatic (interrupt) DMA requests
  - One-Shot or Auto-Repeat Block Transfer modes
  - Channel-to-channel chaining
- Flexible DMA Requests:
  - A DMA request can be selected from any of the peripheral interrupt sources
  - Each channel can select any (appropriate) observable interrupt as its DMA request source
  - A DMA transfer abort can be selected from any of the peripheral interrupt sources
  - Pattern (data) match transfer termination
- Multiple DMA Channel Status Interrupts:
  - DMA channel block transfer complete
  - Source empty or half empty
  - Destination full or half full
  - DMA transfer aborted due to an external event
  - Invalid DMA address generated
- DMA Debug Support Features:
  - Most recent address accessed by a DMA channel
  - Most recent DMA channel to transfer data
- CRC Generation module:
  - CRC module can be assigned to any of the available channels
  - CRC module is highly configurable
- User Selectable Bus Arbitration Priority (refer to **Section 4.2 "Bus Matrix (BMX)"**)
- 8 System Clocks Per Cell Transfer

FIGURE 8-1: DMA BLOCK DIAGRAM