

YUN-RONG (LAUREN) LUO

✉ yunrong@umich.edu | 🌐 <https://lauren-yrluo.github.io>

RESEARCH INTEREST

Formal methods and verification, programming languages, model checking and satisfiability, interactive theorem proving

EDUCATION

University of Michigan, Ann Arbor <i>Ph.D. Candidate in Computer Science and Engineering</i>	Ann Arbor, MI, USA 08/2023-Present
• Research Advisor: Prof. Manos Kapritsos	
National Taiwan University (NTU) <i>M.S. in Electronics Engineering</i>	Taipei, Taiwan 09/2021-2023

- Research Advisor: Prof. Jie-Hong Roland Jiang

<i>B.S. in Electrical Engineering</i>	09/2017-06/2021
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SELECTED PUBLICATIONS

Conference

1. **Yun-Rong Luo**, Aman Goel, Karem Sakallah, "QSM-Cutoff: Systematic Derivation of Quantified Cutoff Formulas for Distributed Protocols.", 2025 International Conference on Computer Aided Verification (CAV), 2025 [[link](#)]
2. Che Cheng*, **Yun-Rong Luo***, Jie-Hong Roland Jiang, "Knowledge Compilation for Incremental and Checkable Stochastic Boolean Satisfiability." 2024 International Joint Conference on Artificial Intelligence (IJCAI), 2024 [[link](#)]
3. Yu-Neng Wang*, **Yun-Rong Luo***, Po-Chun Chien*, Ping-Lun Wang, Hao-Ren Wang, Wan-Hsuan Lin, Jie-Hong Roland Jiang, Chung-Yang Ric Huang, "Compatible Equivalence Checking of X-Valued Circuits." 2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2021 [[link](#)]

Journal

1. **Yun-Rong Luo***, Che Cheng*, Jie-Hong Roland Jiang, "A Resolution Proof System for Dependency Stochastic Boolean Satisfiability." Journal of Automated Reasoning, 2023 [[link](#)]

HONORS AND AWARDS

2021 Research Creativity Award, Ministry of Science and Technology of Taiwan (awarded to 200/3000+ research works)

2020 1st Place, Problem A, 2020 CAD Contest at ICCAD (186 teams competed in 3 problems)

2020 College Student Research Scholarship, Ministry of Science and Technology of Taiwan

TEACHING EXPERIENCE

EECS 376: Foundations of Computer Science (UMich)

Graduate Student Instructor 05/2025-06/2025

EECS 270: Introduction to Logic Design (UMich)

Graduate Student Instructor 08/2024-04/2025

Logic Synthesis and Verification (NTU)

Teaching Assistant 09/2021-01/2022

WORK EXPERIENCE

Cadence Design Systems

R&D Intern, Formal Verification Team Hsinchu, Taiwan

07/2020-09/2020

SKILLS

Languages Mandarin (Native), English (Proficient, TOEFL: 114/120)

Programming Languages C/C++, Python, OCaml, Verilog

Tools Shell scripting, Git, \LaTeX

Verification Tools [Dafny](#), SAT/SMT solvers,