

YUN-RONG (LAUREN) LUO

+1-774-991-9349 | yunrong@umich.edu | <https://lauren-yrluo.github.io>

RESEARCH

Current Topic Analyze the **security** of **distributed protocols** using **formal methods**.

General Interest Software/hardware model checking, Satisfiability (SAT, QBF, SMT), proof systems and proof complexity.

EDUCATION

University of Michigan, Ann Arbor

Ph.D. in Computer Science and Engineering

• Research Advisor: Prof. Karem Sakallah

Ann Arbor MI, USA

08/2023-Present

National Taiwan University (NTU)

M.S. in Electronics Engineering

• Research Advisor: Prof. Jie-Hong Roland Jiang

Taipei, Taiwan

09/2021-2023

B.S. in Electrical Engineering

09/2017-06/2021

PUBLICATIONS

- Yun-Rong Luo**, Aman Goel, Karem Sakallah, "FoRSMIn: Systematic Derivation of Reachability Invariants for Distributed Protocols." (In submission)
- Yun-Rong Luo**, Aman Goel, Karem Sakallah, "SAT-Based Quantified Symmetric Minimization of the Reachable States of Distributed Protocols: An Update." 2024 International Symposium On Leveraging Applications of Formal Methods, Verification and Validation (ISoLA), 2024 [\[link\]](#)
- Che Cheng*, **Yun-Rong Luo***, Jie-Hong Roland Jiang, "Knowledge Compilation for Incremental and Checkable Stochastic Boolean Satisfiability." 2024 International Joint Conference on Artificial Intelligence (IJCAI), 2024 [\[link\]](#)
- Yun-Rong Luo***, Che Cheng*, Jie-Hong Roland Jiang, "A Resolution Proof System for Dependency Stochastic Boolean Satisfiability." Journal of Automated Reasoning, 2023 [\[link\]](#)
- Yu-Neng Wang*, **Yun-Rong Luo***, Po-Chun Chien*, Ping-Lun Wang, Hao-Ren Wang, Wan-Hsuan Lin, Jie-Hong Roland Jiang, Chung-Yang Ric Huang, "Compatible Equivalence Checking of X-Valued Circuits." 2021 IEEE/ACM International Conference On Computer Aided Design (ICCAD), 2021 [\[link\]](#)

SOFTWARE PROJECTS

I am the primary designer of:

- FoRSMIn: an inductive invariant synthesizer for distributed protocols using forward reachability and logic minimization.
- [cert-SSAT](#): a toolchain for certifying results of a stochastic Boolean satisfiability (SSAT) solver.

I contributed to:

- [SharpSSAT](#): a state-of-the-art stochastic Boolean satisfiability (SSAT) solver.

HONORS AND AWARDS

2021 Research Creativity Award, Ministry of Science and Technology of Taiwan (awarded to 200/3000+ research works)

2020 1st Place, Problem A, 2020 CAD Contest at ICCAD (186 teams competed in 3 problems)

2020 College Student Research Scholarship, Ministry of Science and Technology of Taiwan

TEACHING EXPERIENCE

EECS 270: Introduction to Logic Design (UMich)

Graduate Student Instructor

09/2024-12/2024

Logic Synthesis and Verification (NTU)

Teaching Assistant

09/2021-01/2022

WORK EXPERIENCE

Cadence Design Systems

R&D Intern, Formal Verification Team

Hsinchu, Taiwan

07/2020-09/2020

SKILLS

Natural Languages Mandarin (Native), English (Proficient, TOEFL: 114/120)

Programming Languages C/C++, Python, Verilog, Shell scripting, Git, \LaTeX

Tools SAT/SMT solvers, [IVy](#), [Berkeley ABC system](#)