SPINTRONICS

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I. INTRODUCTION

Spintronics is a field of electronics that uses the spin of particles, primarily electrons, to store information [1]. This overview of spintronics will focus on the fundamentals needed to understand spintronics and the applications of spintronics devices. This paper will first review the underlying principles of spintronics: beginning with electron spin and its relationship to magnetism and electron transport. Electron spin will then be used to understand the magnetoresistance phenomena. Two types of magnetoresistance will be discussed in detail: giant magnetoresistance and tunneling magnetoresistance.

Next, electron-spin based devices will be discussed. This begins with spin-valves, which are magnetoresistance-based current valves. Novel spin-based transistors (spin-FETs) and their structure, function, applications, and benefits/costs will be discussed and compared to traditional charge-based transistors. Magnetoresistance Random Access Memory (MRAM), a promising spin-based memory system, will then be reviewed, with an emphasis on its implementation, write/read functionality, and relationship to traditional random-access memories. Three variant implementations of MRAMs will then be discussed in order of oldest to newest technology: field-write, toggle switching, and spin-transfer torque MRAMs. Next, hybrid MTJ-CMOS circuits—specifically, nonvolatile hybrid memory cells—will be discussed. Finally, two applications of these nonvolatile SRAM cells will be examined: nonvolatile-input combinational circuits and reconfigurable combinational circuits. Lastly, future directions for each of these spintronics devices will be discussed.

II. FUNDAMENTALS

The key physical properties that are most relevant to spintronics are the charge and spin of electrons. These concepts will be reviewed and then applied to explain magnetoresistance, a phenomenon that is at the heart of spintronics.

Electron Spin

Electron spin is the intrinsic angular momentum of electrons [2] which is "independent of any translational or orbital motion" [3]. It was discovered via the Stern-Gerlach Experiment [2], which showed that when orbital angular momentum is zero, electrons still display an internal angular momentum of $\pm\frac{\hbar}{2}$.

Angular momentum is quantized. From a long derivation involving the Schrodinger Equation, this can be derived. As shown in Equations 1 and 2, angular momentum (with magnitude $|L|$) and z-projection (L_z) is quantized due to its dependence on discrete quantum numbers [2].

$$|L| = \hbar\sqrt{l(l+1)} \quad (1)$$

$$L_z = m_l\hbar \quad (2)$$

Where l is the angular momentum quantum number with $l = 0, 1, 2, 3$ ..

m_s is the magnetic quantum number with $m_s = -l, -l+1, \dots, 0, \dots, l-1, l$

Electron spin, as a type of angular momentum, is thus quantized. As expressed by Equations 3 and 4, the spin vector can be expressed as having a magnitude of $|S|$ and z-projection S_z [2].

$$|S| = \hbar\sqrt{s(s+1)} \quad (3)$$

$$S_z = m_s\hbar \quad (4)$$

Where s is the spin quantum number with $s = 1/2$

m_s is the spin projection quantum number with $m_s = -s, -s+1, \dots, 0, \dots, s-1$

Where, for electrons, $s = \pm\frac{1}{2}$

These expressions for |S| and S_z give rise to 2 possible spin orientations for the electron; one with $S_z = +\frac{\hbar}{2}$ and one with $S_z = -\frac{\hbar}{2}$, which is consistent with experimental data. When a single electron is considered, it is labelled up-spin if $S_z = +\frac{\hbar}{2}$ and down-spin if $S_z = -\frac{\hbar}{2}$. [3]

Electron Spin, Magnetism, and Electron Transport

Electron spin relates to magnetism. For individual atoms, "uncompensated electron spins are the reason why individual atoms possess local magnetic moments" [4]. Electrons with different spins have magnetic moments pointing in different directions.

Magnetism's relationship to electron spin also carries into the macroscopic scale; the electron spin of constituent atoms affects the magnetic properties of materials. In materials, electrons that have spin magnetic moment along the direction of total (net) magnetic moment of the material are called majority spin or up-spin spin [3]. Other electrons that have spin moments opposite the total moment are called minority spin or down-spin [3]. In paramagnetic materials, there is the same number of up-spin electrons as down-spin electrons. Subsequently, paramagnetic moments have no net magnetic moment. In contrast, ferromagnetic materials have a net difference between the number of up-spin and down-spin electrons [4]. This net difference creates a magnetic moment in the direction that the majority of electron spins.

Due to ferromagnets' net magnetic moment, complex properties arise that affect electrical transport [4]: these properties are characterized as spin polarized transport.

Electrical transport is essentially the movement of free carriers in materials. Free carriers are defined as the "electrons in the conduction band and holes in the valence band" of materials [5]. Free carriers have the ability to carry electrical current [5]; electrical transport is therefore instrumental to understanding and controlling flow of electrical current, which is essential to both modern day electronics and spintronics.

Spin Polarized Transport

Magnetism's effect on electrical transport manifests in a phenomenon called spin polarized transport. Spin polarized transport is when there is an imbalance of spins of a material's constituent atoms that makes the material "spin polarized." Since only ferromagnets have unequal amounts of up and down-spin electrons, spin polarized transport occurs in ferromagnets and not in paramagnets.

Spin polarized transport was characterized by Mott using the two-current model [4]. When temperature is sufficiently low, it has been discovered that "electrons of majority and

minority spin, with magnetic moment parallel and antiparallel to the magnetization of a ferromagnet, respectively, do not mix in the scattering processes [1]. Recalling that these two types of electrons—ones with magnetic moment parallel and antiparallel to the ferromagnet total magnetization—are up-spin and down-spin electrons, respectively, it follows that the total current resulting from the movement of these electrons can be expressed as a sum of two completely independent currents [1,4]. One current arises due to movement of the up-spin electrons, and the other, due to that of the down-spin electrons.

The two-current model allows us to create an equivalent model for electron transport. Using this model, current flow can be represented as two separate, modifiable, and often different paths because up-spin and down-spin electrons are affected in different ways by the magnetic properties of the materials they travel through. This model will be particularly useful in understanding current-in-plane giant magnetoresistance, which will be discussed soon.

Magnetoresistance

Magnetoresistance (MR) is defined as a "change in the resistance of a material or structure caused by the application of a magnetic field" [3].

It can be expressed quantitatively, as shown in Equation 5 [4].

$$MR = \frac{R_H - R_0}{R_H} \quad (5)$$

Where R_H = resistance of sample with applied magnetic field

R_0 = resistance of sample without applied magnetic field

Different types of magnetoresistance are classified by the different physical phenomena that cause them. Spintronics primarily utilizes two forms of magnetoresistance: giant magnetoresistance (GMR) and tunneling magnetoresistance (TMR).

The most basic material configuration in which these two types of magnetoresistance occur are three-layer structures. These structures are composed of two ferromagnetic regions separated by one nonmagnetic region [3]. GMR and TMR will be explained in reference to these classical these three-layer structures. In GMR, this nonmagnetic region is a metal; in contrast, in TMR, the separating material is insulating, but thin enough to allow electrons to move between the two ferromagnetic regions via quantum tunneling [3].

Giant Magnetoresistance

GMR is magnetoresistance that occurs in ferromagnetic-metallic-ferromagnetic multilayer structures. In these multilayer structures, GMR results in resistance being "high when the spins in the ferromagnetic layers are anti-parallel and drops to low when the spins are parallel" [6].

GMR allows one to use magnetic fields to control electrical resistance. If a magnetic field is applied that forces the magnetization of ferromagnetic layers in one direction, resistance decreases significantly [3].

In a manner analogous to MR, GMR can be described quantitatively, as shown in Equation 6 [7].

$$GMR = \frac{\Delta R}{R_P} = \frac{R_{AP} - R_P}{R_P} \quad (6)$$

Where

R_P = resistance of structure with parallel magnetization
R_{AP}= resistance of structure with antiparallel magnetization

There are 2 three-layer implementations of GMR: current-in-plane (CIP) and current-perpendicular-to-plane (CPP). These two implementations differ due to direction of flow of current; "for the CIP implementation, the electric current flows parallel to the layers, and for the CPP implementation, the electric current flows perpendicular to the layers" [3].

Current-perpendicular-to-plane GMR

GMR in CPP implementations can be explained by examining how electron transport is affected by magnetic fields. At a high level, CPP GMR occurs due to the difference in spin scattering in layers with different net magnetizations [7].

Using Mott's two-current model, one can model the 3-layer structure as a circuit of two parallel branches, one for up-spin and one for down-spin electron travel. By electron scattering principles, when an electron travels through a ferromagnetic layer with the same net magnetization as its own moment, it experiences less scattering than an electron with opposing net magnetization would [7]. This means that this situation can be modelled with a small resistance in the electron's path [7]. When the electron travels through a ferromagnetic layer with opposing net magnetization to its own moment, it experiences strong scattering [8] and is accordingly modelled by a large resistance. It follows that "when the magnetizations of the ferromagnetic layers are parallel, the equivalent circuit has resistors with small resistance in series in one branch, and large resistance in the other. When the magnetizations of the layers alternate their directions, the parallel circuits contain both large and small resistors" [7].

Therefore, in the parallel ferromagnet configuration, up-spin electrons encounter low path resistance, and down-spin electrons encounter high path resistance. In antiparallel ferromagnet configuration, up-spin and down-spin electrons encounter the same, intermediate amount of resistance. Since the majority of electrons have up-spin, by definition, the parallel ferromagnet configuration allows for more electrons to flow, resulting in a higher conductivity and a lower resistance [8].

Current-in-plane GMR

GMR in CIP implementations is primarily attributed to nonlocal conductivity in inhomogeneous solids. If the same two-current model was applied to the CIP implementation without consideration of nonlocal conductivity, the antiparallel and parallel configurations would have equal conductivities (See proof in [30]) and there would be no magnetoresistance. Assuming nonlocal conductivity in a CIP structure signifies that the "current within each layer has a contribution due to the field in other layers" which "depends on the [magnetic] moment and orientation" of other layers [30]. The current within each layer (and thus, conductivity) is dependent on the applied magnetic moment, which is the definition of GMR.

Tunneling Magnetoresistance

TMR is a form of magnetoresistance that occurs in ferromagnet-insulator-ferromagnet structures. These types of structures can also be referred to as magnetic tunnel junctions (MTJs).

TMR was discovered and first modelled by Jullière. Jullière's theory has the following key points: 1) tunneling magnetoresistance is determined by the spin of electrons in the ferromagnetic layers and 2) the spin of electrons that preserved before, during, and after tunneling [3].

TMR can be understood by examining the possible tunneling patterns possible in antiparallel and parallel 3-layer ferromagnet-insulator-ferromagnet structures. Broadly, TMR is caused by differences in tunneling probabilities between up-spin and down-spin electrons [7].

When the two ferromagnetic layers have magnetic moments that are in parallel, "the electrons with majority-spin in one ferromagnetic electrode will tunnel into the unoccupied majority-spin sub-band in the other ferromagnetic electrode" [3]. The electrons that have minority spin will also tunnel, but into the "unoccupied state of minority-spin sub-band [3]". Since both minority and majority spin electrons can tunnel from one ferromagnetic layer to the other, tunnel resistance is low.

However, when the ferromagnetic layers have anti-parallel magnetic moments, the "electrons of majority-spin sub-band in one ferromagnetic electrode can only tunnel into the unoccupied state of minority-spin sub-band in other electrode and the electrons in minority-spin sub-band will only tunnel into the unoccupied state of majority-spin sub-band" [3]. This means that in these structures, electrons are able to tunnel more easily when the ferromagnetic layers are antiparallel than when they are parallel [8].

Quantitatively, TMR can be described by Equation 7 [3].

$$TMR = \frac{G_P - G_{AP}}{G_P} = \frac{2P_1P_2}{1-P_1P_2} \quad (7)$$

Where

G_P = conductance of structure with parallel magnetization

G_{AP}= conductance of structure with antiparallel magnetization

P_i = spin polarization of ferromagnetic layer i

$$P_i = \frac{D_{i\uparrow} - D_{i\downarrow}}{D_{i\uparrow} + D_{i\downarrow}}$$

$D_{i\uparrow}$ = density of states at Fermi level for majority spins

$D_{i\uparrow}$ = density of states at Fermi level for minority spins

Where density of states is the proportion of states that are occupied by the system at a given energy

III. APPLICATIONS

Multiple applications of spintronics concepts will be discussed in this section, such as spin-valves, spin-FETs, magnetoresistive random-access memory, and hybrid MTJ-CMOS nonvolatile logic. The previously discussed concepts of giant magnetoresistance and tunneling magnetoresistance will be relevant to understanding how these spintronics devices function. Spin-valves are an example of a GMR-based device, while magnetoresistive random-access memory and hybrid MTJ-CMOS logic are examples of tunneling magnetoresistance-based devices. Spin-FETs, on the other hand, are spin-polarized current based devices.

Spin-valves

Spin valves are simple GMR-based devices. Spin valves consist of the classic 3-layer ferromagnetic-metallic-ferromagnetic structure. One of the ferromagnetic layers is the "pinned

layer" and the other is the "free layer;" in the pinned layer, magnetization is relatively independent of applied magnetic field while in the free layer, magnetization is changeable by applying a small magnetic field [8]. The pinned ferromagnetic layer is "pinned" by connecting it to an antiferromagnetic layer; the interface between these two layers helps resist the changes due to magnetization [8].

In these 3-layer structures, GMR occurs. This results in a high resistance when the ferromagnetic layers are magnetized antiparallel to each other and a low resistance when they are parallel. If the free layer magnetization is parallel to the pinned layer, the valve opens and electrons flow; if it is antiparallel to the pinned layer, the valve closes and electrons cannot flow [8]. Therefore, the valve opening and closing (and thus, current flow) is controlled by the application of a magnetic field. The state of the spin valve is nonvolatile and can therefore maintain its state regardless of power.

Spin valves are most often used in magnetic sensors to detect magnetized particles [18]. A sufficiently strong magnetic field can magnetize the free layer and therefore change the state of the valve [18], allowing a high or low level of current to flow, depending on if the valve layers are magnetized in the parallel or antiparallel configuration. This also allows spin valves to be utilized as magnetic read-heads. Magnetic recording systems, which use magnetic disk and tape, are often used to store data, and use write-heads and read-heads to store and retrieve data, respectively, from the magnetic recording medium [19]. Spin-valves are therefore used as magnetic sensors that detect magnetization differences in the recording medium.

Spin-FETs

Spin-FETs are hybrid spin-based devices that are alternatives to traditional field-effect-transistors (FETs).

Field Effect Transistors

FETs are charge-controlled devices which have 3 terminals, where "the conduction between two electrodes depends on the availability of charge carriers, which is controlled by a voltage applied to a third control electrode" [9]. Conduction electrodes are called the source and drain, and the controlling electrode is the gate.

Traditional FETs are used in electronics as charged based switches, meaning that information is stored in the flow of charge (or lack thereof). In traditional FETs, the source and drain are "wells" made of n or p type semiconductors that sit in the body of the FET, which is made of semiconductor material that is oppositely doped in comparison to the source and drain. The area of the body between the source and drain is the channel. The gate is metallic and is separated from the channel by an insulating layer [9].

P-type semiconductors and n-type semiconductors differ because p-types have positive charge carriers (holes left vacant by electrons), while n-types have negative charge carriers (electrons) [9]. FETs are categorized as NMOS when their wells are made of n-type semiconductors and PMOS when they are made of p-type semiconductors.

In traditional NMOS FETs, when a high voltage is applied to the gate, the gate attracts negative charge carriers. In the p-type body, negative charge carriers move towards the gate, making the region under the gate effectively n-type. This region is the channel, which then can conduct negative charge carriers from source to drain; the FET is on. When there is a low

voltage is applied to the gate, the p-type body prevents negative charge carriers from flowing from source to drain; the FET is off [9].

In traditional PMOS FETs, when the gate is at a low voltage, the gate attracts positive charge carriers. In the n-type body, positive charge carriers move towards the gate, creating an effective p-type channel under the gate. This channel can carry positive charge carriers between the source and drain; the FET is on. When there is a high voltage is applied to the gate, the n-type body prevents positive charge carriers from flowing between the source and drain, and the FET is off [9].

Structure of Spin-FETs

Spin-FETs are a type of FET that utilizes spin-polarized current to encode information [10]. Like other FETs, they have gate, source, and drain terminals, and the voltage gate terminal is used to change the state of the FET.

A Spin-FET's source and drain terminals are made of ferromagnetic materials connected by a semiconducting channel; above this channel, there is an oxide layer, followed by a gate terminal made of metallic materials [10]. The source and drain are magnetized along the direction of current flow [3]. The source acts as a spin polarizer because it polarizes the spin of carriers with the same polarization as its own [10]. In contrast, the drain acts as a spin filter: allowing carriers with the same polarization as its own to pass and rejecting all [10].

Functionality of Spin-FETs

Overall, Spin-FETs modulate the current that flows in a channel between the source and drain depending on the applied gate electrostatic potential (Handbook of Spintronics 30). Current flow begins with the source terminal, which injects electrons into the channel that have the same spin as itself [3].

When a potential is not applied at the gate of the transistor, these electrons proceed through the channel and "arrive at the drain contact with their spins still aligned," and since "the arriving carriers have their spins aligned parallel to the drain's magnetization, the drain transmits all of them and the maximum possible current flows between source and drain contacts" [3].

When a potential is applied to the gate of the transistor, it induces an electric field that is perpendicular to the channel. For clarity, the direction of this 1-dimensional channel (and direction of current flow) will be labelled the x direction, while the direction of the electric field is the y direction. This electric field "induces Rashba spin-orbit interaction the channel, which produces an effective magnetic field that is oriented in a direction perpendicular to the direction of current flow and the gate induced electric field" [3]. This magnetic field is oriented in the z direction, since it is perpendicular to both the channel and electric field.

This magnetic field is characterized by Equation 8 [3].

$$B_{Rashba} = \frac{2m^* a_{46} E_y v}{g \mu_B \hbar} \quad (8)$$

Where

m^* = carrier effective mass

a_{46} = material constant

v = carrier velocity

E_y = gate-induced electric field
g = electron-spin g-factor or gyromagnetic ratio
μ_B = Bohr magneton = $\frac{e\hbar}{2m_e}$ [2]

This magnetic field results in a Larmor precession [3]. A Larmor precession is the change in spin orientation that occurs when a particle passes through a region of uniform magnetic field [11].

Therefore, the Rashba field and subsequent Larmor precession causes each electron to rotate by the same amount, φ_{Rashba}, which is defined by Equation 9 [3].

$$\varphi_{Rashba} = \frac{2m^* a_{46} E_y L}{\hbar} \quad (9)$$

Where
m^* = carrier effective mass
a_{46} = material constant
E_y = gate-induced electric field
L = channel length

One can set gate-induced electric field to allow $\Phi_{Rashba} = (2n + 1)\pi$, where n is an integer. This means that "the carriers arriving at the drain have had their spins rotated by an odd multiple of 180 degrees, which means their spin polarization is antiparallel to the original polarization" [3]. Since the carrier's initial polarization is equal to that of the source and the source and drain were initially polarized in the same direction, the carrier's new polarization is opposite to the drain's polarization. The drain, which blocks carriers with spins opposite to its own, blocks these carriers, preventing current from flowing between the source and drain.

Applications of Spin-FETs

Spin-FETs are often discussed as low-power alternatives to traditional FETs; however, recent literature has suggested this is not the case.

Traditional charge-based devices require a change in charge (ΔQ) in order to change the state of stored data [3]. This is due to the definition of current, expressed below by Equation 10 [3].

$$I = \frac{\Delta Q}{\Delta t} \quad (10)$$

A change in charge (ΔQ) therefore results in a current, I, has a corresponding energy dissipation of P. The relationship between a change in charge and the energy it dissipates is characterized by Equation 11.

$$P = I^2 R\Delta t = \frac{(\Delta Q)^2 R}{\Delta t} \quad (11)$$

Spin-based devices are seen as promising alternatives to charge-based devices because they store data in spin instead of amount of charge, and "switching between [zeroes and ones] them merely requires flipping the spin, without moving the electron in space and causing current flow," [3] which eliminates the aforementioned $I^2 R\Delta t$ dissipation.

As spin-devices, spin-FETs do not experience $I^2 R\Delta t$ dissipation the traditional FETs do. However, spin-based devices require additional energy to modulate spin polarization (energy required to apply voltage to gate); this energy has the possibility to exceed the $I^2 R\Delta t$

dissipation that traditional charge-based devices experience. If this is true, the spin device becomes less energy efficient than traditional devices. There is evidence to suggest that this is the case: in order to modulate electron spins a voltage must be applied to the gate. If the gate is modelled as a capacitor, energy (E) can be described by Equation 12 [3].

$$E = \frac{1}{2} C V_G^2 \quad (12)$$

This means this energy be consumed in order to modulate the spins. This energy is estimated to be roughly equivalent to traditional FETs' $I^2 R \Delta t$ dissipation, which suggests spin devices will not be more power efficient than charge-based FETs [3].

Spin-FETs have also been noted to have interesting oscillatory and transconductance properties, which makes them candidates for creating frequency multipliers and complementary logic devices.

Spin-FETs' most promising application is in low-power nonvolatile logic: circuit systems that maintain their state and data despite a loss in power [3]. As discussed in later sections, MTJs can be integrated into CMOS systems to make CMOS memory systems nonvolatile. However, MTJs deteriorate the circuit performance of the CMOS components; for example, they can degrade operating speed, tolerance to variability, and static noise margin [3]. To resolve these problems, spin-FETs can be used to electrically isolate the CMOS devices from nonvolatile memory elements (MTJs), such that they have little or no effect on the CMOS circuit operation [3].

Magnetoresistive Radom Access Memory

Magnetoresistive Random Access Memory (MRAM) is a type of spintronic device which uses electron spin to store digital memory.

Memory

Memory types can be broken down into 3 groups based on their access patterns: read/write memories, mostly read/rarely written memories, and ready-only memories. Read/write memories can be categorized their access pattern: either random access or non-random access. Random access memories (RAMs) will be focused on because many recent advances in spintronics have been focused on developing spin-based RAMs [12].

Another way of categorizing memory is by volatility. Volatile memory means that if power is turned off, stored data is lost; conversely, in a nonvolatile memory, that data would be preserved [12].

One final way to categorize different types of memory is as either static or dynamic. The key difference between static and dynamic memory is refreshing. In dynamic memory, if the data is not periodically refreshed (reloaded or rewritten to each cell), the data will decay and be corrupted over time. Static RAM does not require refreshing; as long as power is supplied to the memory, stored data will be preserved [12].

Dynamic Random-Access Memory

There are two types of commonly used RAMs: dynamic and static. Dynamic Random-Access Memory (DRAM) is a type of random-access memory that is structurally dense, fast to

read and write to, volatile, and requires refreshing [3]. The basic memory unit-cell for DRAM is a selection transistor and a capacitor. The unit-cell for DRAM is configured in the following way:

- The drain of the transistor is connected to the bit line (BL)
- The gate of the transistor is connected to the word line (WL)
- The source of the transistor is connected to one terminal of the capacitor
- The other terminal of the capacitor is connected to ground [17]

In order to read from the DRAM cell, WL goes high (turning on the transistor) and BL becomes the value stored on the capacitor [17]. Since reading requires the transfer of charge stored on the capacitor, the read operation is destructive and requires a write following every read. In order to write to the DRAM cell, WL goes high (turning on the transistor) while BL is set to the desired value; the cell then stores the value of BL.

Static Random-Access Memory

Static Random-Access Memory (SRAM) is a type of random-access memory that is structurally less dense, extremely fast to read and write to, volatile, and does not require refreshing [3]. The unit-cell for SRAM is a 6-transistor cell consisting of a pair of inverters (2 transistors each) and two setting transistors. The unit-cell for SRAM is configured in the following way:

- The input of each inverter is connected to the output of the other inverter, creating a loop with two nodes that store the cell's stored information. One node is the stored data bit (x), and the other is the inverted stored data bit ($\overline{x}$). This configuration can be referred to as a pair of cross-coupled inverters.
- The data bit node is connected to the source of one of the setting transistors. This transistor's drain is connected to the inverted bit line $\overline{BL}$, which is the inverted value of BL
- The inverted data bit node is connected to the source of the other setting transistor. This transistor's drain is connected to the bit line (BL)
- Both setting transistors have gates that are connected to the word line (WL) [17]

To read from the SRAM cell, the WL goes high, turning on the transistors and pulling BL to the stored value (x) and pulling $\overline{BL}$ to the inverted stored value ($\overline{x}$). To write to the SRAM cell, the BL is set to the desired value to-be stored. The WL is then enabled, which allows the BL and $\overline{BL}$ value to overwrite the stored values of x and $\overline{x}$, respectively.

Overall, DRAM is less expensive (due to high possible cell density), while SRAM is extremely fast to read and write to, nonvolatile, and uses less power (does not require refreshing) [3]. These trade-offs result in most memory systems having both DRAM and SRAM components. SRAM is used for cache memory, or data that is used often and repeatedly. A larger amount of data is stored in DRAM, since it is cheaper and more compact; DRAM is used for main memory, which is used less often and can afford the increased wait time. In an ideal world, memory would have the access time of SRAM but the compactness/density capability of DRAM. This ideal has the potential to be realized in MRAM cells [12].

Magnetoresistive RAMs

MRAM is a type of random-access memory that uses electron spin to store information. MRAM has the potential to be advantageous over SRAM and DRAM because it is nonvolatile, has fast read and write times, and is comparable in size to DRAM. DRAM unit cells can be as small as 6-8 F^2 [3] while novel STT MRAM cells can be as small as 6-10 F^2 [4]. MRAM unit-cells are composed of a selection transistor and a magnetoresistive element (MRAM Fundamentals, Yoda). Single-bit data is read out of these unit-cells using the magnetoresistance effect.

Commercialized MRAM use TMR-based structures. For TMR-based MRAM, the MRAM magnetoresistive element in each unit-cell is a MTJ. One of the MTJ's two ferromagnetic layers is the storage layer; this layer has a changeable magnetization direction that reflects the bit stored [3]. The second layer is called the reference layer, which has a fixed magnetization that is not easily changeable.

These MRAMs use TMR to read the information stored out of MTJ-FET data cells [3]. In MTJs, TMR dictates that when the magnetization of the storage layer is parallel to the reference layer, the MTJ is in a low-resistance state; conversely, when the magnetization of the storage layer is anti-parallel to the reference layer, the MTJ is in a high-resistance state [13].

There are two types of MRAMs that use TMR: field-write and spin-transfer torque MRAMs. These MRAMs both use the same unit-cells (MTJ with a FET) but they have different overall structures because they write to the MTJ cells in different ways.

Field-write MRAM

In a field-write MRAM, the unit-cells are configured in the following way:

- Each MTJ is situated between two perpendicular wires: the bit line (BL) and the word line (WL) (31148_03)
- The MTJ's storage layer is connected to the bit line (BL)
- The MTJ's reference layer is connected to the FET's drain
- The FET's gate is connected to the read line (RL)
- The FET's source is grounded

In order to read from the cell, the RL for that cell must go high and a weak voltage is applied to its BL [14]. When the RL is high, the FET is turned on and allows current from the BL to flow through the MTJ via to ground (at the source of the FET). By Ohm's law, for the same applied voltage, a larger current will flow if the MTJ is in a low resistance than when it is in a high resistance state. Therefore, by identifying if the current detected is large or small, the "state" or information in the MTJ can be read [14].

In order to write to the cell, currents are applied to its WL and BL [4]. Since the WL and BL are perpendicular, any pair of WLs and BLs acts on only 1 cell. The magnetization direction of the cell's storage layer is determined by the magnetic fields that arise from these currents (H_{WL} and H_{BL}, respectfully) [4].

In order for the cell's magnetization to be polarized in a particular direction, the vector sum of the magnetic fields H_{WL} and H_{BL} must be greater than a certain threshold [4]. Let x be the axis along the BL. If the sum of H_{WL} and H_{BL} is greater than this threshold and H_{BL} is in the positive x direction, then the sign of the MTJ's storage layer polarization in the x direction will be positive. If the sum of H_{WL} and H_{BL} is greater than this threshold but H_{BL} is in the negative x direction, then the sign of the MTJ's storage layer polarization in the x direction will be negative. The sign of the MTJ's storage layer polarization in the x direction will be equivalent to

H_{BL}'s sign while $H_{WL} + H_{BL}$ is greater than the required threshold. However, if one decreases both magnetic fields to zero while keeping the H_{BL}'s sign at the desired value up until it goes to zero, the storage layer polarization will "latch" at the desired polarization until a new magnetic field is applied that crosses the required threshold [4].

The polarization of the MTJ cell's storage layer is thus dependent by the direction of the magnetic fields created by WL and BL. Since the information stored in the MTJ depends on if the cell's storage layer has a polarization parallel or antiparallel to the reference layer, controlling the polarization of the storage layer allows one to control the information stored. Therefore, the information stored in the MRAM cell is controllable by WL and BL [14].

The primary benefit of MRAMs over traditional RAM schemes is fast read and write times. In MRAM arrays, the read/write cycle time was as low as 5 ns, while that of a single MRAM cell was 100 ps [4].

One problem with the field-write MRAM is its large current requirement. Since the efficiency of field generation by the BL and WL lies is small, the required WL current was on the order of milliamperes, which requires relatively thick wires to travel (MRAM Fundamentals and Devices, Yoda). The large current requirement not only affected power required, but also memory density, due to wire thickness [3]. For this reason, memory density never exceeded 256 megabits [3].

Another problem with the field-write MRAM is crosstalk between adjacent lines [4]. As different fields are being created by applying currents to different lines, it is possible for cells to become unintentionally magnetized such that $H_{WL} + H_{BL}$ is greater than the required threshold and the data stored within these cells becomes corrupted. Any cell that experiences a net magnetic field larger than the threshold will have its stored bit rewritten. This problem was solved by using the toggle-switching method.

Toggle Switching MRAM

The toggle switching MRAM is in many ways similar to the field-write MRAM. The toggle switching method requires that 1) MRAM MTJ cell's free ferromagnetic layer is replaced by two weakly anti-parallel coupled ferromagnetic layers and 2) the long axis of the MTJ cell is shifted 45 degrees with respect to the WL instead of being parallel to it [15]. These fundamentally changes the polarization behavior of the cell. Instead of "latching" the direction of the BL field as the stored polarization, it toggles its stored polarization to the opposite direction when a specific H_{WL} and H_{BL} sequence is applied. Without going in to too much detail, this sequence is analogous to the sequence of fields required to latch the value for field-write MRAMs, but more complicated due to the configuration of the toggle switching cell.

Since the requirement to toggle the value is more complicated than that of the field-write MRAM (where the requirement is solely that the applied magnetic field is greater than some threshold), unintentional changing of the toggle-switching MRAM cell is unlikely. Toggle switching allowed MRAM to become reliable enough to be used commercially for the first time [4].

However, toggle switching MRAM cells must be read at the start of the write cycle. The target cell is read and then toggled if the current stored bit does not match the state of the desired bit [15]. This read can be performed while preparing for and beginning the write

sequence, such that only a slight timing delay is suffered [15]. However, this increases the complexity of the toggle switching MRAM write.

Additionally, toggle switching MRAMs still are limited in cell density and have high power consumptions as conventional field-write MRAMs are. This problem is resolved by using Spin-Transfer Torque MRAM.

Spin-Transfer Torque MRAM

The Spin-Transfer Torque (STT) MRAM is a newer type of MRAM. STT MRAM uses a novel methodology to write to MRAM cells that does not have require large-current like field-write MRAMs do, allowing for denser MRAMs to be created. STT MRAMs use the same unit-cells (a MTJ and a FET) that field-write MRAMs do, just in a modified configuration.

In a STT MRAM, the unit-cells are configured in the following way:

- The MTJ's storage layer is connected to the bit line true (BLT)
    - In field-write MRAM, the MTJ's storage layer is connected to the bit line (BL)
- The MTJ's reference layer is connected to the FET's drain (Same as field-write)
- The FET's gate is connected to the read line (RL) (Same as field-write)
- The FET's source is connected to the bit line complementary (BLC)
    - In field-write MRAM, the FET's source is grounded

The read operation is essentially the same for STT MRAMs as in field-write MRAMs. In order to read from the MTJ cell, the RL for that cell must be high and BLC must be grounded, and a weak voltage is applied to its BL. The current that results indicates if the MTJ is in the high-resistance or low-resistance state, thus allowing one to read from the cell. The applied voltage must be very small (typically ~0.1V) in order to avoid disturbing the value contained in the cell [3].

STT MRAMs use the spin-transfer torque effect to write to the storage layer of MTJ cells. The spin-transfer torque effect is characterized by the "exchange of spin angular momentum between a transport spin current carried by electrons and a ferromagnetic material" [3]. This exchange of angular momentum can therefore be described as the spin-current exerting a torque on the ferromagnetic material [3]. This current transfers some of its momentum to the free layer, inducing a torque that can switch the ferromagnetic polarization [3].

The origins of current polarization are also essential understanding STT MRAMs. As previously discussed in reference to GMR, when an electron travels through a ferromagnetic layer with the same net magnetization as its own it does not scatter (Principles of Nanomagnetism). It follows that as a non-polarized current travels through a polarized ferromagnetic layer, its electrons which have the same spin polarity as the layer scatter less than those which have opposing spin polarity [14]. Therefore, the majority of electrons leaving the ferromagnetic layer have the same spin as the layer [14]. This results in a current that is polarized along the polarization of the ferromagnetic layer.

This effect is utilized to write a magnetization value to MTJ cells. In order to put the cell into the low-resistance state from the high-resistance state, a positive voltage is applied to the BLT, the word line of the cell is activated, and the BLC is grounded [14]. Since current flows from high to low potential, "write current" flows from the BLT through the MTJ and FET to the BLC [14]. Since electrons flow in the opposite direction of current, the electrons flow from the

reference layer to the storage layer. Due to the origins of current polarization, these electrons are polarized in the same direction as the free layer. Due to the spin-transfer torque effect, the MTJ's ferromagnetic storage layer adopts the polarization of the reference layer. Therefore, the MTJ is in the parallel, low-resistance state [14].

In order to put the cell into the high-resistance state from the low-resistance state, the BLT is grounded, the word line of the cell is activated, and a positive voltage applied to the BLC [14]. A write current flows from the BLC to the BLT and electrons flow from the storage layer to the reference layer. When this current reaches the reference layer, it scatters. Electrons with the same polarization as the reference layer do not scatter significantly and pass though the reference layer. Electrons with opposing polarization to the reference layer scatter and are reflected back to the stored layer. Due to the spin transfer-torque effect, these reflected electrons exert a torque on the stored layer, making it adopt a polarization opposite to that of the reference layer [16]. The MTJ is now in the antiparallel, low-resistance state.

Hybrid MTJ-CMOS Nonvolatile Logic

Hybrid MTJ-CMOS components have been created in order to create effective low-power nonvolatile logic circuits. Complementary Metal Oxide Semiconductor (CMOS) is a technology and general structure for circuits which involves using complementary pairs of PMOS and NMOS transistors to implement logic functions (described in Spin-FET section). Novel MTJ-CMOS logic involves integrating MTJs into typical CMOS architectures, allowing CMOS logic to gain nonvolatile properties [3].

Volatile systems require additional hardware to maintain stored data when power is shut off. One way of implementing this is with power-gating architectures; this involves grouping circuits into "power domains" that can be shut down when they are not in use, thus reducing power consumptions [3]. In order to save power by shutting down unused memory circuits, data from these devices would have to be transferred to volatile forms of memory. This requires a lot of additional hardware, delays, and power consumption to implement.

A potential solution to this problem of logic volatility is the use of MTJ-CMOS memory cells: primarily, MTJ-CMOS SRAM cells and MTJ-CMOS Flip-flops As an example, MTJ-CMOS SRAM cells will be discussed in detail.

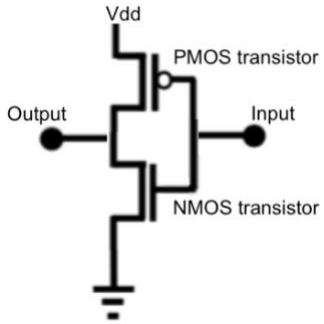
MTJ-CMOS SRAM Cells

MTJ-CMOS SRAM cells are generally composed of 2 MTJs, a data-sense amplifier, and a write circuit. The two MTJs store two complementary values (x and $\overline{x}$) to store one nonvolatile data bit [16]. The MTJs therefore have complementary resistance states; one will be in the high-resistance (antiparallel) state, while the other will be in the low-resistance (parallel) state.

Data sense amplifiers (DSA) are CMOS-based circuits that are used to read the stored data in the MTJs [16]. A typical DSA is based off of a pair of cross-coupled inverters, a configuration where the output of one inverter (INV1) is connected to the input of another (INV2), and the output of INV2 is connected INV1's input. The node that connects INV1's output to INV2's input will be denoted as x, while the node that connects INV2's output to INV1's input will be denoted as $\overline{x}$. These two nodes have complementary values due to the nature of inverters; if a zero is stored at x, it goes through INV1 and stores a one at $\overline{x}$, which goes through INV2 which reinforces the zero initially stored at x. Likewise, if a zero is stored at x, a one must

be stored at $\overline{x}$. This creates a bi-stable circuit that can store 1 bit of data with value x and complement $\overline{x}$. The data stored at x and $\overline{x}$ are volatile values: if power is lost, the inverters would no longer function and the data would be lost.

An inverter (INV) is classically composed of two transistors (shown to the right, modified from [16]). The first transistor is a NMOS transistor; and as described in the Spin-FET section, it conducts current from drain to source when a logic zero (low voltage) is applied to its gate. The second transistor is a PMOS transistor, meaning that it conducts current when a logic one (high voltage, often referred to as V_{DD}) is applied to its gate. Both gates are connected, and this node is referred to as the input of the inverter. The PMOS transistor's source is connected to the NMOS transistor's drain; and this node is the output of the inverter. The PMOS transistor's drain is connected to V_{DD} and the NMOS transistor's source is connected to GND.



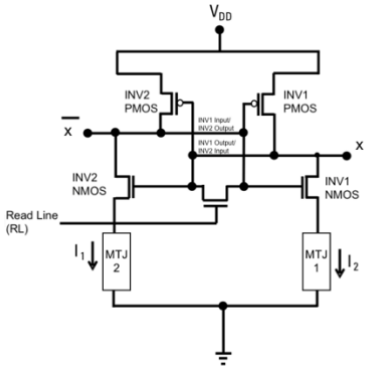
When a high voltage is applied to the inverter's input, the NMOS transistor is activated, which connects the output node to GND (logic zero). When a low voltage is applied to the inverter's input, the PMOS transistor is activated, which connects the output node to V_{DD} (logic one).

This cross-coupled inverter DSA is connected to the 2 nonvolatile storage MTJs (MTJ1 and MTJ2) [16]. They are configured in the following way:

- The source of INV1's NMOS transistor is connected to one side of MTJ1 (in classical inverters, the source of this transistor would be connected to GND)
- The source of the second inverter's NMOS transistor is connected to one side of MTJ2
- For each MTJ, one side is connected to ground, and the other is connected to the source of a FET (as described above) [16]

Lastly, a FET is connected to the inputs of both inverters, with the source connected to one INV1's input and the drain connected to INV2's input. This FET's gate is connected to the read line (RL).

The overall DSA-MTJ structure is shown below (modified from [16]).



This configuration allows the nonvolatile MTJs to set the values stored in the volatile bi-stable inverter circuit. The bi-stable inverter circuit can also be thought to be reading data from the MTJs. When the RL is asserted, the inverter circuit enters a metastable state, in which both output voltages are in an indeterminate, intermediate range. Current begins to flow from x and $\overline{x}$ through their respective NMOS FETs, through the MTJs, to GND. This lowers the voltages

stored at x and $\overline{x}$; however, one of the voltages will decrease faster than the other. Since the MTJs have different resistance states, the MTJ in the high-resistance (antiparallel) state will allow less current to flow to GND than the MTJ in the low-resistance (parallel) state. This will lower the voltage of the node (x or $\overline{x}$) connected to the low-resistance MTJ faster than the other node. RL is unasserted. Once the low-resistance MTJ's node decreases below some threshold, the cross coupled-inverters will identify that node as a zero, which will force the other node to a one. Therefore, x become a zero if its corresponding MTJ is in the low-resistance state (and $\overline{x}$ will be a one); and x become a one if its corresponding MTJ is in the high-resistance state (and $\overline{x}$ will be a zero).

The values stored in the MTJs are stored and written to using an STT-based system [16]. Using the same general principle as STT MRAMs, transistors are used to flow polarized currents through the MTJs, which can set their ferromagnetic layers to be in the parallel or anti-parallel states; thus allowing one to write new values to the MTJs.

MTJ-CMOS Combinational Circuits

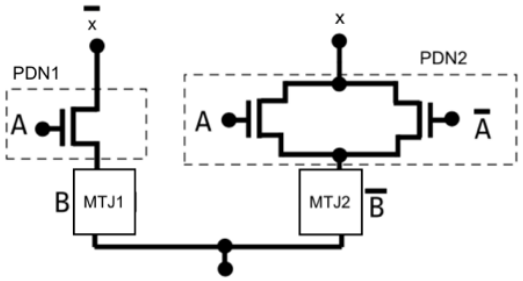
MTJ-CMOS combinational circuits are generally composed of 2 MTJs, a data-sense amplifier, a write circuit, and 2 pull-down networks [16]. MTJ-CMOS combinational circuits allow one to use data stored in MTJs as inputs to digital logic functions. They are comparable to traditional CMOS combinational circuits, which also implement logic functions, but do not use MTJs. CMOS combinational circuits are fully volatile, such that no data is preserved if power is lost. The MTJ-CMOS combinational circuit has an advantage over traditional CMOS combinational circuits in that its MTJ data inputs are nonvolatile.

Structurally, they use the same base as MTJ-CMOS Memory cells but have pull-down networks that add additional functionality [16]. The pull-down network (PDN), consisting of NMOS devices, is the part of the MTJ-combinational circuit that implements the logic operation. This means that the bit stored in the MTJs is essentially operated on by a logic function (dependent on the PDN and the inputs provided to the PDN) which results in an output that is stored at x or $\overline{x}$ in the cross-coupled inverter circuit. They are called pull-down networks because they set or "pull" the output of the logic function to zero depending on the values of the PDN inputs.

There are two pull down networks (PDN1, PDN2) that are inserted between the DSA and the MTJ at the node that connects the sources of the DSA's NMOS inverters and their respective MTJs [16].

For example, a 2-input AND can be implemented which takes the stored bit in the MTJs as one input (B) and an external input (A) as another. To implement this one would create a PDN which stores a logic one at x if the MTJ bit and the external input are both logic one, and a logic zero at $\overline{x}$ if they are not both one [16]. By convention, the MTJ anti-parallel state is considered logic zero, since it results in less current flow, while the MTJ parallel state is considered a logic one, since it results in a higher amount of current flow.

An example 2-input AND CMOS-MTJ PDN is shown below. Note that the write circuit, and DSA are not shown.



(Modified from [16])

The functionality of the PDN can be explained by determining the values of x and $\overline{x}$ at different values of A and B. For all values of A and B, initially, outputs x and $\overline{x}$ are all pre-charged to an initial, intermediate value, such that x or $\overline{x}$ can be set to 1 or 0 based off of the PDNs [16].

One essential principle to understanding the CMOS-MTJ network is that current flow is largest in the path of least resistance. In order to understand how this circuit will, the response of the CMOS-MTJ circuit to all possible combinations of values for A and B will be considered.

When B = A = 1, $\overline{x}$ has a lower resistance path to GND than x, resulting in a larger current flowing from $\overline{x}$ to GND, $\overline{x}$ going to logic zero, and logic 1 being stored in x.

When B = 1 and A = 0, $\overline{x}$ has a high resistance path because A = 0 and the transistor in PDN1 is off; there is no way for current to flow from $\overline{x}$ to GND. x has a lower resistance path because A = 0 turns on of the transistors in PDN2 (making the PDN resistance low) and $\overline{B} = 1$, such that MTJ2 is in the parallel (low resistance state). A larger current flows from x to GND than from $\overline{x}$ to GND, making x go to logic zero, and causing logic 1 to be stored in $\overline{x}$.

When B = 0 and A = 1, the path from $\overline{x}$ to GND has a higher resistance than that of x because x has an MTJ in its path that is in the high resistance state, while $\overline{x}$ has a MTJ in its path that is in the low resistance state.). Again, a larger current flows from x to GND than from $\overline{x}$ to GND, making x go to logic zero, and causing logic 1 to be stored in $\overline{x}$.

When B = A = 0, the PDN1 transistor is off, and no current flows from $\overline{x}$ to GND. There is a path between x and GND because A = 0 turns on one of the transistors in PDN2, and although B = 1 creates a high-resistance element in the current path, it is still a lower resistance path than that of $\overline{x}$. Therefore, a current flows from x to GND, making x go to logic zero, and causing logic 1 to be stored in $\overline{x}$.

From this analysis, it becomes clear that logic 1 is stored in x only when A = B = 1, and the circuit represents a 2-input AND, where A and B are inputs.

MTJ-CMOS Reconfigurable Combinational Circuits

MTJs also can be integrated into traditional CMOS circuits to make reconfigurable combinational logic gates. Combinational circuits are circuits that have inputs that are directly determined from their outputs by performing logical operations on them (eg: AND, OR, NOT). For reconfigurable logic circuits, the operations performed by the circuit can be determined by setting the state of the MTJs [16].

There is not a comparable CMOS technology that can easily replicate this functionality. CMOS Programmable Logic Devices (PLDs), such as Complex Programmable Logic Devices (CPLDs) and Field-Gate Programmable Arrays (FPGAs), can also be reconfigured to implement

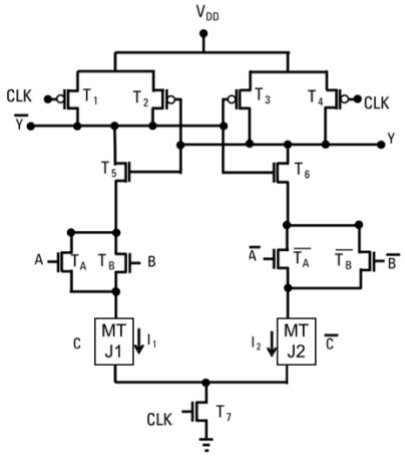
various, changeable functions. However, their architecture is completely different, often involving arrays of logic elements.

Logic elements are composed of look-up tables and flip flops, where the look-up tables implement the desired logic function and produce an output that is stored in the flip-flop [17]. Look-up tables are often implemented via SRAM cells that are connected to multiplexors. A multiplexor is a transistor-based device that can set 1 output to be equivalent to one of its 2^n inputs by using n selection lines [17]. Each input of the multiplexor is connected to an SRAM cell. When a n bit selection signal is applied to the multiplexor, exactly one of the 2^n inputs is connected to the output. This sets the output to be the value of the SRAM cell connected to that input. By programming the SRAM cells to store the desired output for each possible n-bit selection line input, one can implement any logic function.

These logic elements are far more complicated than the MTJ-CMOS reconfigurable circuits that can be implemented by utilizing spintronics and MTJs. Although MTJ-CMOS reconfigurable circuits cannot implement any logic function as logic-element based circuits can, they offer an alternative, potentially simpler method to implement specific reconfigurable functions.

The MTJ-CMOS reconfigurable logic circuit works similarly to the MTJ-CMOS combinational circuit previously described. It has a similar structure to the MTJ-CMOS combinational circuit; containing a DSA, MTJs, write circuits, and PDNs [16]. For example, a reconfigurable AND/OR can be implemented which takes in 2 volatile inputs (A, B) and uses 1 stored bit in the MTJs as a control input (C) that determines if the logical operation is AND or OR [16]. The output of the logic operation is stored at node Y.

An example AND/OR CMOS-MTJ network is shown below. Note that the MTJ write circuit is not shown, but the DSA, MTJs, and PDNs are. As was also required for the MTJ-CMOS combinational circuit, the output nodes (Y and $\bar{Y}$) need to be pre-charged to the same value. In this particular implementation, this is done by transistors T1 and T4 which "pull" Y and $\bar{Y}$) up to V_{DD} whenever the signal CLK is asserted.



(Modified from [16])

When MTJ1 is in the antiparallel (high resistance) state, and MTJ2 is in the parallel (low resistance state), the reconfigurable logic gate is an AND (A AND B). When A = B = 0, T_A and T_B

are off, such that there is no path from $\bar{Y}$ to GND, making Y to GND the path of least resistance. Current flows from Y to GND, discharging Y and pulling Y to 0, and $\bar{Y}$ to 1. When A = 0 and B = 1 or when A = 1 and B = 0, exactly 1 transistor is active in each PDN. The path of least resistance is therefore determined by the state of the MTJs. Since MTJ2 is in the higher resistance state, more current flows from Y to GND than from $\bar{Y}$ to GND, discharging Y and pulling Y to 0, and $\bar{Y}$ to 1. When A = B = 1, $\bar{T}_A$ and $\bar{T}_B$ are off, such that there is no path from Y to GND. A nonzero amount of current flows from $\bar{Y}$ to GND, discharging $\bar{Y}$ and pulling $\bar{Y}$ to 0, and Y to 1. By examining Y for these various values of A and B, it is determined that Y is 1 only when both A and B are 1, making the logic operation an AND [16].

When MTJ1 is in the parallel (low resistance) state, and MTJ2 is in the antiparallel (high resistance state), the reconfigurable logic gate is an OR (A OR B). This can again be determined by analyzing the resistance of the circuit's PDNs with different values of A and B. When A = B = 0 or when A = B = 1, the circuit exhibits the same behavior (respectively) as described when C is in the antiparallel state. However, when A = 0 and B = 1 or when A = 1 and B = 0, exactly 1 transistor is active in each PDN. The path of least resistance is therefore determined by the state of the MTJs. Since MTJ2 is in the lower resistance state, more current flows from $\bar{Y}$ to GND than from Y to GND, discharging $\bar{Y}$ and pulling $\bar{Y}$ to 0, and Y to 1. By examining Y for these various values of A and B, it is determined that Y is 0 only when both A and B are 0, making the logic operation an OR [16].

IV. FUTURE DIRECTIONS

There are many areas that require further exploration and development in the field of spintronics. Overall, energy efficiency and scalability are the largest problems for spintronics devices.

Spin-FETs are an example of a spin-based devices that faces energy efficiency problems. Currently, the main limitations for spin-FET efficiency and use are low spin injection efficiency, low spin-filtering efficiency, extraneous/undesired spin orbit interaction, undesired magnetic fields, and spin relaxation [10]. Two examples of how researchers have been trying to increase spin-FET power efficiency are 1) to incorporate new materials to have better spin transport inside the channel and 2) to use dielectrics to insulate the spin-FET channel and decrease leakage current [10].

MRAMs are the spintronics device that have the most potential to revolutionize current technology. As previously discussed, legacy SRAM and DRAM hierarchies are both volatile, and efficient and scalable MRAM devices would allow for memory that has fast read/write accessibility that is also nonvolatile [3]. MRAMs give the potential to create "normally-off computers" which would be extremely low power because they can store information without power [3]. These computers could be completely turned off while the device is still "on," saving power without the user even knowing. However, MRAM also faces scalability problems. Despite the development of STT MRAM, this MRAM is still limited to a scalability of around 124 Mb due to its high write current requirement [3]. In addition to scalability, process variations and thermal fluctuations result in write-access errors, which also limit the use of MRAMs [13]. Therefore, further research and development must be done in MRAM design before it can be widely used.

Overall, the switching speed of MTJ-based spintronics devices has been improved in recent years, which has reduced the switching current [13]. This improvement therefore affects the MRAM and MTJ-CMOS devices previously discussed. MTJ-CMOS devices face the same energy efficiency and scalability challenges as other spintronics devices [3]. Other areas of further interest to optimize MTJ-CMOS devices include improving readout signal-to-noise ratio, increasing manufacturing yield, and exploring new nonvolatile circuit architectures [3].

Summary

This paper has reviewed the fundamental concepts and applications of spintronics, including contemporary devices and potential future directions for their continued development. Relevant fundamental concepts included electron spin, electron transport, spin-polarized electron transport, and magnetoresistance. The devices discussed include spin-valves, spin-FETs, Magnetoresistance Random Access Memory, and hybrid MTJ-CMOS circuits.

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