

**Batt to 12V Buck Calculations**  
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## Design Requirements for Buck Selection

$V_{in}$ : 24V-60V

- 24V is what the eCVT motors run off of
- 60V is  $V_{max}$  according to Baja SAE rules

$V_{out}$ : 12V

- 12V is what we send around the car and what we cascade off of for 3V3 and 5V

$I_{load}$ : 8.4A nominal, 12A for FOS of 1.43

- Calculated in Power draw section

Efficiency: > 90%

$F_{sw}$ : 500 kHz

- Better efficiency
- Cleaner output ripple

Operating temperature range: -40C to 100C

Output ripple: 10%

## Power Draw of the entire system

Components	Power Draw (W)	Operating Voltage (V)	Current Draw (A)
Electronics System run off of battery	327.364	24.00	13.64
Electronics system run off of 12v buck	100.844	12.00	8.40
Motherboard	317.38	24.00	13.22
eCVT	1.78	3.30	0.19
SAS	0.70	3.30	0.21
TL	0.70	3.30	0.21
DAQ	0.57	3.30	0.17
Radio	1.31	12.00	0.62
IMU/GPS	1.02	12.00	0.53
Front Breakout	1.26	12.00	0.64
Rear Breakout	1.03	12.00	0.59
Dashboard	0.89	12.00	0.50

$$12A/8.40A = 1.43 \text{ FOS}$$

📈 Electronics System Calculator (Last Year's System)

## Inductor Selection

**Ripple current**

$$\Delta I_L = 0.3 \cdot I_{L\max}$$

$$\Delta I_L = 0.3 \cdot 12$$

$$\Delta I_L = 3.6A$$

**inductor**

$$L = \frac{V_{out} \left(1 - \frac{V_{out}}{V_{in}}\right)}{\Delta I_L \cdot f_{sw}}$$

$$L = \frac{12V \left(1 - \frac{12V}{60V}\right)}{3.6A \cdot 500kHz}$$

$$L = \frac{12V (1 - 0.2)}{3.6A \cdot 500kHz}$$

$$L = \frac{9.6}{1800000}$$

$$L = 5.3 \text{ } \mu\text{H}$$

## Mosfet Selection

- $V_{DS} = 60V$
- $I_D = 48A$
- $V_{GateSource} = -4 \text{ to } 6V$
- $Q_G = 5nC$
- $R_{DS} = 2.6 \text{ mOhms}$

[EPC2031](#)

## C<sub>in</sub> Selection

duty cycle

$$\frac{V_{out}}{V_{in}}$$

$$\frac{12}{60}$$

$$D = 0.2$$

C<sub>in</sub>

$$C_{in} \geq \frac{D(1-D) \cdot I_{out}}{\Delta V_{in\_pp} \cdot f_{sw}}$$

$$C_{in} \geq \frac{0.2(1-0.2) \cdot 12A}{60V \cdot 500kHz}$$

$$\geq \frac{0.2(0.8) \cdot 12}{30000000}$$

$$\geq \frac{1.92}{30000000}$$

$$C_{in} \geq 0.64 nF$$

## C<sub>out</sub> Selection

~~C<sub>out</sub>~~

$$C_0 = \frac{(1-D)}{\frac{\Delta V_0}{V_0} 8Lf^2}$$

$$= \frac{(1-0.2)}{\frac{12.08V}{12V} \cdot 8(5.6\mu H)(500kHz)^2}$$

$$= \frac{0.8}{1.0006 \cdot 8(14000000)}$$

$$= \frac{0.8}{11274666.67}$$

$$C_0 \geq 0.7nF$$



## $R_{\text{sense}}$ Selection

$R_{\text{sense}}$

$$R_{\text{sense}} = \frac{V_{\text{sense(max)}}}{I_{\text{L(max)}} + \frac{\Delta I_{\text{L}}}{2}}$$

$$R_{\text{sense}} = \frac{50\text{mV}}{12\text{A} + \frac{3.6\text{A}}{2}}$$

$$R_{\text{sense}} = \frac{50\text{mV}}{13.8}$$

$$R_{\text{sense}} = 3.6\text{m}\Omega$$

## Frequency Resistor Selection

operating frequency

$$R_{\text{freq}} = \frac{37 \text{ MHz}}{500 \text{ kHz}}$$

$$R_{\text{freq}} = 74 \text{ k}\Omega$$
$$73.2 \text{ k}\Omega$$

$V_{fb}$  Selection

Output voltage

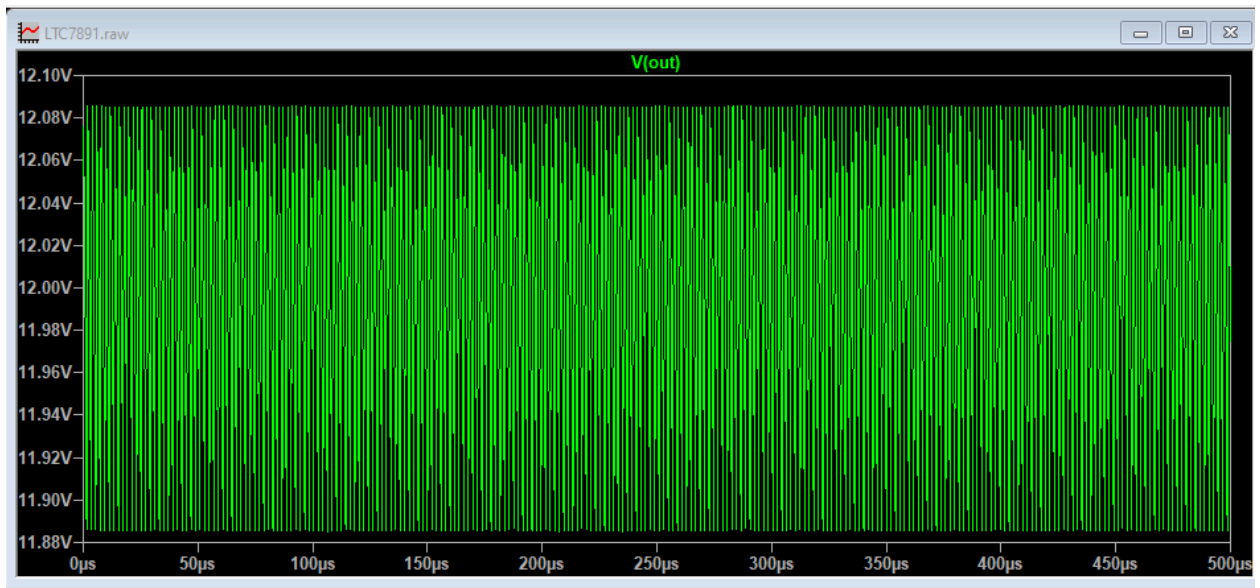
$$V_{out} = 0.8V \left( 1 + \frac{R_B}{R_A} \right)$$

$$R_B = 10K \left( \frac{12V}{0.8V} - 1 \right)$$

$$R_B = 10K(14)$$

$$R_B = 140K$$

## Voltage Output Ripple Simulation



Voltage Output Ripple

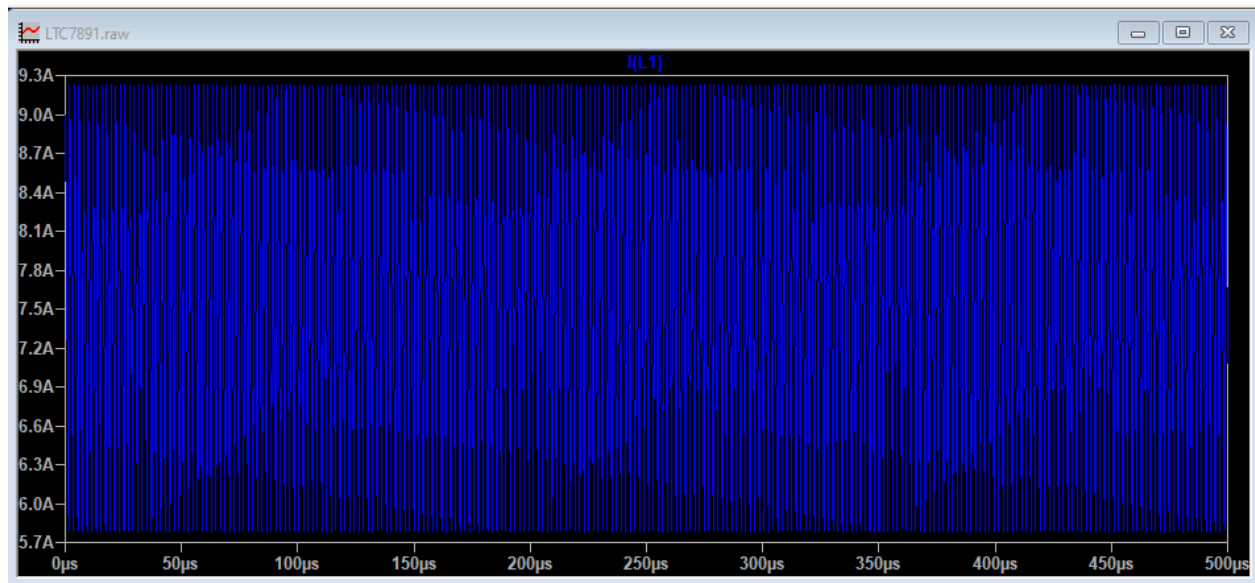
$$12.09V - 11.88V$$

$$= 0.21V$$

$$12V$$

$$= 1.7\%$$

## Current through the Inductor Simulation



### Test Points

- $V_{in}$
- $V_{out}$
- Switching node

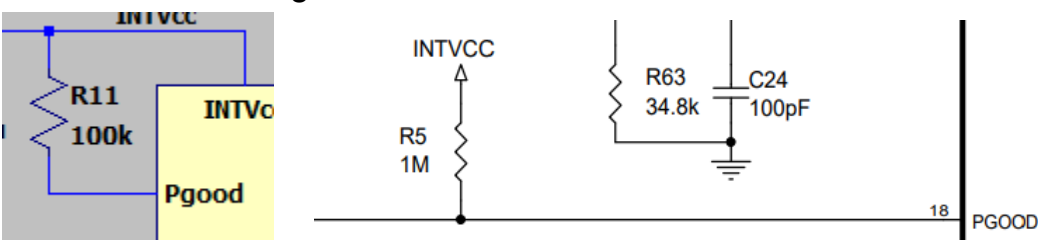
## Questions

1. 

1	PLLIN/SPREAD	External Synchronization Input to Phase Detector/Spread Spectrum Enable. When an external clock is applied to PLLIN/SPREAD, the phase-locked loop forces the rising TGxx signal to synchronize with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to INTV <sub>CC</sub> to enable spread spectrum dithering of the oscillator, or to GND to disable spread spectrum dithering.
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- a. Tie to ground right?
2. 

6	VPRG	Output Voltage Control Pin. VPRG sets the adjustable output mode using external feedback resistors or the fixed 12 V or 5 V output mode. Floating VPRG programs the output from 0.8 V to 60 V with an external resistor divider, regulating V <sub>FB</sub> to 0.8 V. Connect VPRG to INTV <sub>CC</sub> or GND to program the output to 12 V or 5 V, respectively, through an internal resistor divider on V <sub>FB</sub> .
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- a. Leave floating right?
3. 

9	BSTV <sub>CC</sub>	Bootstrap Diode Anode Connection Pin. Place an optional external Schottky diode between the BSTV <sub>CC</sub> and BOOST pins to bypass most of the 7 $\Omega$ switch resistance between DRV <sub>CC</sub> and BOOST.
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- a. Leave floating?

4. 

The first diagram shows the INTVCC pin connected to a 100k resistor (R11) which is tied to the INTVCC pin. The second diagram shows the INTVCC pin connected to a 1M resistor (R5) which is tied to the INTVCC pin. The third diagram shows the PGOOD pin connected to a 34.8k resistor (R63) which is tied to the PGOOD pin. The fourth diagram shows the PGOOD pin connected to a 100pF capacitor (C24) which is tied to the PGOOD pin.
- a. 100k or 1M res?
5. Cout and Cin caps