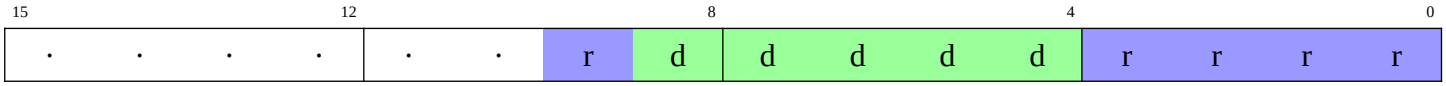
Opcode structures

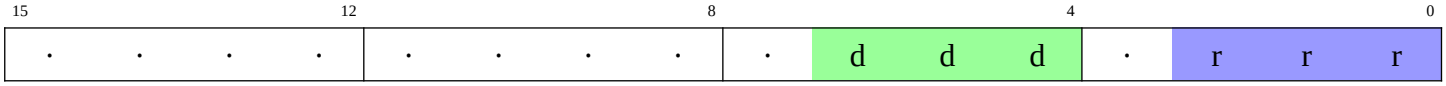
Two registers

MNEMONIC RD, RR



ADC, ADD, AND, CLR*, CP, CPC, CPSE, EOR, LSL*, MOV, MUL, OR, ROL*, SBC, SUB, TST*.

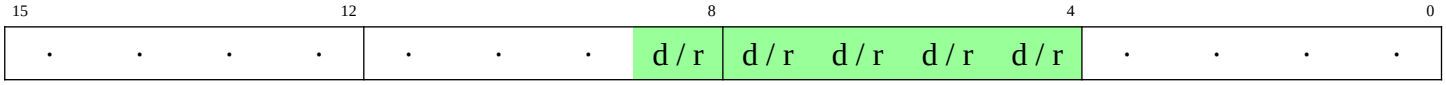
MOVW : (R1:R0 .. R31:R30),
MULS, MULSU : (R16 .. R31).



FMUL, FMULS, FMULSU : (R24 .. R31).

One register

MNEMONIC RD or MNEMONIC RR



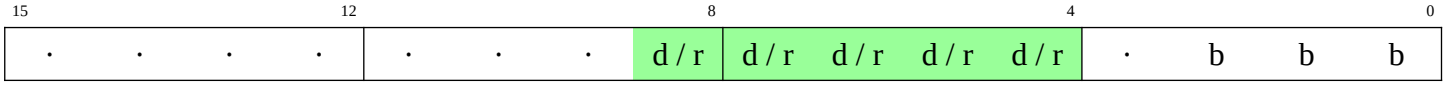
ASR, COM, DEC, ELPM (2), ELPM (3), INC, LAC, LAS, LAT, LD, LDD (1)*, LPM (2), LPM (3), LSR, NEG, PUSH, POP, ROR, ST, STD (1)*, SWAP, XCH.

MNEMONIC RD

SER*.

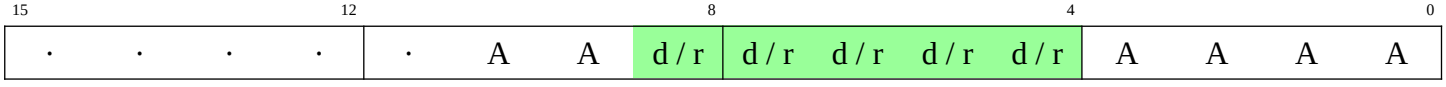
One (R0 .. R31) register and another operand

MNEMONIC RD, B or MNEMONIC RR, B



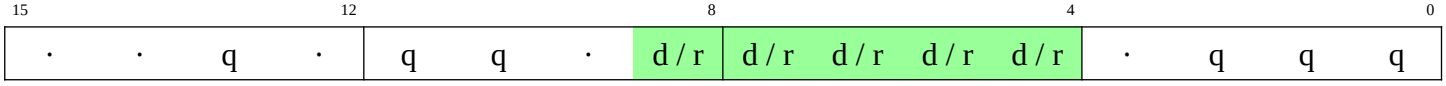
BST, BLD, SBRC, SBRS.

* MNEMONIC A, RR o MNEMONIC RD, A



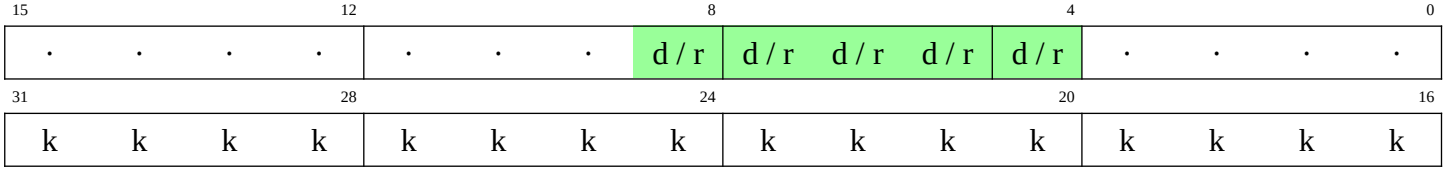
IN, OUT.

* MNEMONIC RD, xxx+Q or MNEMONIC xxx+Q RR



LDD (2), STD (2).

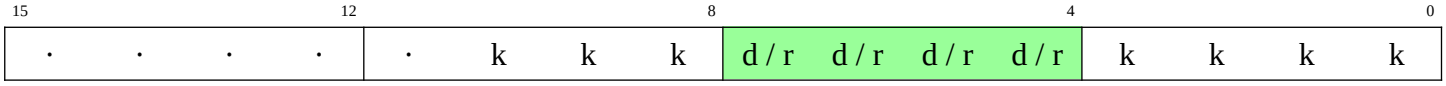
* MNEMONIC RD, K or MNEMONIC K, RR



LDS (1), STS (1).

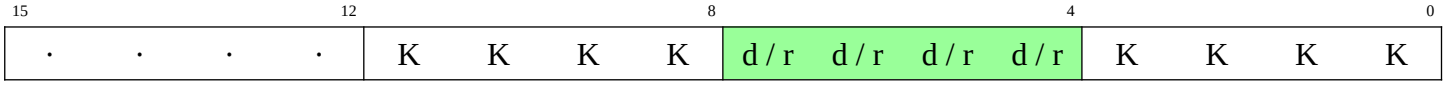
One (R16 .. R31) register and another operand

* MNEMONIC RD, K or MNEMONIC K, RR



LDS (2), STS (2).

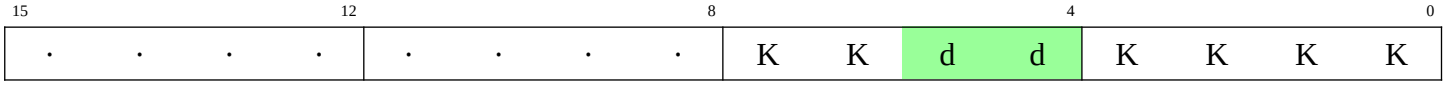
MNEMONIC RD, K or MNEMONIC RR, K



ANDI, CBR, CPI, LDI, ORI, SBCI, SBR, SUBI.

One (R{24,26,28,30}) register and another operand

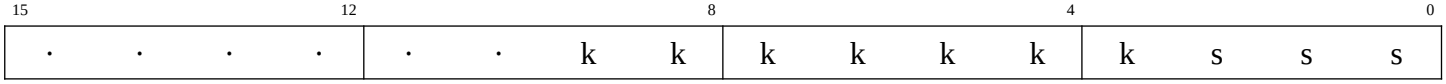
MNEMONIC RD, K



ADIW, SBIW

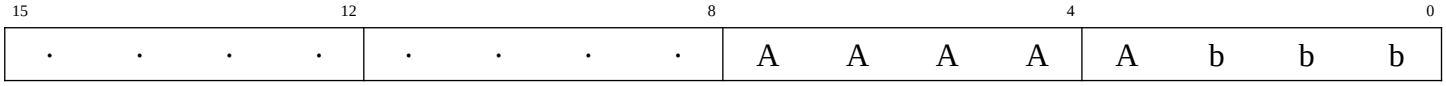
Two operands

MNEMONIC S, K



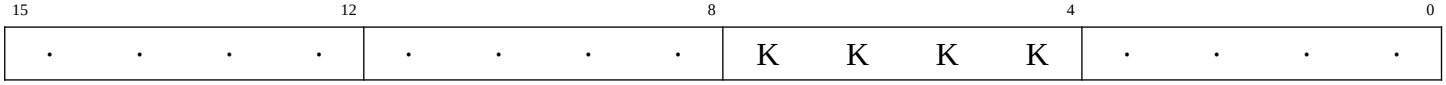
BRBC, BRBS.

MNEMONIC A, B

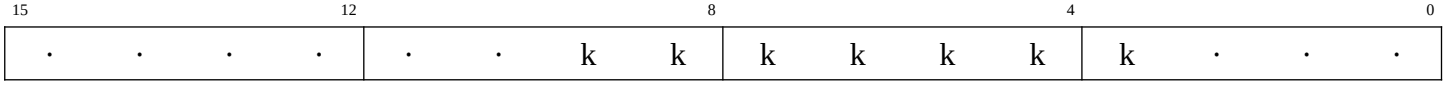


CBI, SBI, SBIC, SBIS.

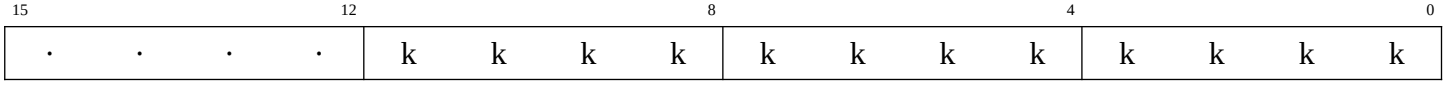
One operand



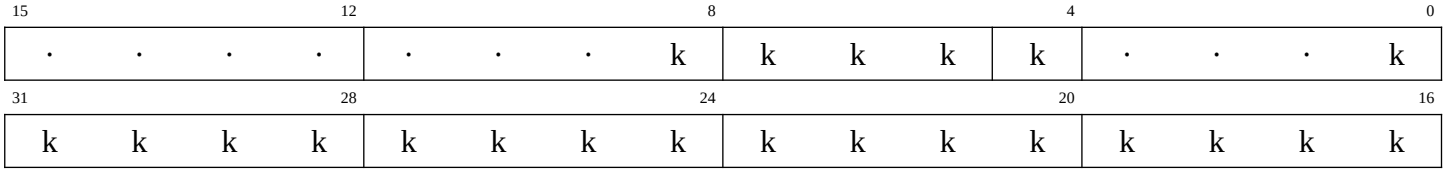
DES.



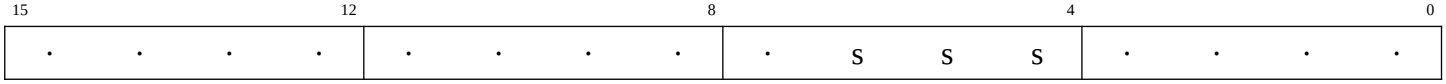
BREQ*, BRGE*, BRHC*, BRHS*, BRID*, BRIE*, BRLO*, BRLT*, BRMI*, BRNE*, BRPL*, BRSH*, BRTC*, BRTS*, BRVC*, BRVS*.



RCALL, RJMP.

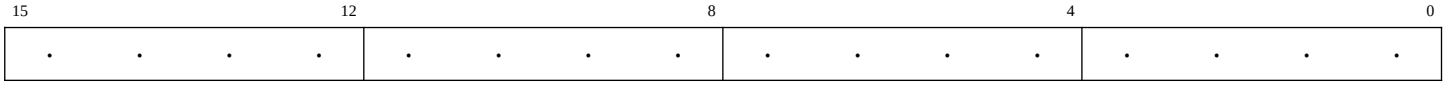


CALL, JMP.



BCLR, BSET.

No operand



BREAK, CLC*, CLH*, CLI*, CLN*, CLS*, CLT*, CLV*, CLZ*, EICALL, EIJMP, ELPM (1) ICALL, IJMP, LPM (1), NOP, RET, RETI, SEC*, SEH*, SEI*, SEN*, SES*, SET*, SEV* SEZ*, SLEEP, SPM.