TRANSISTOR SMALL SIGNAL AMPLIFIERS

Topic Outcomes

- Describe and analyze the operation of an amplifier
- Discuss the different transistor equivalent model
- Calculate different parameters for transistor amplifier

Introduction

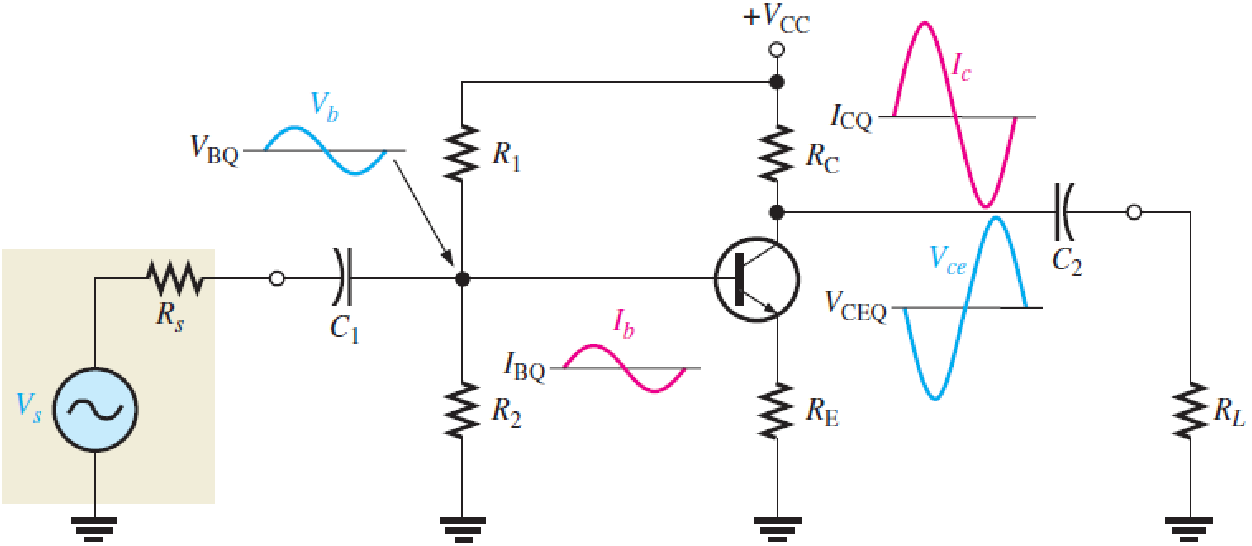
- This module will discuss how a transistor is used as a small signal amplifier.
- There are three models commonly used in the small-signal ac analysis of transistor networks: the $\mathbf{r_e}$ **model**, the **hybrid π model**, and the **hybrid equivalent model**.
- This module will emphasize the r_e model only.
- Small-signal refers to the use of signals that take up a relatively small percentage of an amplifier's operational range.
- This module will focus on converting transistor bias to its equivalent ac model by using r_e model.
- The students will learn how to reduce an amplifier to an equivalent dc and ac circuit for easier analysis. The applications of other theorem such as Kirchhoff's current and voltage law, etc. to determine the equations for different parameters is also covered by topic.
- Most importantly, the application of dc analysis contributes in determining ac resistance of BJT and current source of FET.

Amplifier Operation

- Now we know that in DC biasing, the transistor is purely DC operation.
- DC analysis in transistors are done to **establish an operating point (Q-point)** which variations of current and voltage occur in response to an input signal.
- In some applications where a small signal must be amplified, **variations about the Q-point are very small**. Small-signal amplifiers are designed to amplify small ac signals.
- Sometimes it refers to **linear amplification**.
- Applications where small signal voltages must be amplified include antennas and microphones.

Linear Amplification

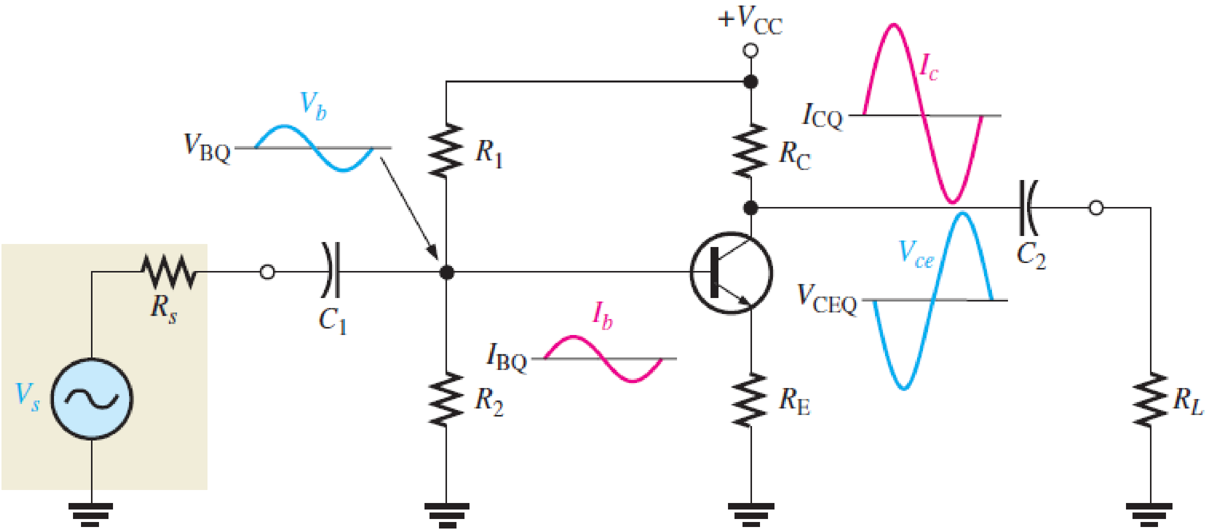
- A **linear amplifier** provides **amplification** of a signal **without any distortion** so that the **output signal** is an **exact amplified replica** of the input signal.
- A voltage-divider biased transistor with a sinusoidal ac source capacitively coupled to the base through C1 and a load capacitively coupled to the collector through C2 is shown in the figure. The **coupling capacitors block DC** and thus **prevent** the internal source resistance, R_S, and the load resistance, R_L, **from changing the dc bias voltages** at the base and collector.



Amplifier with voltage divider bias driven by an AC voltage source

Linear Amplification

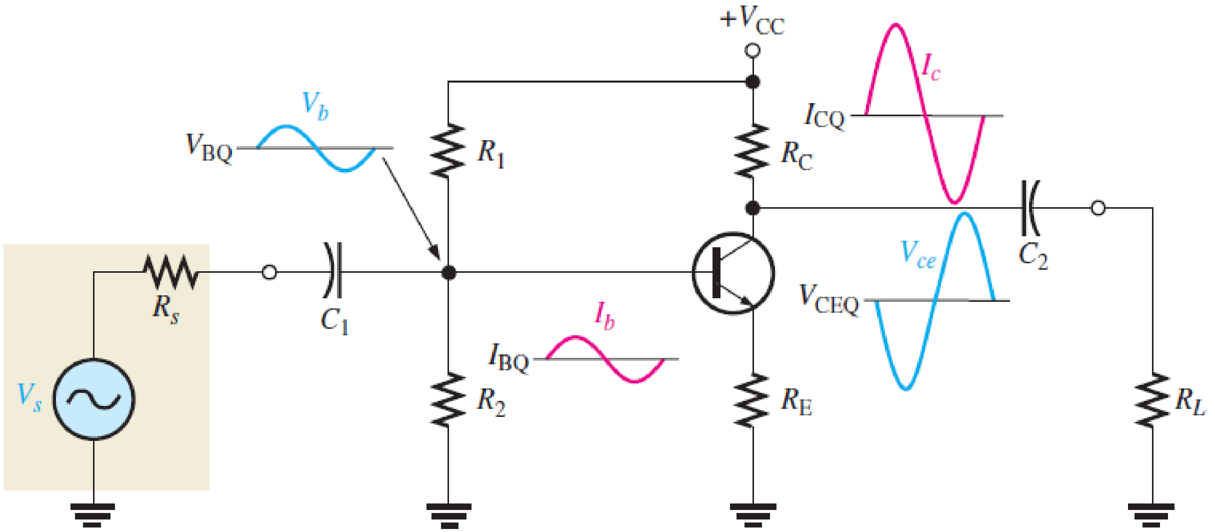
- The **capacitors** ideally appear as **shorts to the signal voltage**. The sinusoidal **source voltage** causes the **base voltage to vary** sinusoidally **above** and **below** its dc bias level, V_{BQ}. The **resulting variation** in base current **produces a larger variation** in collector current because of the current gain of the transistor.



Amplifier with voltage divider bias driven by an AC voltage source

Linear Amplification

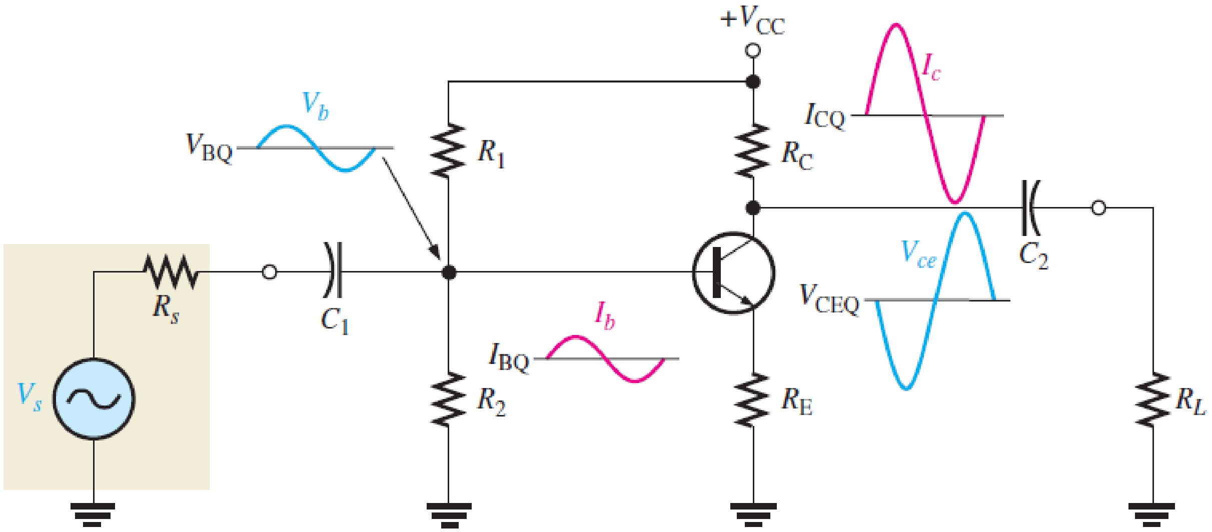
- As the **sinusoidal collector current increases**, the **collector voltage decreases**. The collector current varies above and below its Q-point value, I_{CQ}, in phase with the base current.



Amplifier with voltage divider bias driven by an AC voltage source

Linear Amplification

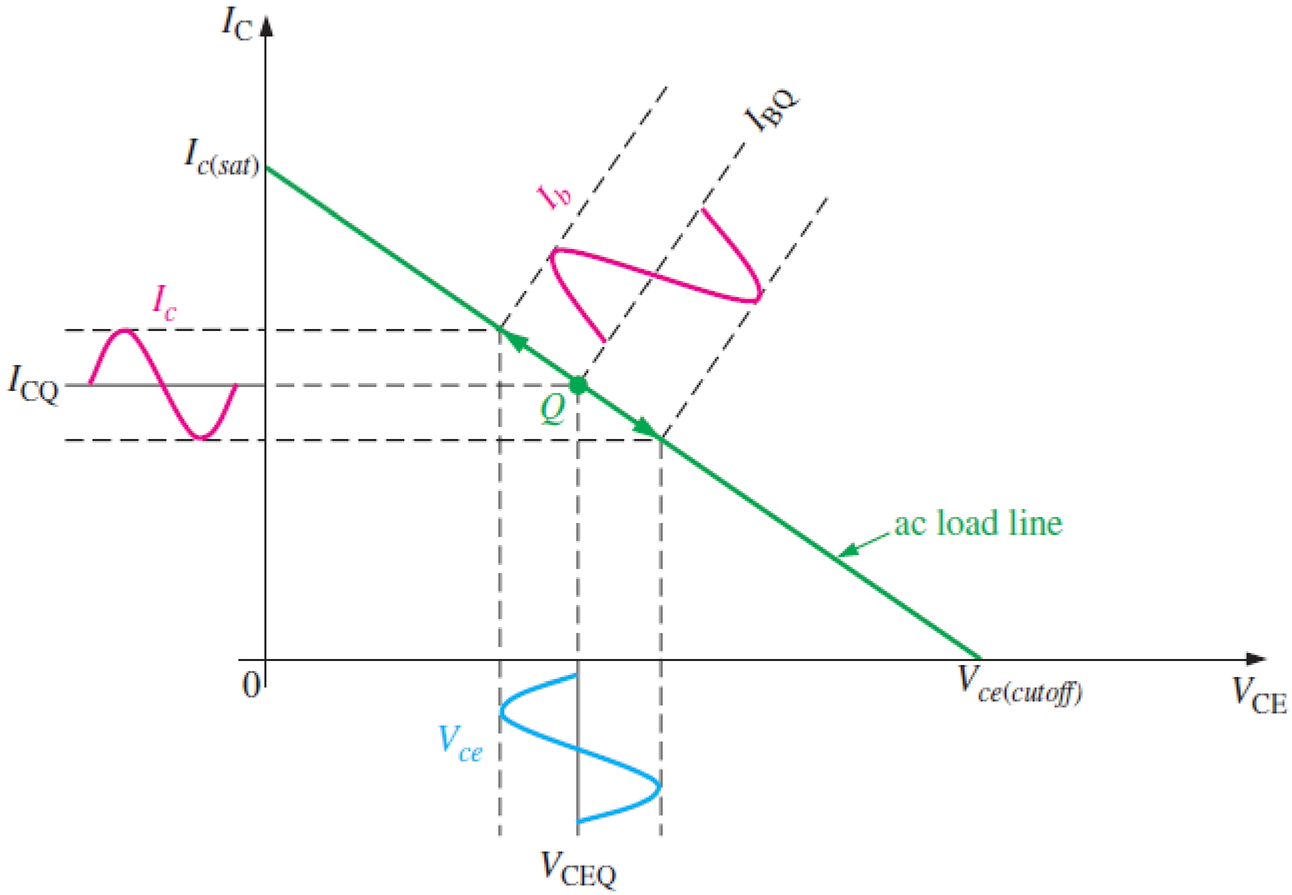
- The sinusoidal collector-to-emitter voltage varies above and below its Q-point value, V_{CEQ}, **180º out of phase** with the base voltage, as illustrated in the figure.
- A transistor always produces a **phase inversion** between the base voltage and the collector voltage.



Amplifier with voltage divider bias driven by an AC voltage source

Linear Amplification

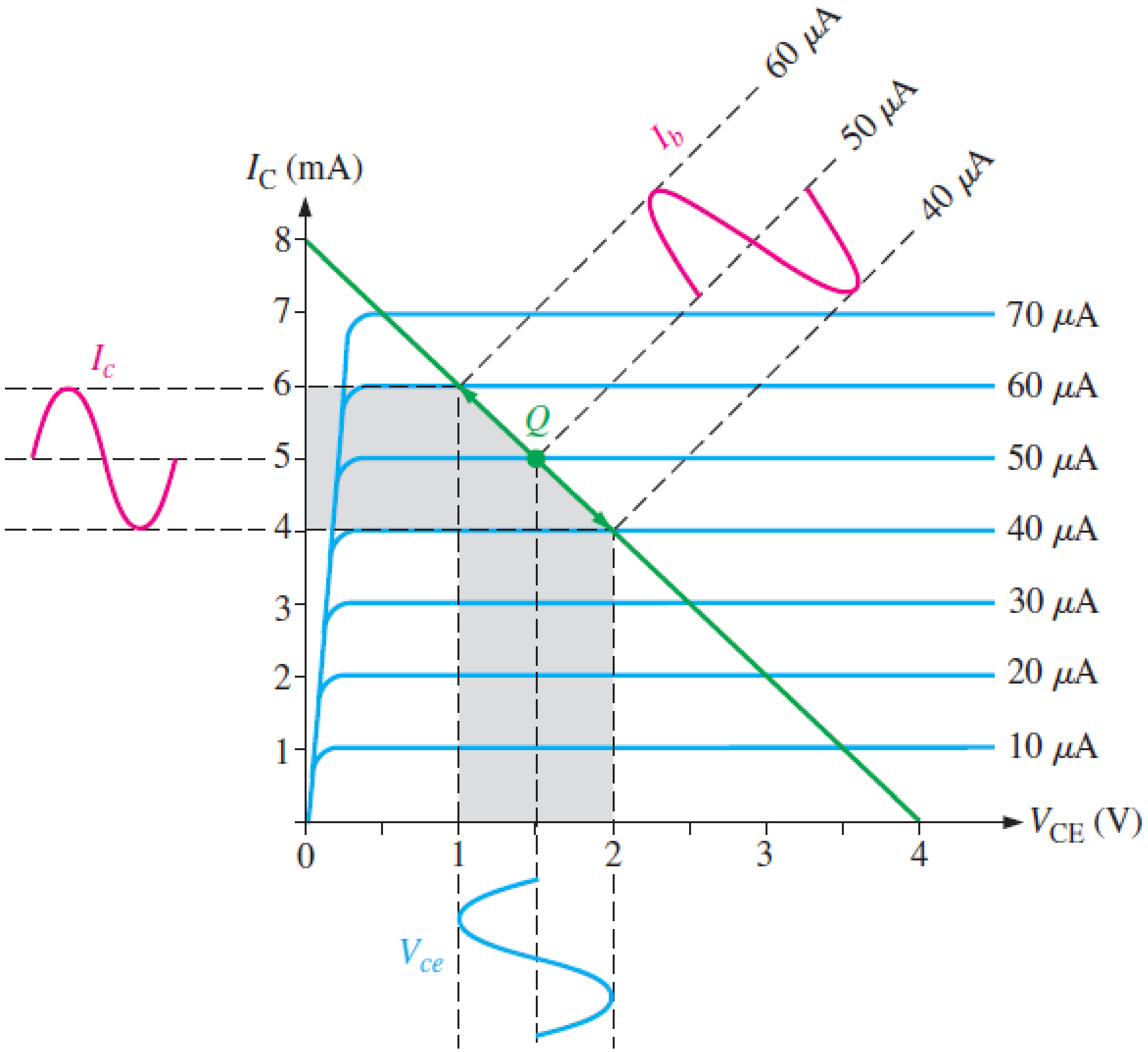
- The **AC signal varies along the AC load line**, which is different from the DC load line because the **capacitors are seen ideally as a short to the AC signal** but an open to the DC bias.
- The sinusoidal voltage at the base produces **a base current that varies above and below the Q-point** on the AC load line, shown by the arrows.



AC Load Line Operation of the Amplifier

Linear Amplification

- In this example, the load line extends 10μA above and below the Q-point base current value of 50 μA .
- The resulting peak to peak collector current is at 2 mA (varying from 4mA to 6mA)
- The resulting collector-to-emitter voltage is 1V (varying from 1V to 2V)



AC Load Line Operation of the Amplifier

BJT Small Signal Modelling

Transistor AC Models

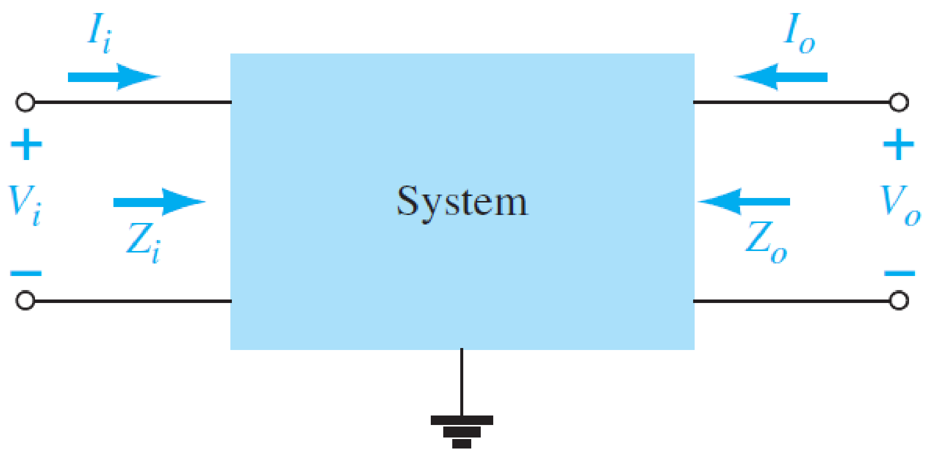
- Discuss transistor models
- List and define the r parameters
- Describe the r-parameter transistor model
- Determine r'e using a formula
- Compare ac beta and dc beta
- List and define the h parameters

BJT Small Signal Modelling

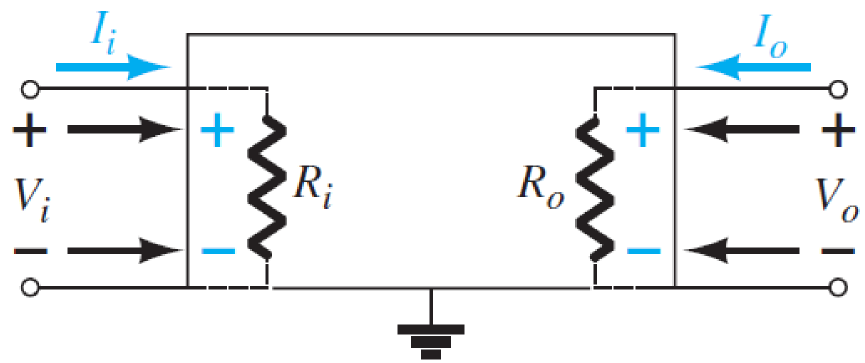
- A model is a **combination of circuit elements**, properly chosen, that best **approximates the actual behavior** of a semiconductor device under specific operating conditions.
- Once the AC equivalent circuit is determined, the schematic symbol for the device can be replaced by this equivalent model. The basic methods of circuit analysis applied to determine the desired small-signal parameters.
- Out of the three ac transistor modes (r_e model, the hybrid π model, and the hybrid equivalent model), the **r_e model became the more desirable approach**.
- This is because important parameters were determined by the actual conditions (rather than using data sheet values).

BJT Small Signal Modelling

- Both **input and output current are defined to enter to the system**.
- Notice that the output current is entering to the system rather than leaving, thus the negative sign must apply.
- If V_0 has the opposite polarity, a negative sign must be apply.
- Z_i is the impedance **“looking into”** the system” and Z_0 is the impedance **“looking back into”** the system.
- Looking in the 2nd figure, both input and output impedance are both positive values and resistive.



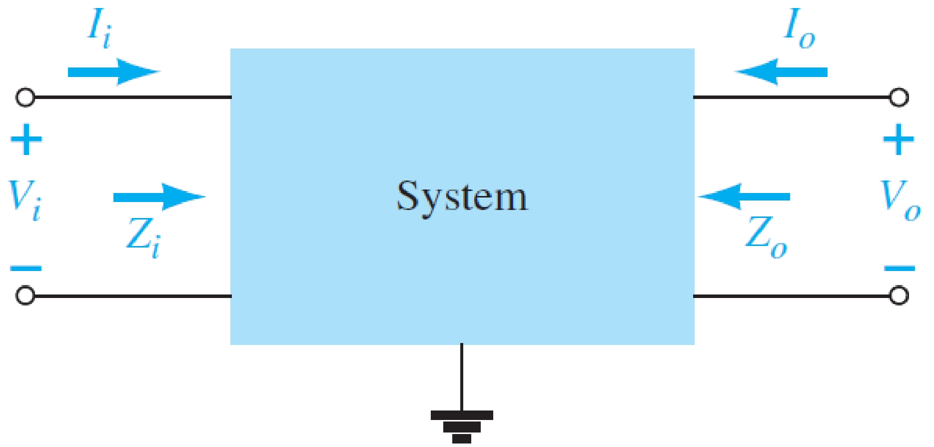
Defining the important parameters of any system



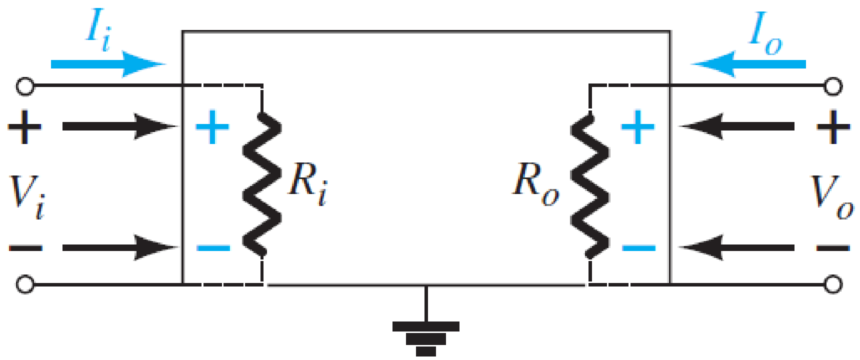
Defining the important parameters of any system

BJT Small Signal Modelling

- For the direction of I_i and I_0, the resulting voltage across the resistive elements will have the same polarity as V_i and V_0, respectively if not then a negative sign would be applied.
- For each $Z_i = V_i/I_i$ and $Z_0=V_0/I_0$ with positive results, if they all have defined directions and polarity in the 1st figure.
- If the output current of an actual system has a direction opposite to the equivalent network, a minus sign must be applied because the output voltage must be defined appearing in the 1st figure.



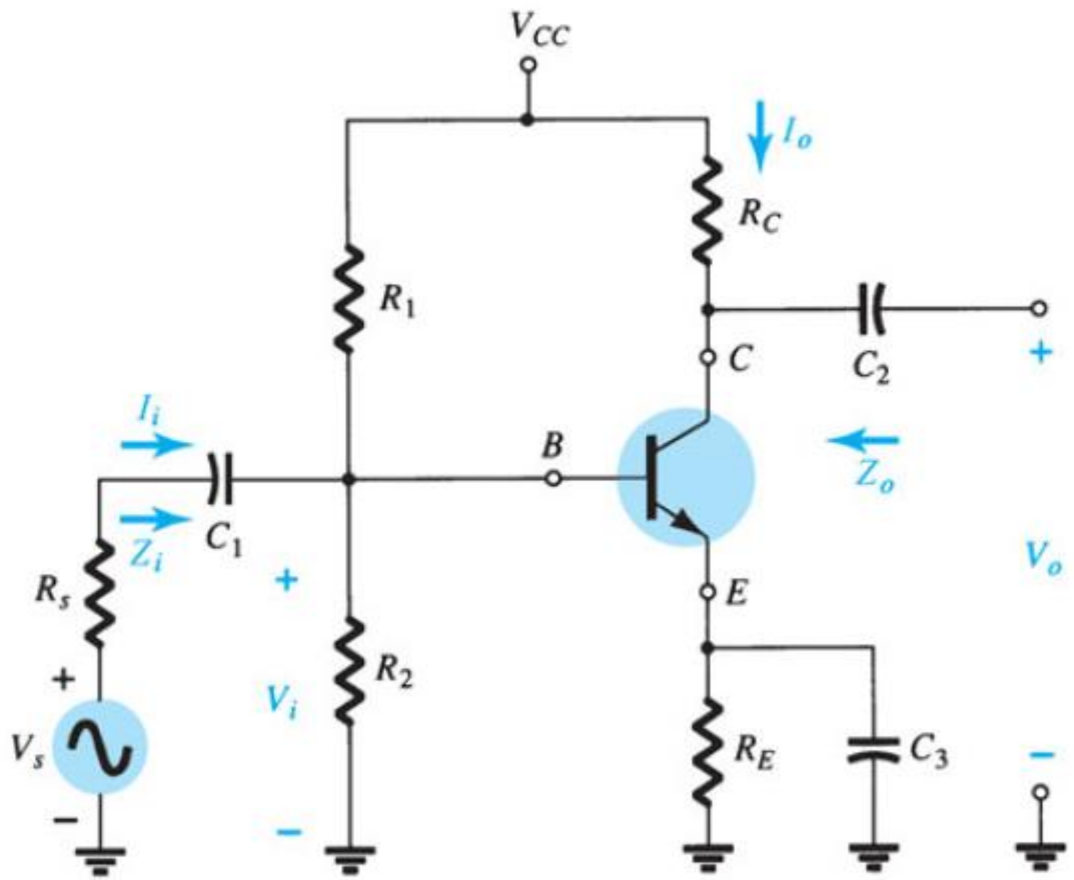
Defining the important parameters of any system



Defining the important parameters of any system

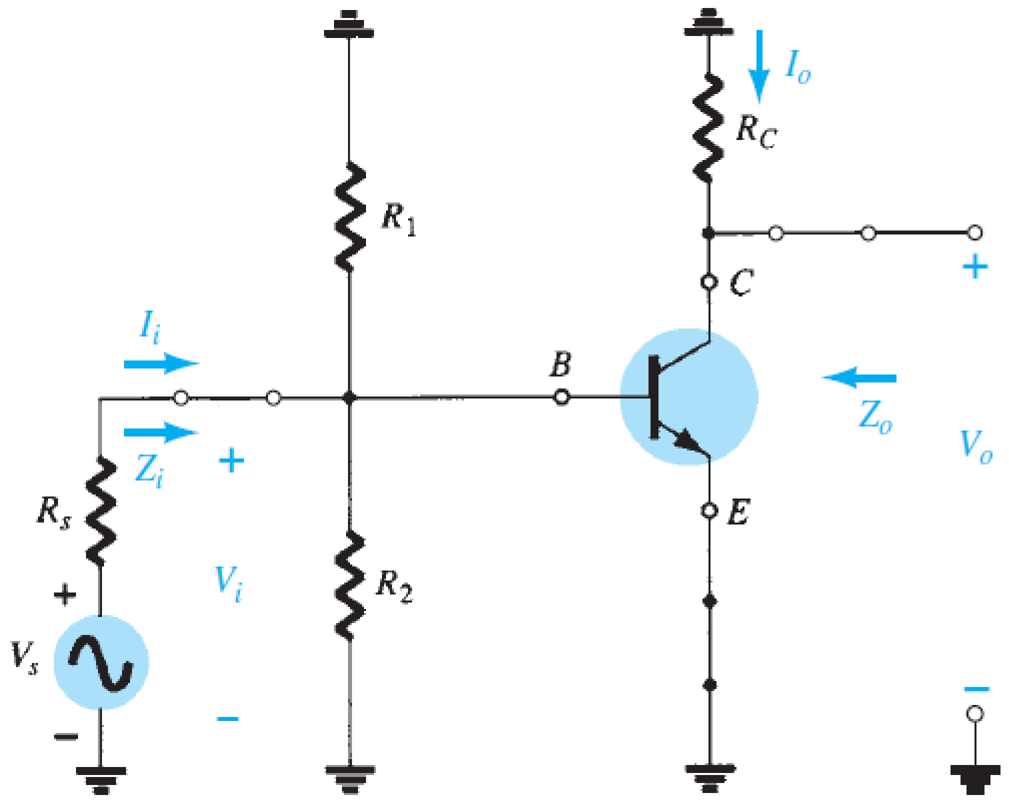
BJT Small Signal Modelling

- Steps in obtaining the AC equivalent of a transistor network
  1. Set all **DC sources to zero** and replace them with a **short-circuit** equivalent.
  2. Replace all **capacitors** by a **short-circuit** equivalent.
  3. Remove all elements bypassed by the short circuit
  4. Redraw the network in a more convenient and logical form
  5. Introduce the equivalent model of the transistor in the circuit.



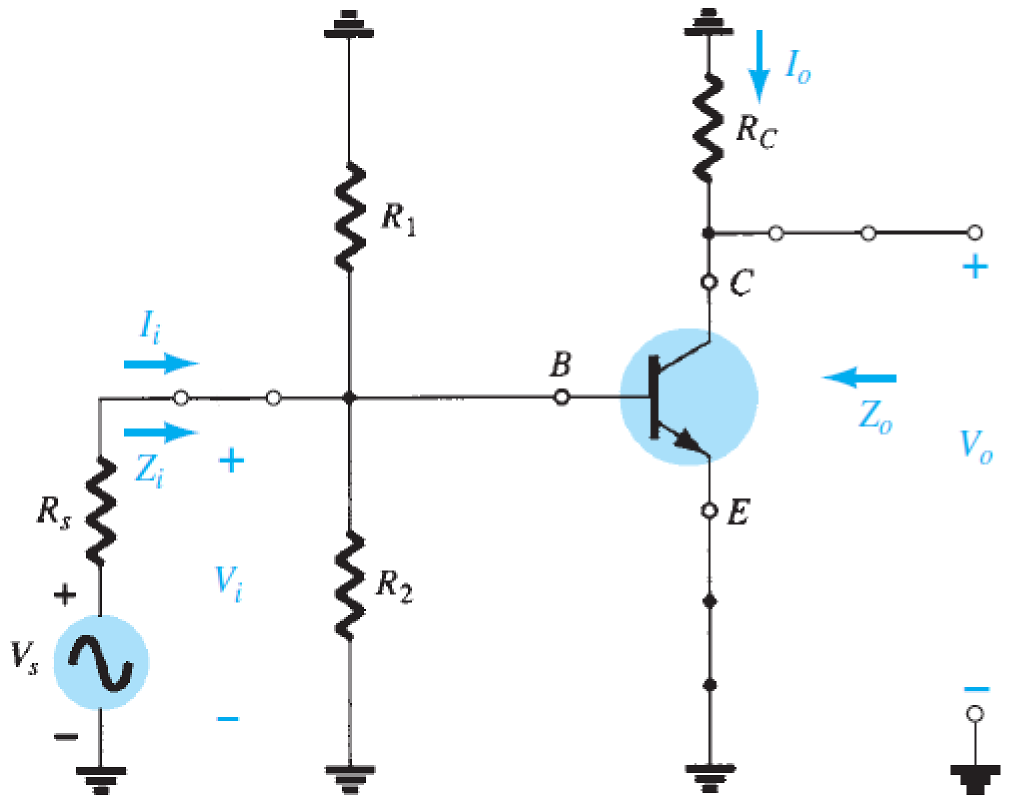
BJT Small Signal Modelling

- Steps in obtaining the AC equivalent of a transistor network
  1. Set all **DC sources to zero** and replace them with a **short-circuit** equivalent.
  2. Replace all **capacitors** by a **short-circuit** equivalent.
  3. Remove all elements bypassed by the short circuit
  4. Redraw the network in a more convenient and logical form
  5. Introduce the equivalent model of the transistor in the circuit.



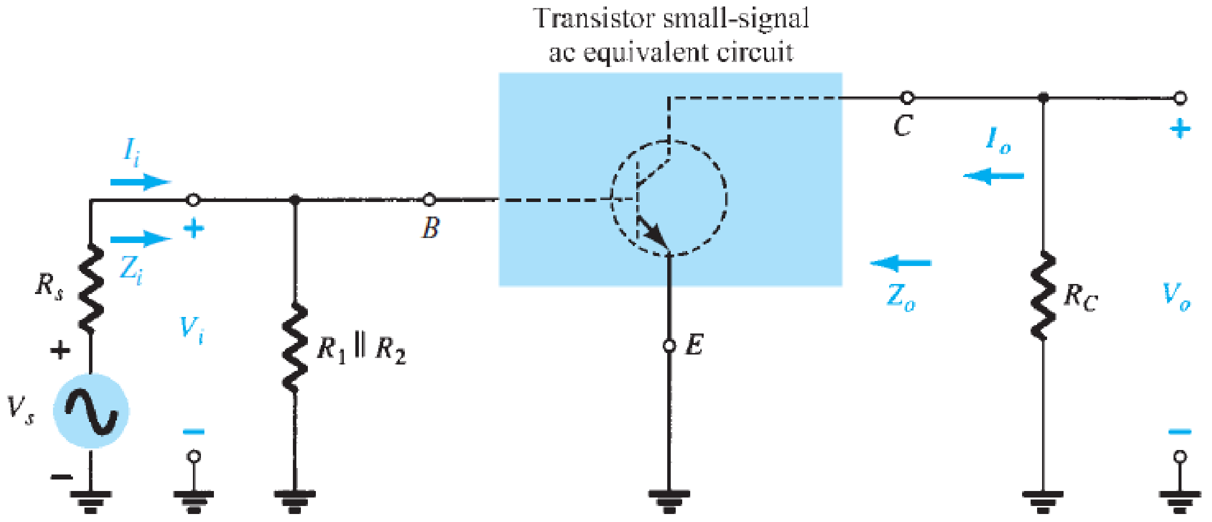
BJT Small Signal Modelling

- Steps in obtaining the AC equivalent of a transistor network
  1. Set all **DC sources to zero** and replace them with a **short-circuit** equivalent.
  2. Replace all **capacitors** by a **short-circuit** equivalent.
  3. Remove all elements bypassed by the short circuit
  4. Redraw the network in a more convenient and logical form
  5. Introduce the equivalent model of the transistor in the circuit.



BJT Small Signal Modelling

- Steps in obtaining the AC equivalent of a transistor network
  1. Set all **DC sources to zero** and replace them with a **short-circuit** equivalent.
  2. Replace all **capacitors** by a **short-circuit** equivalent.
  3. Remove all elements bypassed by the short circuit
  4. Redraw the network in a more convenient and logical form
  5. Introduce the equivalent model of the transistor in the circuit.



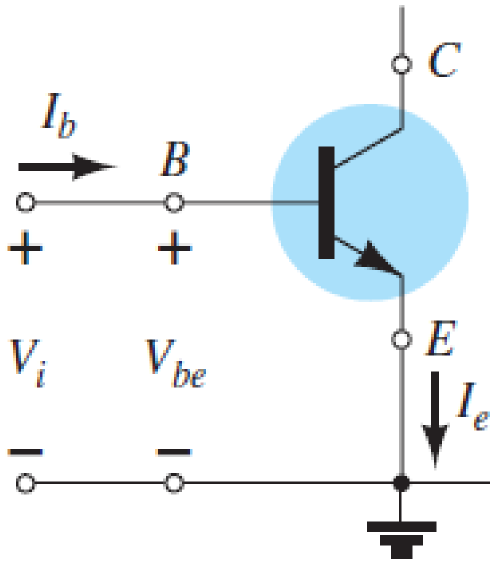
The r_e transistor model

r_e model

- The r_e model reflects the operation of the BJT at **mid-frequencies**.
- The r_e model is an equivalent network that is used to predict the performance of the transistor amplifier.
- r_e represents the resistance **looking into the emitter terminal** of a transistor.

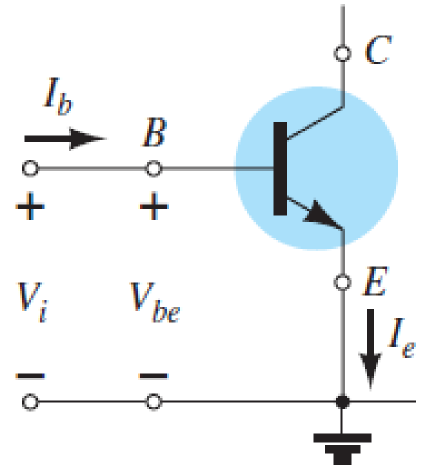
r_e model

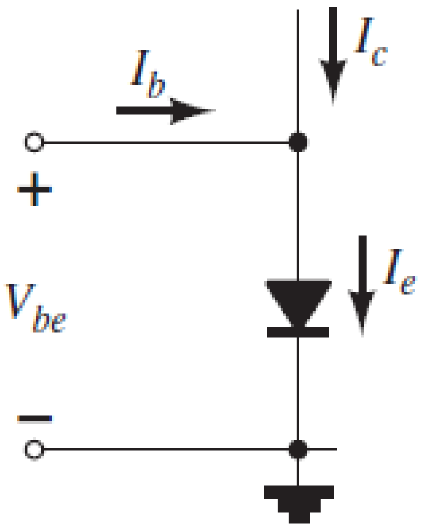
- Using the transistor characteristics and approximation, the equivalent circuit for common emitter configuration is shown.
- Notice that the applied voltage v_i is same as the voltage across-base emitter v_{be} with the input current being the base current.



r_e model

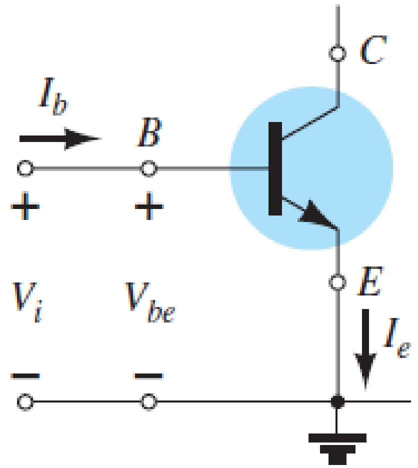
- Using the transistor characteristics and approximation, the equivalent circuit for common emitter configuration is shown.
- Notice that the applied voltage v_i is same as the voltage across-base emitter v_{be} with the input current being the base current.

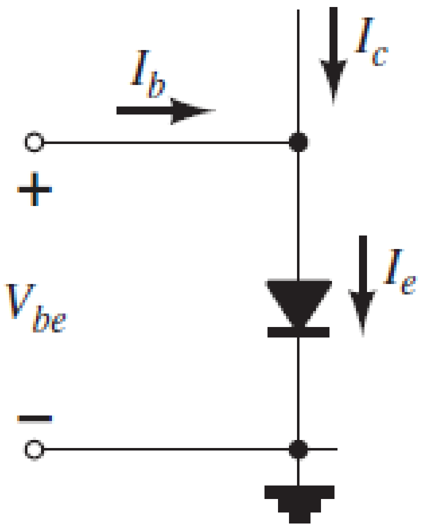




r_e model

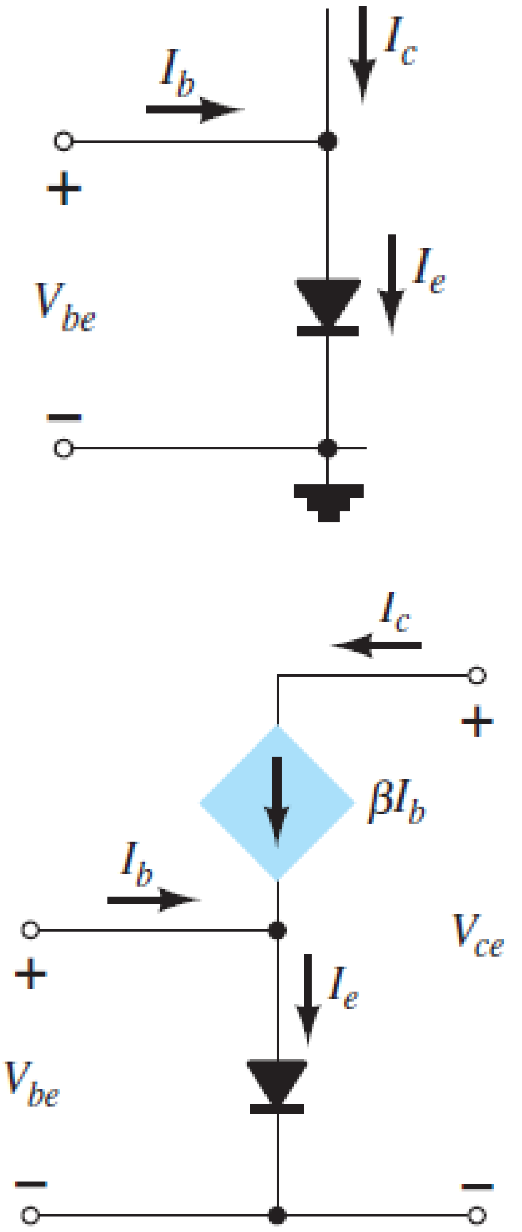
- Given a different level of current I_E, the characteristic curve of the voltage across the base-emitter V_{be} is the same to a forward biased diode.
- Therefore, the input side is simply a single diode with current I_e as shown in the figure.





r_e model

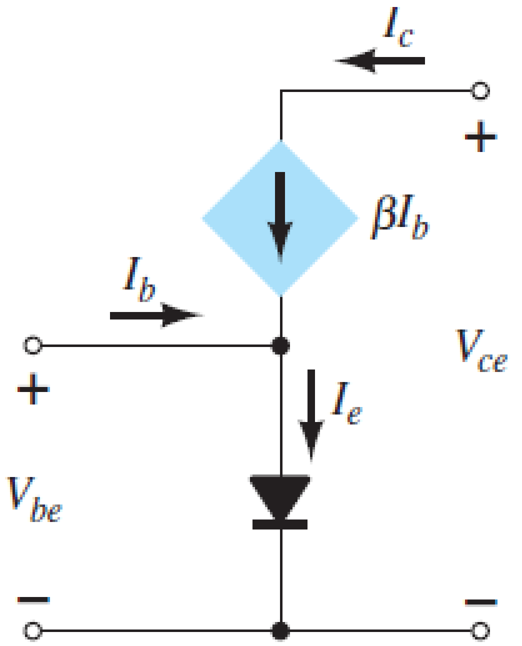
- To establish a component of the network that will relate I_e to the output characteristics, the output section can be replaced by a controlled source whose magnitude is beta times the base current (βI_b)



r_e model

- The model can be improved by first replacing the diode by its equivalent resistance as determined by the level of I_E (quiescent emitter current).
- Since diode AC resistance is

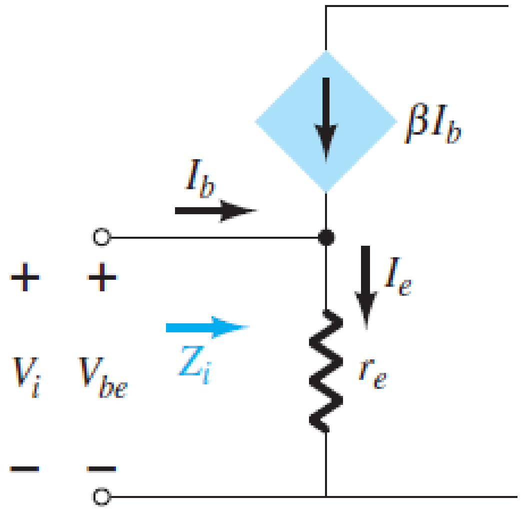
$$\mathrm{r_d} = 26mV/I_D \therefore r_e = 26mV/I_E$$



$$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

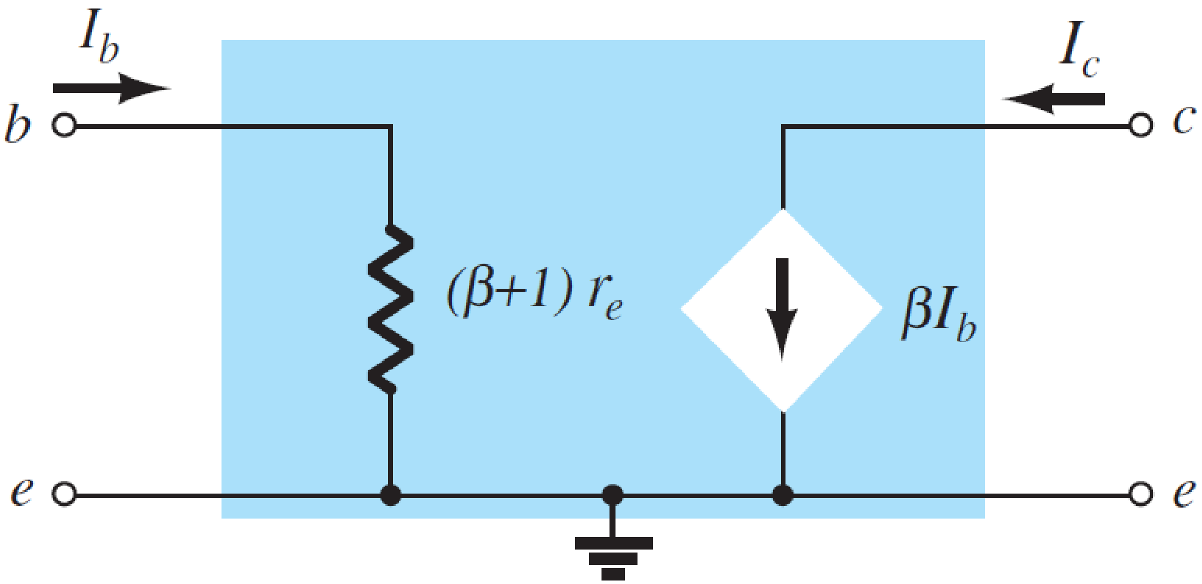
Solving for V_{be}:

$$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$
$$V_{be} = (\beta + 1) I_b r_e$$
$$Z_i = \frac{(\beta + 1) I_b r_e}{I_b}$$
$$Z_i = (\beta + 1) r_e \cong \beta r_e$$



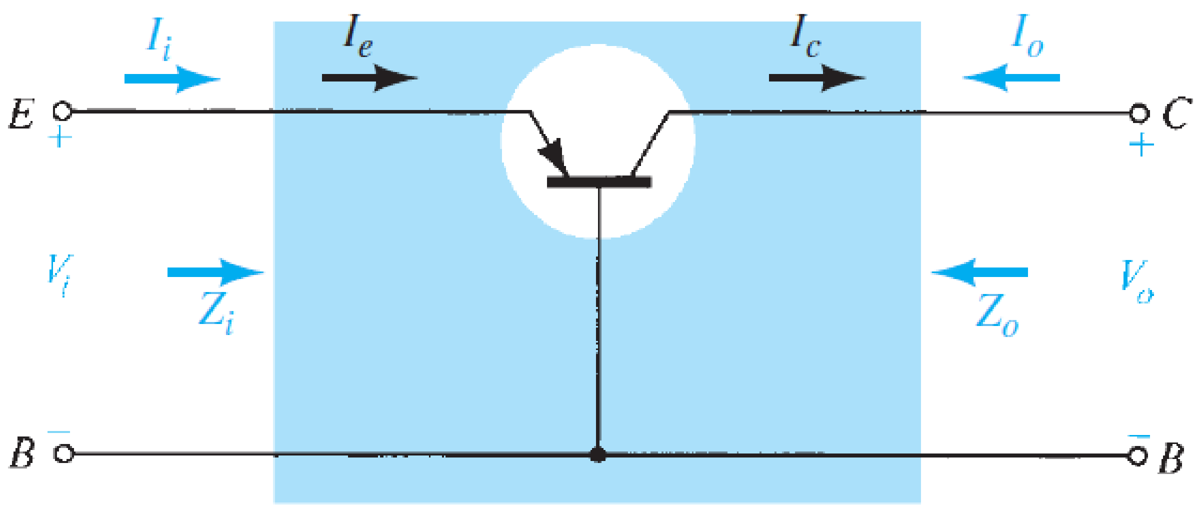
r_e model

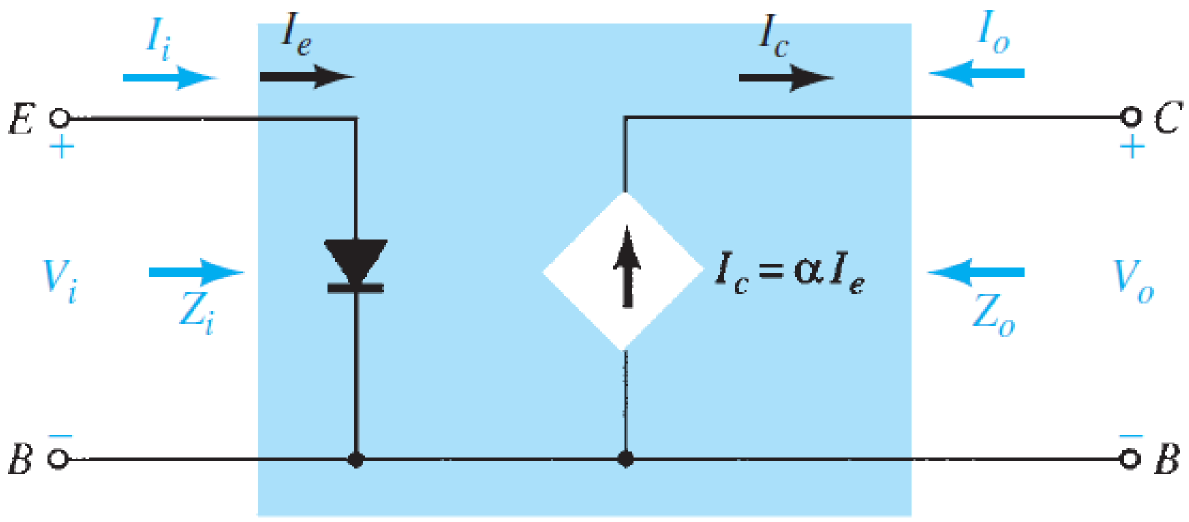
- The result Z_i is the impedance seen “looking into” the base of the network.



r_e model

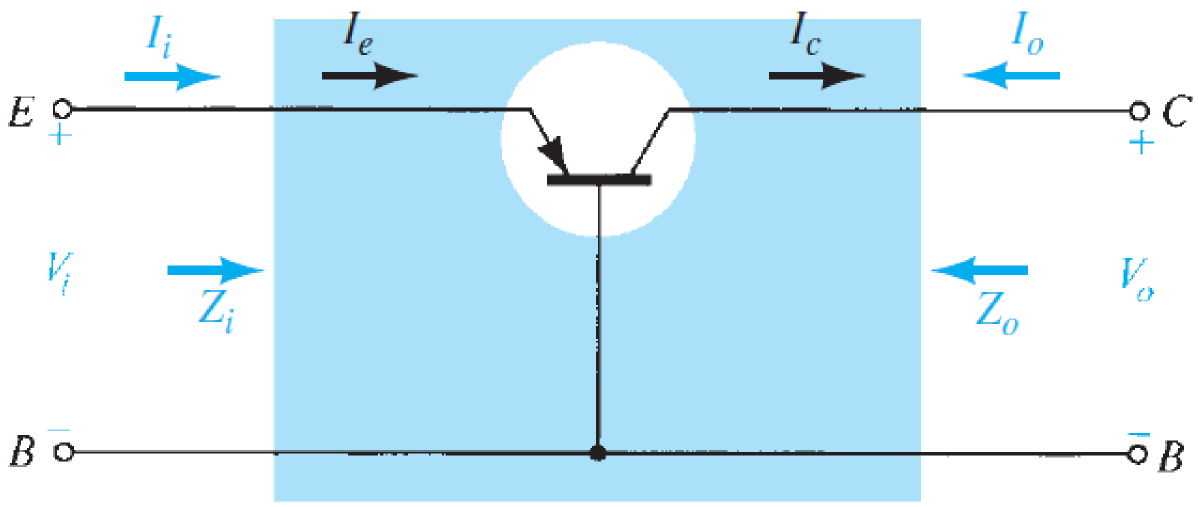
- For common base configuration, the same steps could be done and would result in the circuit below.

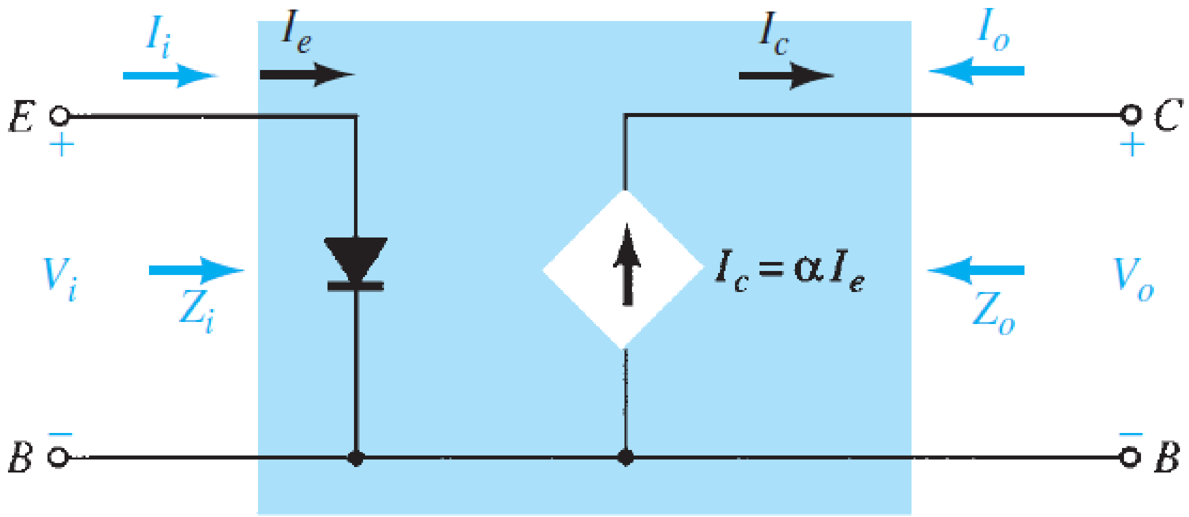




r_e model

- Zi is the impedance “looking into” the system, whereas Zo is the impedance “looking back into” the system from the output side.
- Av is the voltage gain; Av=Vo/Vi



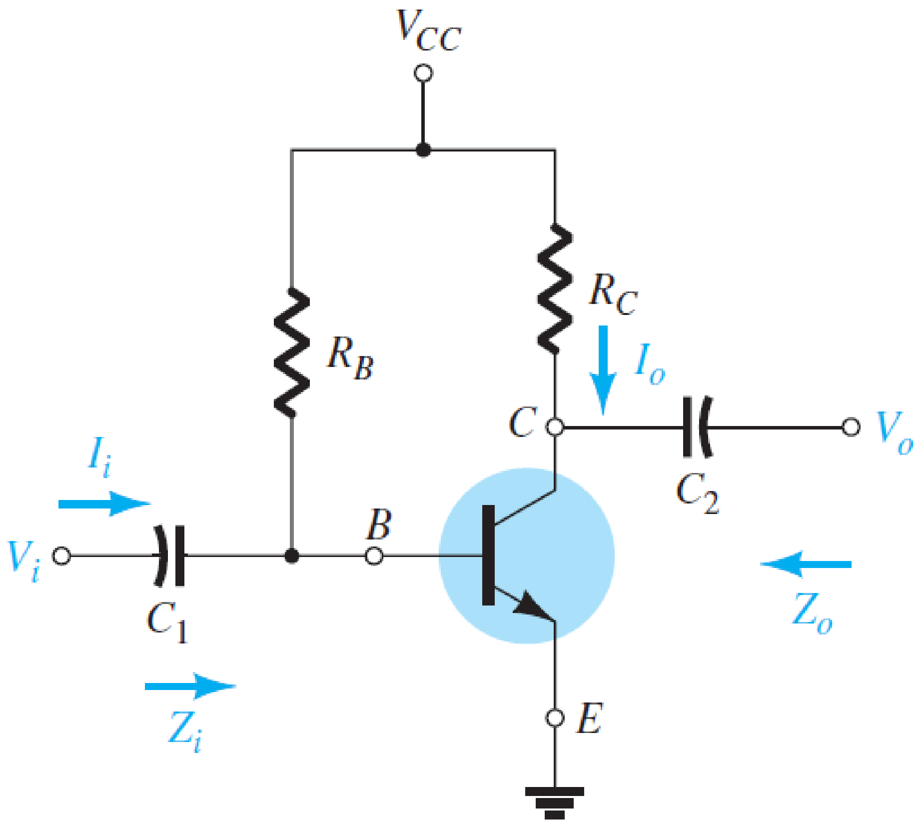


Small Signal Analysis

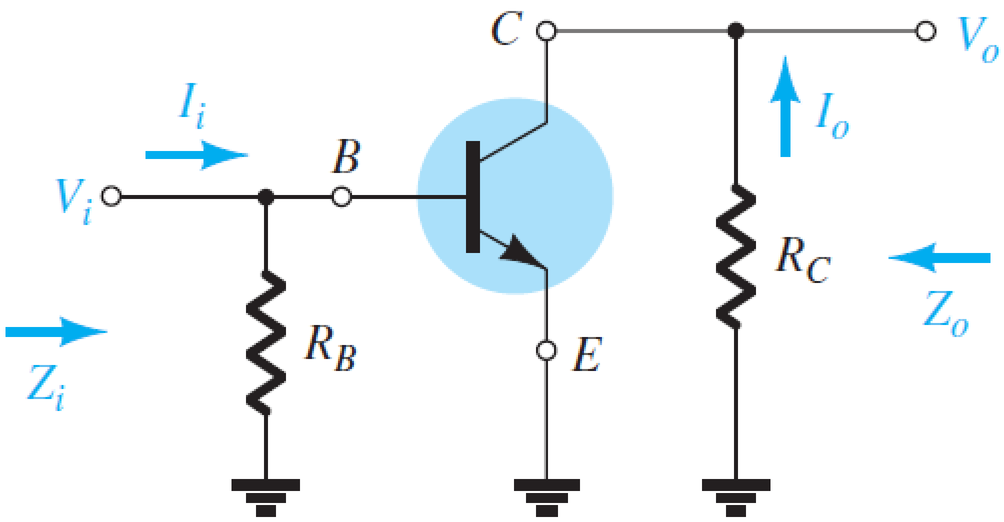
Small Signal Analysis Procedure

1. Perform DC Analysis
2. Compute internal model parameters
3. Draw the AC small signal equivalent
4. Perform the circuit analysis.

Common Emitter Fixed Bias Configuration

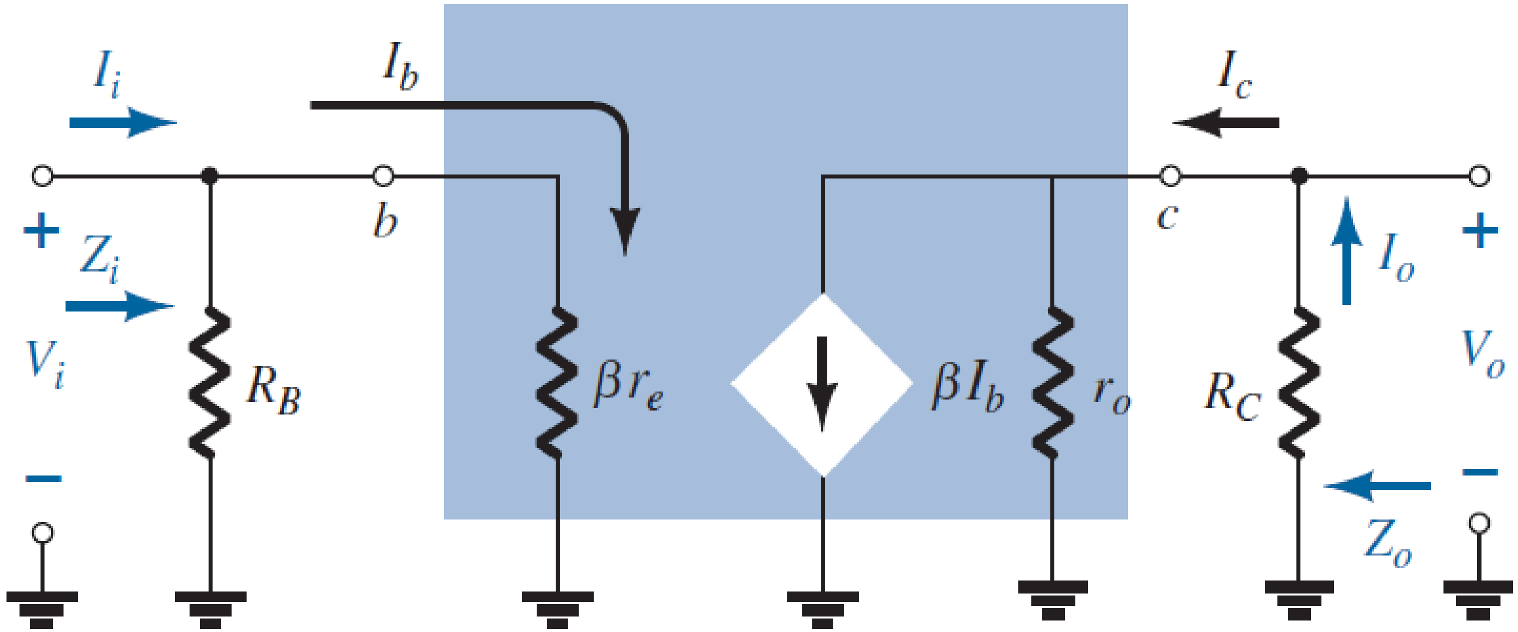


Common Emitter Fixed Bias Configuration



Circuit after removing elements bypassed by short-circuit

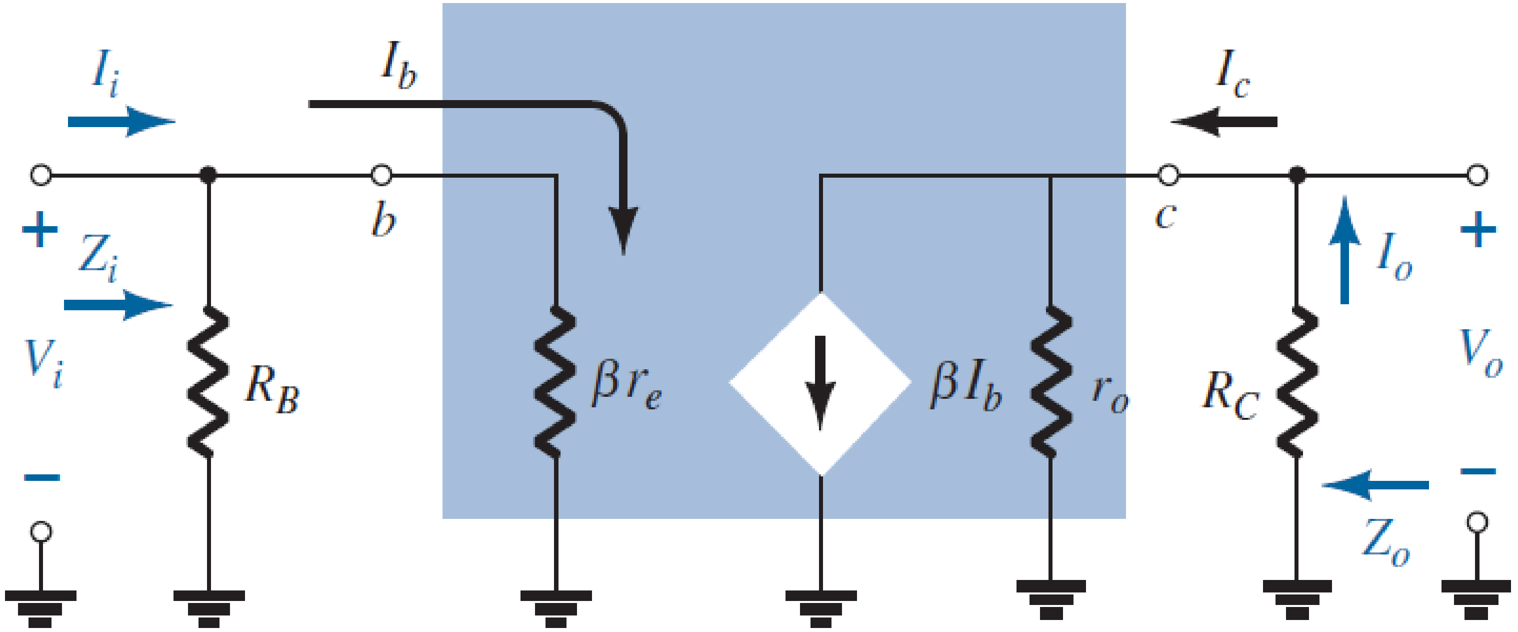
Common Emitter Fixed Bias Configuration



Substituting the r_e model into the network

Common Emitter Fixed Bias Configuration

Parameters to be obtained:
Z_i - input impedance
Z_0 – output impedance
A_V – Voltage gain

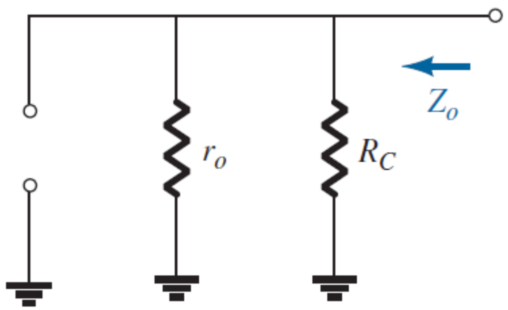


$$\boldsymbol{Z_i = R_B || \beta r_e}$$

$$If\ R_B \geq 10\beta r_e\ ;\ \boldsymbol{Z_i \cong \beta r_e}$$

$$\boldsymbol{Z_o = R_C || r_o}$$

$$If\ r_o \geq 10R_C\ ;\ \boldsymbol{Z_o \cong R_C}$$



Common Emitter Fixed Bias Configuration

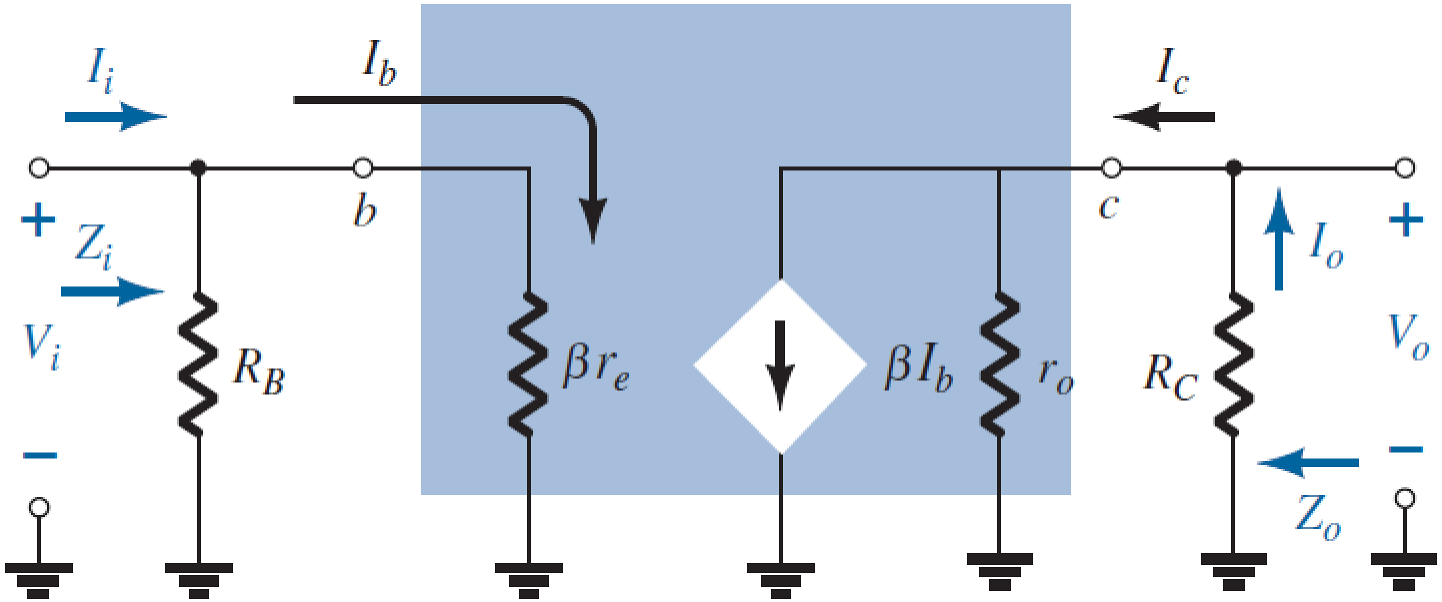
Parameters to be obtained:
Z_i - input impedance
Z_0 – output impedance
A_V – Voltage gain

$$V_o = -(\beta I_b)(R_C||r_o);\ I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C||r_o) = -\frac{V_i(R_C||r_o)}{r_e}$$

$$\boldsymbol{A_v = \frac{V_o}{V_i} = -\frac{R_C||r_o}{r_e}}$$

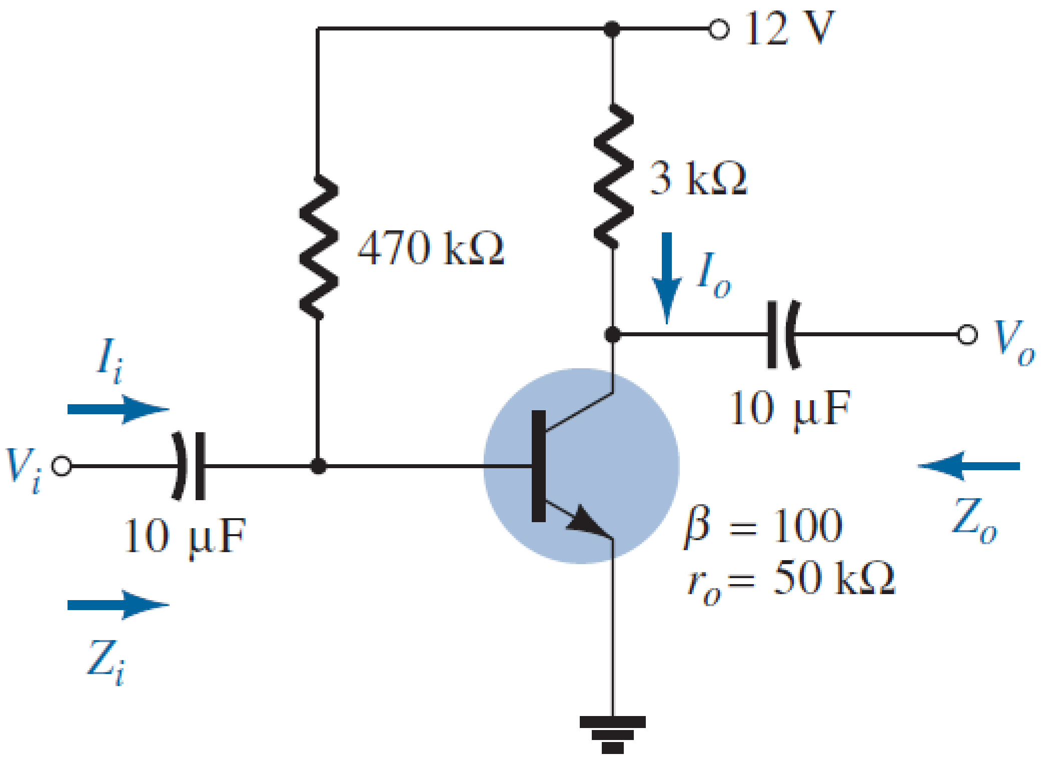
$$If\ r_o \geq 10R_C\ ;\boldsymbol{A_v = -\frac{R_C}{r_e}}$$



Common Emitter Fixed Bias Configuration

For the given network:

- a. Determine re.
- b. Find Zi (with ro =∞Ω).
- c. Calculate Zo (with ro = ∞Ω).
- d. Determine av (with ro = ∞Ω).
- e. Repeat parts (c) and (d) including ro = 50 k Ω in all calculations and compare results.



Common Emitter Fixed Bias Configuration

Solution

- a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12V - 0.7V}{470k\Omega} = 24.04\mu A$$

$$I_E = (\beta + 1)I_B = 101(24.05\mu A) = 2.428mA$$

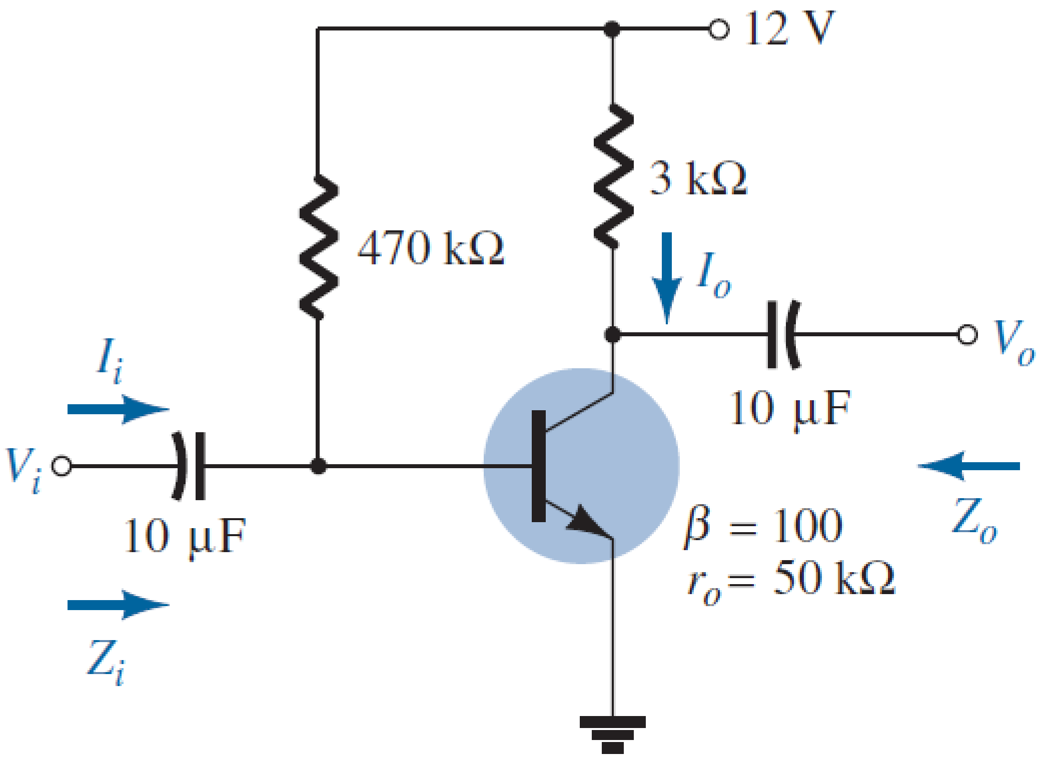
$$r_e = \frac{26mV}{I_E} = \frac{26mV}{2.428mA} = \mathbf{10.71\Omega}$$

- b. $\beta r_e = (100)(10.71\Omega) = 1.071k\Omega$

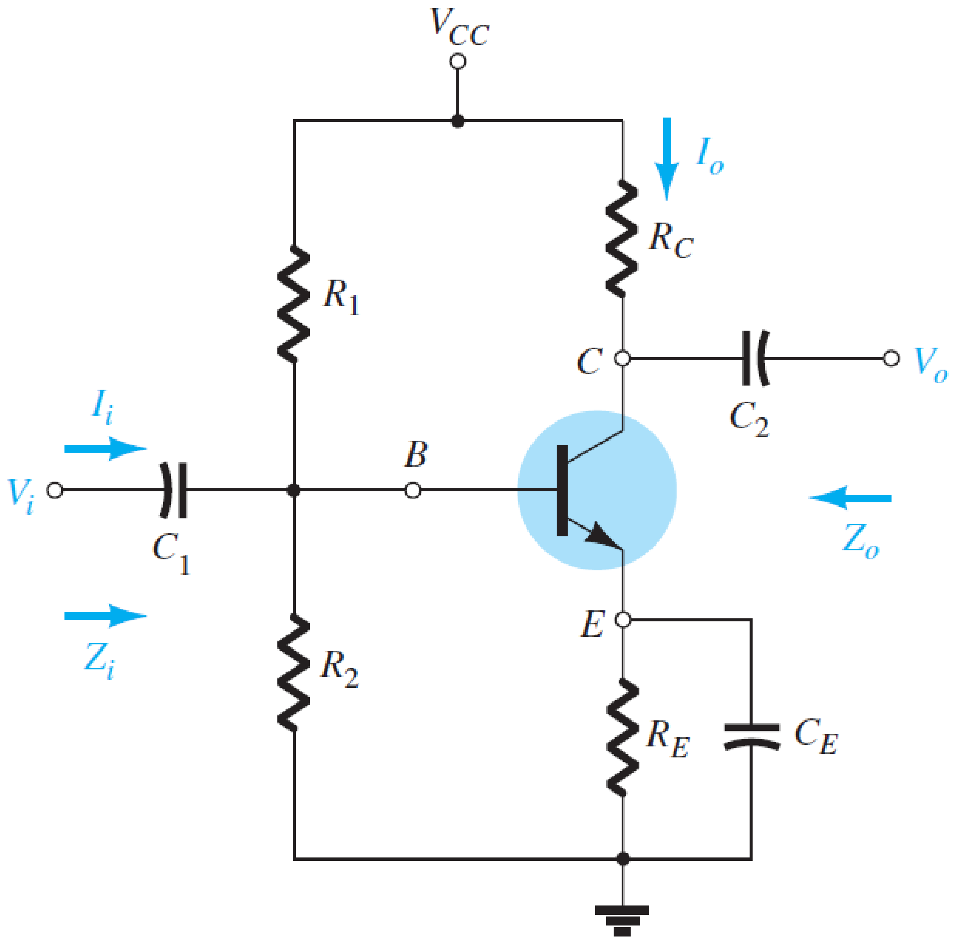
$$Z_i = R_B||\beta r_e = 470k\Omega||1.071k\Omega = \mathbf{1.07k\Omega}$$

- c. $Z_o = R_C = \mathbf{3k\Omega}$
- d. $A_v = -\frac{R_C}{r_e} = \frac{3k\Omega}{10.71\Omega} = \mathbf{-280.11}$
- e. $Z_o = R_C||r_o = 50k\Omega\,||\,3k\Omega = \mathbf{2.83k\Omega}\ vs\ 3k\Omega$

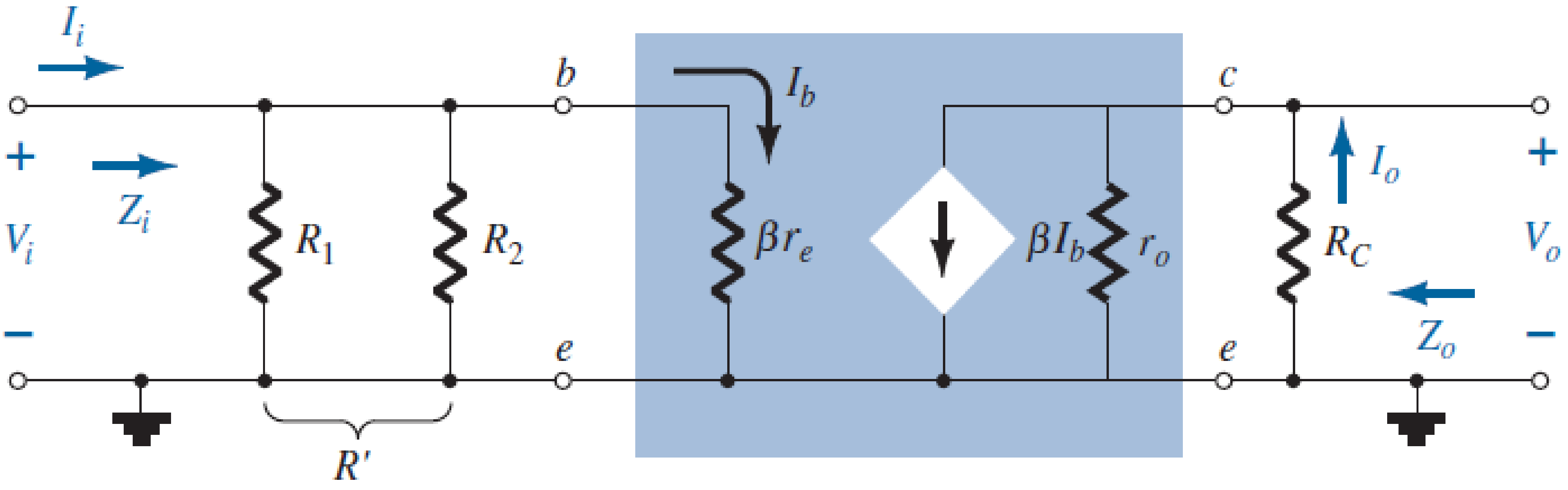
$$A_v = -\frac{ro||R_C}{r_e} = -\frac{2.83k\Omega}{10.71\Omega} = \mathbf{-264.24}\ vs\ -280.11$$



Common Emitter Voltage Divider Bias Configuration

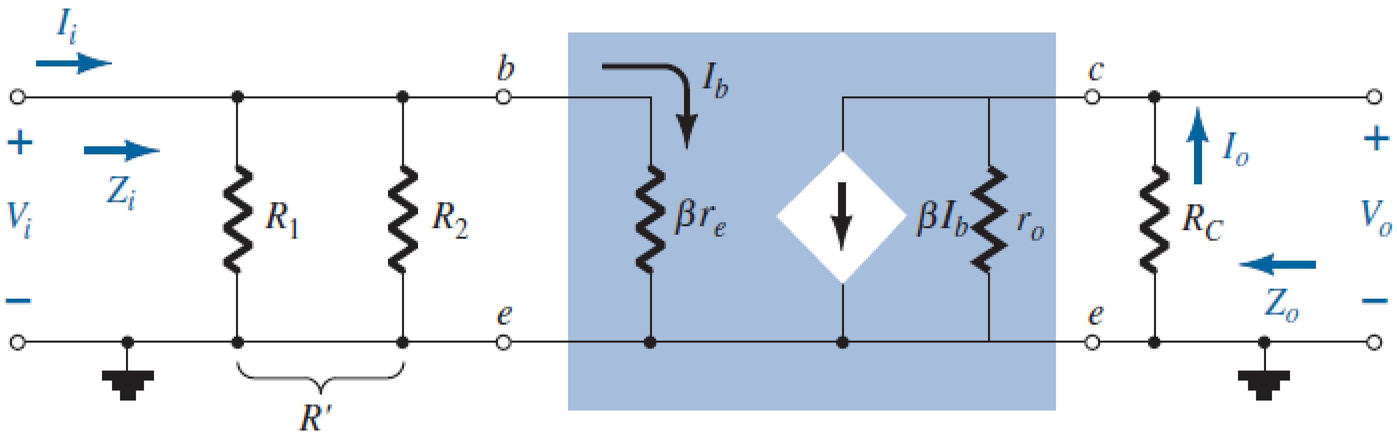


Common Emitter Voltage Divider Bias Configuration



Common Emitter Voltage Divider Bias Configuration

Parameters to be obtained:
Z_i - input impedance
Z_0 – output impedance
A_V – Voltage gain



$$Z_i = R_1||R_2||\beta r_e$$

$$Z_o = R_C||r_o$$
$$If\ r_o \geq 10R_C\ ; Z_o \cong R_C$$

$$V_o = -(\beta I_b)(R_C||r_o);\ I_b = \frac{V_i}{\beta r_e}$$

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C||r_o) = -\frac{V_i(R_C||r_o)}{r_e}$$

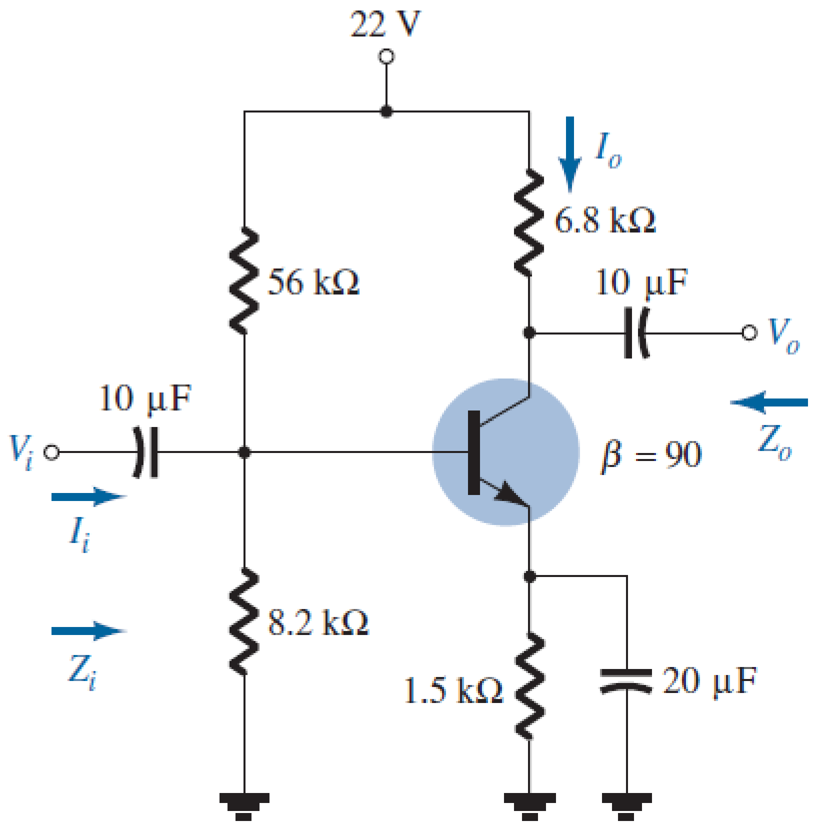
$$A_v = \frac{V_o}{V_i} = -\frac{R_C||r_o}{r_e}$$

$$If\ r_o \geq 10R_C\ ; A_v = -\frac{R_C}{r_e}$$

Common Emitter Voltage Divider Bias Configuration

For the given network:

- a. Determine re.
- b. Find Zi (with ro =∞Ω).
- c. Calculate Zo (with ro = ∞Ω).
- d. Determine av (with ro = ∞Ω).
- e. The parameters of parts (b) through (d) if ro = 50 k Ω and compare results.



Common Emitter Voltage Divider Bias Configuration

Solution

- a. DC analysis: Testing $\beta R_E > 10R_2$, 90(1.5kΩ)>10(8.2kΩ)=135kΩ>82kΩ

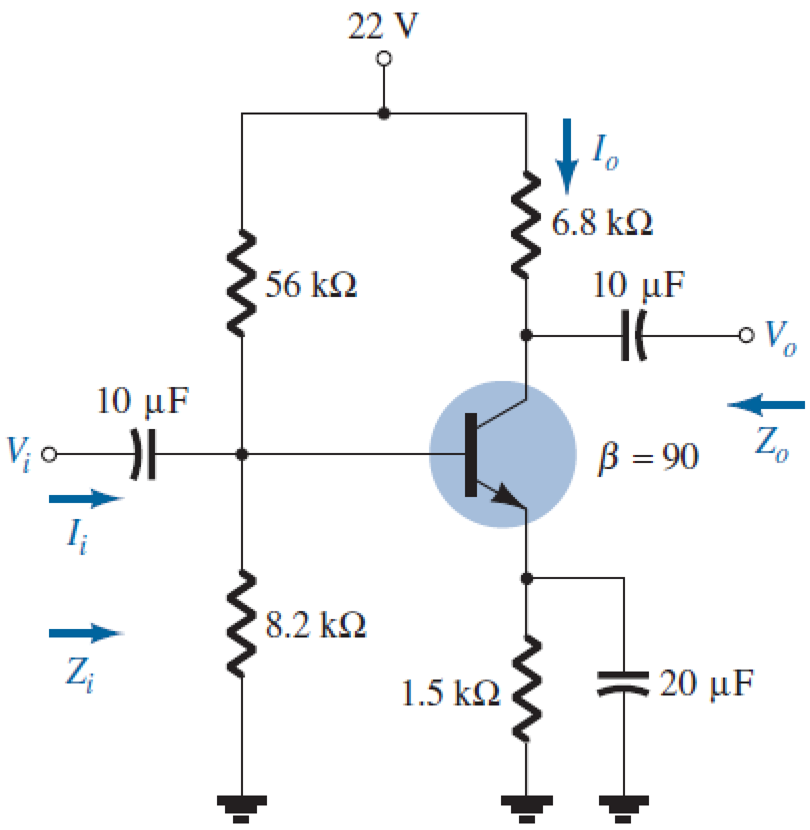
Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{8.2\text{k}\Omega(22V)}{56\text{k}\Omega + 8.2k\Omega} = 2.81V$$

$$V_E = V_B - V_{BE} = 2.81V - 0.7V = 2.11V$$

$$I_E = \frac{V_E}{R_E} = \frac{2.11V}{1.5k\Omega} = 1.41mA$$

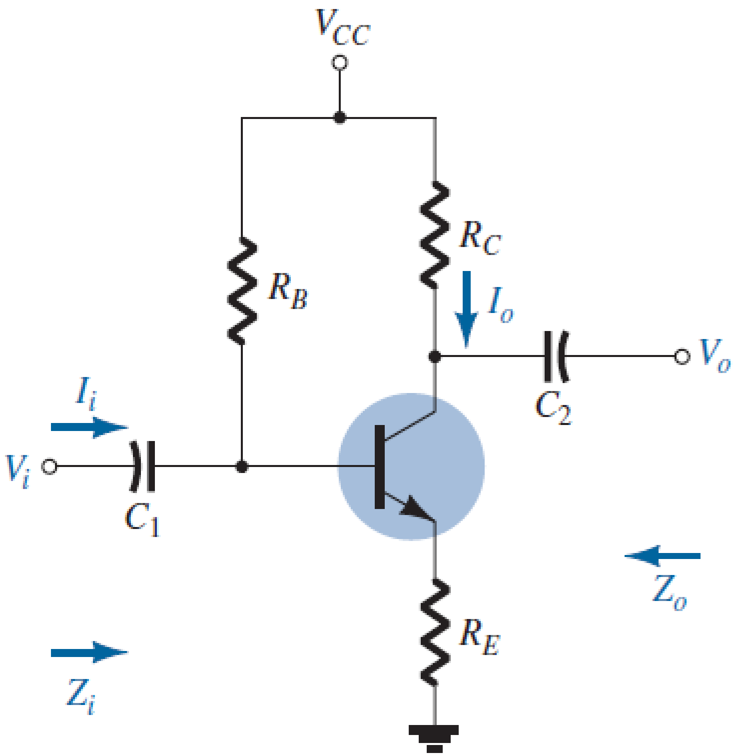
$$r_e = \frac{26mV}{I_E} = \frac{26mV}{1.41mA} = \mathbf{18.44\Omega}$$

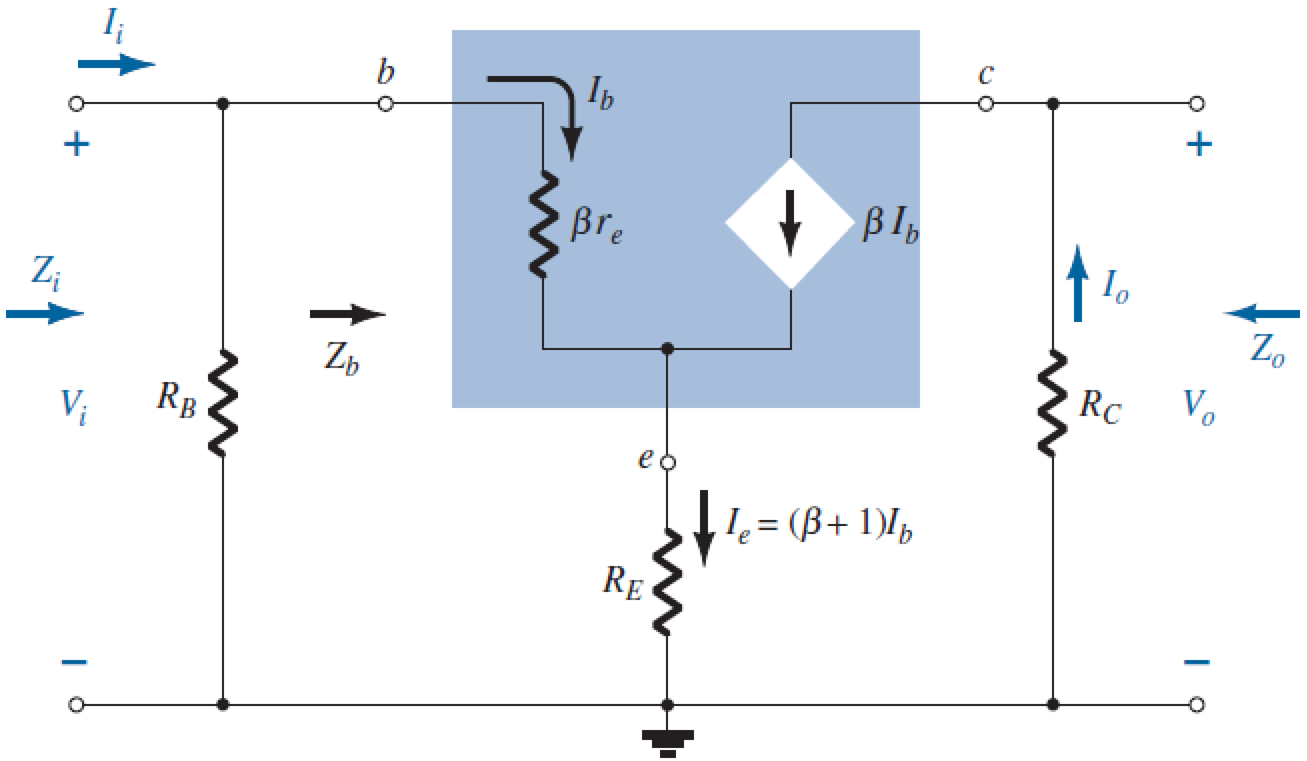


- b. $Z_i = R_1||R_2||\beta r_e = 56k\Omega||8.2k\Omega||(90)(18.44\Omega) = \mathbf{1.35k\Omega}$
- c. $Z_o = R_C = \mathbf{6.8k\Omega}$
- d. $A_v = -\frac{R_C}{r_e} = \frac{6.8\text{k}\Omega}{18.44\Omega} = \mathbf{-368.76}$
- e. $Z_i = \mathbf{1.35k\Omega}$; $Z_o = R_C||r_o = 6.8\text{k}\Omega\,||\,50\text{k}\Omega = \mathbf{5.89k\Omega}\ vs\ 6.8k\Omega$

$$A_v = -\frac{ro||R_C}{r_e} = -\frac{5.89\text{k}\Omega}{18.44\Omega} = \mathbf{-324.3}\ vs\ -368.76$$

Common Emitter-Bias (Unbypassed) Configuration





Common Emitter Emitter-Bias (Unbypassed)Configuration

Parameters to be obtained:

Z_i - input impedance

Z_0 – output impedance

A_V – Voltage gain

$$V_i = I_b\beta r_e + I_e R_E ; = I_b\beta r_e + (\beta + 1) I_b R_E$$

$$\boldsymbol{Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1) R_E \cong \beta(r_e + R_E)}$$

$$\boldsymbol{Z_i = R_B \parallel Z_b}$$

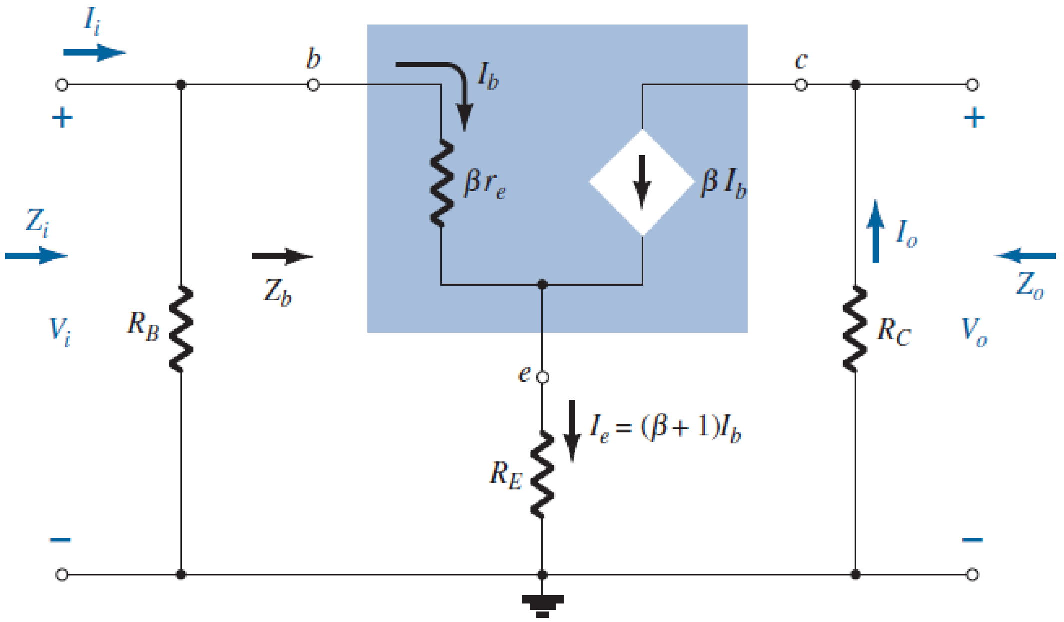
$$\boldsymbol{Z_O = R_C}$$

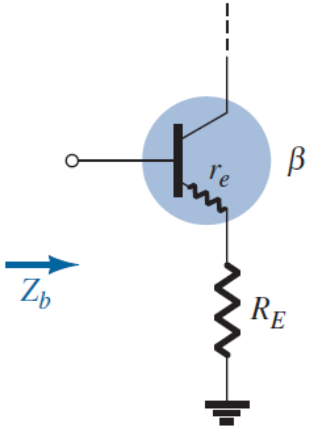
$$I_b = \frac{V_i}{Z_B} \; ; \; V_o = -I_o R_C = -\beta I_b R_C = -\beta\left(\frac{V_i}{Z_B}\right) R_C$$

$$\boldsymbol{A_V = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_B}}$$

If $Z_b \cong \boldsymbol{\beta(r_e + R_E)}$; $A_V = \frac{V_o}{V_i} \cong \frac{R_C}{r_e + R_E}$

If $Z_b \cong \boldsymbol{\beta(R_E)}$; $A_V = \frac{V_o}{V_i} \cong \frac{R_C}{R_E}$





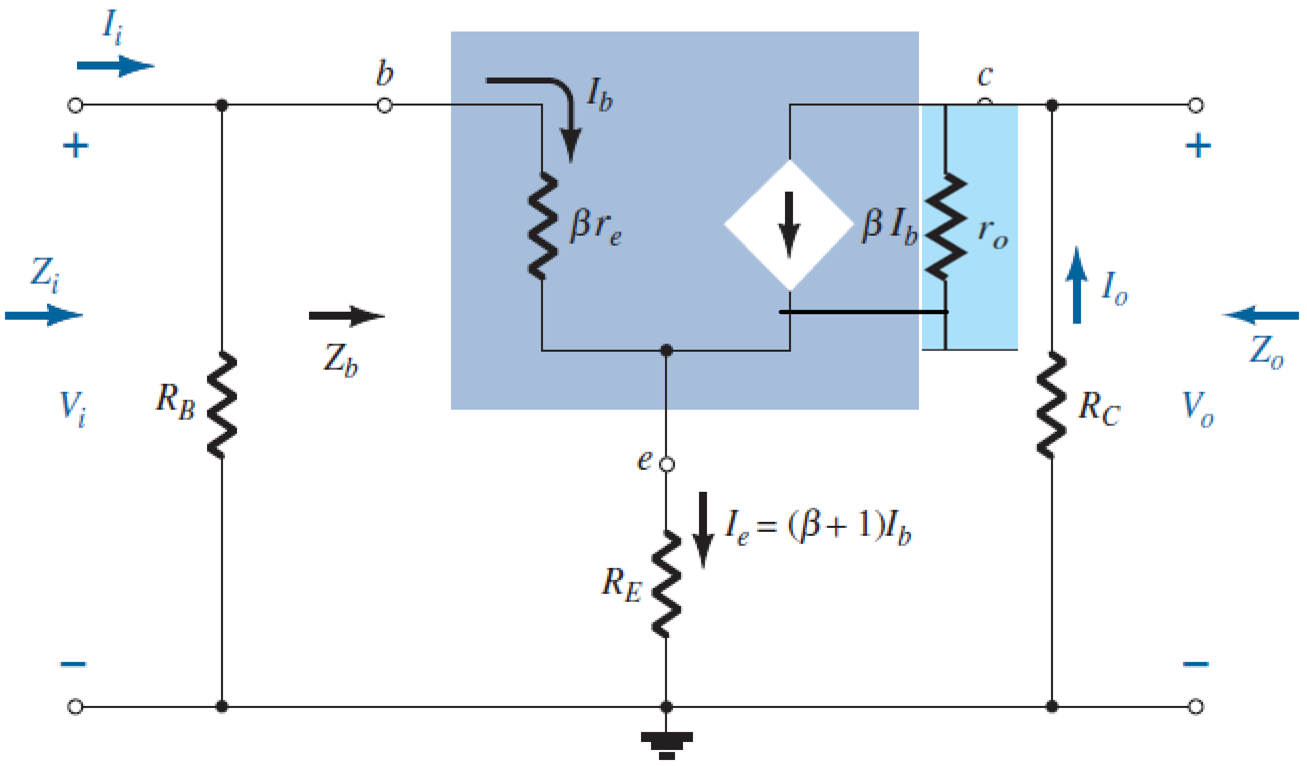
Common Emitter Emitter-Bias (Unbypassed)Configuration with r_o

$$Z_b = (\beta+1)r_e + \frac{(\beta+1) + \frac{R_C}{r_o}}{1 + \frac{R_C + R_E}{r_o}} \mathrm{R_E}$$

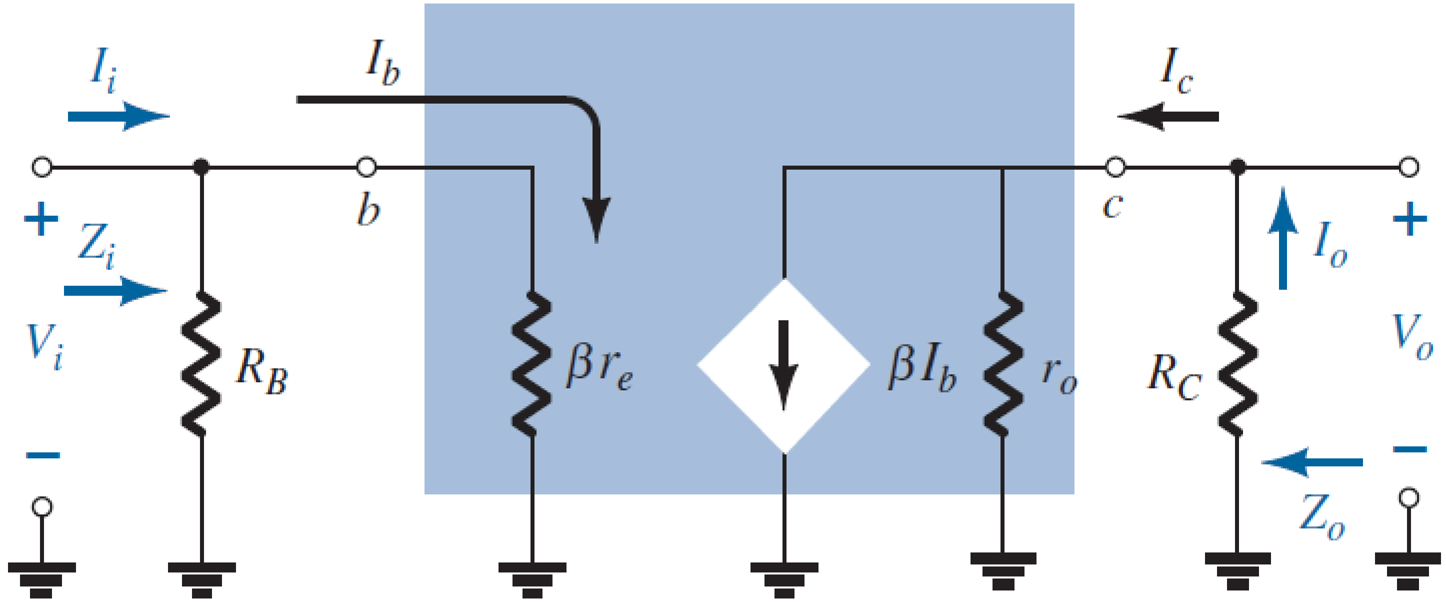
$$Z_i = R_B \parallel Z_b$$

$$Z_O = R_C \parallel \left(r_o + \frac{\beta(r_o + r_e)}{1 + \frac{\beta r_e}{R_E}} \right)$$

$$A_V = -\frac{\frac{\beta R_C}{Z_b}\left(1 + \frac{r_e}{r_o}\right) + \frac{R_C}{r_o}}{(\beta+1) + \frac{(\beta+1) + \frac{R_C}{r_o}}{1 + \frac{R_c + R_E}{r_o}} R_E}$$



Common Emitter Emitter-Bias (Bypassed)Configuration



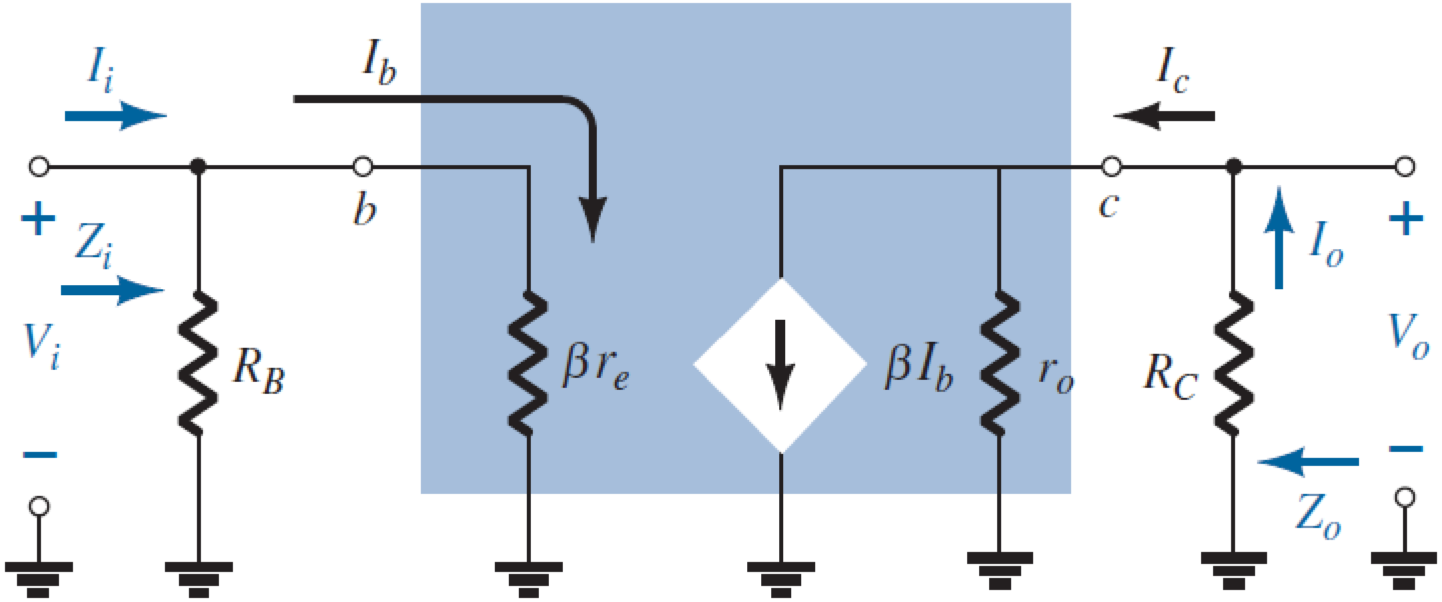
Common Emitter Emitter-Bias (Bypassed)Configuration

Parameters to be obtained:

Z_i - input impedance

Z_0 - output impedance

A_V - Voltage gain



$$\boldsymbol{Z_i = R_B || \beta r_e}$$

$$If\ R_B \geq 10\beta r_e\ ; \boldsymbol{Z_i \cong \beta r_e}$$

$$\boldsymbol{Z_o = R_C || r_o}$$

$$If\ r_o \geq 10R_C\ ; \boldsymbol{Z_o \cong R_C}$$

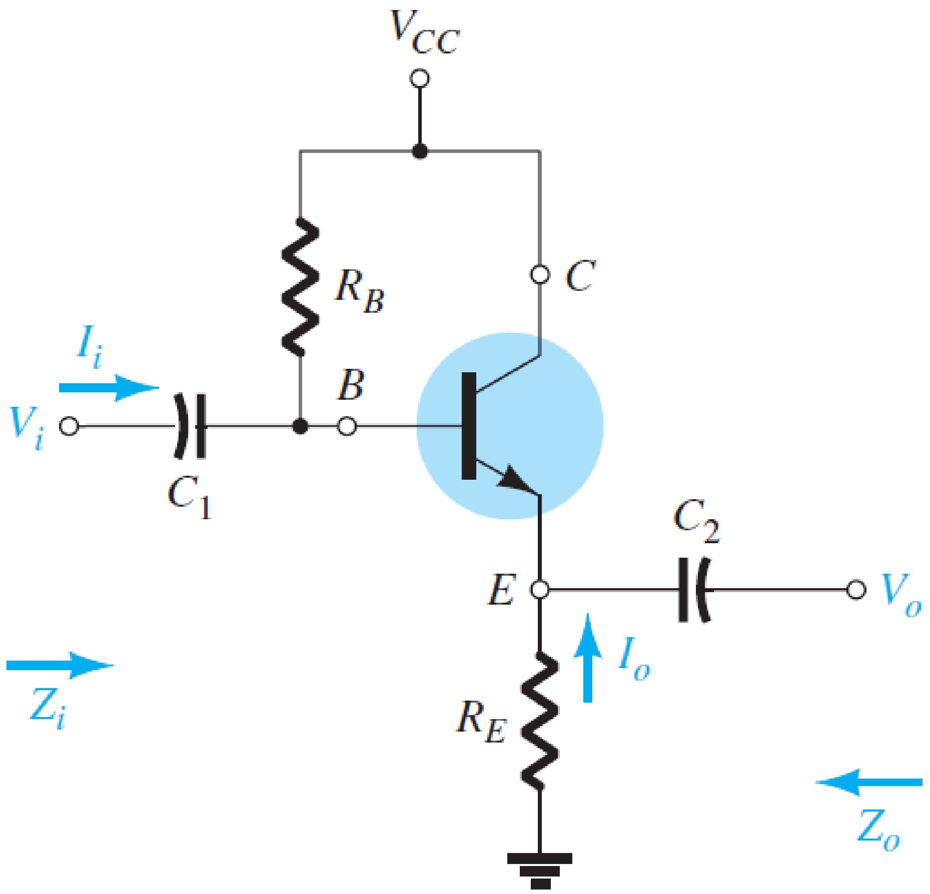
$$V_o = -(\beta I_b)(R_C||r_o);\ I_b = \frac{V_i}{\beta r_e}$$

$$V_o\ = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C||r_o) = -\frac{V_i(R_C||r_o)}{r_e}$$

$$\boldsymbol{A_v = \frac{V_o}{V_i} = -\frac{R_C||r_o}{r_e}}$$

$$If\ r_o \geq 10R_C\ ; \boldsymbol{A_v = -\frac{R_C}{r_e}}$$

Common Collector (Emitter Follower) Configuration



Common Collector (Emitter Follower) Configuration

Z_i:

$$Z_b = (\beta + 1)r_e + (\beta + 1)R_E$$
$$Z_i = R_B \parallel Z_b$$

Z_0:

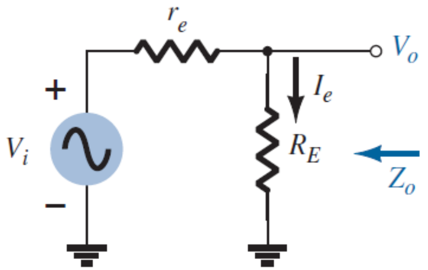
$$I_b = \frac{V_i}{Z_b}$$

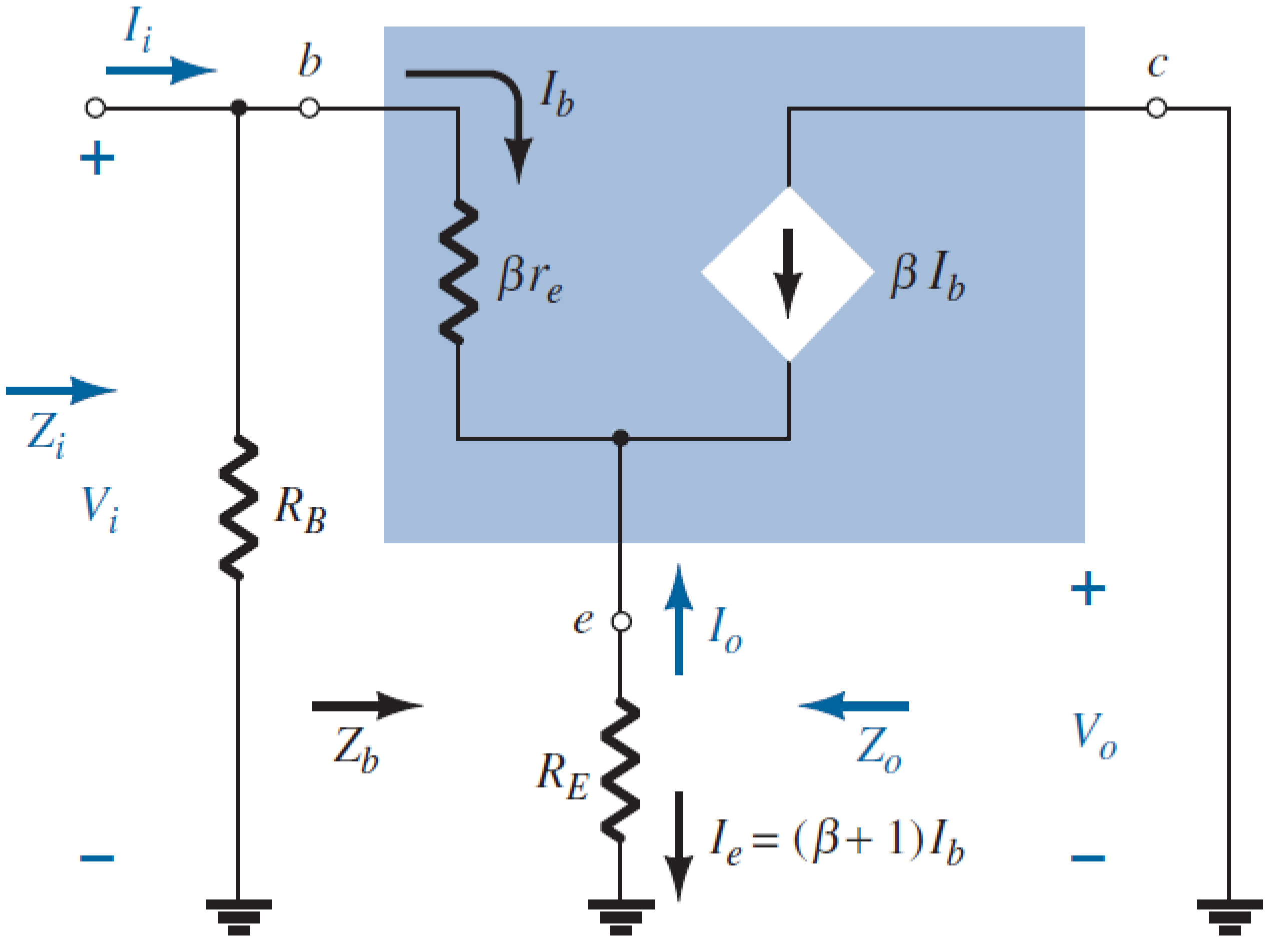
Then multiplying both sides by $(\beta + 1)$ gives I_e

$$I_e = \frac{(\beta + 1)V_i}{(\beta + 1)(r_e + R_E)}$$
$$I_e = \frac{V_i}{r_e + R_E}$$

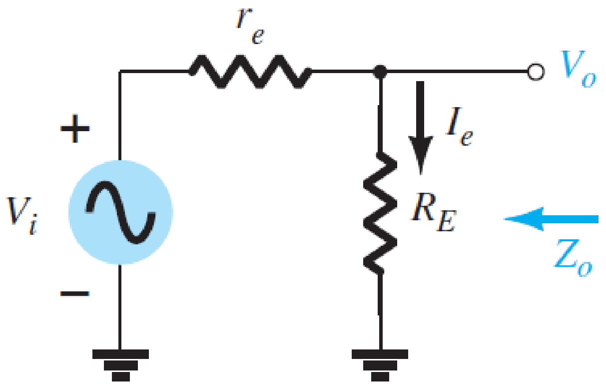
Constructing this circuit:

$\therefore Z_o = R_E \parallel r_e$





Common Collector (Emitter Follower) Configuration



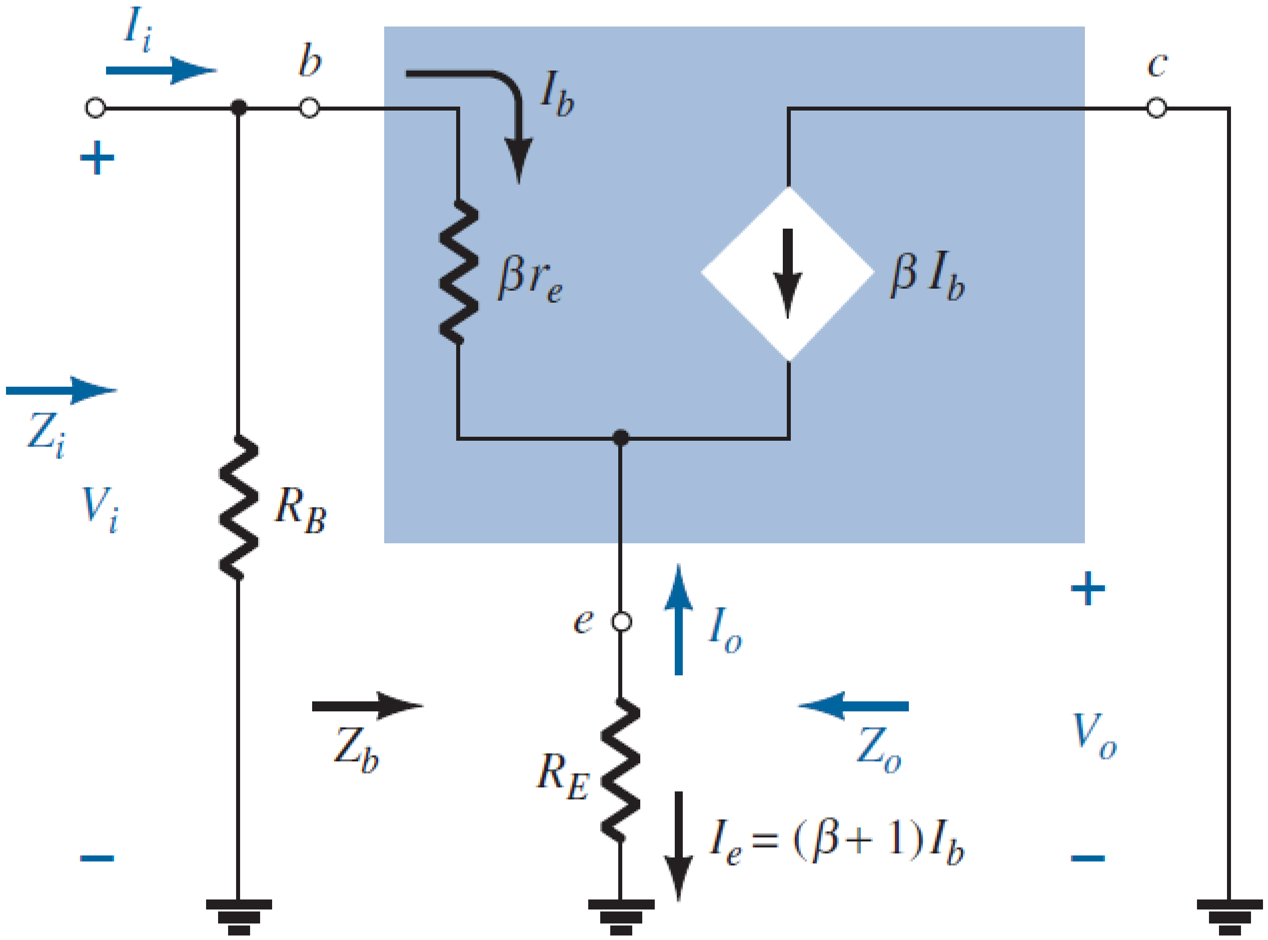
A_V:

$$V_o = V_i \frac{R_E}{r_e + R_E}$$

$$A_V = \frac{V_O}{V_I} = \frac{R_E}{r_e + R_E}$$

Since $R_E >> r_e$

$$A_V \cong 1$$



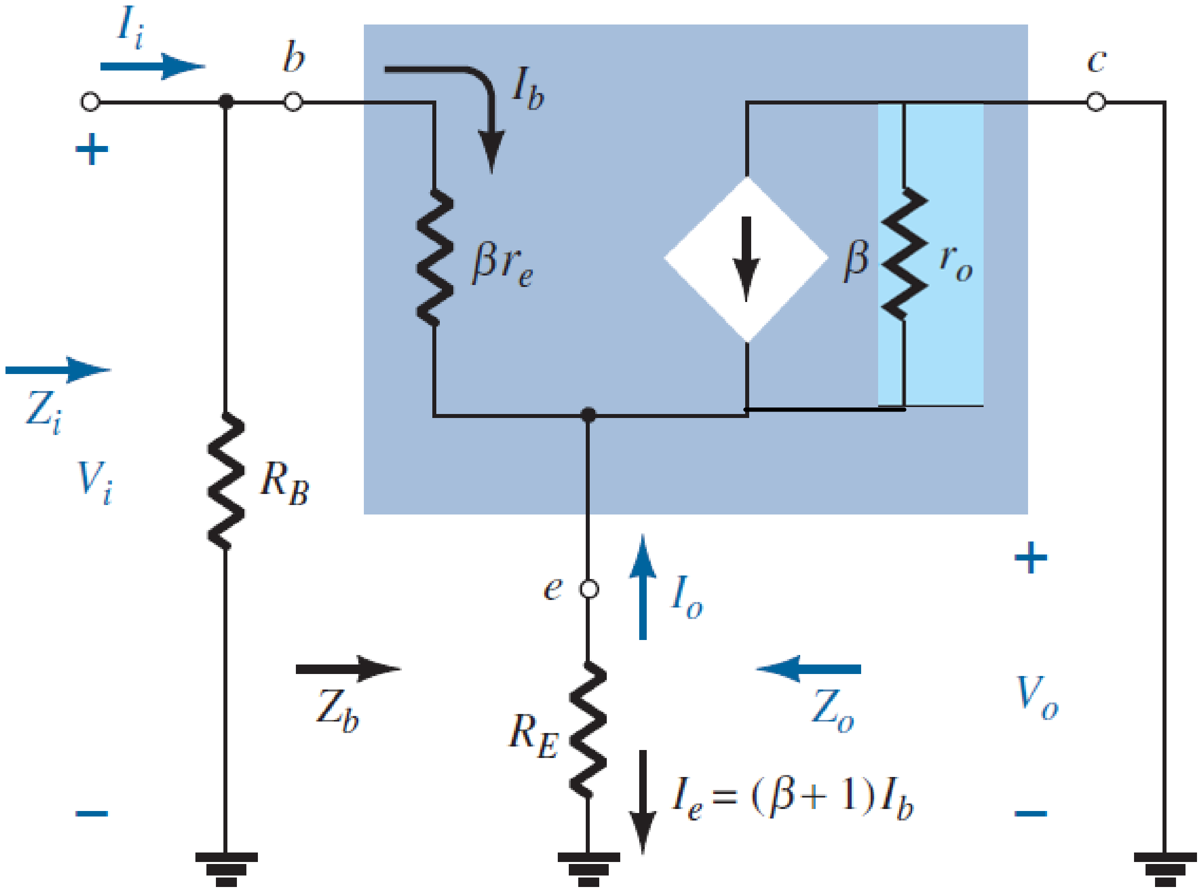
Common Collector (Emitter Follower) Configuration with r_o

$$Z_b = (\beta + 1)r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}}$$

$$Z_i = R_B || Z_b$$

$$Z_O = r_o \parallel R_E \parallel r_e$$

$$A_V = \frac{\frac{(\beta + 1)R_E}{Z_b}}{1 + \frac{R_E}{r_o}}$$



Common Collector (Emitter Follower) Configuration

- For the emitter-follower given network

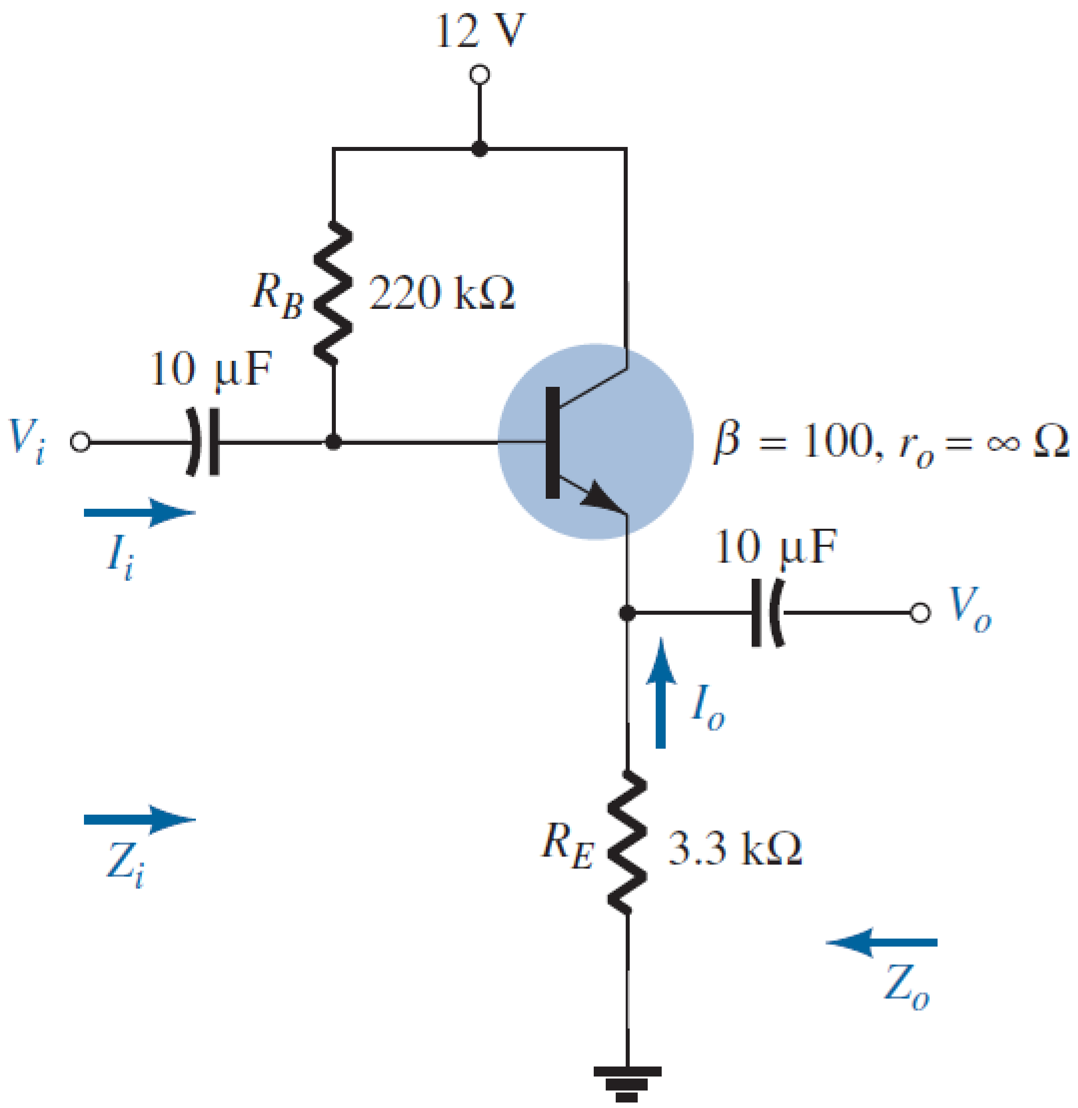
a. re.

b. Zi.

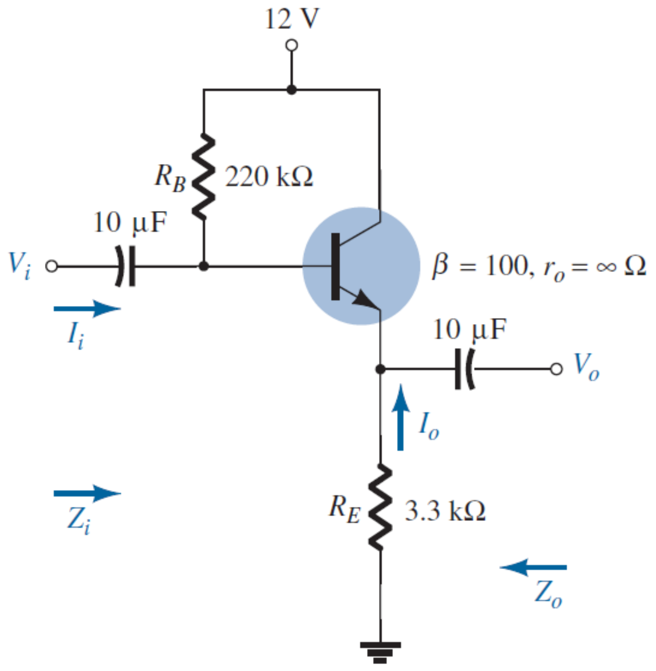
c. Zo.

d. Av.

e. Repeat parts (b) through (d) with ro = 25 kΩ and compare results.



Common Collector (Emitter Follower) Configuration



a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{12\text{ V} - 0.7\text{ V}}{220\text{ k}\Omega + (101)3.3\text{ k}\Omega} = 20.42\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(20.42\ \mu\text{A}) = 2.062\text{ mA}$$

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{2.062\text{ mA}} = \mathbf{12.61\ \Omega}$$

b. $$Z_b = \beta r_e + (\beta + 1)R_E = (100)(12.61\ \Omega) + (101)(3.3\text{ k}\Omega) = 1.261\text{ k}\Omega + 333.3\text{ k}\Omega = 334.56\text{ k}\Omega \cong \beta R_E$$

$$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 334.56\text{ k}\Omega = \mathbf{132.72\text{ k}\Omega}$$

c. $$Z_o = R_E \| r_e = 3.3\text{ k}\Omega \| 12.61\ \Omega = \mathbf{12.56\ \Omega} \cong r_e$$

d. $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\text{ k}\Omega}{3.3\text{ k}\Omega + 12.61\ \Omega} = \mathbf{0.996 \cong 1}$$

e. Checking the condition $r_o \geq 10R_E$, we have

$$25\text{ k}\Omega \geq 10(3.3\text{ k}\Omega) = 33\text{ k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_b = \beta r_e + \frac{(\beta + 1)R_E}{1 + \dfrac{R_E}{r_o}} = (100)(12.61\ \Omega) + \frac{(100 + 1)3.3\text{ k}\Omega}{1 + \dfrac{3.3\text{ k}\Omega}{25\text{ k}\Omega}} = 1.261\text{ k}\Omega + 294.43\text{ k}\Omega = 295.7\text{ k}\Omega$$

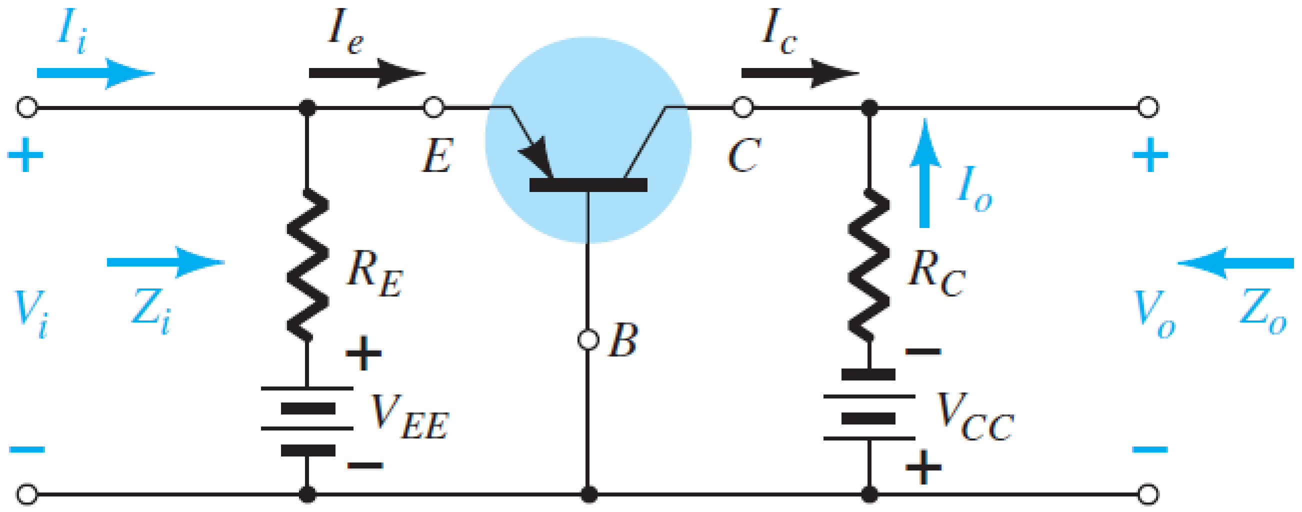
with $$Z_i = R_B \| Z_b = 220\text{ k}\Omega \| 295.7\text{ k}\Omega = \mathbf{126.15\text{ k}\Omega} \text{ vs. } 132.72\text{ k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_E \| r_e = \mathbf{12.56\ \Omega} \quad \text{as obtained earlier}$$

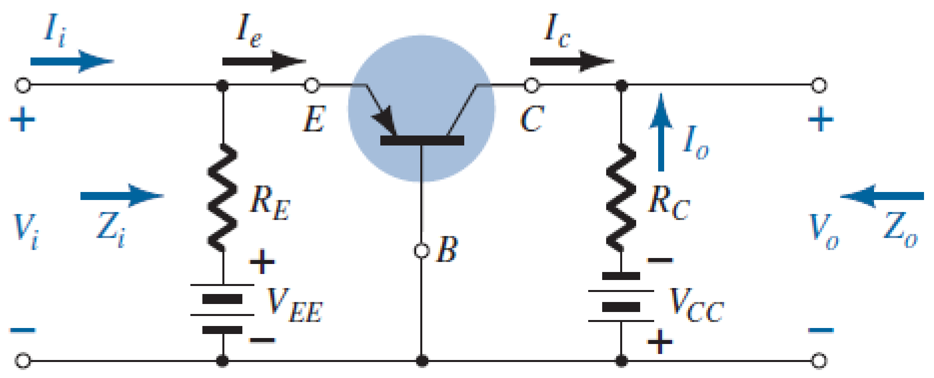
$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \dfrac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\text{ k}\Omega)/295.7\text{ k}\Omega}{\left[1 + \dfrac{3.3\text{ k}\Omega}{25\text{ k}\Omega}\right]} = \mathbf{0.996 \cong 1}$$

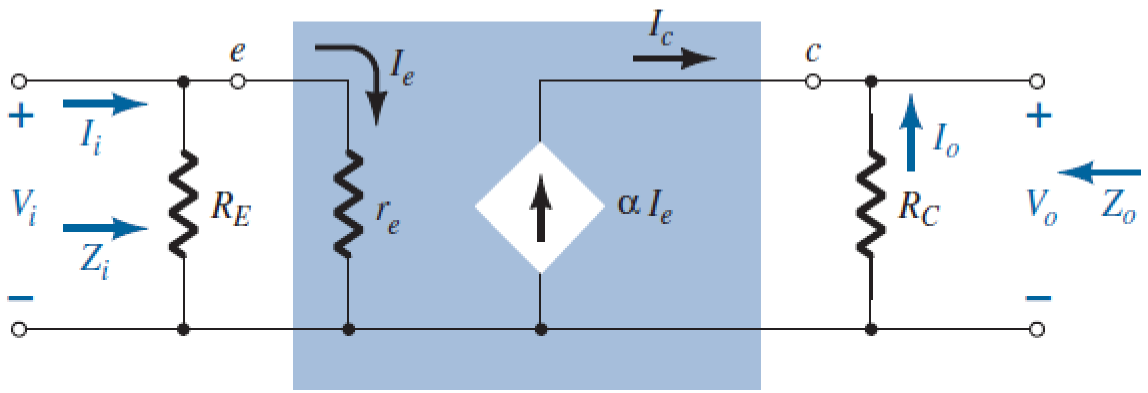
matching the earlier result.

Common Base Configuration



Common Base Configuration



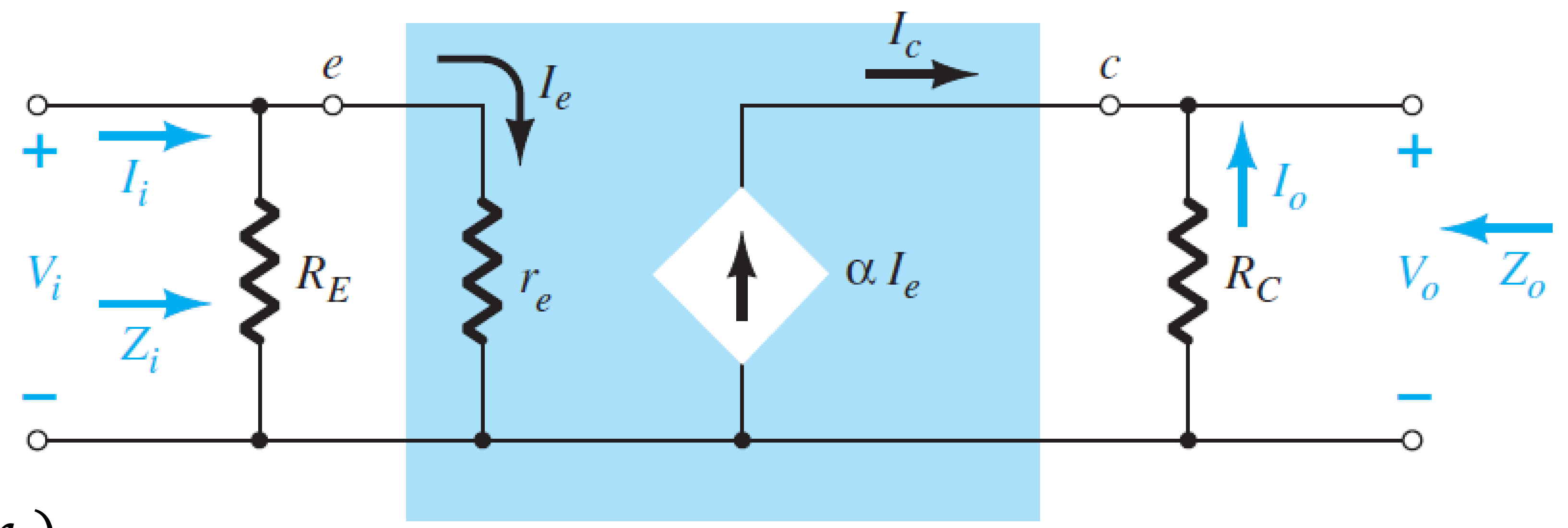


Common Base Configuration

Parameters to be obtained:
Z_i - input impedance
Z_0 – output impedance
A_V – Voltage gain

$$Z_i = R_E || r_e$$

$$Z_o = R_C$$



$V_o = -I_o R_C = -(-I_c) R_C = \alpha I_e R_C$; $I_e = (V_i / r_e)$
$V_o = \alpha (V_i / r_e)\ R_C$

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

Common Base Configuration

- For the network

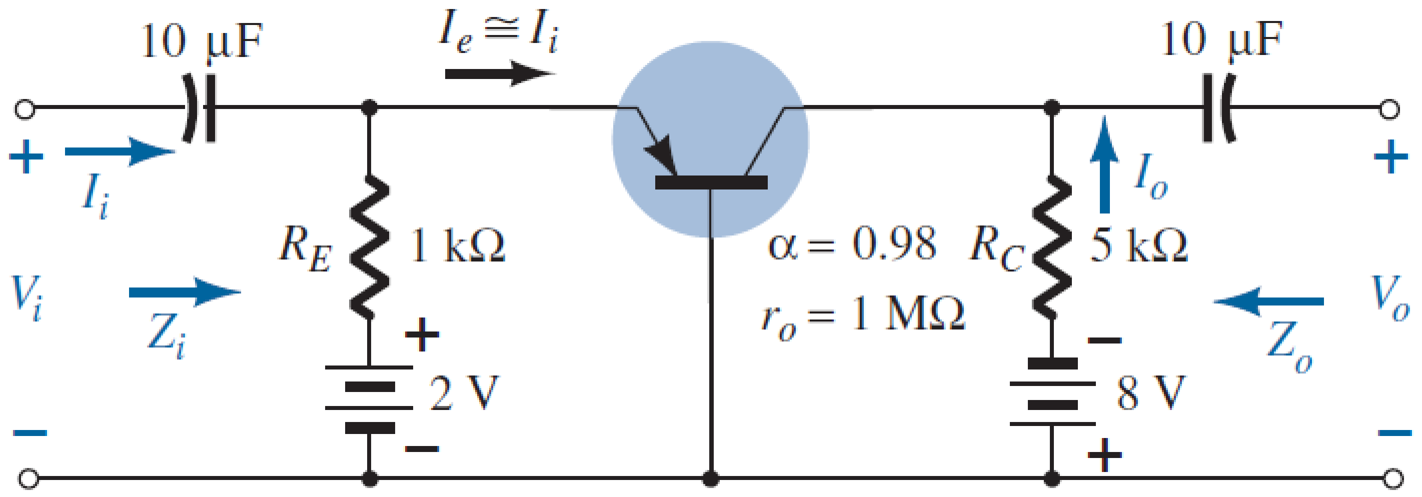
a. re.

b. Zi.

c. Zo.

d. av.

e. ai.



Common Base Configuration

Solution:

a. $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \dfrac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$

$r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$

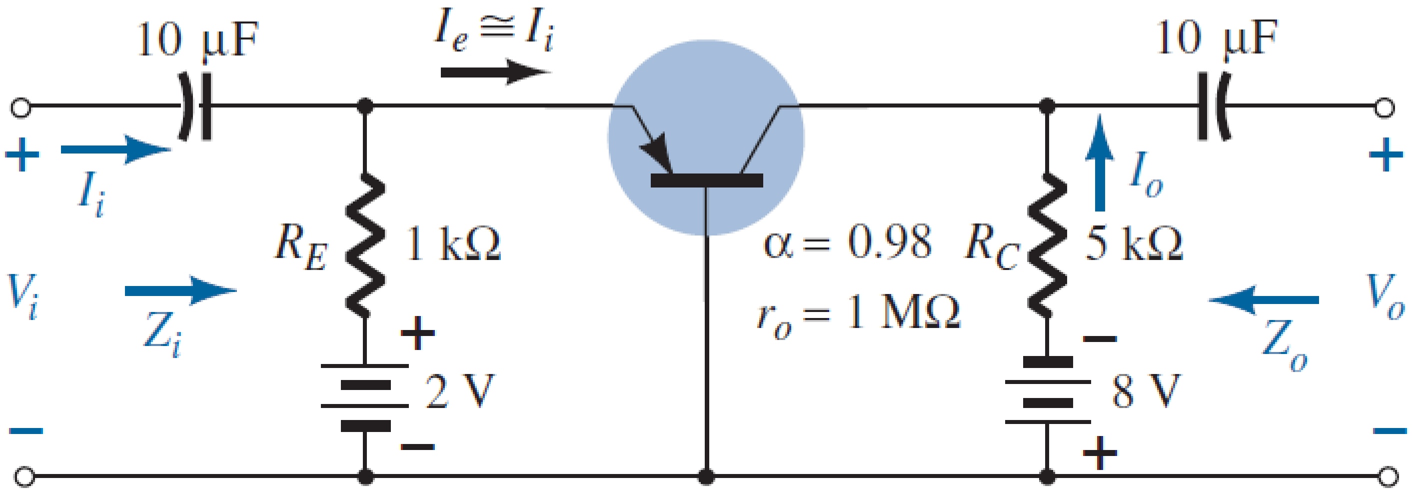
b. $Z_i = R_E \| r_e = 1\text{ k}\Omega \| 20\ \Omega$

$= \mathbf{19.61\ \Omega} \cong r_e$

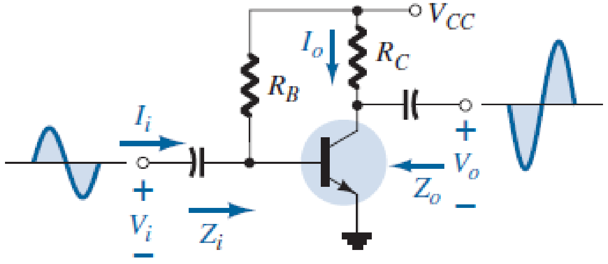
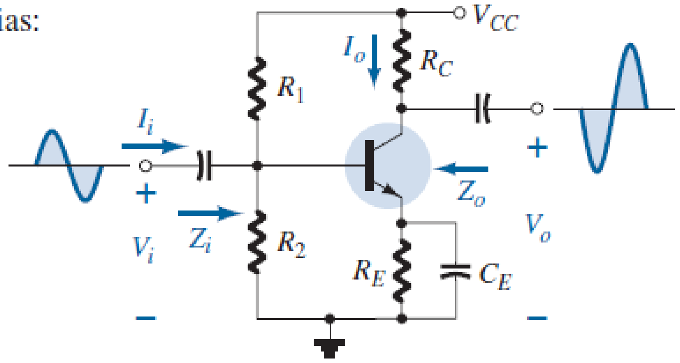
c. $Z_o = R_C = \mathbf{5\text{ k}\Omega}$

d. $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$

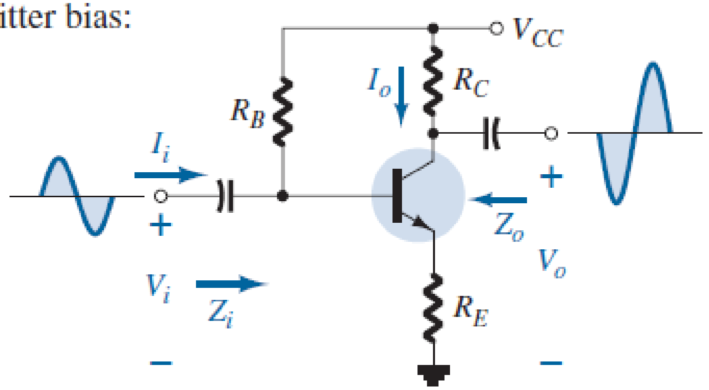
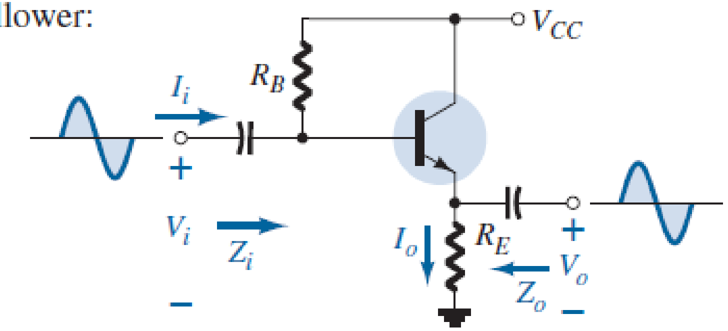
e. $A_i = \mathbf{-0.98} \cong -1$



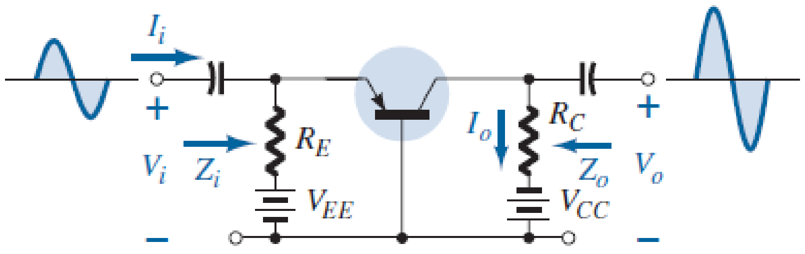
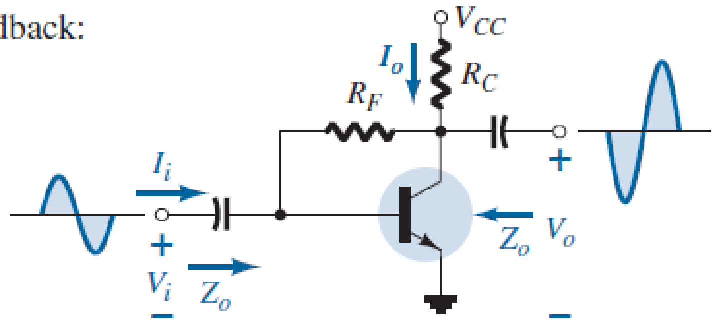
Summary Table

Configuration	Z_i	Z_o	A_v	A_i
Fixed-bias: 	Medium (1 kΩ) $= \boxed{R_B \| \beta r_e}$ $\cong \boxed{\beta r_e}$ $(R_B \geq 10\beta r_e)$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{(R_C \| r_o)}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (100) $= \boxed{\frac{\beta R_B r_o}{(r_o + R_C)(R_B + \beta r_e)}}$ $\cong \boxed{\beta}$ $(r_o \geq 10R_C,$ $R_B \geq 10\beta r_e)$
Voltage-divider bias: 	Medium (1 kΩ) $= \boxed{R_1 \| R_2 \| \beta r_e}$	Medium (2 kΩ) $= \boxed{R_C \| r_o}$ $\cong \boxed{R_C}$ $(r_o \geq 10R_C)$	High (−200) $= \boxed{-\frac{R_C \| r_o}{r_e}}$ $\cong \boxed{-\frac{R_C}{r_e}}$ $(r_o \geq 10R_C)$	High (50) $= \boxed{\frac{\beta (R_1 \| R_2) r_o}{(r_o + R_C)(R_1 \| R_2 + \beta r_e)}}$ $\cong \boxed{\frac{\beta (R_1 \| R_2)}{R_1 \| R_2 + \beta r_e}}$ $(r_o \geq 10R_C)$

Summary Table

Unbypassed emitter bias: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$ (any level of r_o)	Low (−5) $= \boxed{-\dfrac{R_C}{r_e + R_E}}$ $\cong \boxed{-\dfrac{R_C}{R_E}}$ $(R_E \gg r_e)$	High (50) $\cong \boxed{-\dfrac{\beta R_B}{R_B + Z_b}}$
Emitter-follower: 	High (100 kΩ) $= \boxed{R_B \| Z_b}$ $Z_b \cong \beta(r_e + R_E)$ $\cong \boxed{R_B \| \beta R_E}$ $(R_E \gg r_e)$	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Low (≅1) $= \boxed{\dfrac{R_E}{R_E + r_e}}$ $\cong \boxed{1}$	High (−50) $\cong \boxed{-\dfrac{\beta R_B}{R_B + Z_b}}$

Summary Table

Common-base: 	Low (20 Ω) $= \boxed{R_E \| r_e}$ $\cong \boxed{r_e}$ $(R_E \gg r_e)$	Medium (2 kΩ) $= \boxed{R_C}$	High (200) $\cong \boxed{\dfrac{R_C}{r_e}}$	Low (−1) $\cong \boxed{-1}$
Collector feedback: 	Medium (1 kΩ) $= \boxed{\dfrac{r_e}{\dfrac{1}{\beta} + \dfrac{R_C}{R_F}}}$ $(r_o \geq 10R_C)$	Medium (2 kΩ) $\cong \boxed{R_C \| R_F}$ $(r_o \geq 10R_C)$	High (−200) $\cong \boxed{-\dfrac{R_C}{r_e}}$ $(r_o \geq 10R_C)$ $(R_F \gg R_C)$	High (50) $= \boxed{\dfrac{\beta R_F}{R_F + \beta R_C}}$ $\cong \boxed{\dfrac{R_F}{R_C}}$

JFET Small Signal Modelling

JFET Small Signal Modelling

- A major component of the FET AC model is the fact that an AC voltage applied to the input gate-to-source terminals will control the currents from the drain to source terminals, that is:
  - The **gate-to-source voltage** controls the **drain-to-source (channel) current** of a JFET
- Considering Shockley's equation

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

- From the equation, the change in I_D will result from a change in V_{GS} that can be determined using the **transconductance factor, g_m**, in the following relationship

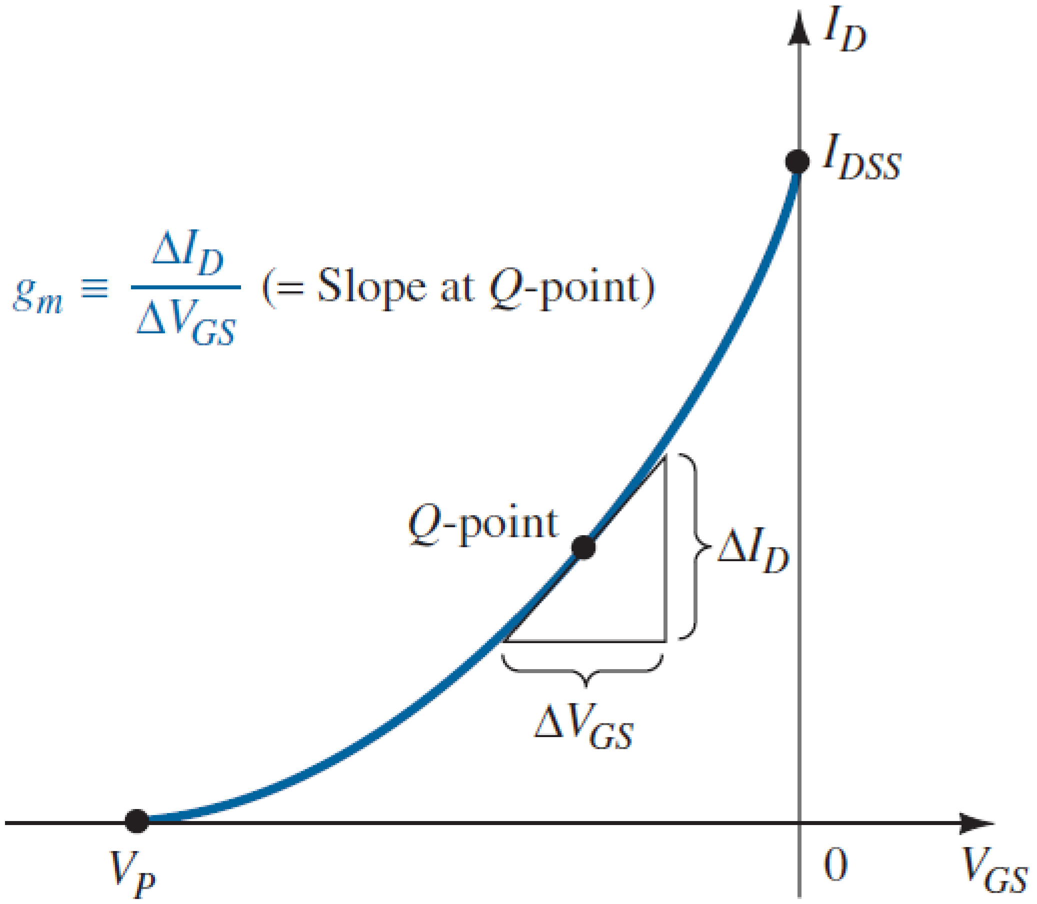
$$\Delta I_D = g_m \Delta V_{GS}$$

JFET Small Signal Modelling

- The prefix "trans" shows that it establishes a relationship between an output and input quantity.
- Conductance is the **current-to-voltage** ratio similar to the conductance of a resistor (1/R).
- Solving for the transconductance:

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boldsymbol{g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)}$$



JFET Small Signal Modelling

- Solving g_m is same as finding the AC resistance of the diode that is:
  - The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.
- Taking the derivative of I_D with respect to V_{GS} (using Shockley's equation)

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

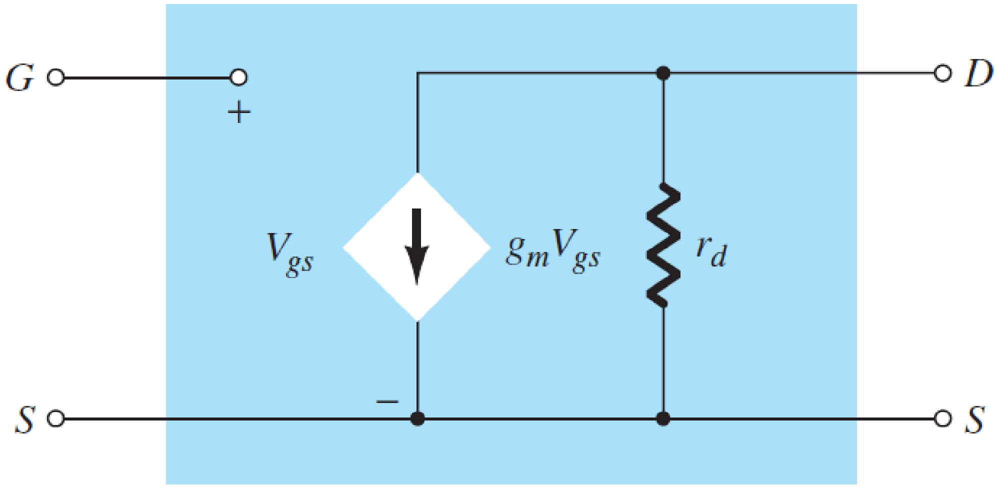
$$g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}}\left[I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2\right]$$

$$= 2I_{DSS}\frac{d}{dV_{GS}}\left(1-\frac{V_{GS}}{V_P}\right) = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)\left(0-\frac{1}{V_P}\right)$$

$$\boldsymbol{g_m = \frac{2I_{DSS}}{|V_P|}\left(1-\frac{V_{GS}}{V_P}\right)}$$

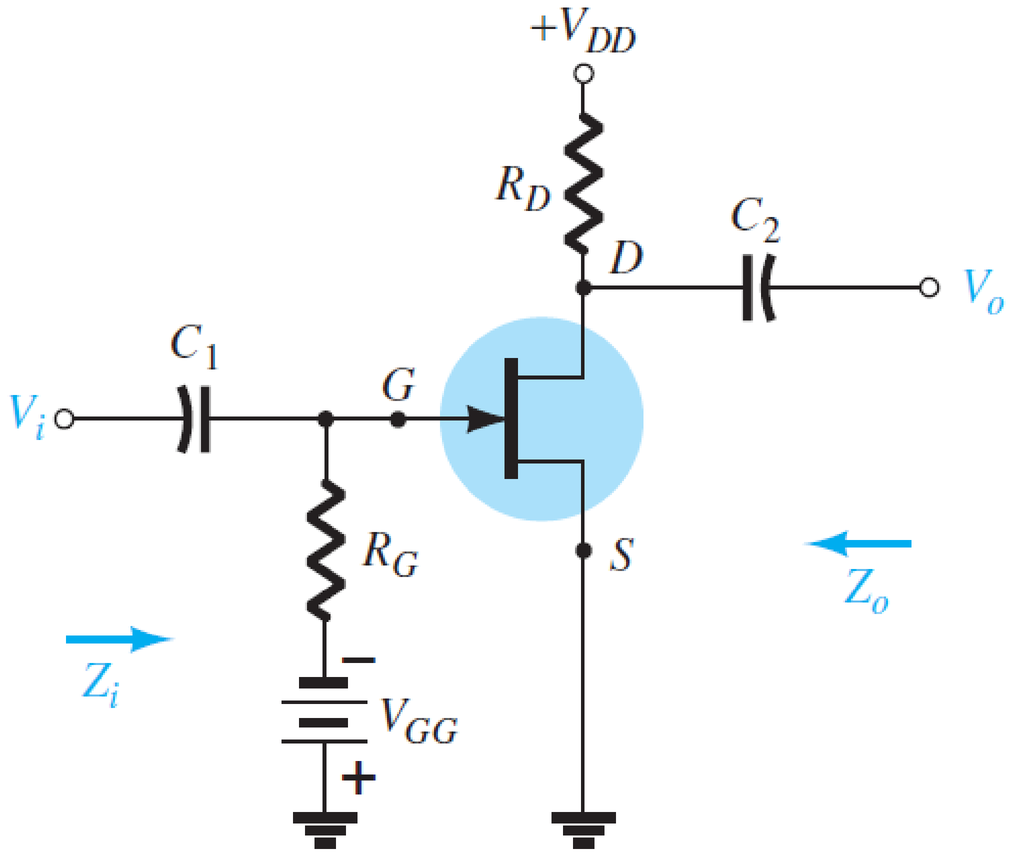
JFET AC Equivalent Model

- The input impedance of all commercially available JFETs is very large such that we could assume that the input terminal is an open-circuit
  - $\boldsymbol{Z_i = \infty\Omega}$
- The output impedance typically appears in datasheets as g_{os} or y_{os} with a unit of S (siemens). In equation form:
  - $\boldsymbol{Z_O = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}}}$
- The control of I_D by V_{GS} is represented by a current source g_mV_{GS}. It is pointing from drain to source to establish a 180^0 phase shift between output and input voltages.

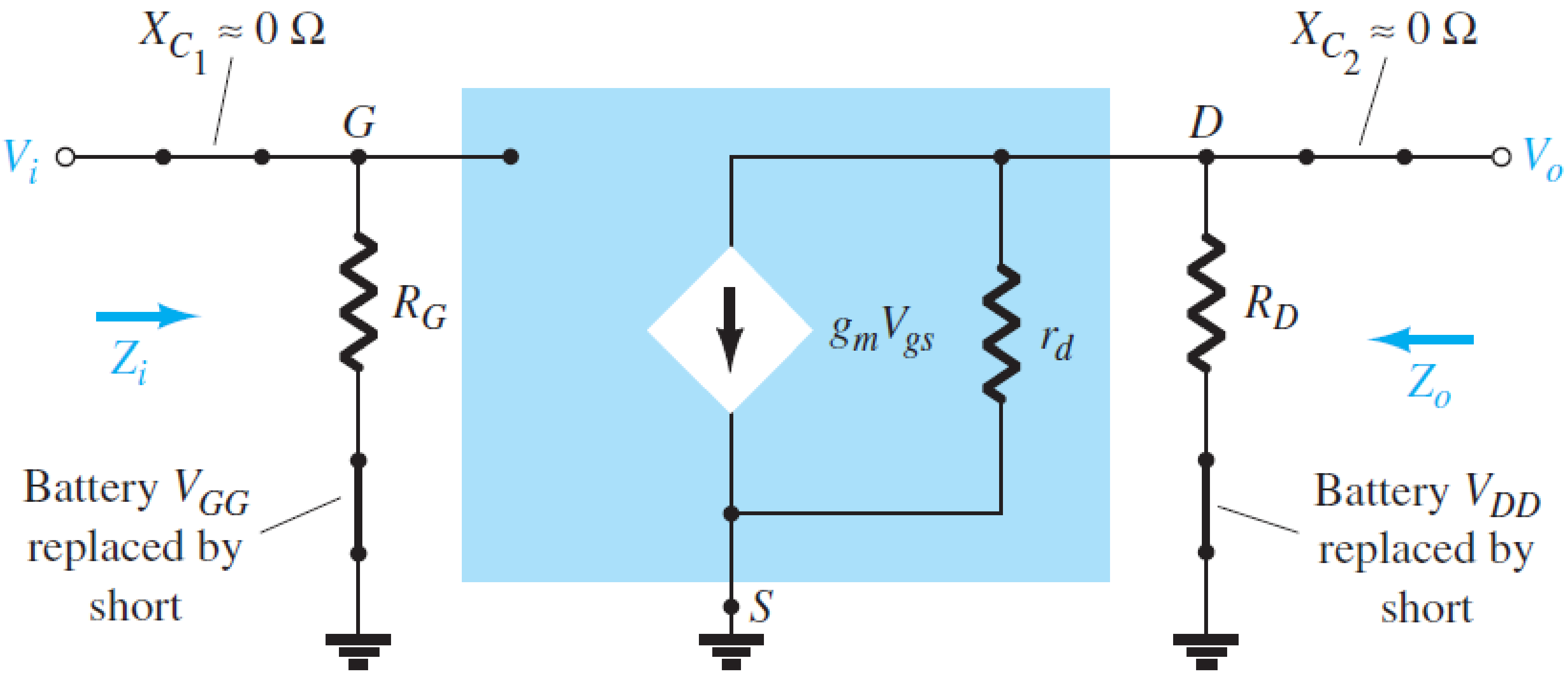


JFET AC Equivalent Circuit

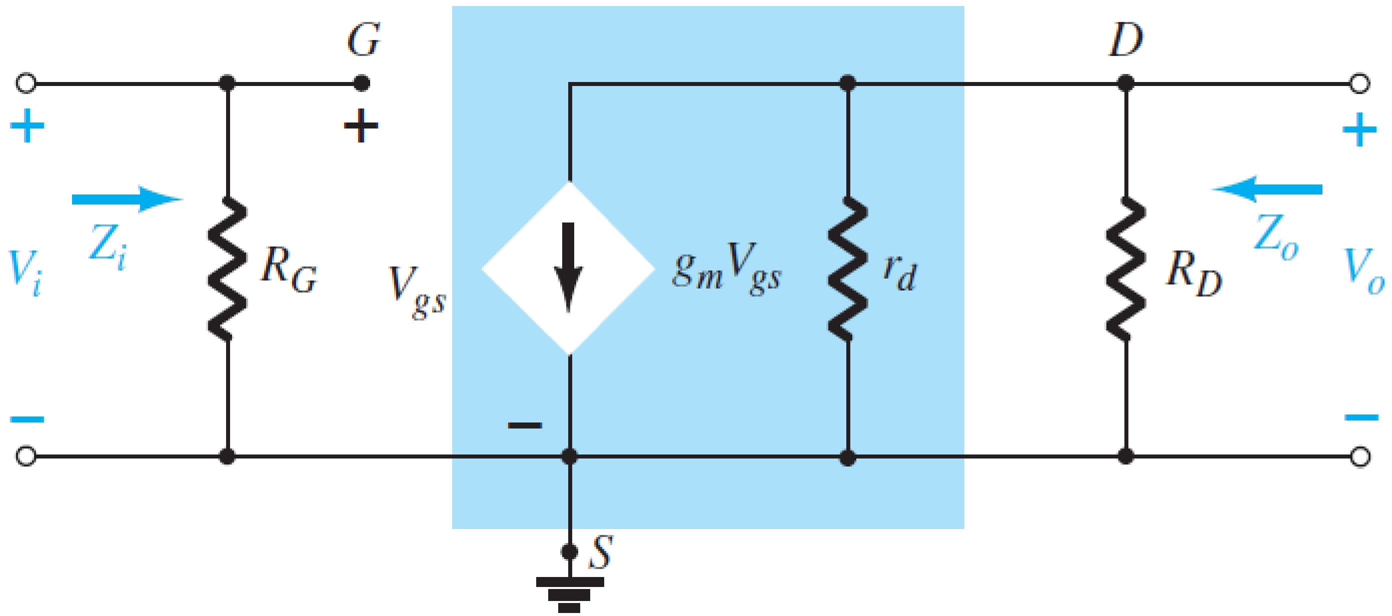
JFET Fixed Bias Configuration



JFET Fixed Bias Configuration



JFET Fixed Bias Configuration



JFET Fixed Bias Configuration

Parameters to be obtained:
Z_i - input impedance
Z_0 – output impedance
A_V – Voltage gain

$$g_m = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$Z_i = R_G$$

$$Z_o = R_D || r_d$$

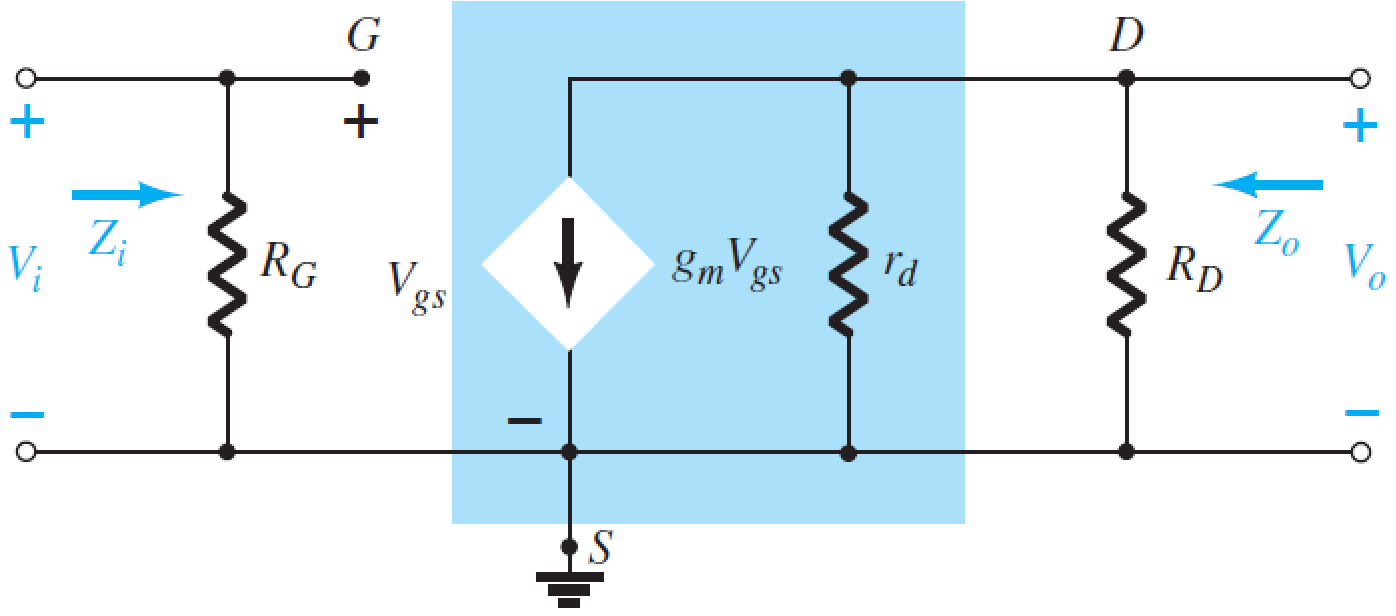
$$If\ r_d \geq 10R_D\ ; Z_o \cong R_D$$

$$V_o = -g_m V_{GS}(r_d||R_D);\ V_{GS} = V_i$$

$$V_o = -g_m V_i (r_d||R_D)$$

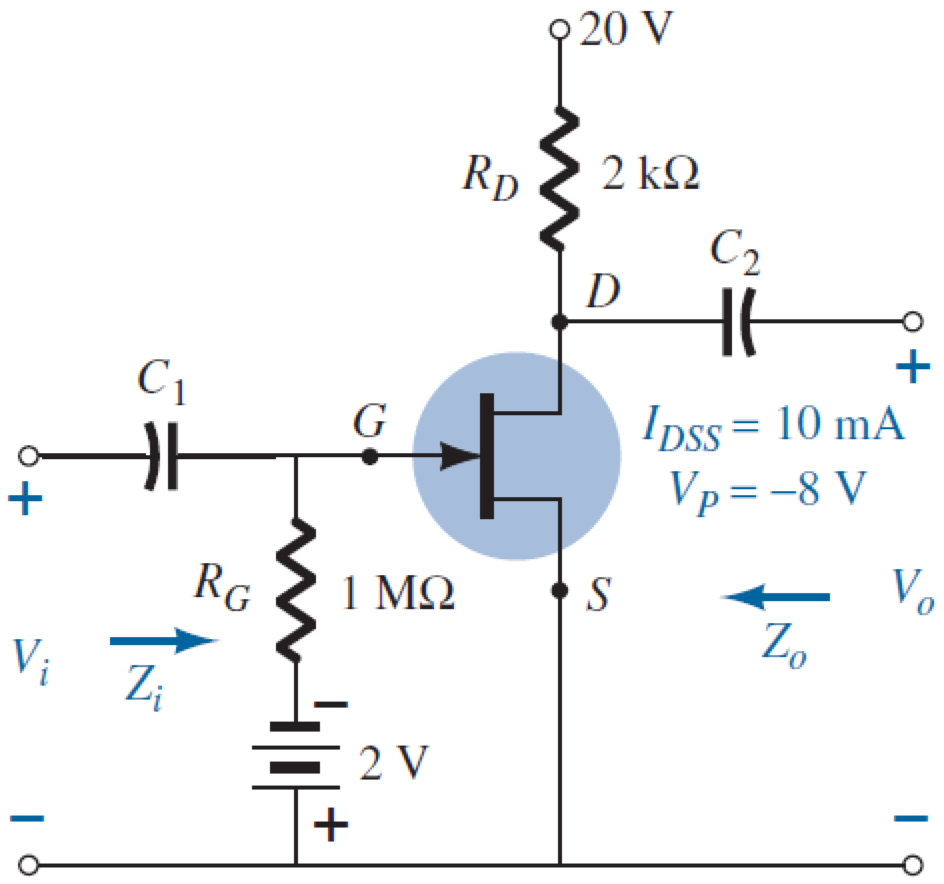
$$A_v = \frac{V_o}{V_i} = -g_m\,(r_d||R_D)$$

$$If\ r_d \geq 10R_D\ ; A_v = -g_m R_D$$



JFET Fixed Bias Configuration

- The fixed-bias configuration had an operating point defined by VGSQ = -2 V and IDQ = 5.625 mA, with IDSS = 10 mA and VP = -8 V. The network is redrawn with an applied signal Vi. The value of yos is provided as 40 µS.
- a. Determine gm.
- b. Find rd.
- c. Determine Zi.
- d. Calculate Zo.
- e. Determine the voltage gain Av.
- f. Determine Av ignoring the effects of rd.



JFET Fixed Bias Configuration

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{40\ \mu\text{S}} = \mathbf{25\text{ k}\Omega}$$

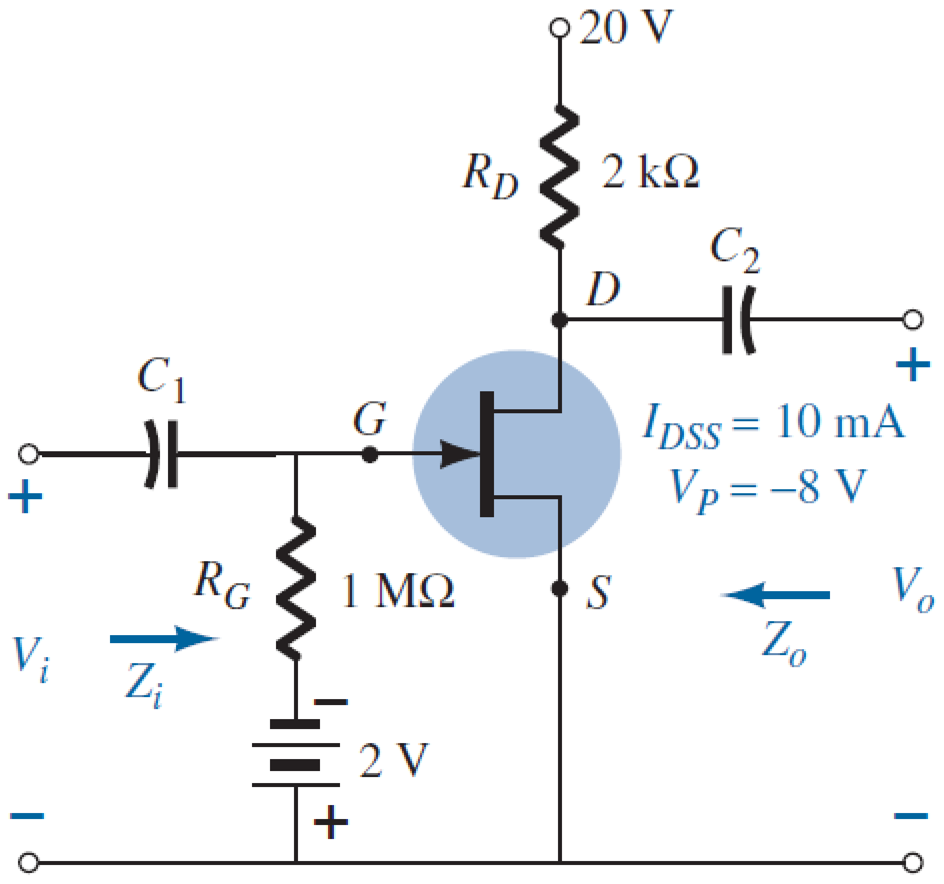
c. $$Z_i = R_G = \mathbf{1\text{ M}\Omega}$$

d. $$Z_o = R_D \| r_d = 2\text{ k}\Omega \| 25\text{ k}\Omega = \mathbf{1.85\text{ k}\Omega}$$

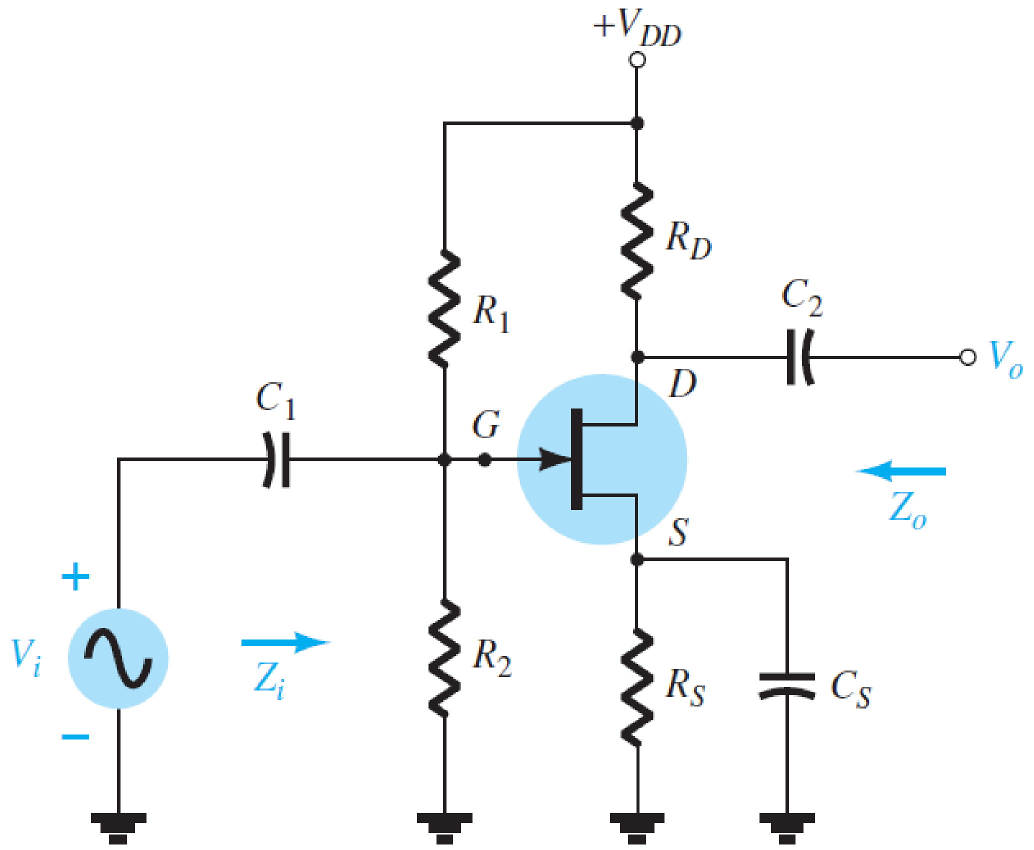
e. $$A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\text{ k}\Omega) = \mathbf{-3.48}$$

f. $$A_v = -g_m R_D = -(1.88\text{ mS})(2\text{ k}\Omega) = \mathbf{-3.76}$$

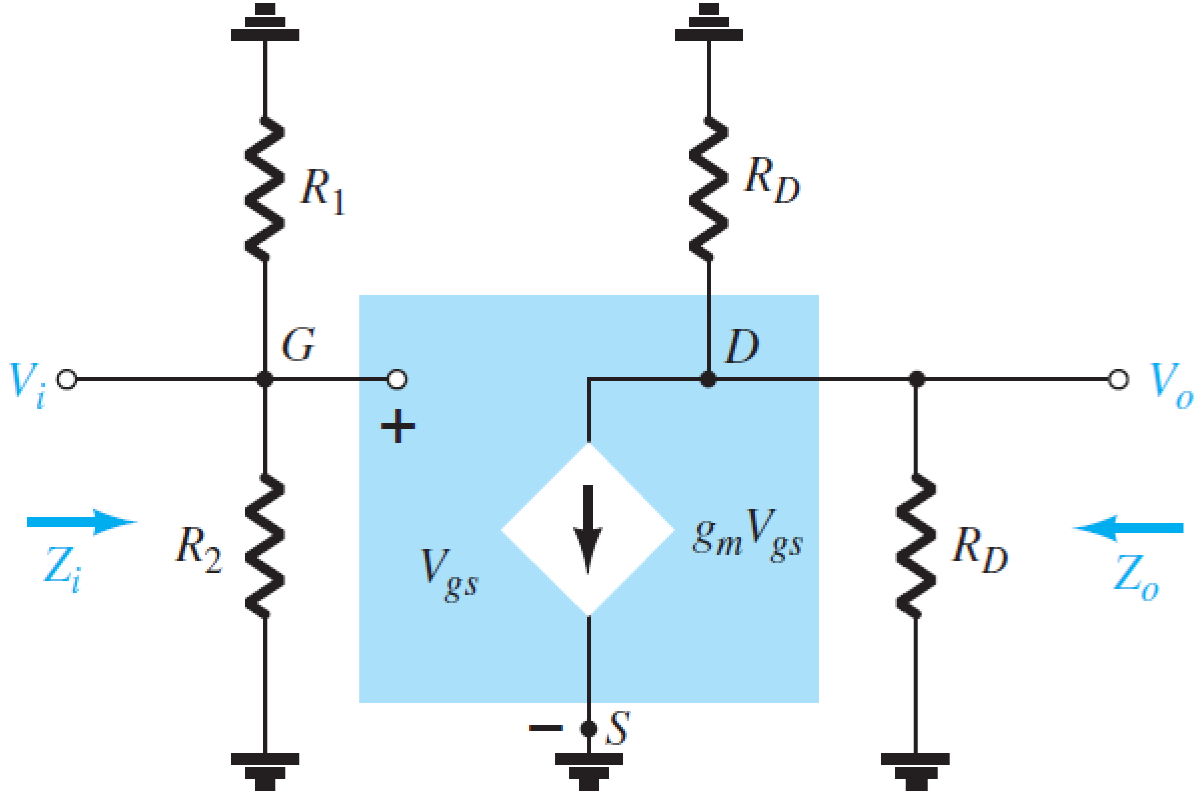
As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.



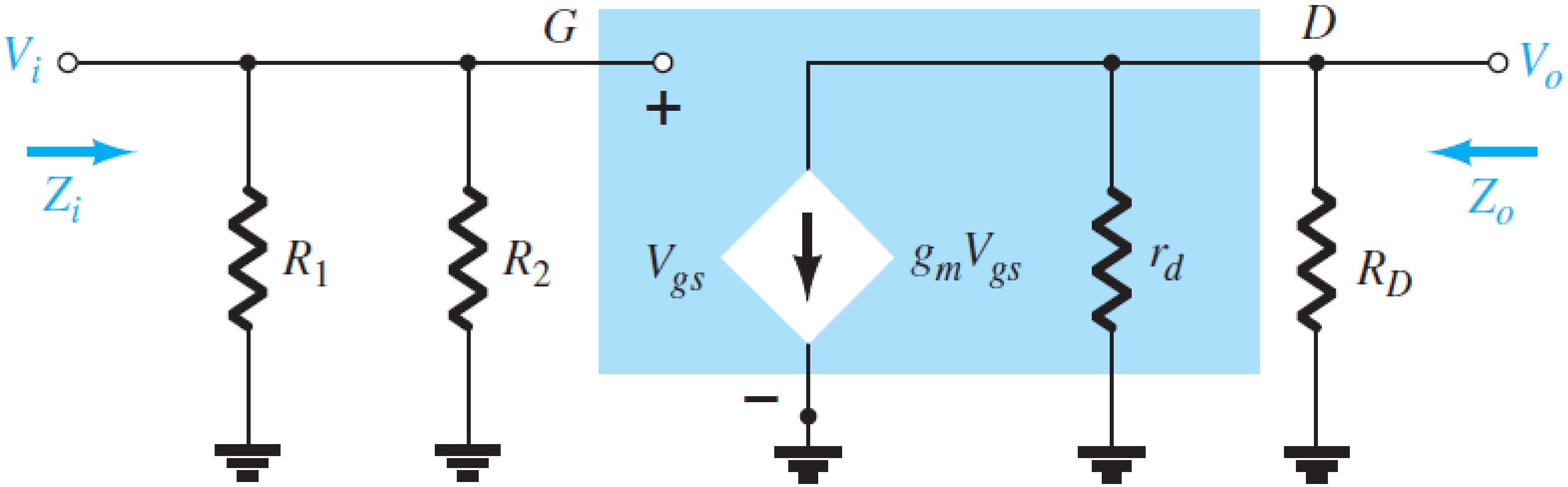
JFET Voltage Divider Bias Configuration



JFET Voltage Divider Bias Configuration



JFET Voltage Divider Bias Configuration



JFET Voltage Divider Bias Configuration

Parameters to be obtained:

Z_i - input impedance

Z_0 – output impedance

A_V – Voltage gain

$$\boldsymbol{Z_i = R_1 || R_2}$$

$$\boldsymbol{Z_o = R_D || r_d}$$

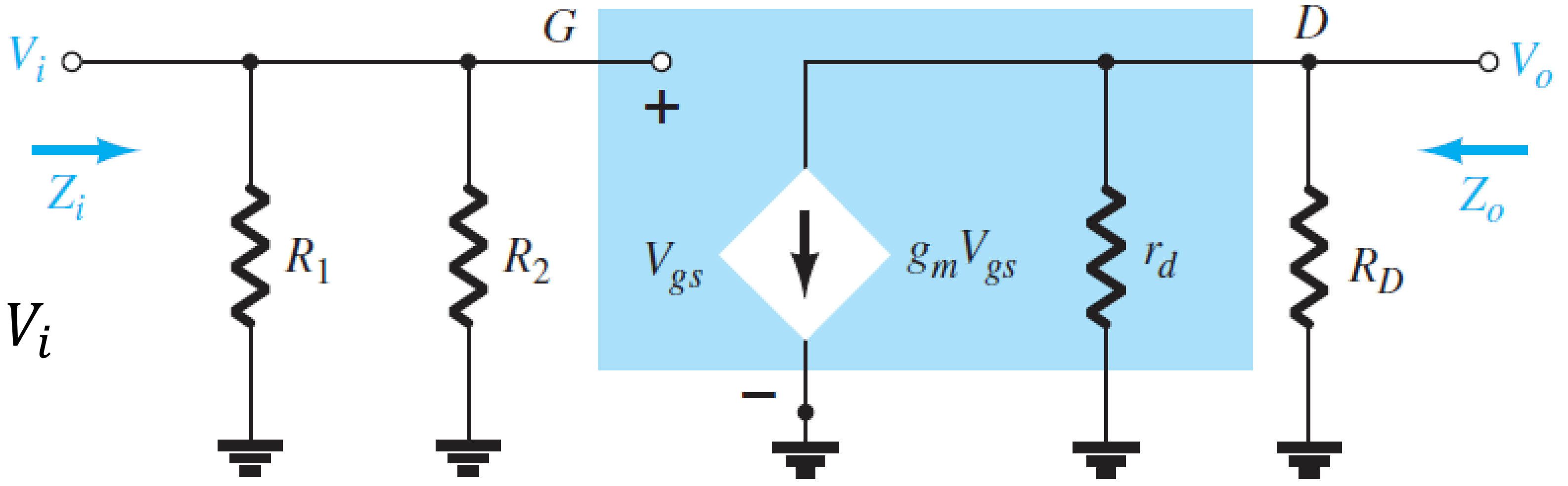
$$If\ r_d \geq 10R_D\ ; \boldsymbol{Z_o \cong R_D}$$

$$V_o = -g_m V_{GS}(r_d || R_D);\ V_{GS} = V_i$$

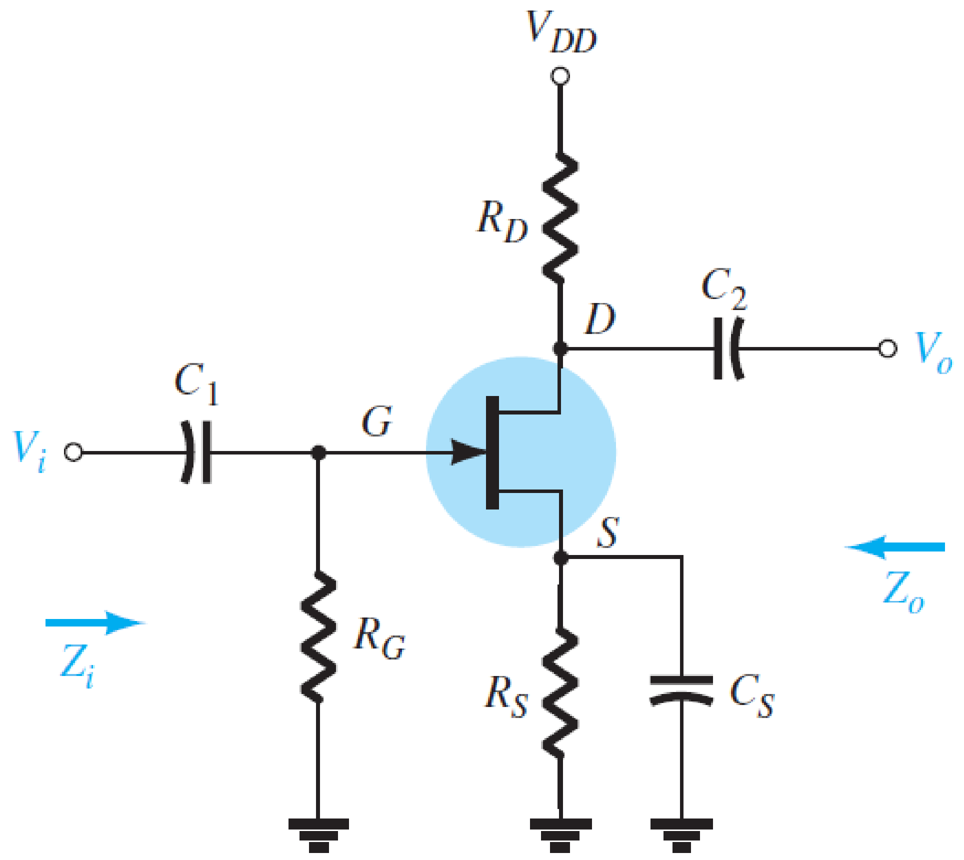
$$V_o = -g_m V_i (r_d || R_D)$$

$$\boldsymbol{A_v = \frac{V_o}{V_i} = -g_m\ (r_d || R_D)}$$

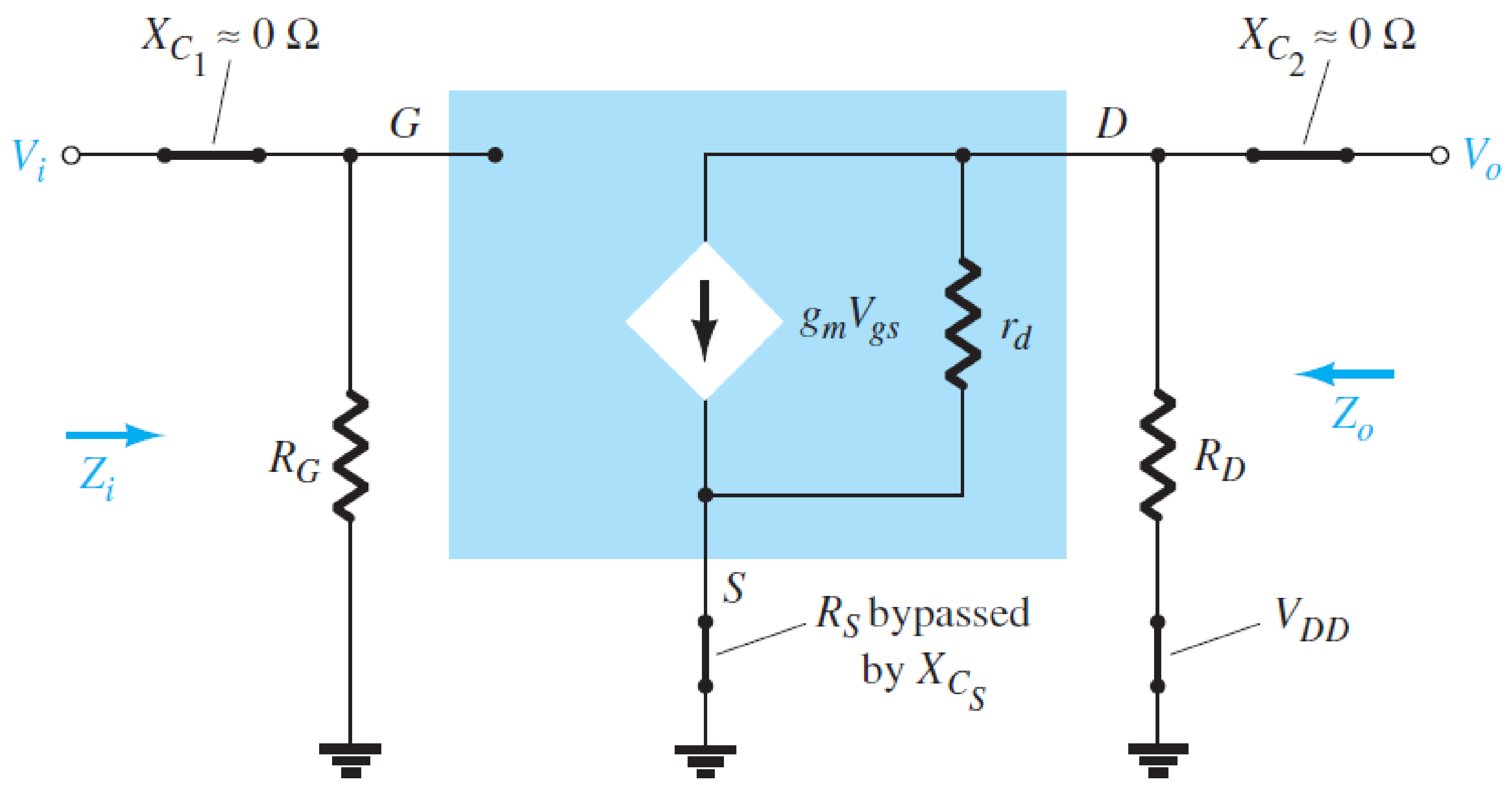
$$If\ r_d \geq 10R_D\ ; \boldsymbol{A_v = -g_m R_D}$$



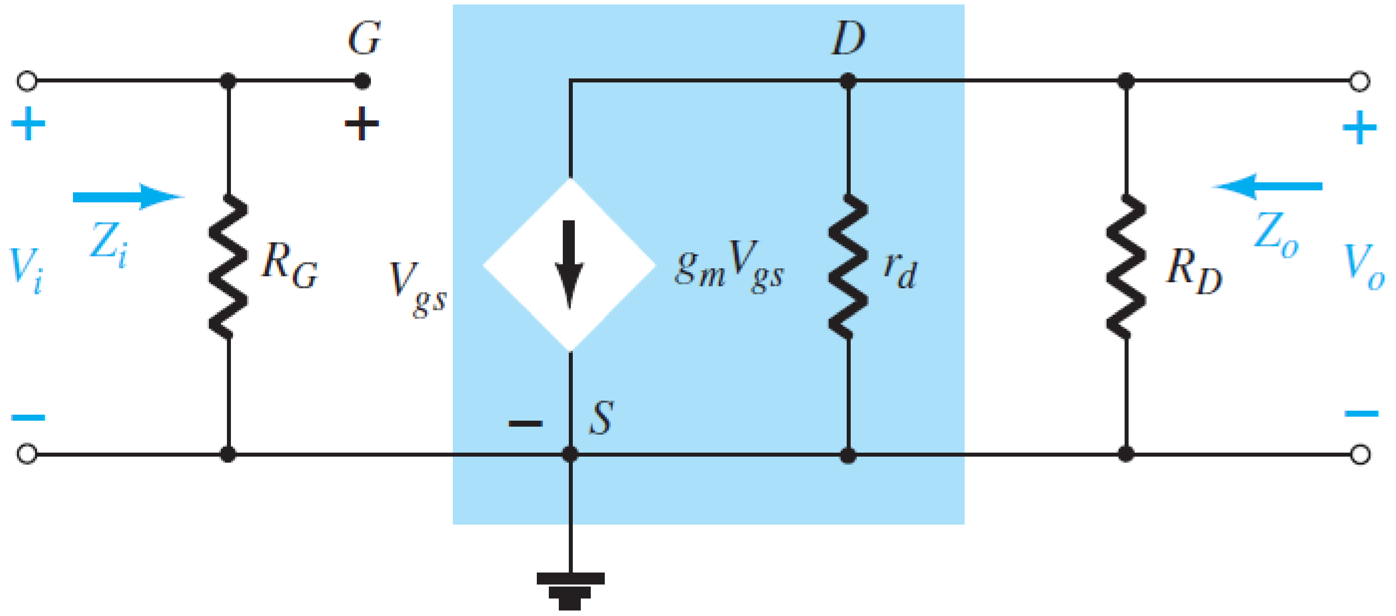
JFET Self Bias Configuration (Bypassed R_S)



JFET Self Bias Configuration (Bypassed R_S)



JFET Self Bias Configuration (Bypassed R_S)



JFET Self Bias Configuration (Bypassed R_S)

Parameters to be obtained:

Z_i - input impedance

Z_0 – output impedance

A_V – Voltage gain

$$\boldsymbol{Z_i = R_G}$$

$$\boldsymbol{Z_o = R_D || r_d}$$

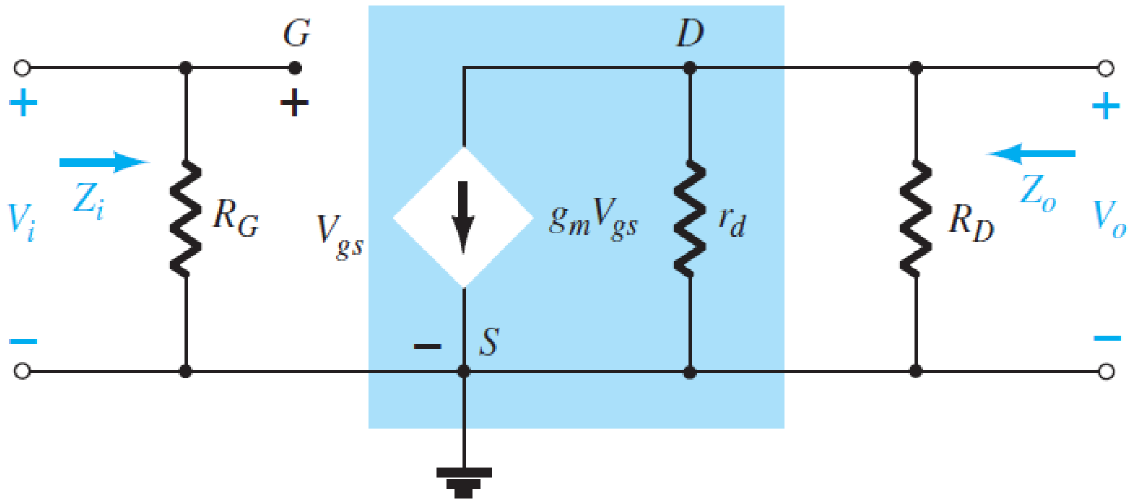
$$If\ r_d \geq 10R_D\ ;\boldsymbol{Z_o \cong R_D}$$

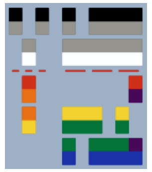
$$V_o = -g_m V_{GS}(r_d||R_D);\ V_{GS} = V_i$$

$$V_o = -g_m V_i(r_d||R_D)$$

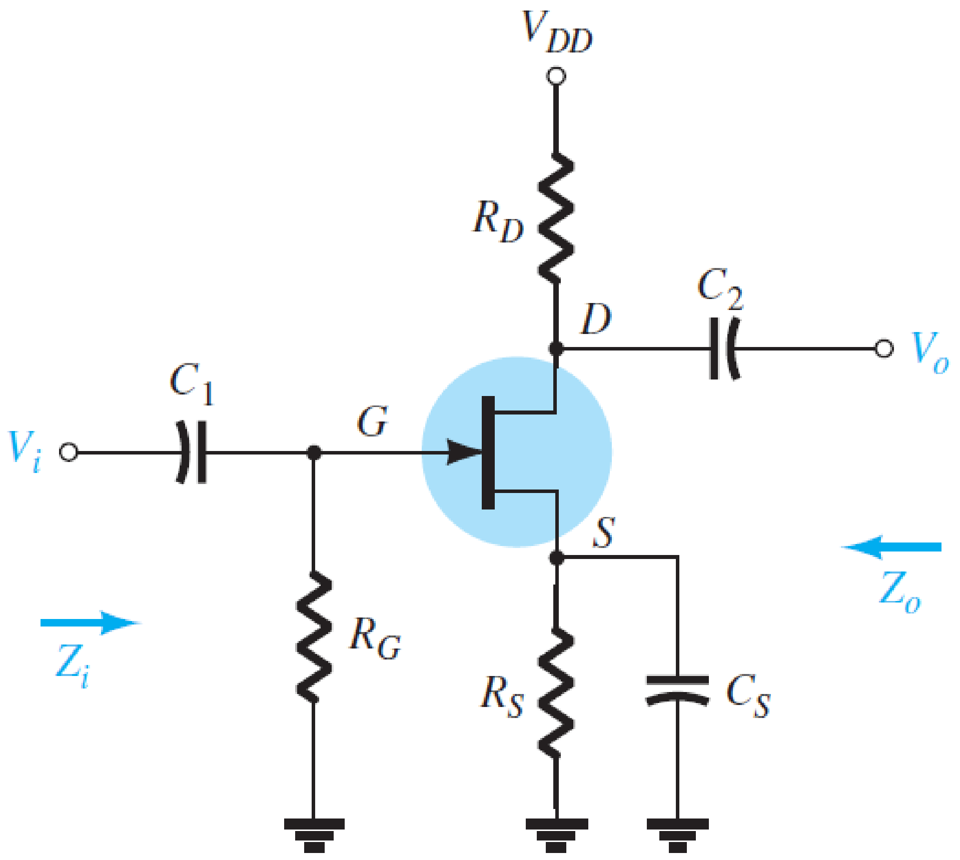
$$\boldsymbol{A_v = \frac{V_o}{V_i} = -g_m\ (r_d||R_D)}$$

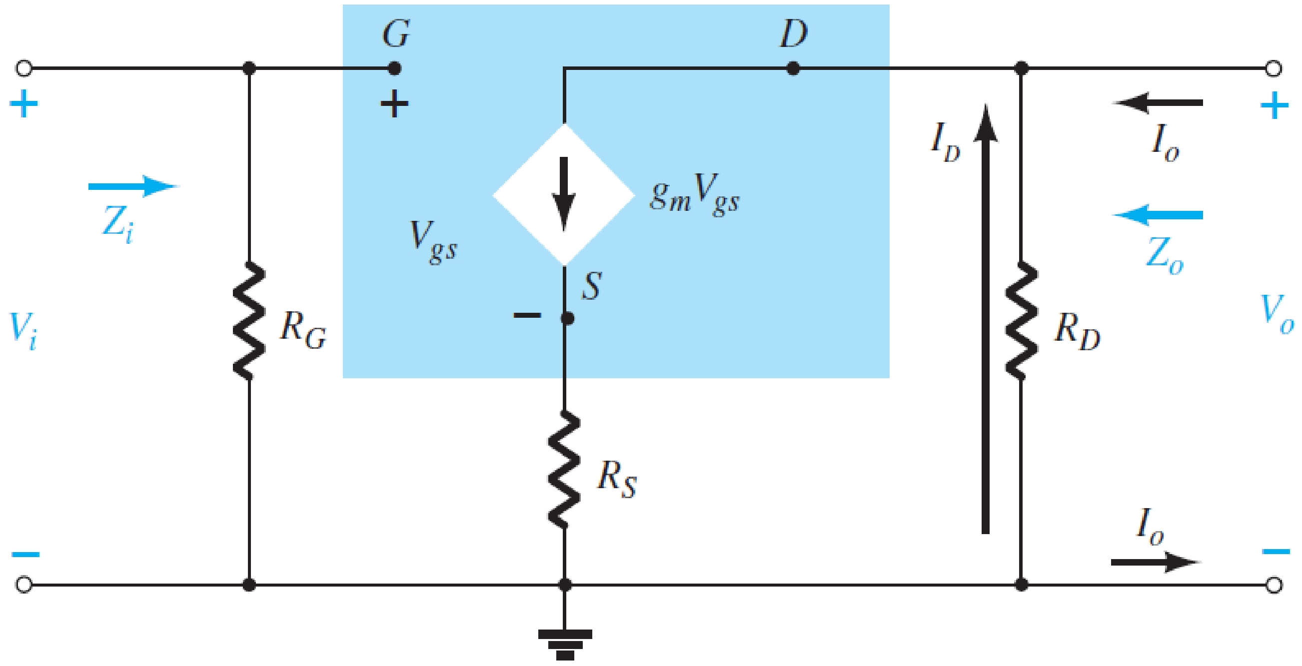
$$If\ r_d \geq 10R_D\ ;\boldsymbol{A_v = -g_m R_D}$$





JFET Self Bias Configuration (Unbypassed R_S)



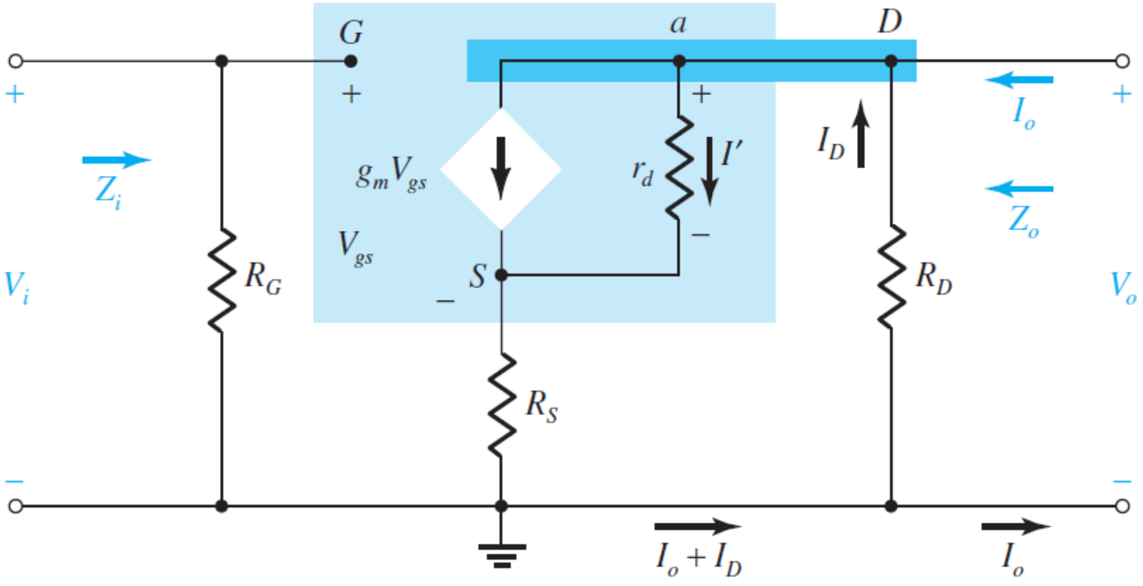


JFET Self Bias Configuration (Unbypassed R_S) with r_d

$$Z_i = R_G$$

$$Z_O = \frac{\left[1 + g_m R_S + \frac{R_S}{r_d}\right]}{\left[1 + g_m R_S + \frac{R_S}{r_d} + \frac{R_D}{r_d}\right]} R_D$$

$$A_V = -\frac{g_m R_D}{1 + g_m R_S + \frac{R_D + R_S}{r_d}}$$

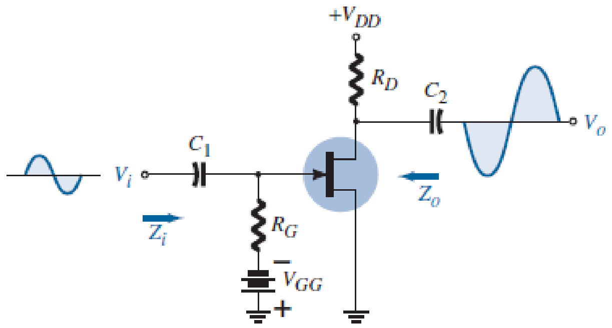
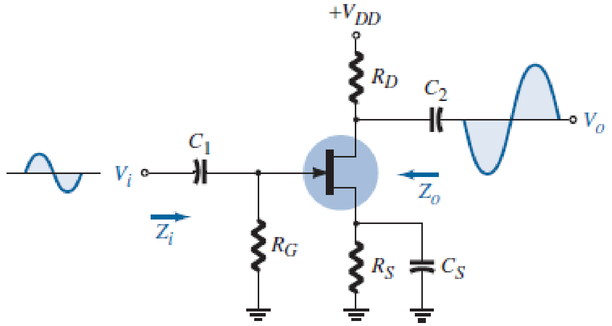


D-MOSFET and E-MOSFET Small Signal Modelling

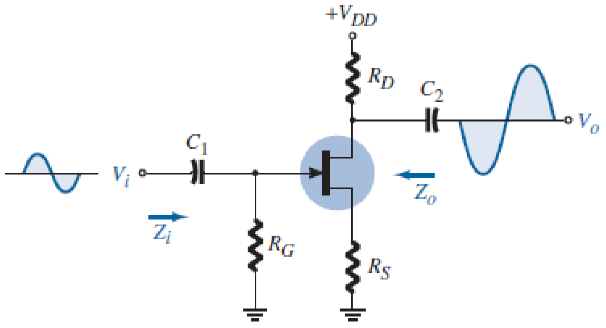
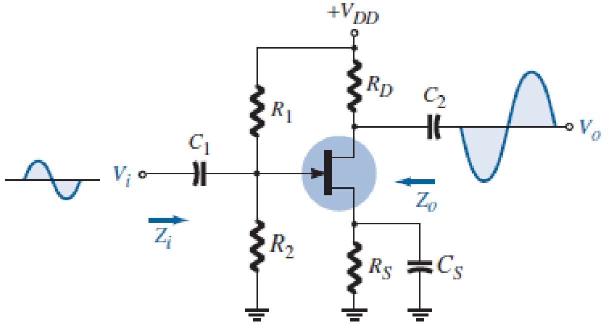
- The small signal analysis for D-MOSFET and E-MOSFET is same as JFET

- For E-MOSFET; $g_m = 2k(V_{GSQ} - V_{GS(Th)})$

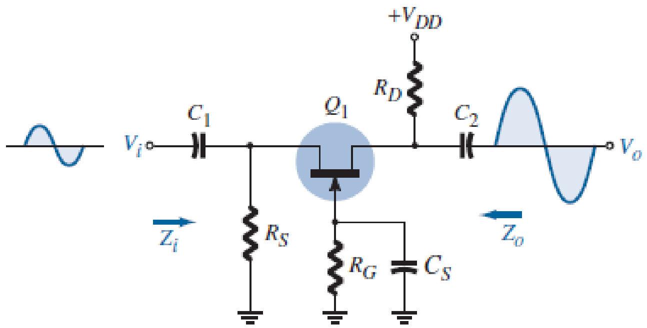
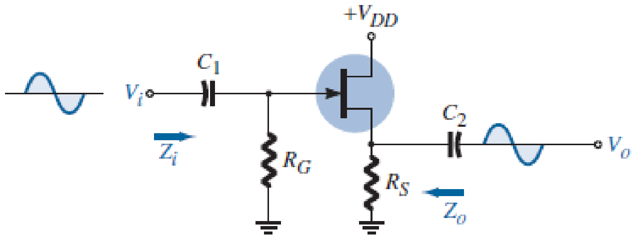
Summary Table

Fixed-bias [JFET or D-MOSFET] 	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $_{(r_d \geq 10\,R_D)}$	Medium (−10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $_{(r_d \geq 10\,R_D)}$
Self-bias bypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= \boxed{R_G}$	Medium (2 kΩ) $= \boxed{R_D \Vert r_d}$ $\cong \boxed{R_D}$ $_{(r_d \geq 10\,R_D)}$	Medium (−10) $= \boxed{-g_m(r_d \Vert R_D)}$ $\cong \boxed{-g_m R_D}$ $_{(r_d \geq 10\,R_D)}$

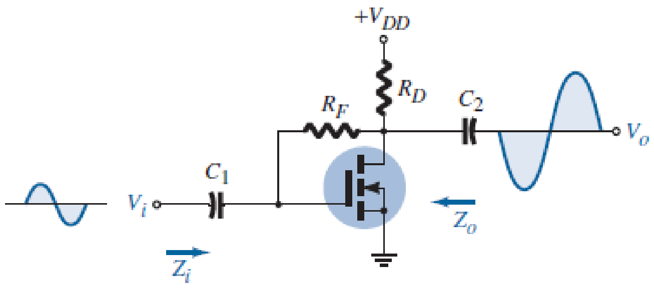
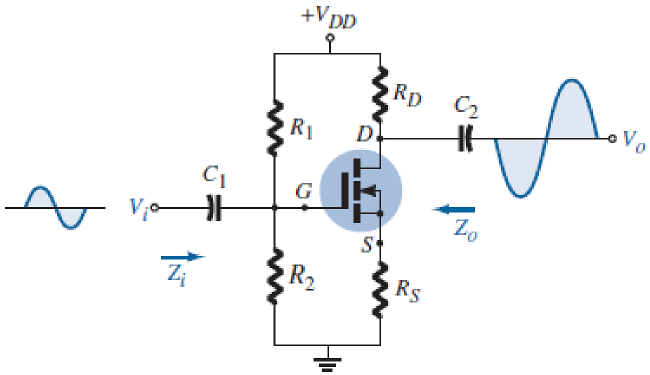
Summary Table

Self-bias unbypassed R_S [JFET or D-MOSFET] 	High (10 MΩ) $= \boxed{R_G}$	$= \boxed{\dfrac{\left[1 + g_mR_S + \dfrac{R_S}{r_d}\right]R_D}{\left[1 + g_mR_S + \dfrac{R_S}{r_d} + \dfrac{R_D}{r_d}\right]}}$ $= \boxed{R_D}$ $\quad r_d \geq 10\,R_D$ or $r_d = \infty\,\Omega$	Low (-2) $= \boxed{\dfrac{g_mR_D}{1 + g_mR_S + \dfrac{R_D + R_S}{r_d}}}$ $\cong \boxed{-\dfrac{g_mR_D}{1 + g_mR_S}}$ $\quad [r_d \geq 10\,(R_D + R_S)]$
Voltage-divider bias [JFET or D-MOSFET] 	High (10 MΩ) $= \boxed{R_1 \| R_2}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $\quad (r_d \geq 10\,R_D)$	Medium (-10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_mR_D}$ $\quad (r_d \geq 10\,R_D)$

Summary Table

Configuration	Z_i	Z_o	$A_v = \frac{V_o}{V_i}$
Common-gate [JFET or D-MOSFET] 	Low (1 kΩ) $= \boxed{R_S \Big\| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]}$ $\cong \boxed{R_S \Big\| \frac{1}{g_m}}$ $(r_d \geq 10 R_D)$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(R_d \geq 10 R_D)$	Medium (+10) $= \boxed{\frac{g_m R_D + \frac{R_D}{r_d}}{1 + \frac{R_D}{r_d}}}$ $\cong \boxed{g_m R_D}$ $(r_d \geq 10\, RD)$
Source-follower [JFET or D-MOSFET] 	High (10 MΩ) $= \boxed{R_G}$	Low (100 kΩ) $= \boxed{r_d \| R_S \| 1/g_m}$ $\cong \boxed{R_S \| 1 \| g_m}$ $(r_d \geq 10 R_S)$	Low (<1) $= \boxed{\frac{g_m(r_d \| R_S)}{1 + g_m(r_d \| R_S)}}$ $\cong \boxed{\frac{g_m R_S}{1 + g_m R_S}}$ $(r_d \geq 10 R_S)$

Summary Table

Drain-feedback bias E-MOSFET 	Medium (1 MΩ) $= \boxed{\dfrac{R_F + r_d \| R_D}{1 + g_m(r_d \| R_D)}}$ $\cong \boxed{\dfrac{R_F}{1 + g_m R_D}}$ $(r_d \geq 10\, R_D)$	Medium (2 kΩ) $= \boxed{R_F \| r_d \| R_D}$ $\cong \boxed{R_D}$ $(R_F, r_d \geq 10 R_D)$	Medium (−10) $= \boxed{-g_m(R_F \| r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(R_F, r_d \geq 10 R_D)$
Voltage-divider bias E-MOSFET 	Medium (1 MΩ) $= \boxed{R_1 \| R_2}$	Medium (2 kΩ) $= \boxed{R_D \| r_d}$ $\cong \boxed{R_D}$ $(r_d \geq 10\, R_D)$	Medium (–10) $= \boxed{-g_m(r_d \| R_D)}$ $\cong \boxed{-g_m R_D}$ $(r_d \geq 10\, R_D)$