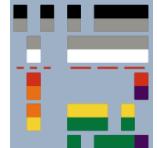


TRANSISTOR BASICS AND BIASING

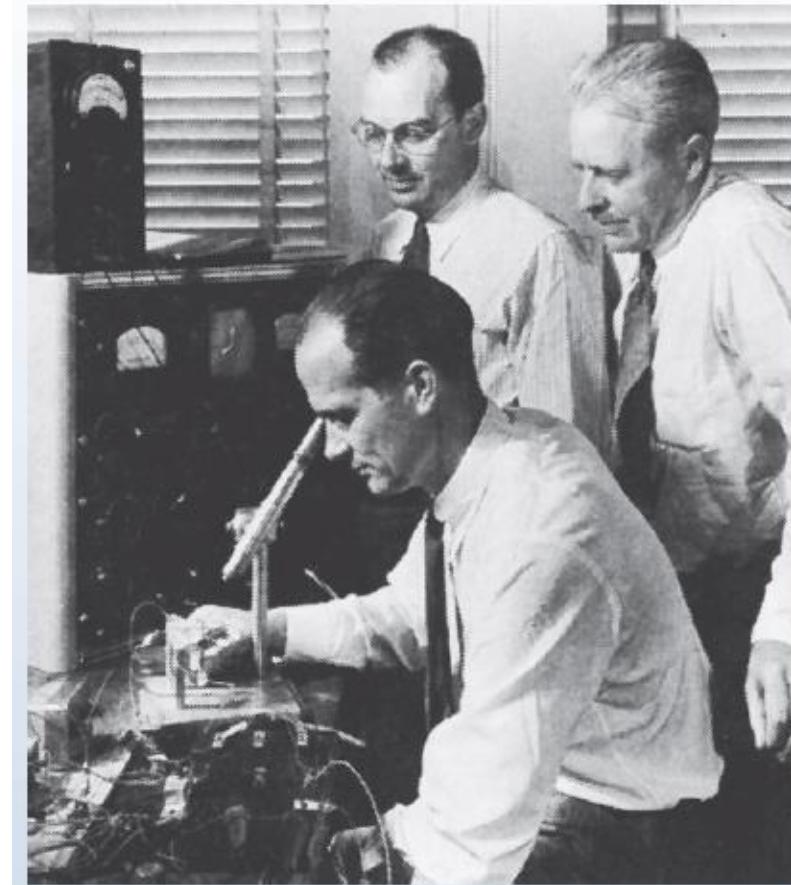


Topic Outcomes

- Become familiar with the basic construction and operating characteristics of the Bipolar Junction Transistor and Field Effect Transistors
- Be able to perform a load-line analysis of the most common BJT configurations and FET networks.
- Discuss and analyze various BJT and FET biasing configurations.

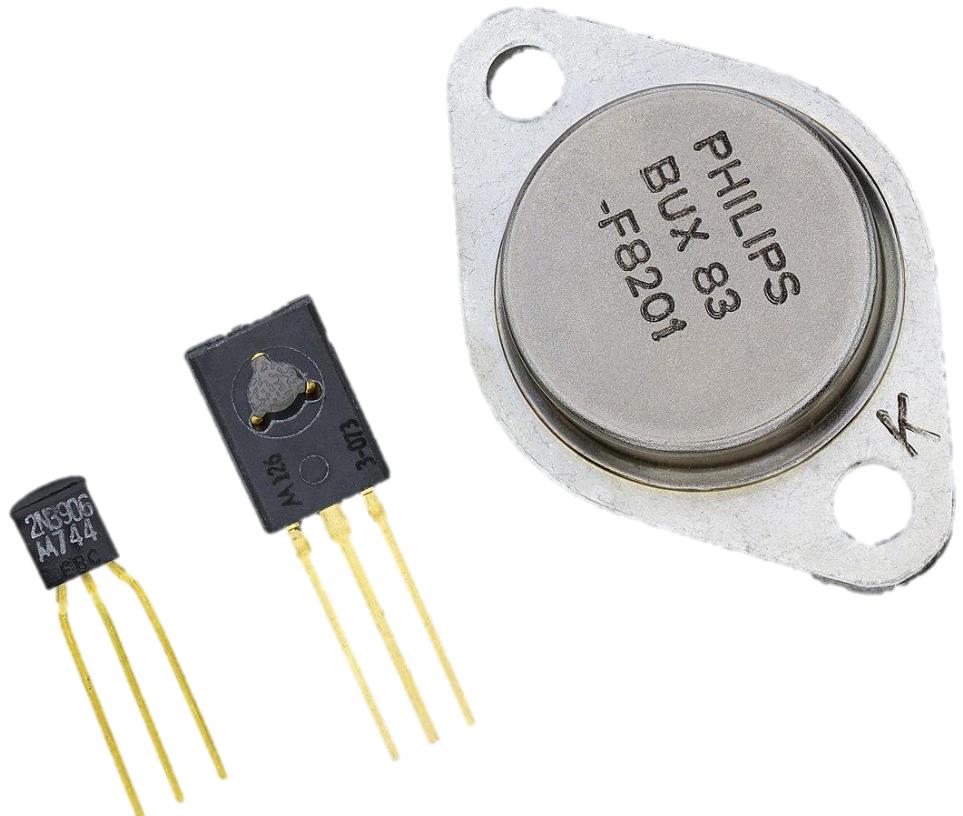
History

- 1904, the **vacuum-tube diode** was introduced by **J. A. Fleming**
- 1906, Lee De Forest added a third element, called the control grid, to the vacuum diode, resulting in the first amplifier, the **triode**.
- December 23, 1947, It was on the afternoon of this day that Dr. S. **William Shockley, Walter H. Brattain**, and **John Bardeen** demonstrated the amplifying action of the first transistor at the Bell Telephone Laboratories



Transistors

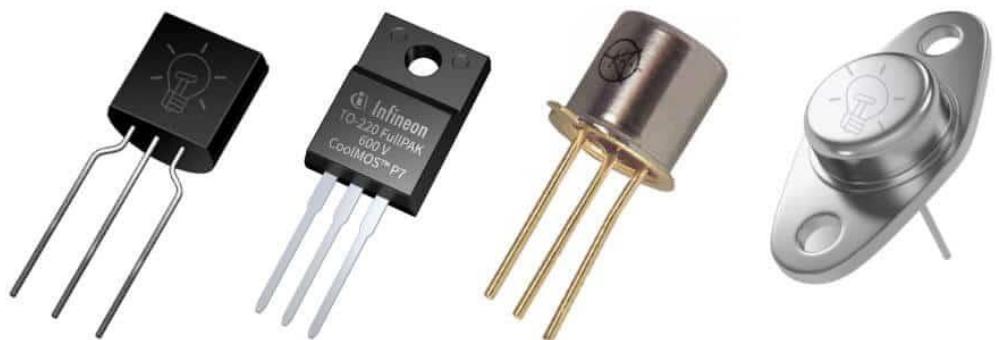
- The transistor is a **three-layer semiconductor** device consisting of either **two *n*- and one *p*-type** layers of material or **two *p*- and one *n*-type layers of material**. The former is called an **NPN transistor**, and the latter is called a **PNP transistor**.



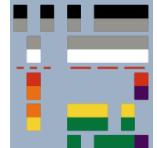
Transistor

- Common Types
 - Bipolar Junction Transistor (BJT)
 - NPN
 - PNP
 - Field Effect Transistor (FET)
 - JFET
 - N-type channel
 - P-type channel
 - MOSFET
 - Depletion Mode
 - Enhancement Mode

Types of Transistors
(BJT, FET, MOSFET, IGBT & Special Transistors)



Bipolar Junction Transistors



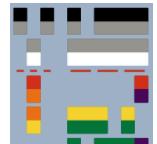
Transistor Fundamentals

- **Bipolar junction transistors (BJTs)** are three terminal semiconductor devices which could be used to amplify signals.
- The term **"bipolar"** reflects the fact that **holes** and **electrons** participate in the injection process into oppositely polarized material.
- It was introduced on **December 23, 1947** by **Walter H. Brattain** and **John Bardeen** at **Bell Telephone Laboratories**.



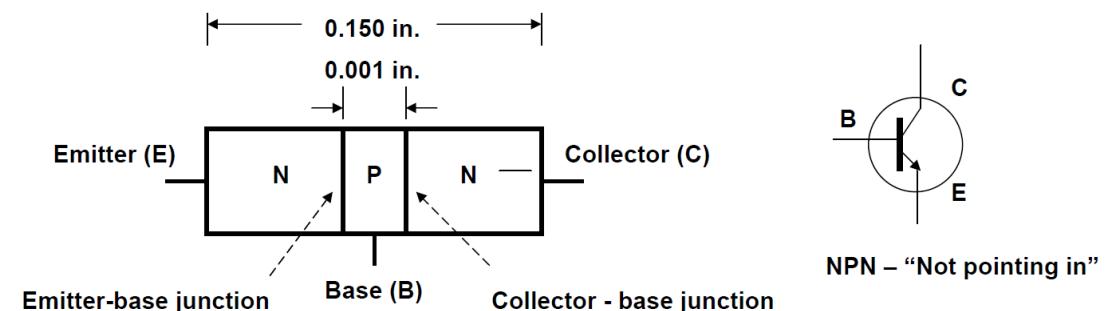
Transistor Fundamentals

- The **advantages** of transistors are:
 - Smaller and lightweight
 - No heater requirements (unlike vacuum tubes)
 - More power efficient than vacuum tubes because it absorbs less power and does not need a heating element
 - Rugged construction and are therefore less prone to damage
 - It can operate upon power up because it does not need to be warmed-up before it operates (unlike vacuum tubes).
 - It can operate with lower voltages.
 - It is cheaper because the materials used are abundant and less expensive.



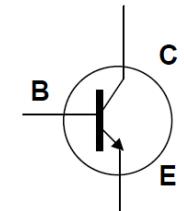
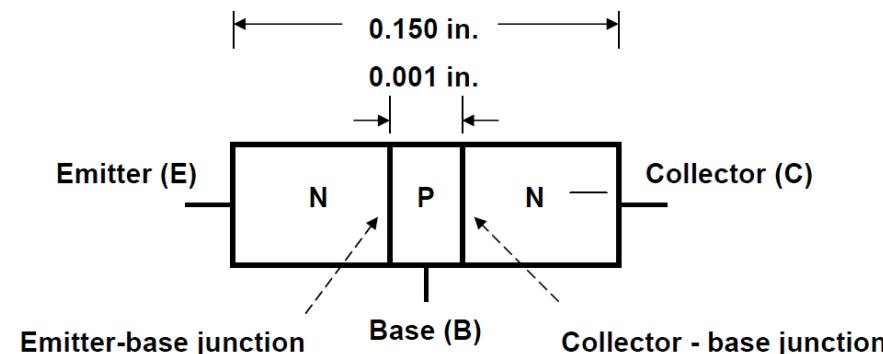
Bipolar Junction Transistors

- The two basic types of bipolar junction transistor are **NPN** and **PNP** transistor.
- NPN and PNP transistors could be constructed using **Silicon, Germanium, or GaAs** as the base material.
- The three layers / terminals of a BJT are the **emitter (E)**, **base (B)**, and **collector (C)**.
- The **emitter** layer is **heavily doped**, the **collector** is **lightly doped**, and the **base** is **lightly doped**.
- The **less doped** a material is, the **less is its conductivity** or the **higher is its resistance**.
- The **emitter** and **collector** layers are **wider** than the base layer.



Transistor Construction

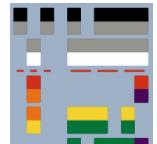
- The construction is similar to **two diodes** whose **anodes** are connected but its operation is **quite different**.
- Just like in a semiconductor diode, the **majority carriers** in the **n-type material** are **electrons** and the **majority carriers** in the **p-type** material are **holes**.
- Through the application of **biasing voltages** and /or **signals**, the emitter-base junction and collector-base junction can be made **forward or reverse biased**, but the required biasing is dependent on the application for which the transistor is used.
- The **direction of the arrow in the emitter** is the **same as the direction of conventional current flow** in the emitter.
- For the transistor shown, the ratio of the total width to that of the center layer is $0.150/0.001 = 150:1$.



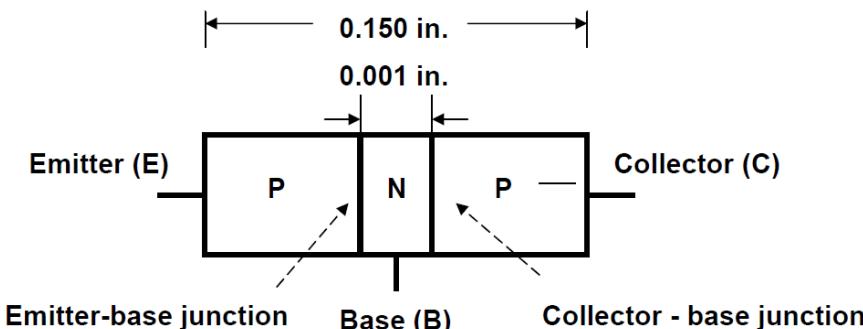
NPN – “Not pointing in”

**Construction of
NPN BJT**

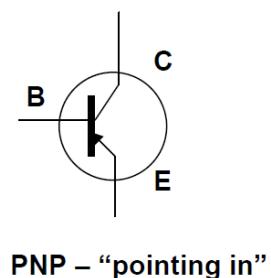
**Schematic Symbol of
NPN BJT**



Transistor Construction

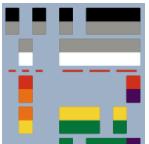


**Construction of
PNP BJT**



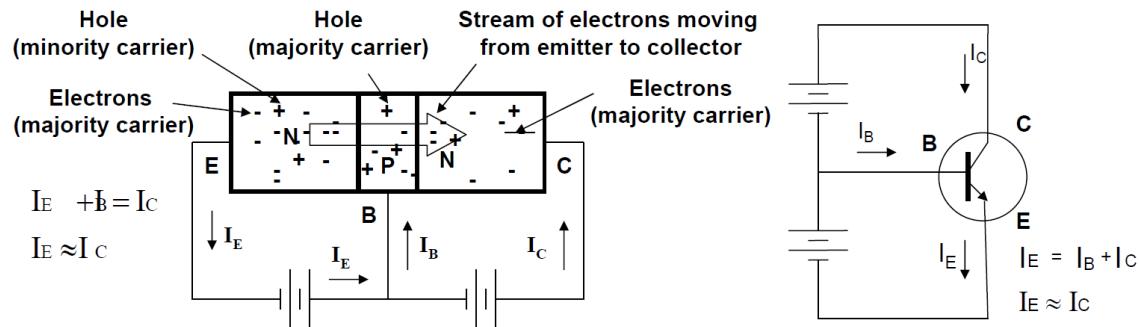
**Schematic Symbol of
PNP BJT**

- The construction is similar to **two diodes** whose **cathodes** are connected but its operation is **quite different**.
- Just like in a semiconductor diode, the **majority carriers** in the **n-type material** are **electrons** and the **majority carriers** in the **p-type** material are **holes**.
- Through the application of **biasing voltages** and /or **signals**, the emitter-base junction and collector-base junction can be made **forward or reverse biased**, but the required biasing is dependent on the application for which the transistor is used.
- The **direction of the arrow in the emitter** is the **same as the direction of conventional current flow** in the emitter.
- For the transistor shown, the ratio of the total width to that of the center layer is $0.150/0.001 = 150:1$.



Transistor Operation

- **NPN transistor** with typical biasing voltages applied between the emitter and the base, and between the collector and the base.
- The biasing voltages make the **emitter-base junction forward biased** while the **collector-base junction reversed biased**.
- Since the **emitter-base junction is forward biased**, there will be **electron flow** (majority carrier) from the **emitter to the base**.
- Since the **base layer is very thin** and has **low conductivity** (few majority carriers), electrons from the emitter **will not contribute much** to the **base current** but instead, the electrons will **move on into the collector layer** and will be attracted towards the positive terminal of the battery between the collector and the base.
- The result is that the **emitter current** is **almost equal** to the **collector current** and there will be relatively **low base current**.

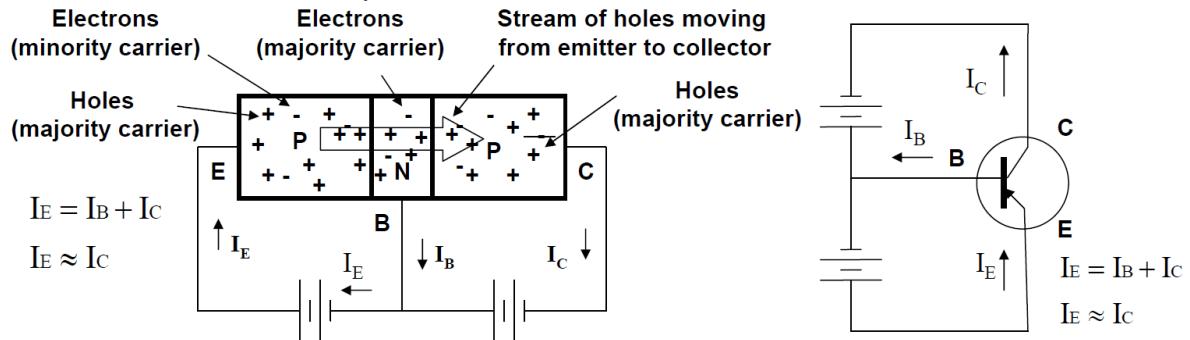


NPN BJT with Biasing Voltages

1



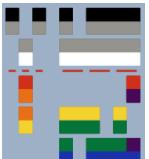
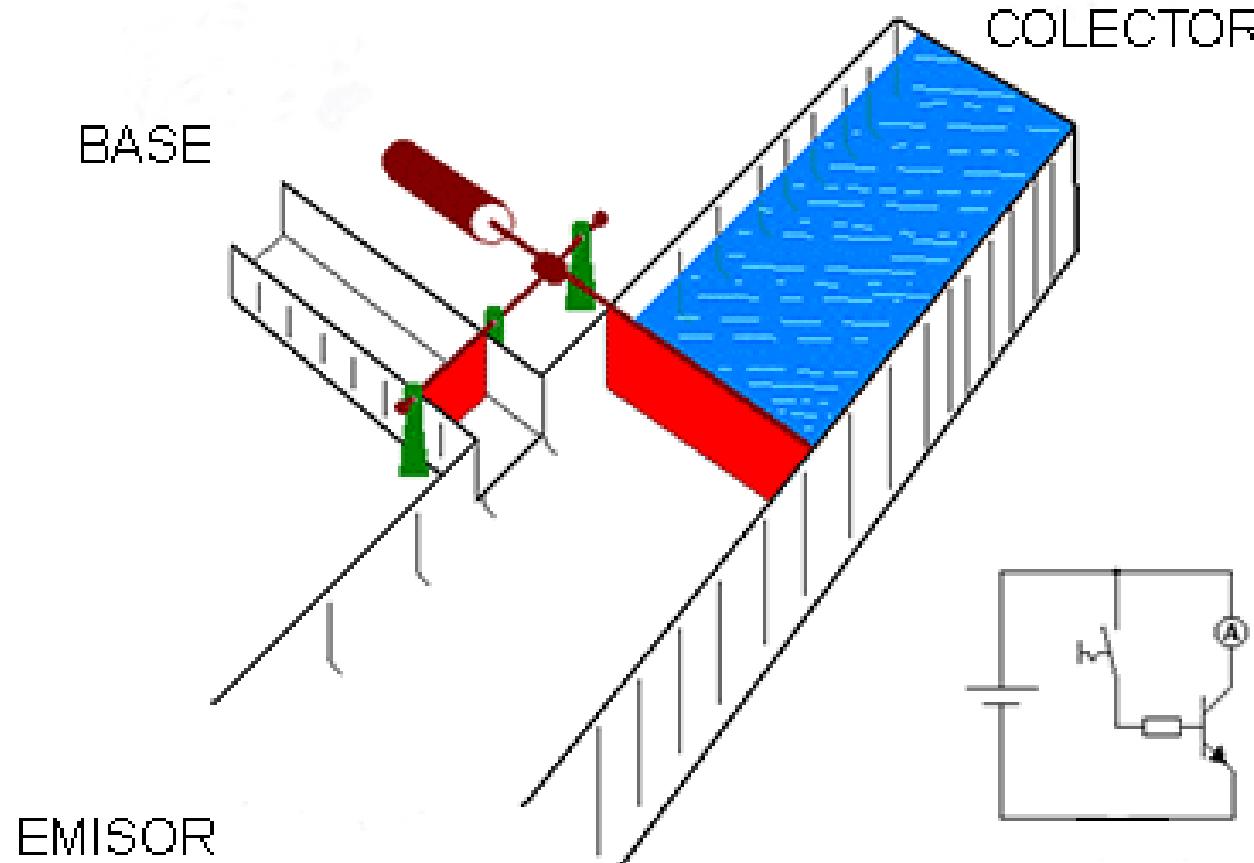
Transistor Operation



PNP BJT with Biasing Voltages

- **PNP transistor** with typical biasing voltages applied between the emitter and the base, and between the collector and the base.
- The biasing voltages make the **emitter-base junction forward biased** while the **collector-base junction reversed biased**.
- Since the **emitter-base junction is forward biased**, there will be **hole flow** (majority carrier) from the **emitter to the base**.
- Since the **base layer is very thin** and has **low conductivity** (few majority carriers), holes from the emitter **will not contribute much** to the **base current** but instead, the holes will **move on into the collector layer** and will be attracted towards the positive terminal of the battery between the collector and the base.
- The result is that the **emitter current** is **almost equal** to the **collector current** and there will be relatively **low base current**.

Transistor Operation



Transistor Operation

- For both NPN and PNP transistors, the **electron flow is opposite** to the **conventional current flow**.
- The **emitter current (I_E)** is equal to the **sum** of the base current (I_B) and collector current (I_C).

$$I_E = I_B + I_C$$

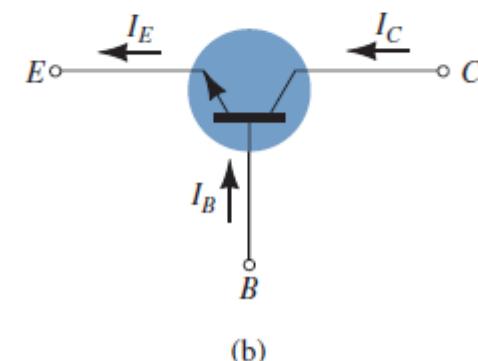
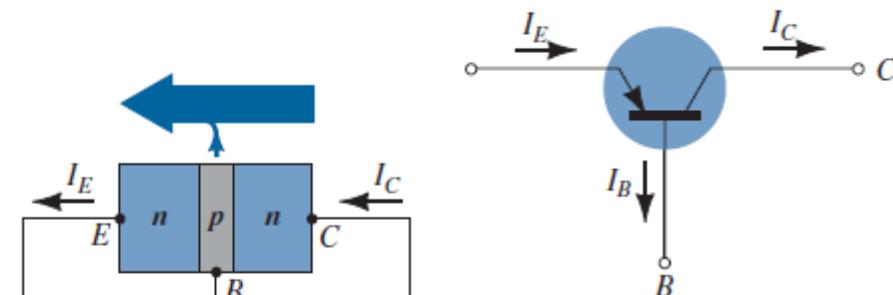
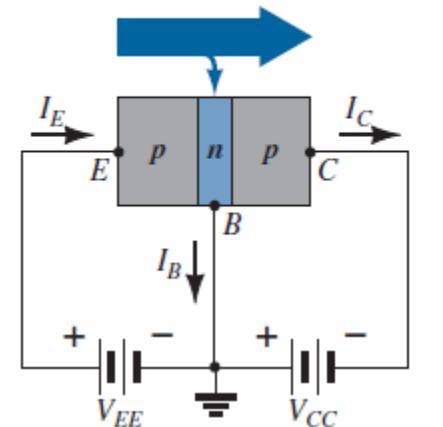
$$I_E \approx I_C$$

- Typical values of **base current** are in the range of **microamperes** if the **emitter and collector currents** are in the **miliampere range**.
- The **collector current** is comprised of **majority carriers** and **minority carriers**.
- The **collector current** due to the **minority carriers** is the **leakage current (I_{CO})**.

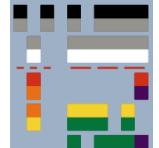
$$I_C = I_{C\text{ majority}} + I_{C\text{ minority}} = \text{collector current}$$

$$I_{C\text{ minority}} = I_{CO} = \text{collector leakage current}$$

- The **leakage current (I_{CO})** is **present** as long as the voltage supply between the base and collector is present with the indicated polarity, even if the voltage supply between the base and emitter is **removed**.
- The **leakage current (I_{CO})** is **temperature sensitive** and it **increases** when the temperature of the device increases.

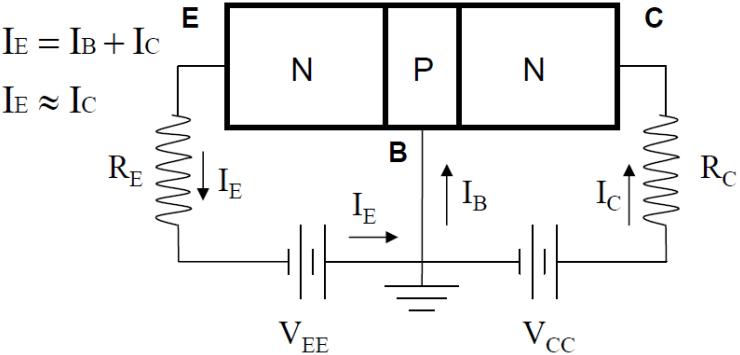
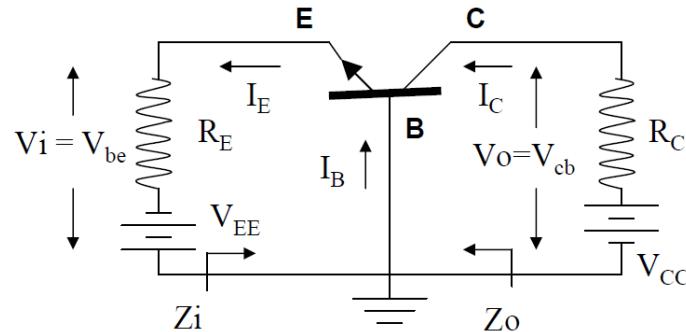


Transistor Configurations

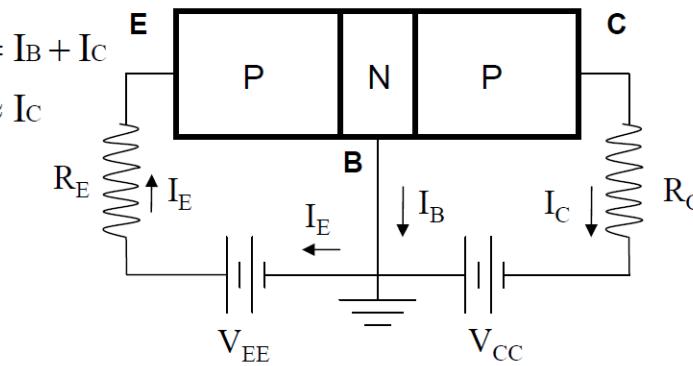
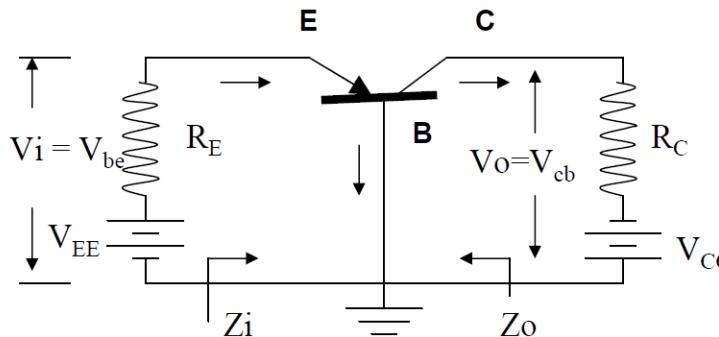


Common Base Configuration

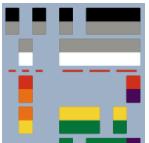
- **Common Base** - derived from the fact that the base is common to both the **input and output sides** of the configuration
- The base is **common** to the **output (V_o)** and the **input (V_i)**, and the **base** is usually **closest to or connected to the ground**.
- The **input** is between the **base and the emitter** while the **output** is between the **base and the collector**.
- The **input** is **usually at the left side** of the circuit while the **output** is **usually at the right side** of the circuit.
- The **base-emitter junction** is **forward biased** and the **collector-base junction** is **reverse biased**.
- Has **low current gain** but **high voltage gain**.



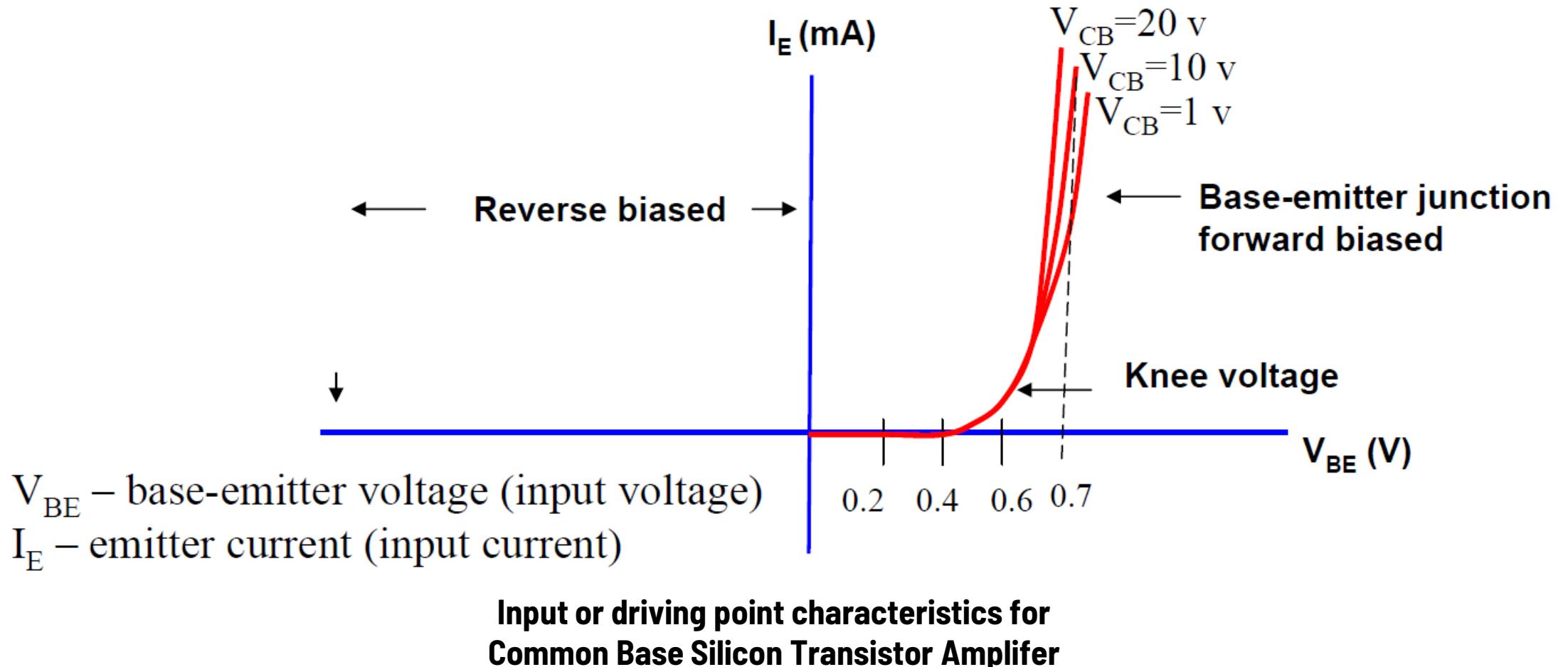
Common Base NPN Transistor Configuration



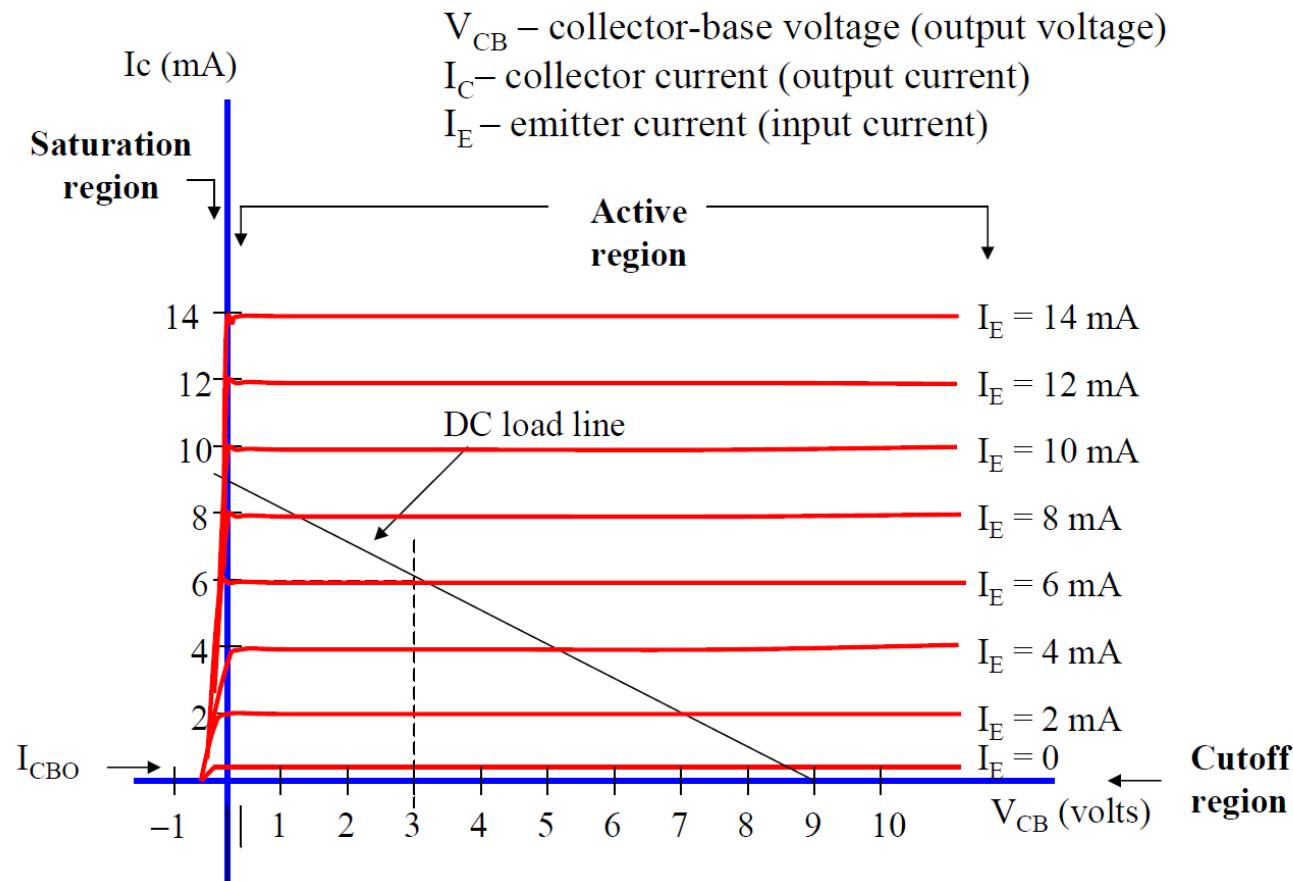
Common Base PNP Transistor Configuration



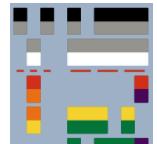
Common Base Configuration



Common Base Configuration

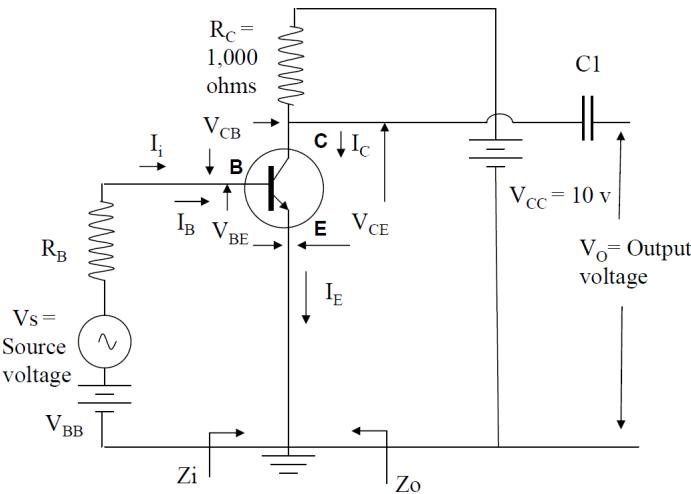


Output or collector characteristics for
Common Base Silicon Transistor Amplifier

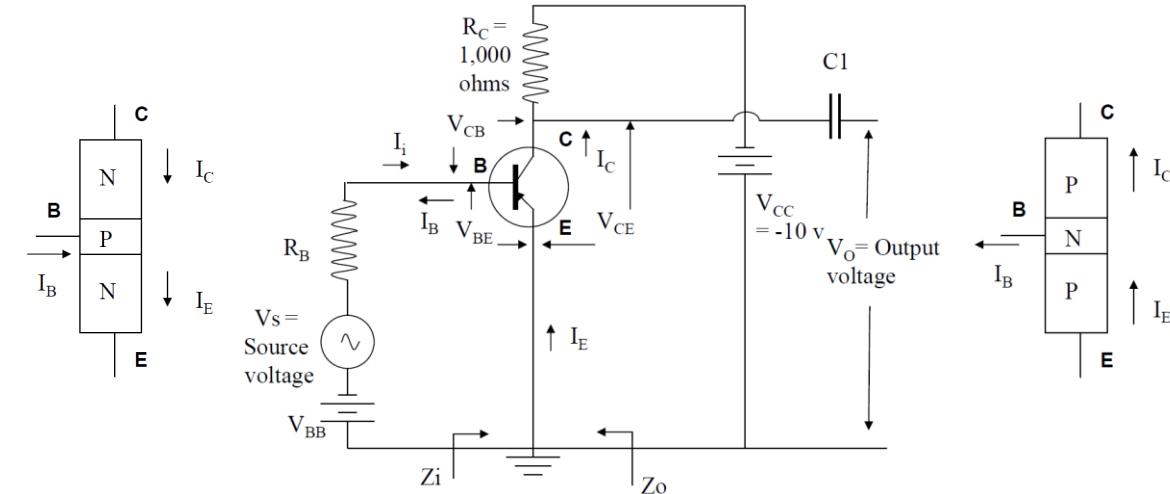


Common Emitter Configuration

- The emitter is **common** to the **output (V_o)** and the **input (V_i)**, and the **emitter** is usually **closest to** or **connected to the ground**.
- The **input** is between the **base and the emitter** while the **output** is between the **emitter and the collector**.
- The most frequently encountered transistor configuration

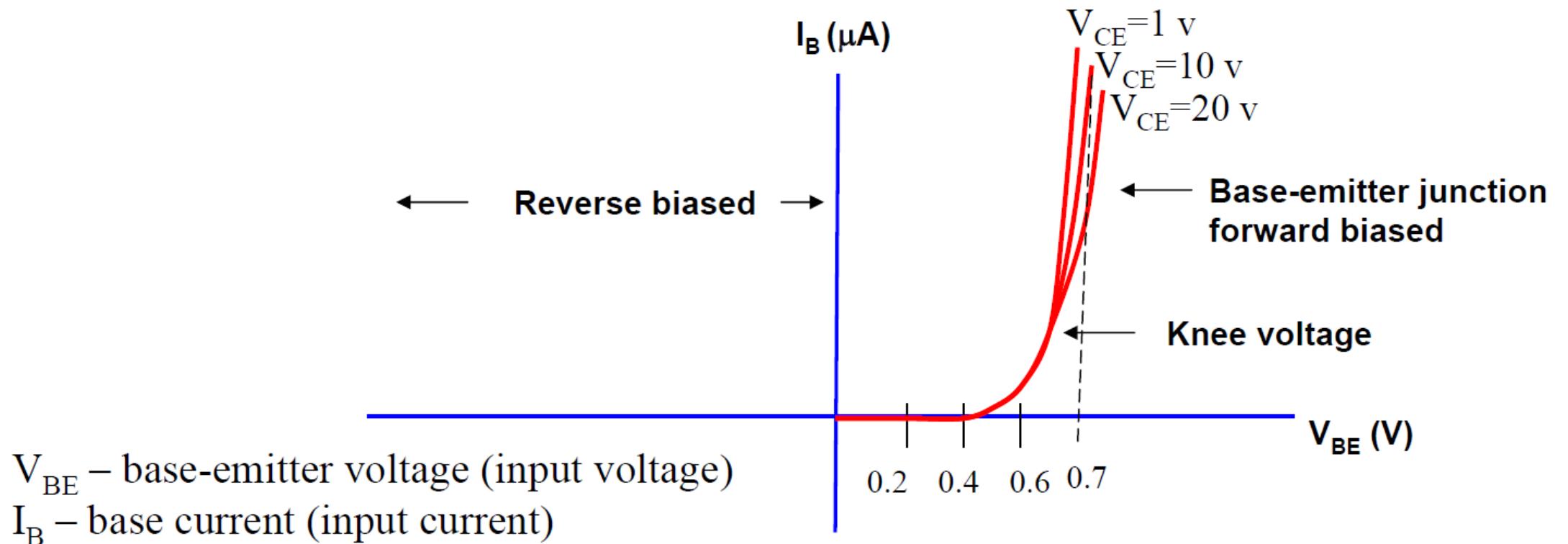


Common Emitter
NPN Transistor Configuration



Common Emitter
PNP Transistor Configuration

Common Emitter Configuration



**Input or driving point characteristics for
Common Emitter Silicon Transistor Amplifier**

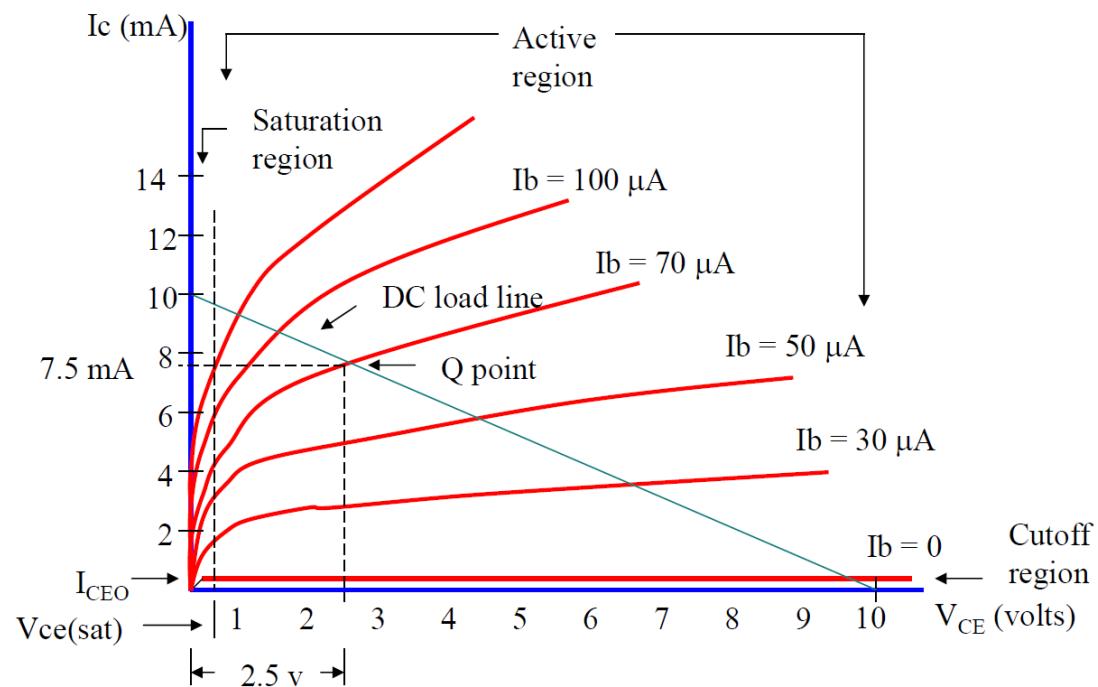
Common Emitter Configuration

V_{CE} – collector-emitter voltage (output voltage)

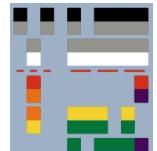
I_C – collector current (output current)

I_b – base current (input current)

I_{CEO} – collector leakage current for common emitter configuration

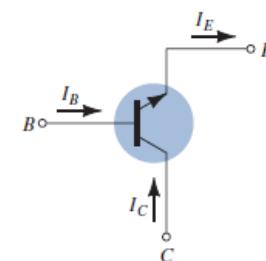
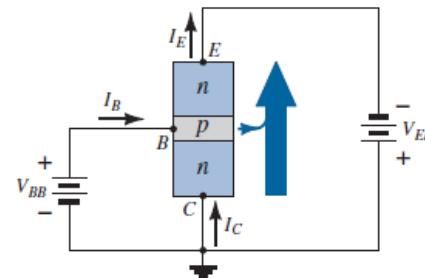


**Output or collector characteristics for
Common Emitter Silicon Transistor Amplifier**

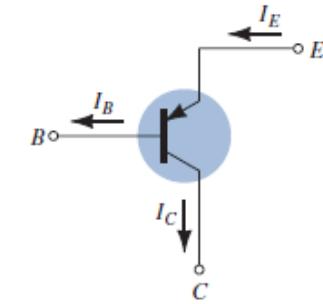
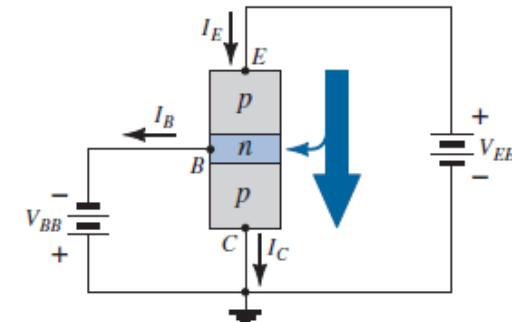


Common Collector Configuration

- The **collector** is **common** to the **output (V_o)** and the **input (V_i)**, and the **collector** is **connected to the ground for ac signals**. For **ac signal analysis**, dc voltages are considered **shorted**.
- The **input signal** is at the **base** while the **output** is taken at the **emitter**.
- Sometimes called **Emitter Follower**
- Has **unity voltage gain**

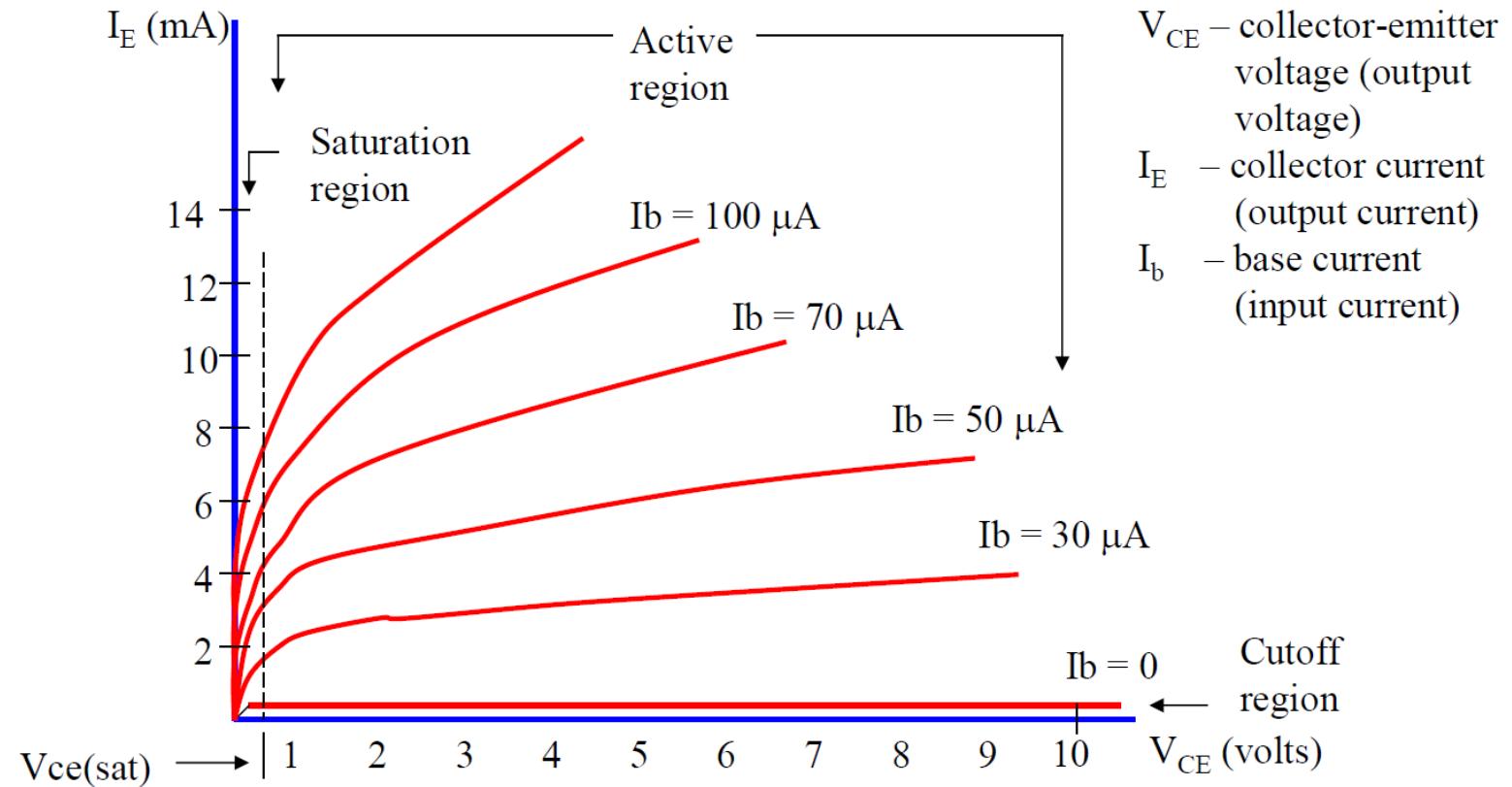


Common Collector
NPN Transistor Configuration



Common Collector
PNP Transistor Configuration

Common Collector Configuration



Output characteristics for
Common Collector Silicon Transistor Amplifier

Other Transistor Basics

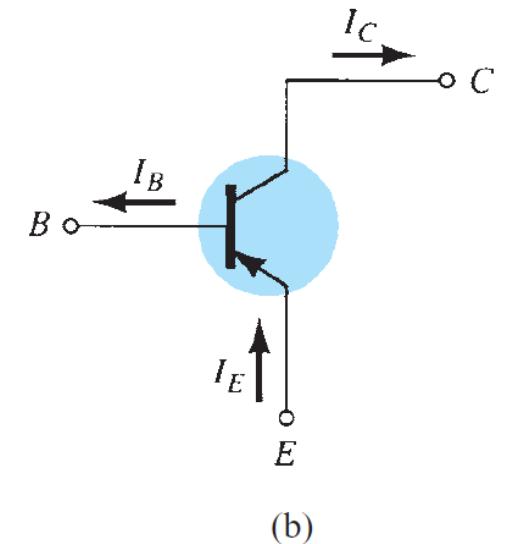
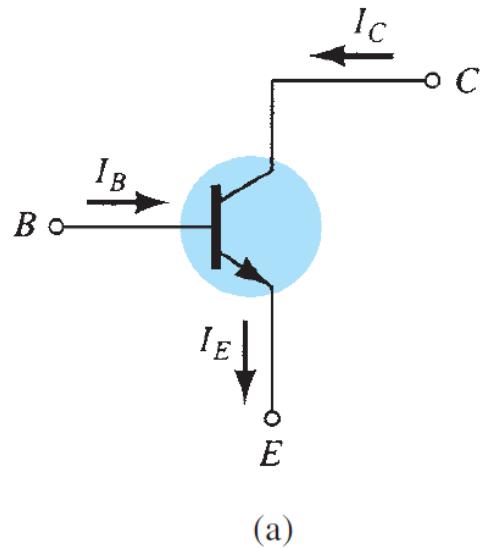
- For each transistor there is a region of operation on the characteristics that will ensure that the maximum ratings are not being exceeded and the output signal exhibits minimum distortion.
- All of the limits of operation are defined on a typical transistor specification sheet

Operating Regions

- In the **active region** the base-emitter junction is forward-biased, whereas the collector-base junction is reverse-biased. Active - Operating range of the amplifier
 - once a transistor is in the “on” state, the base-to-emitter voltage will be assumed to be the following: $V_{BE} = 0.7V$
- In the **cutoff region** the base-emitter and collector-base junctions of a transistor are both reverse-biased. Cutoff - The amplifier is basically off. There is voltage, but little current
- In the **saturation region** the base-emitter and collector-base junctions are forward-biased. Saturation – The amplifier is fully on. There is current but little voltage.

Transistor Currents

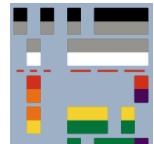
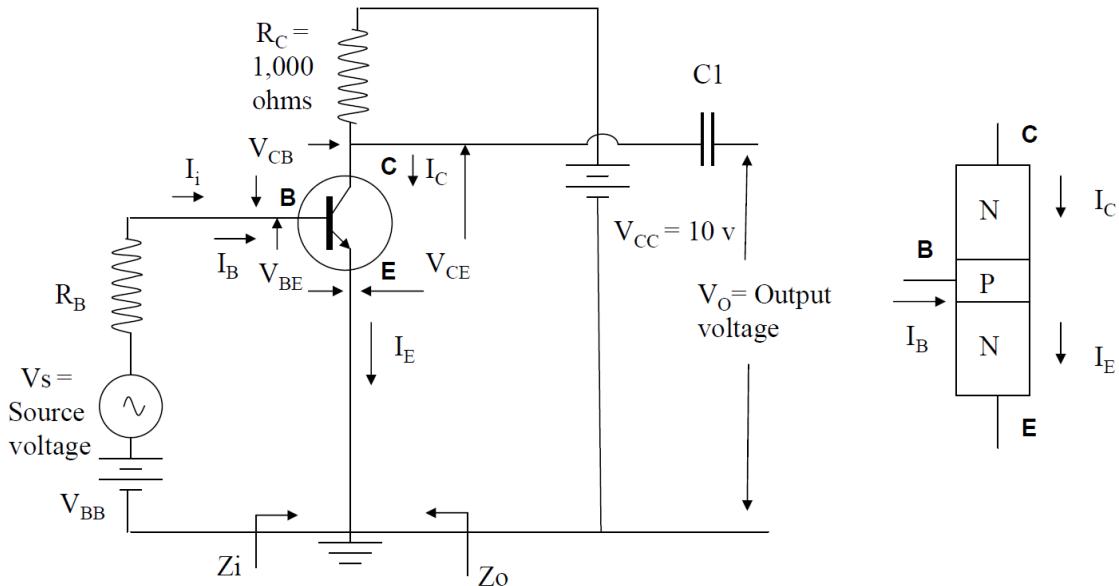
- I_B - Base current
- I_C - Collector current
- I_E - Emitter current



**Transistor Currents for (a) NPN ; B(PNP)
transistors**

Transistor Voltages

- **V_{CC} – collector biasing voltage.** This is a power supply that is directly or indirectly applied to the collector terminal of the transistor.
- **V_{BB} – base biasing voltage.** This is a DC voltage that is used to bias the base of the transistor. It may be directly applied from a DC applied voltage or may be applied to the base by a resistor circuit.
- **V_{EE} – emitter biasing voltage.** For common emitter, V_{EE} will be nothing more than a ground connection.
- **V_C** – Collector-to-ground voltage
- **V_B** – Base-to-ground voltage
- **V_E** – Emitter-to-ground voltage
- **V_{BE}** – voltage between base-emitter junction. Also equal to $(V_B - V_E) \approx 0.7\text{Volts}$
- **V_{CE}** – voltage between collector-emitter junction. Also equal to $(V_C - V_E)$



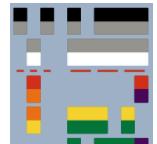
Current gain

- Current gain for Common Base is alpha (α) which **is less than one but close to one.**
 - Typical values are in the range of **0.9 to 0.998**.
- Current gain for Common Emitter is beta (β) which is **always greater than 1.**
 - Typical values are in the range of **50 to 400**.
 - Usually specified as h_{FE} on specification sheets.
- Current gain for Common Collector is gamma (γ) which is **always greater than 1.**
 - Always greater than β .
- Current gain relationships

$$\alpha = \frac{I_C}{I_E}; \quad \beta = \frac{I_C}{I_B}; \quad \gamma = \frac{I_E}{I_B}$$

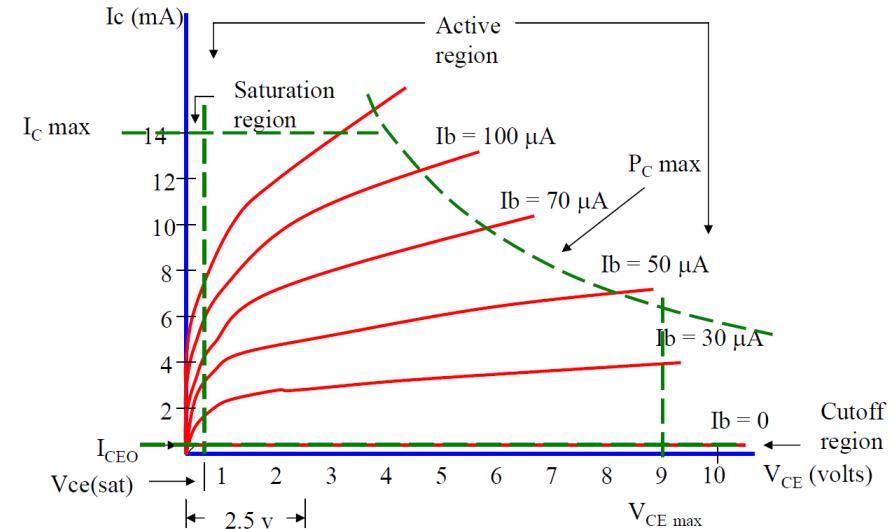
$$I_C = \alpha I_E; \quad I_C = \beta I_B; \quad I_E = \gamma I_B$$

$$\alpha = \frac{\beta}{\beta+1}; \quad \beta = \frac{\alpha}{1-\alpha}; \quad \gamma = \beta + 1$$

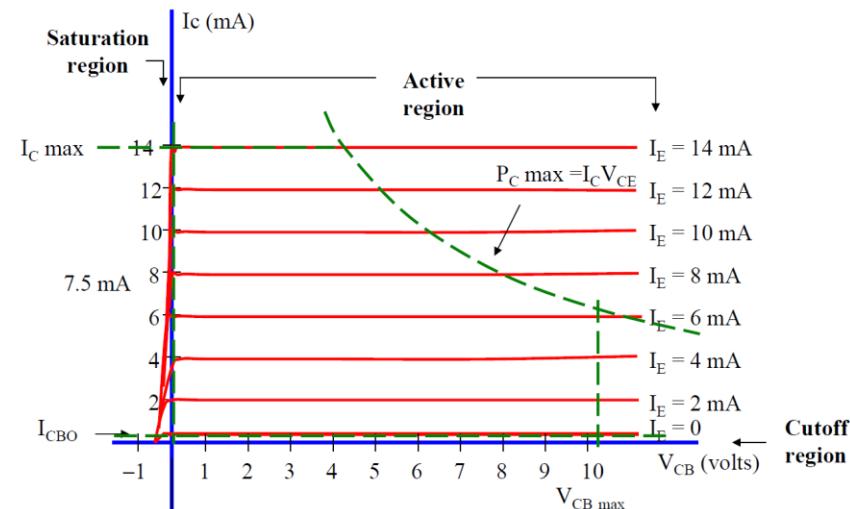


Power Dissipation

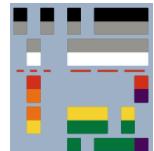
- The equations define the linear (undistorted) region of operation for a transistor.
- Common Base: $P_{Cmax} = V_{CB}I_C$
- Common-Emitter: $P_{Cmax} = V_{CE}I_C$
- Common-Collector: $P_{Cmax} = V_{CE}I_E$



Common Emitter Limits of Operation



Common Base Limits of Operation



Transistor Specification Sheet

MAXIMUM RATINGS

Rating	Symbol	2N4123	Unit
Collector-Emitter Voltage	V_{CEO}	30	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector Current – Continuous	I_C	200	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	625 5.0	mW mW°C
Operating and Storage Junction Temperature Range	T_j, T_{stg}	-55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C W

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit

OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage (1) ($I_C = 1.0 \text{ mA}\text{dc}$, $I_E = 0$)	$V_{(BR)CEO}$	30		Vdc
Collector-Base Breakdown Voltage ($I_C = 10 \mu\text{A}\text{dc}$, $I_E = 0$)	$V_{(BR)CBO}$	40		Vdc
Emitter-Base Breakdown Voltage ($I_E = 10 \mu\text{A}\text{dc}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	Vdc
Collector Cutoff Current ($V_{CB} = 20 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	50	nA\text{dc}
Emitter Cutoff Current ($V_{BE} = 3.0 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	50	nA\text{dc}



Transistor Specification Sheet

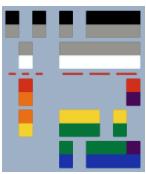
ON CHARACTERISTICS

DC Current Gain(1) ($I_C = 2.0 \text{ mA}_\text{dc}$, $V_{CE} = 1.0 \text{ V}_\text{dc}$) ($I_C = 50 \text{ mA}_\text{dc}$, $V_{CE} = 1.0 \text{ V}_\text{dc}$)	h_{FE}	50 25	150 —	—
Collector-Emitter Saturation Voltage(1) ($I_C = 50 \text{ mA}_\text{dc}$, $I_B = 5.0 \text{ mA}_\text{dc}$)	$V_{CE(\text{sat})}$	—	0.3	V_dc
Base-Emitter Saturation Voltage(1) ($I_C = 50 \text{ mA}_\text{dc}$, $I_B = 5.0 \text{ mA}_\text{dc}$)	$V_{BE(\text{sat})}$	—	0.95	V_dc

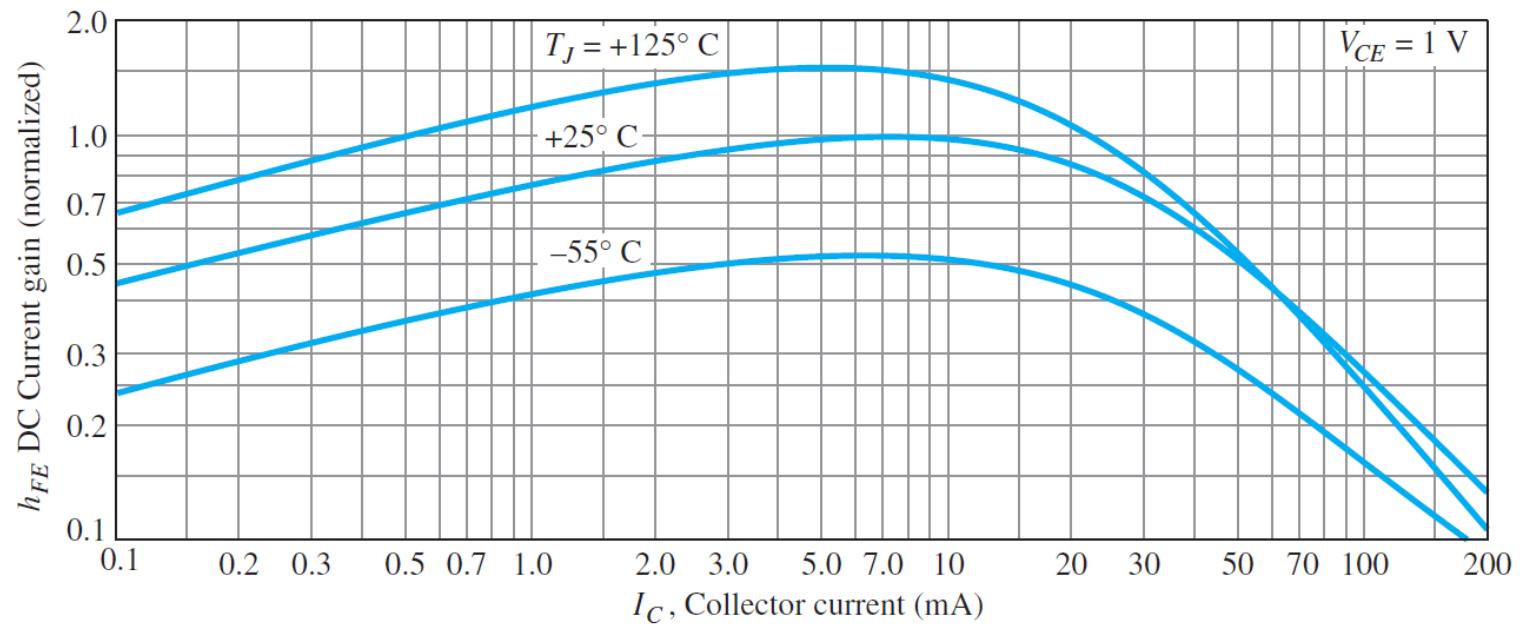
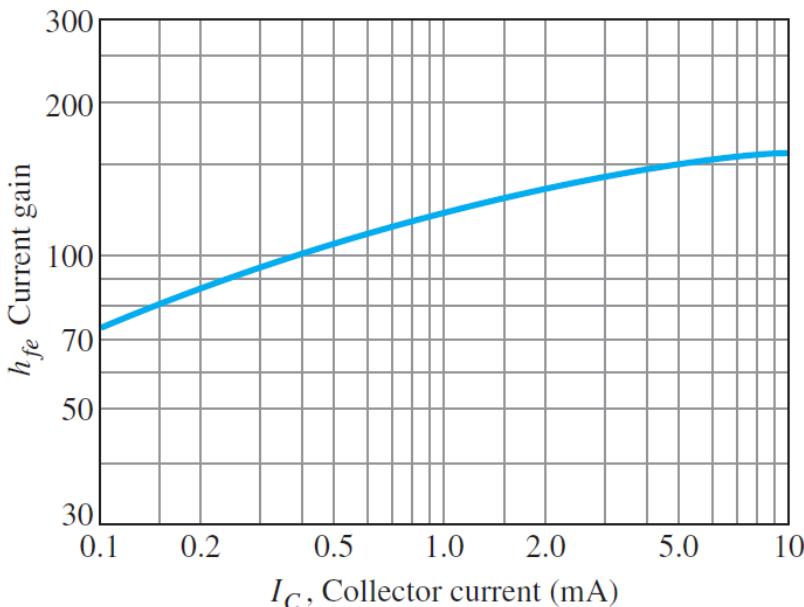
SMALL-SIGNAL CHARACTERISTICS

Current-Gain – Bandwidth Product ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 20 \text{ V}_\text{dc}$, $f = 100 \text{ MHz}$)	f_T	250	—	MHz
Output Capacitance ($V_{CB} = 5.0 \text{ V}_\text{dc}$, $I_E = 0$, $f = 100 \text{ MHz}$)	C_{obo}	—	4.0	pF
Input Capacitance ($V_{BE} = 0.5 \text{ V}_\text{dc}$, $I_C = 0$, $f = 100 \text{ kHz}$)	C_{ibo}	—	8.0	pF
Collector-Base Capacitance ($I_E = 0$, $V_{CB} = 5.0 \text{ V}$, $f = 100 \text{ kHz}$)	C_{cb}	—	4.0	pF
Small-Signal Current Gain ($I_C = 2.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}_\text{dc}$, $f = 1.0 \text{ kHz}$)	h_{fe}	50	200	—
Current Gain – High Frequency ($I_C = 10 \text{ mA}_\text{dc}$, $V_{CE} = 20 \text{ V}_\text{dc}$, $f = 100 \text{ MHz}$) ($I_C = 2.0 \text{ mA}_\text{dc}$, $V_{CE} = 10 \text{ V}$, $f = 1.0 \text{ kHz}$)	h_{fe}	2.5 50	— 200	—
Noise Figure ($I_C = 100 \mu\text{A}_\text{dc}$, $V_{CE} = 5.0 \text{ V}_\text{dc}$, $R_S = 1.0 \text{ k ohm}$, $f = 1.0 \text{ kHz}$)	NF	—	6.0	dB

(1) Pulse Test: Pulse Width = 300 μs . Duty Cycle = 2.0%

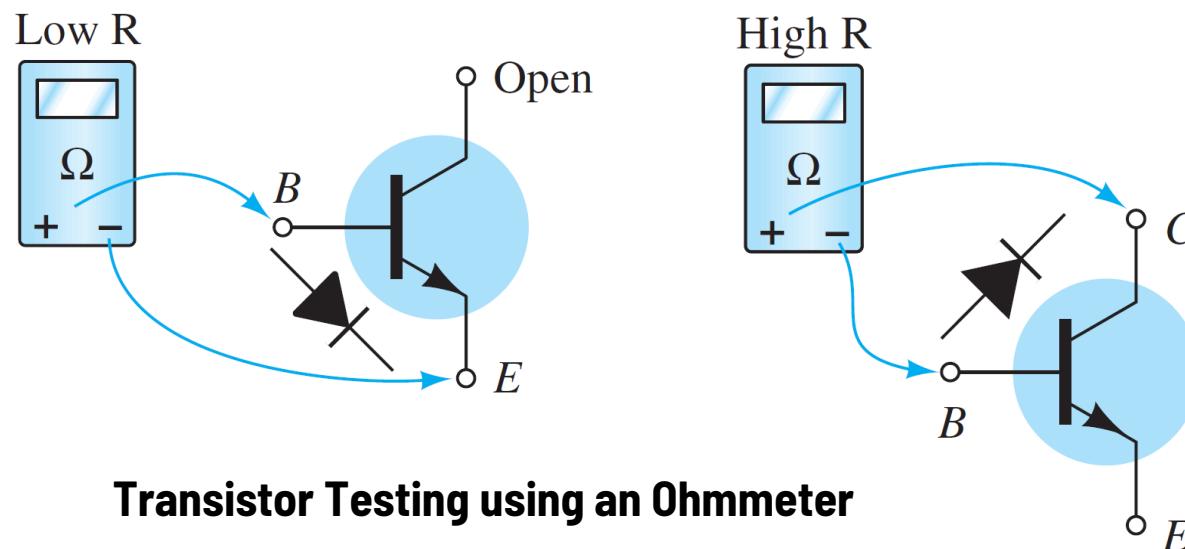


Transistor Specification Sheet



Transistor Testing

- Curve tracer - provides a graph of the characteristic curves.
- DMM - some DMMs measure β_{DC} or h_{FE}
- Ohmmeter

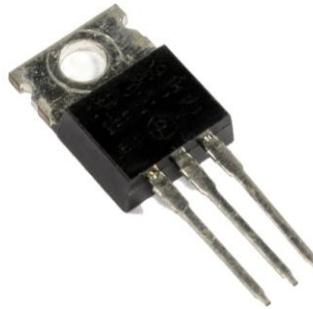


Transistor Testing using an Ohmmeter

Transistor Casing and Terminal Identification



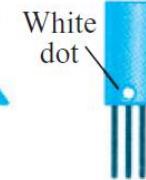
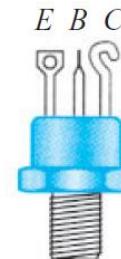
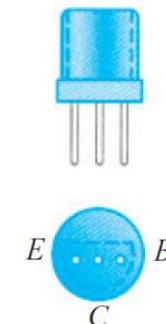
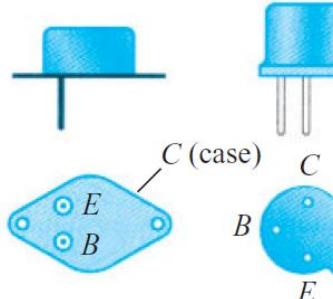
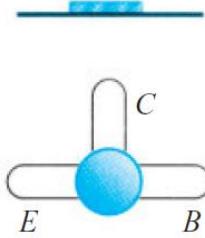
TO-92



TO-220

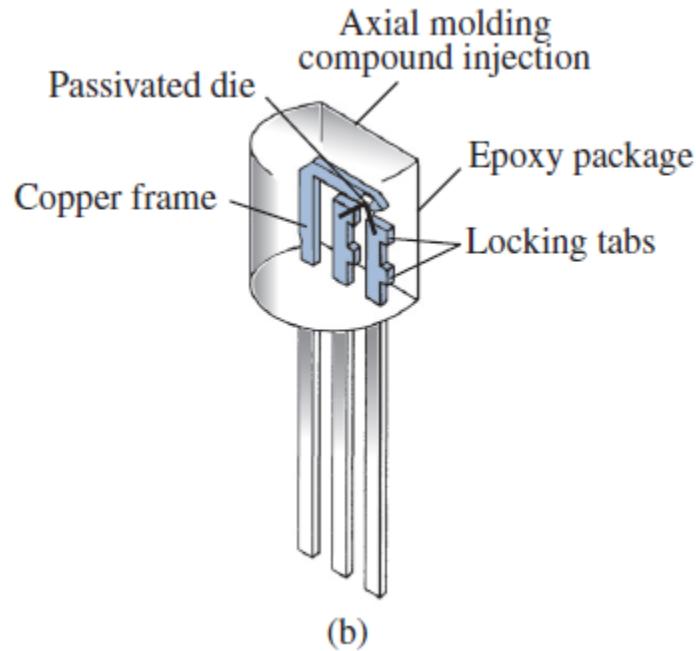


TO-3

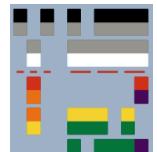


Transistor Terminal
Identification

Transistor Casing and Terminal Identification



**Internal construction of a
Fairchild transistor in a T0-92
package**



Equations

Equations

$$I_E = I_C + I_B,$$

$$\alpha_{dc} = \frac{I_C}{I_E},$$

$$\beta_{dc} = \frac{I_C}{I_B},$$

$$I_C = \beta I_B,$$

$$I_C = I_{C_{\text{majority}}} + I_{CO_{\text{minority}}},$$

$$\alpha_{ac} = \left. \frac{\Delta I_C}{\Delta I_E} \right|_{V_{CB}=\text{constant}},$$

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{V_{CE}=\text{constant}},$$

$$I_E = (\beta + 1)I_B,$$

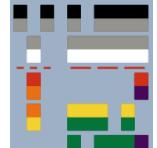
$$V_{BE} \equiv 0.7 \text{ V}$$

$$I_{CEO} = \left. \frac{I_{CBO}}{1 - \alpha} \right|_{I_B=0 \mu\text{A}}$$

$$\alpha = \frac{\beta}{\beta + 1}$$

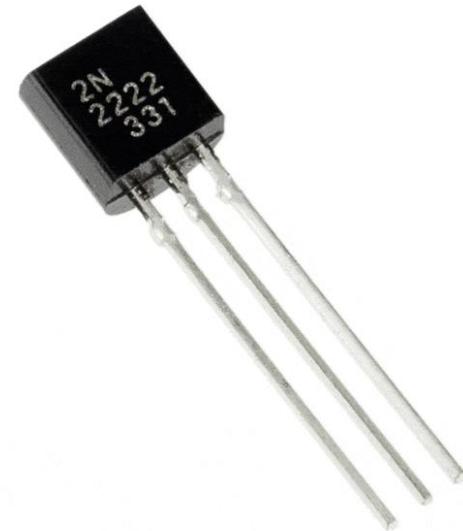
$$P_{C_{\text{max}}} = V_{CE} I_C$$

DC Transistor Biasing



Transistor Biasing

- Transistor biasing means to **keep the input circuit** (i.e. base-emitter junction) **always forward biased** and **output circuit** (i.e. collector-base junction) **always reverse biased**. To ensure this, the following basic conditions must be fulfilled:
 1. There should be **proper zero signal current flow**. In other words, in the **absence of signal**, the collector current should be at least equal to the maximum collector current due to signal alone.
 2. There should be **proper minimum V_{BE}** . For **silicon transistors**, this value should **not fall below 0.7V** and for **germanium transistor** it should **not fall below 0.5V**.
 3. There should be **proper minimum V_{CE}** . For **silicon transistors**, this value should **not fall below 1V** and for **germanium transistors**, it should **not fall below 0.5 V**
- The conditions (1) ensure the base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, conditions (3) ensure that collector-base junction shall remain properly reverse at all times.



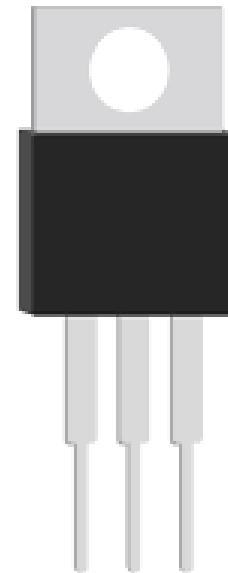
$$V_{BE} \approx 0.7 \text{ V}$$

$$I_E = (\beta + 1)I_B \approx I_C$$

$$I_C = \beta I_B$$

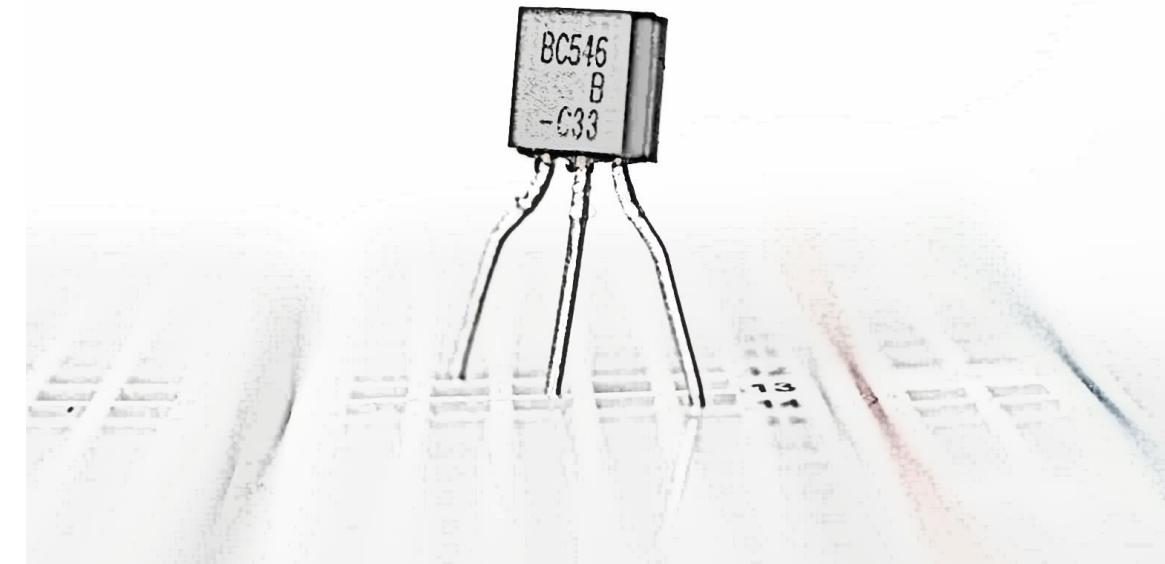
Transistor Biasing

- **Biasing** – refers to the DC voltages applied to a transistor in order to turn it on so that it can amplify the AC signal.
- Biasing and the Three States of Operation:
 - **Active or Linear** Region Operation
 - **Base-Emitter** junction is **forward biased**
 - **Base-Collector** junction is **reverse biased**
 - **Cutoff** Region Operation
 - **Base-Emitter** junction is **reverse biased**
 - **Base-Collector** junction is **reverse biased**
 - **Saturation** Region Operation
 - **Base-Emitter** junction is **forward biased**
 - **Base-Collector** junction is **forward biased**



Methods of Transistor Biasing

- In practice, transistor biasing is obtained by utilizing the battery V_{CC} connected in the output circuit. The following are the most commonly methods of biasing:
 - Fixed-bias circuit
 - Emitter-stabilized bias circuit
 - Collector-emitter loop
 - Voltage divider bias circuit
 - DC bias with voltage feedback



Fixed Bias Circuit

- The fixed-bias circuit is the simplest transistor dc bias configuration. Even though the network employs an npn transistor, the equations and calculations apply equally well to a pnp transistor configuration merely by changing all current directions and voltage polarities.

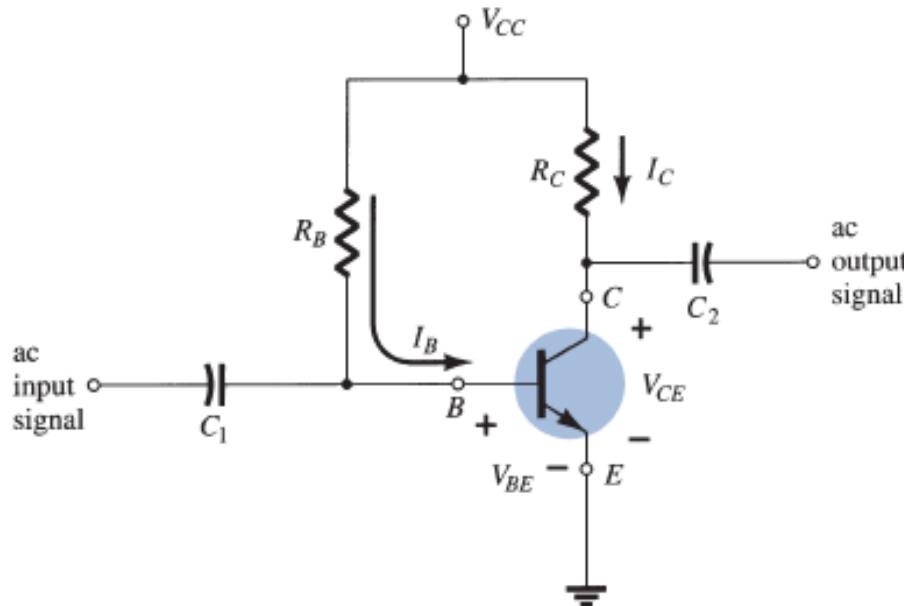


FIG. 2
Fixed-bias circuit.

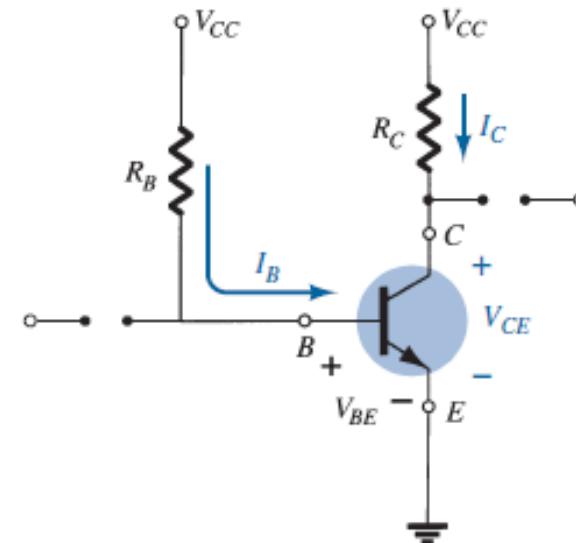


FIG. 3
DC equivalent of Fig. 2.

Fixed Bias Circuit

- The circuit can be analyzed using KVL
- Forward bias of base-emitter:

$$V_{BB} = V_{CC} = I_B R_B + V_{BE} = I_B R_B + 0.7V$$

$$I_B = \frac{V_{BB} - 0.7V}{R_B}$$

- Collector-emitter Loop:

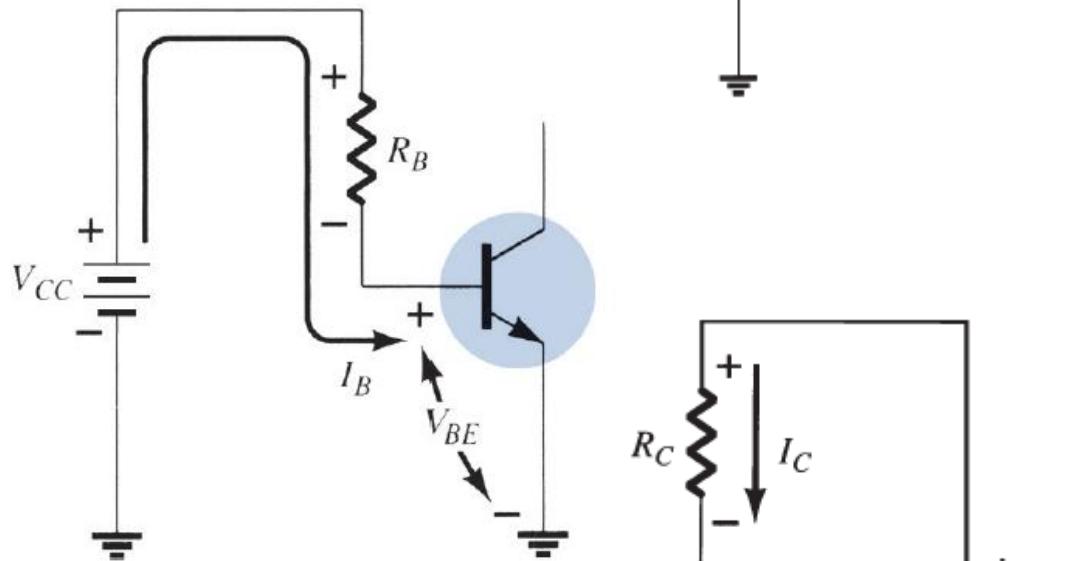
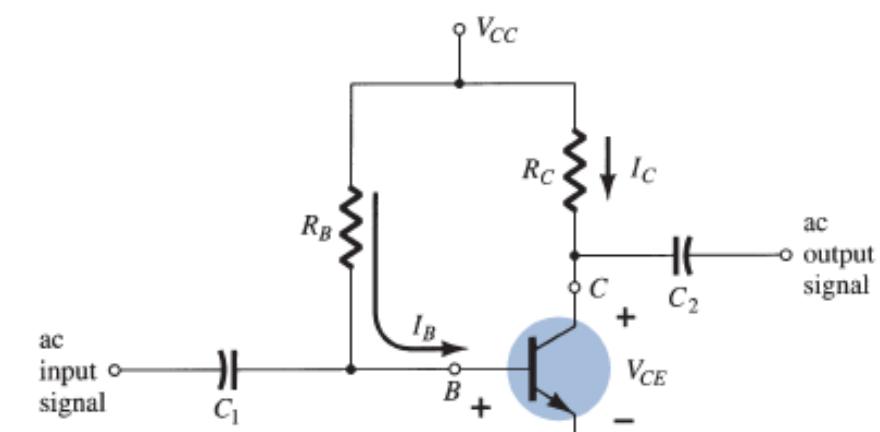
$$V_{CC} - I_C R_C - V_{CE} = 0 \rightarrow V_{CE} = V_{CC} - I_C R_C$$

$$V_{CE} = V_C - V_E ; V_E = 0 ; V_{CE} = V_C$$

$$V_{BE} = V_B - V_E ; V_{BE} = V_B$$

- The base-emitter and collector-emitter parameters are related by:

$$\begin{aligned} I_C &= \beta I_B \\ I_E &= I_B + I_C = (\beta + 1) I_B \end{aligned}$$



Fixed Bias Circuit

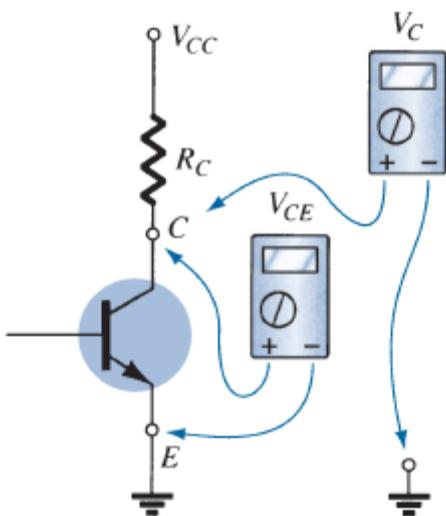
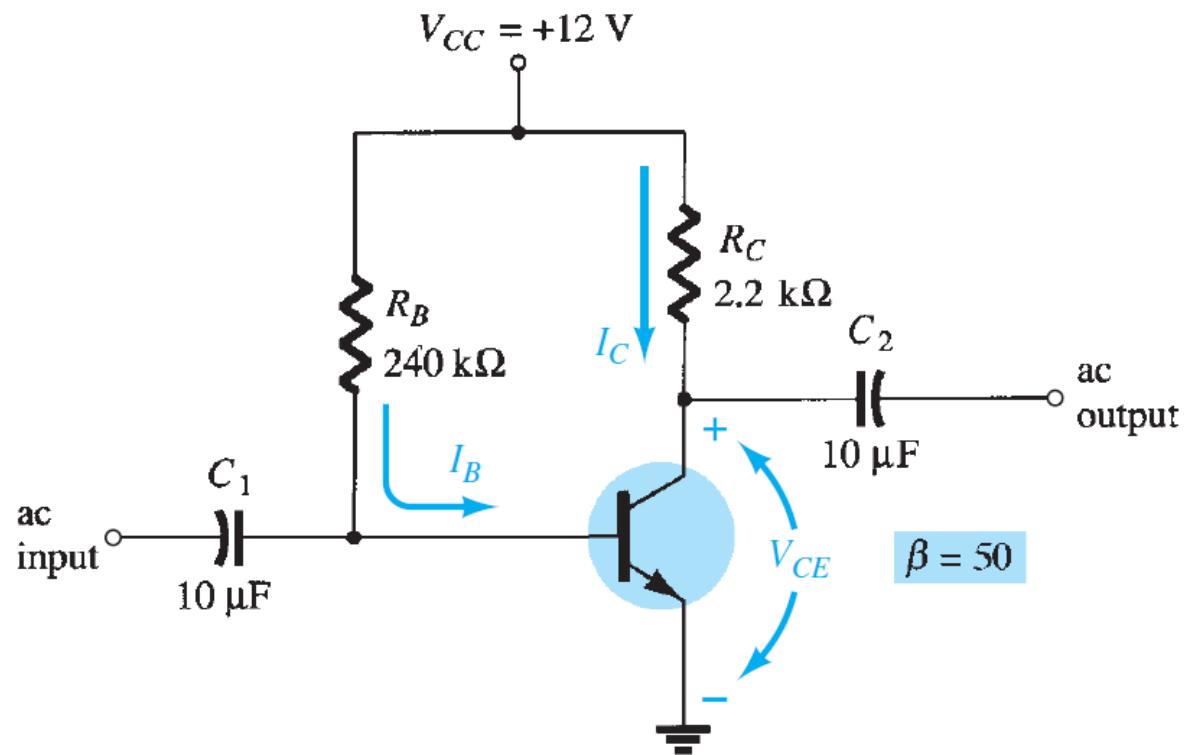


FIG. 6
Measuring V_{CE} and V_C .

Fixed Bias Circuit

- For the circuit shown, determine:

- I_{BQ} and I_{CQ}
- V_{CEQ}
- V_B and V_C
- V_{BC}



Fixed Bias Circuit

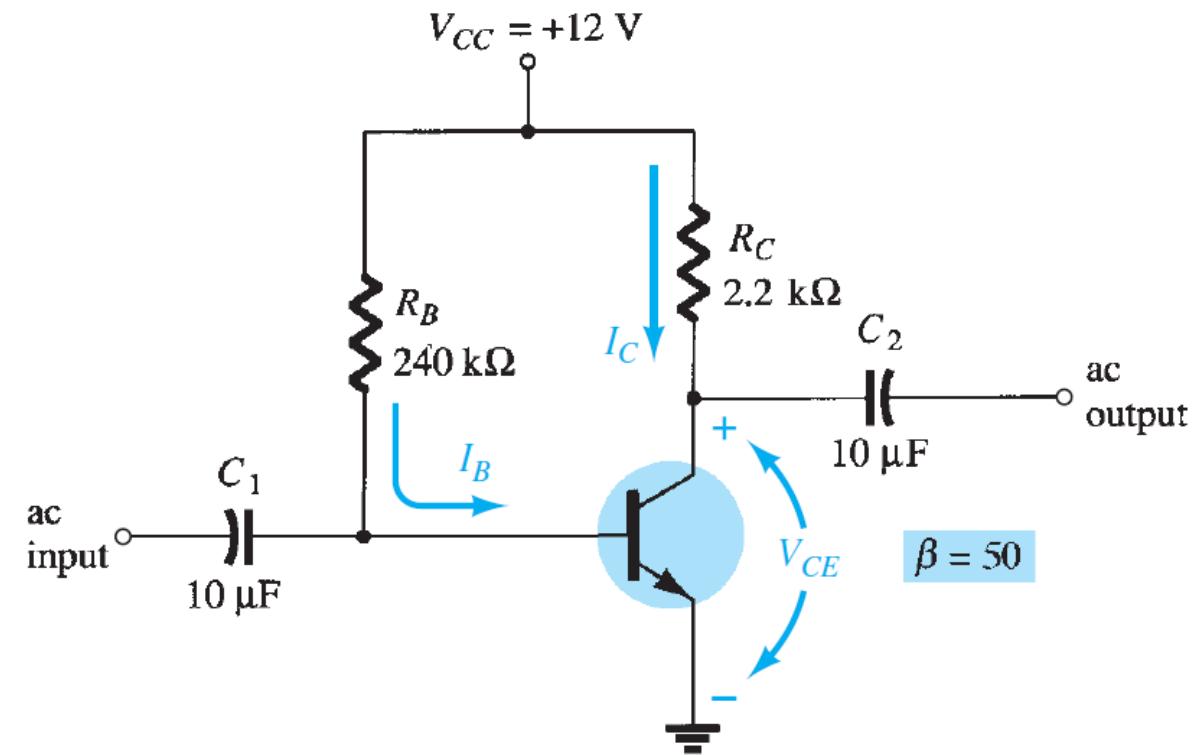
- Solution

At Base to Emitter Loop (KVL):

$$V_{CC} = I_B R_B + V_{BE}$$
$$12V = I_B(240 \text{ k}\Omega) + 0.7V$$
$$I_{BQ} = 47.0833 \mu\text{A}$$

Since $I_C = \beta I_B$

$$I_C = (50)47.0833 \mu\text{A}$$
$$I_{CQ} = 2.3542 \text{ mA}$$



Fixed Bias Circuit

- Solution

At Collector to Emitter Loop (KVL):

$$\begin{aligned}V_{CE} &= -I_C R_C + V_{CC} \\V_{CE} &= -2.3542mA (2.2k\Omega) + 12V \\V_{CEQ} &= \mathbf{6.8208 V}\end{aligned}$$

Since, $V_{BE} = V_B - V_E = 0.7V$

and $V_E = 0V$ (since it is connected directly to the ground)

$$\therefore V_B = 0.7V$$

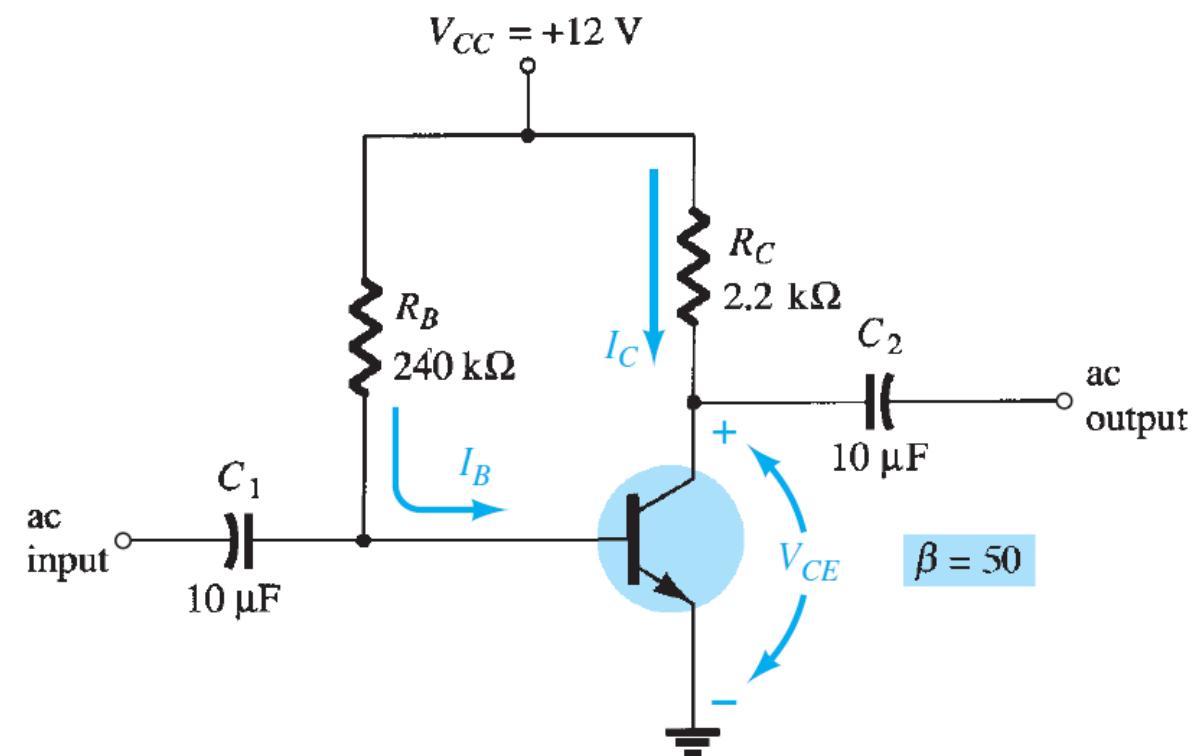
Since, $V_{CE} = V_C - V_E$ and $V_E = 0V$

$$\therefore V_C = \mathbf{6.8207 V}$$

$$V_{BC} = V_B - V_C$$

$$V_{BC} = 0.7V - 6.8208 V$$

$$V_{BC} = \mathbf{-6.1208V}$$



Emitter Stabilized Bias Circuit

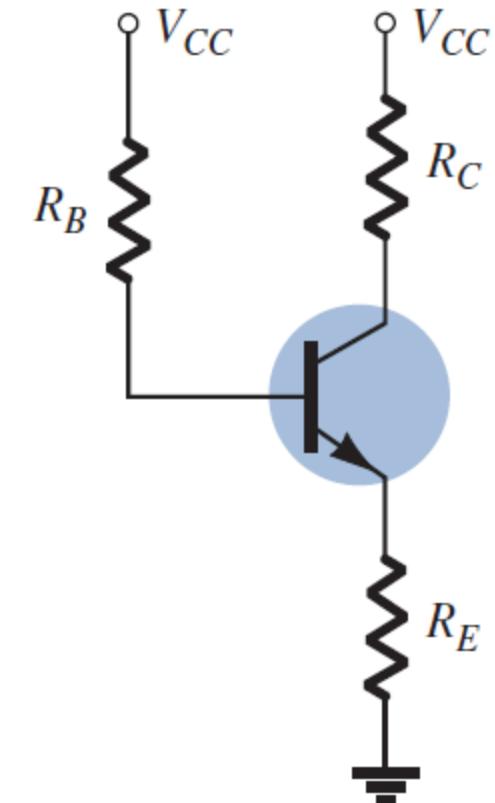
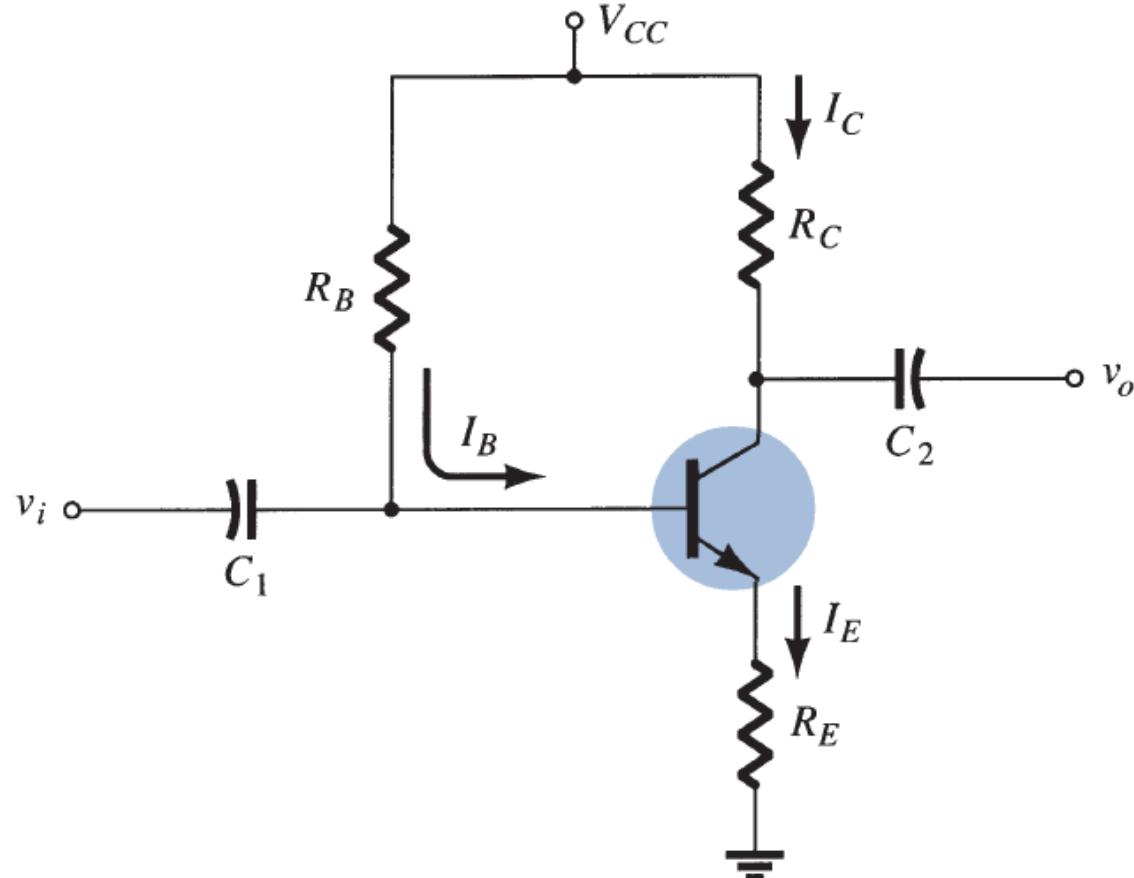


FIG. 18

DC equivalent of Fig. 17.

Emitter Stabilized Bias Circuit

- The circuit can be analyzed using KVL
- Base-emitter Loop:

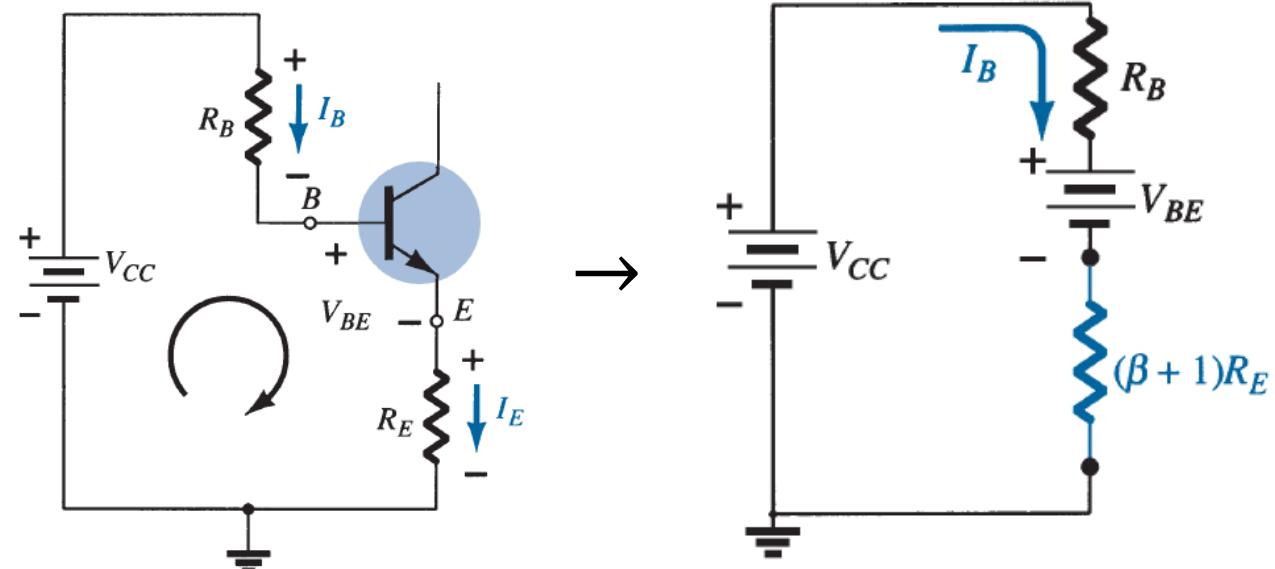
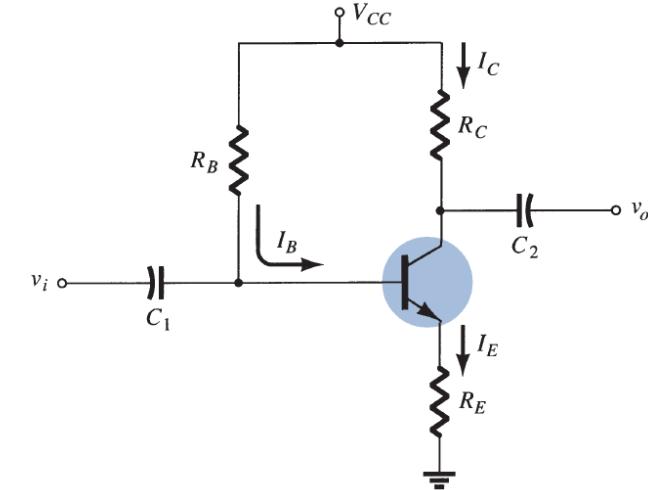
$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

Since $I_E = (\beta + 1)I_B$

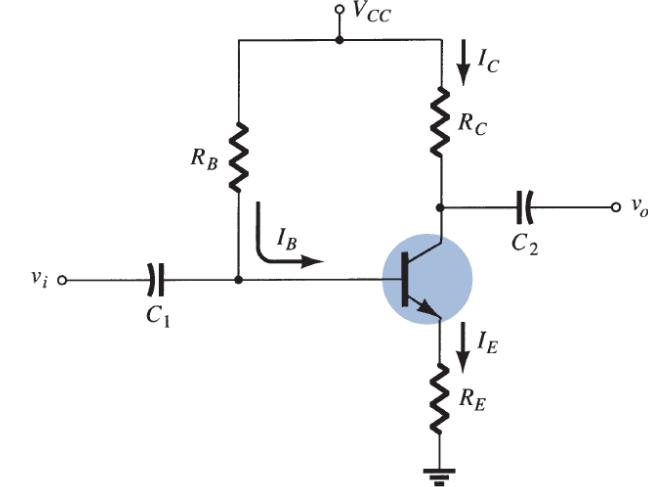
$$V_{CC} = I_B R_B + 0.7V + (\beta + 1)I_B R_E$$

$$I_B = \frac{V_{CC} - 0.7V}{R_B + (\beta + 1)R_E}$$

$$V_B = V_{BE} + V_E$$



Emitter Stabilized Bias Circuit



- The circuit can be analyzed using KVL
- Collector-emitter Loop:

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\text{If } I_E \approx I_C, V_{CE} = V_{CC} - I_C(R_C + R_E)$$

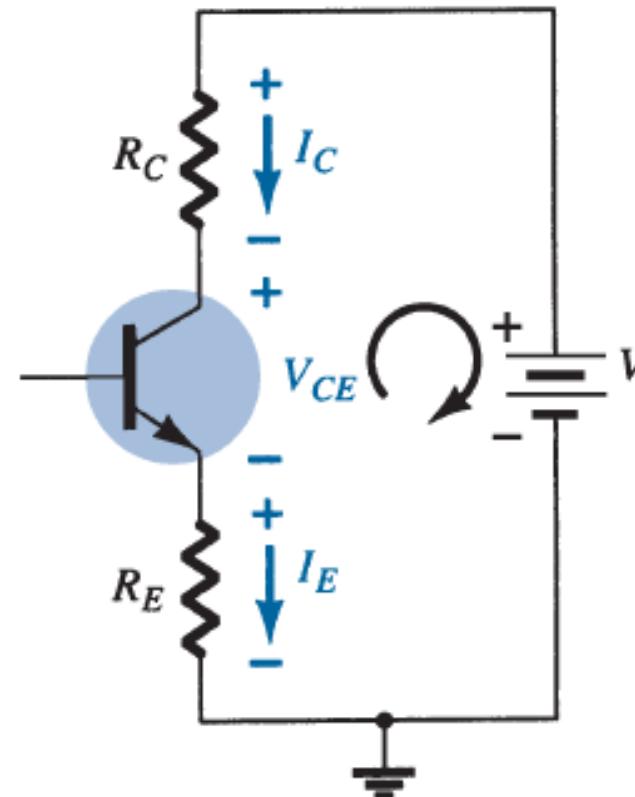
$$V_E = I_E R_E$$

$$V_C = V_{CE} + V_E \text{ or } V_C = V_{CC} - I_C R_C$$

- The Base-emitter and Collector-emitter parameters are related by:

$$I_C = \beta I_B$$

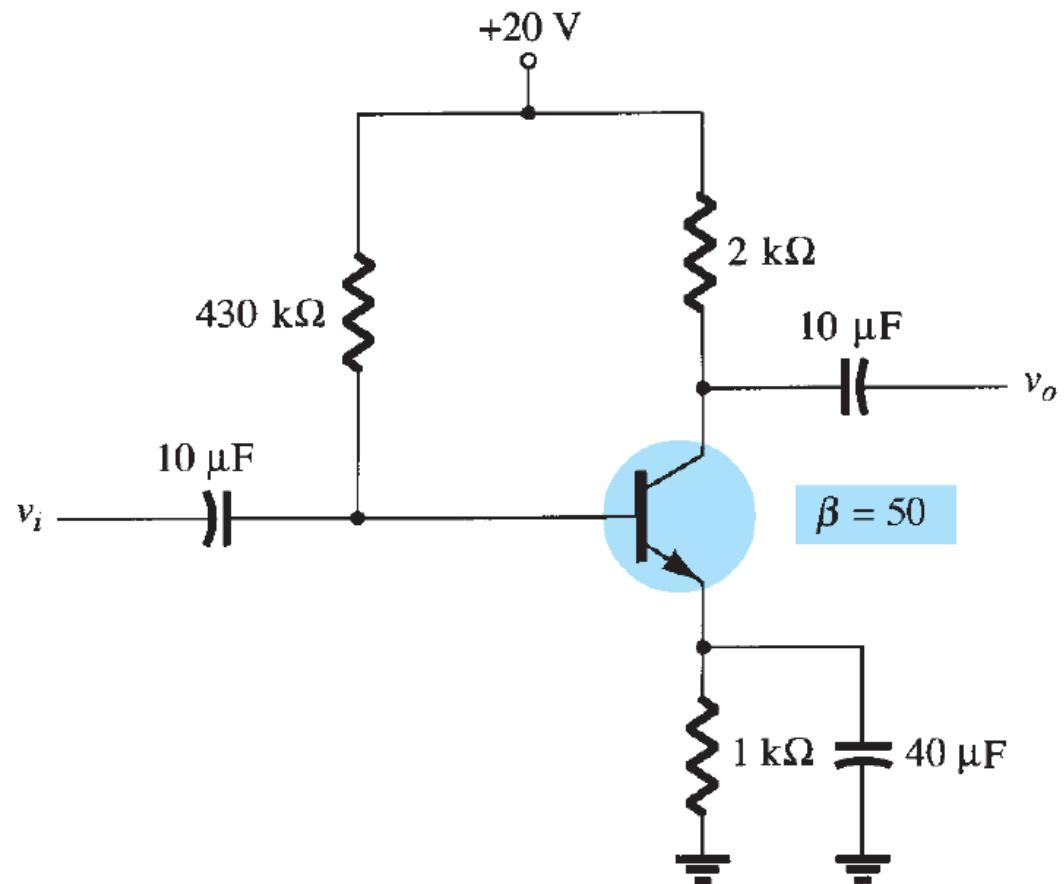
$$I_E = I_B + I_C = (\beta + 1) I_B$$



Emitter Stabilized Bias Circuit

- For the circuit shown, determine:

- I_{BQ}
- I_{CQ}
- V_{CE}
- V_C
- V_E
- V_B
- V_{BC}



Emitter Stabilized Bias Circuit

- Solution

Input loop:

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$
$$V_{CC} = I_B R_B + 0.7V + (\beta + 1)I_B R_E$$
$$20V - 0.7V$$

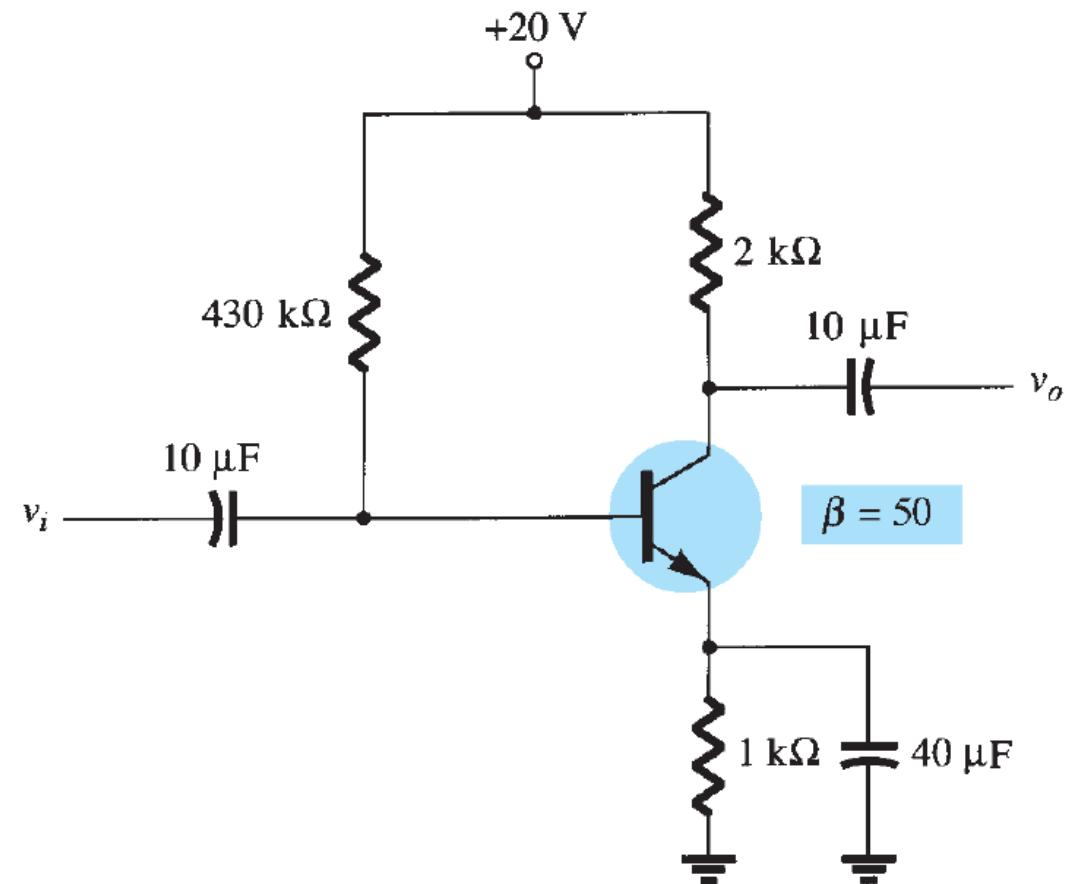
$$I_B = \frac{20V - 0.7V}{430k\Omega + (50 + 1)1k\Omega}$$

$$I_{BQ} = 40.1247 \mu A$$

$$I_C = \beta I_B$$

$$I_C = 50 (40.1247 \mu A)$$

$$I_C = 2.0062 mA$$



Emitter Stabilized Bias Circuit

- Solution

Output loop:

$$V_{CE} = -I_C R_C + V_{CC} - I_E R_E$$

Since $I_E = (\beta + 1)I_B$

$$V_{CE} = -I_C R_C + V_{CC} - (\beta + 1)I_B R_E$$

$$V_{CE} = -(2.0062 \text{ mA})(2\text{k}\Omega) + 20\text{V} - (50 + 1)(40.1247 \mu\text{A})(1\text{k}\Omega)$$

$$\mathbf{V_{CEQ} = 13.9412 \text{ V}}$$

Since $V_{CE} = V_C - V_E$

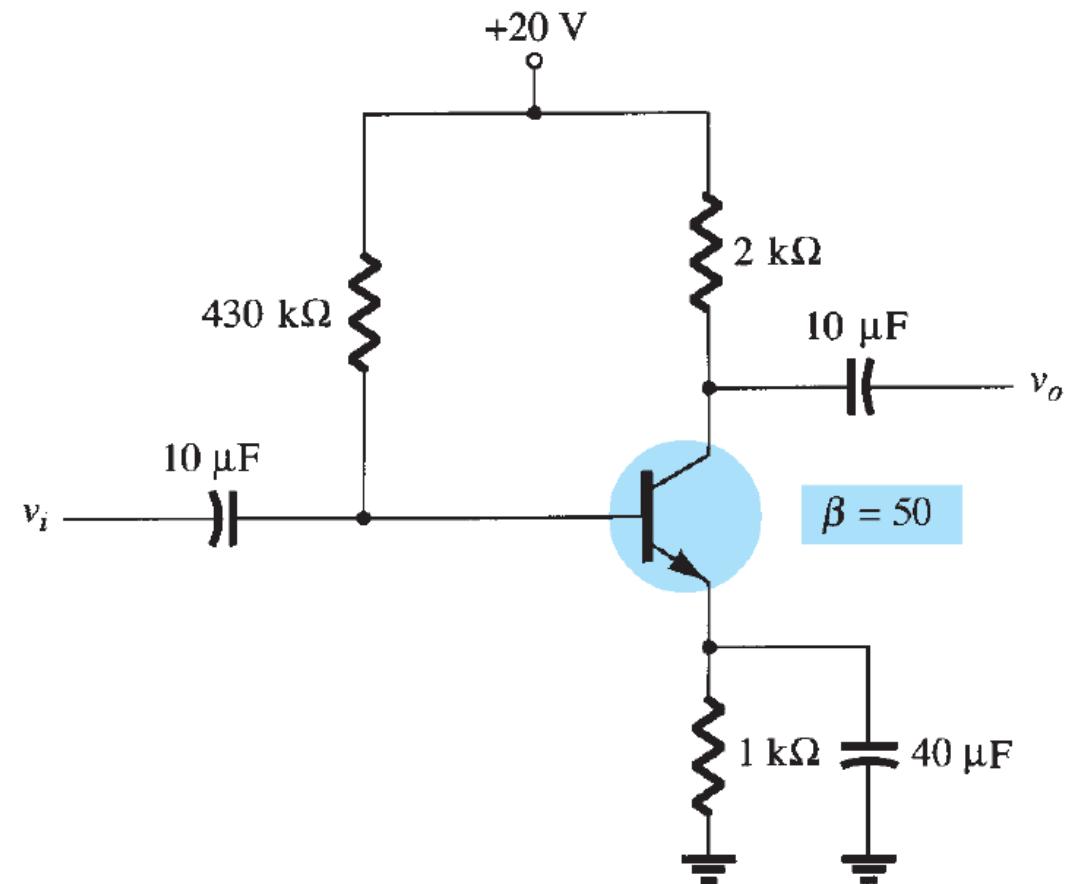
$$V_E = I_E R_E = (\beta + 1)I_B R_E$$

$$V_E = (50 + 1)(40.1247 \mu\text{A})(1\text{k}\Omega)$$

$$\mathbf{V_E = 2.0464 \text{ V}}$$

$$V_C = V_{CE} + V_E$$

$$\mathbf{V_C = 15.9876}$$



Emitter Stabilized Bias Circuit

- Solution

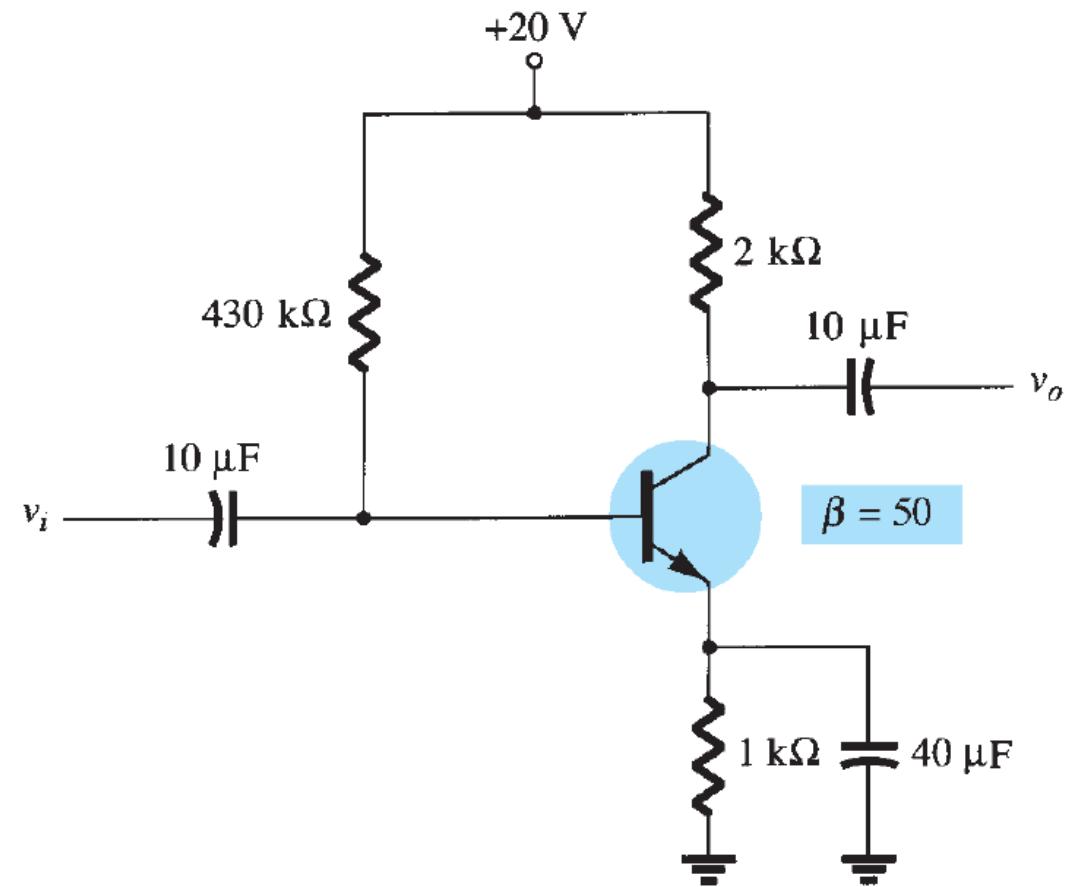
Since $V_{BE} = V_B - V_E = 0.7V$

$$V_B = 0.7V + 2.0464V$$

$$V_B = 2.7464V$$

$$\therefore V_{BC} = V_B - V_C$$

$$V_{BC} = -13.2412 V$$



Emitter Stabilized Bias Circuit

- Solution

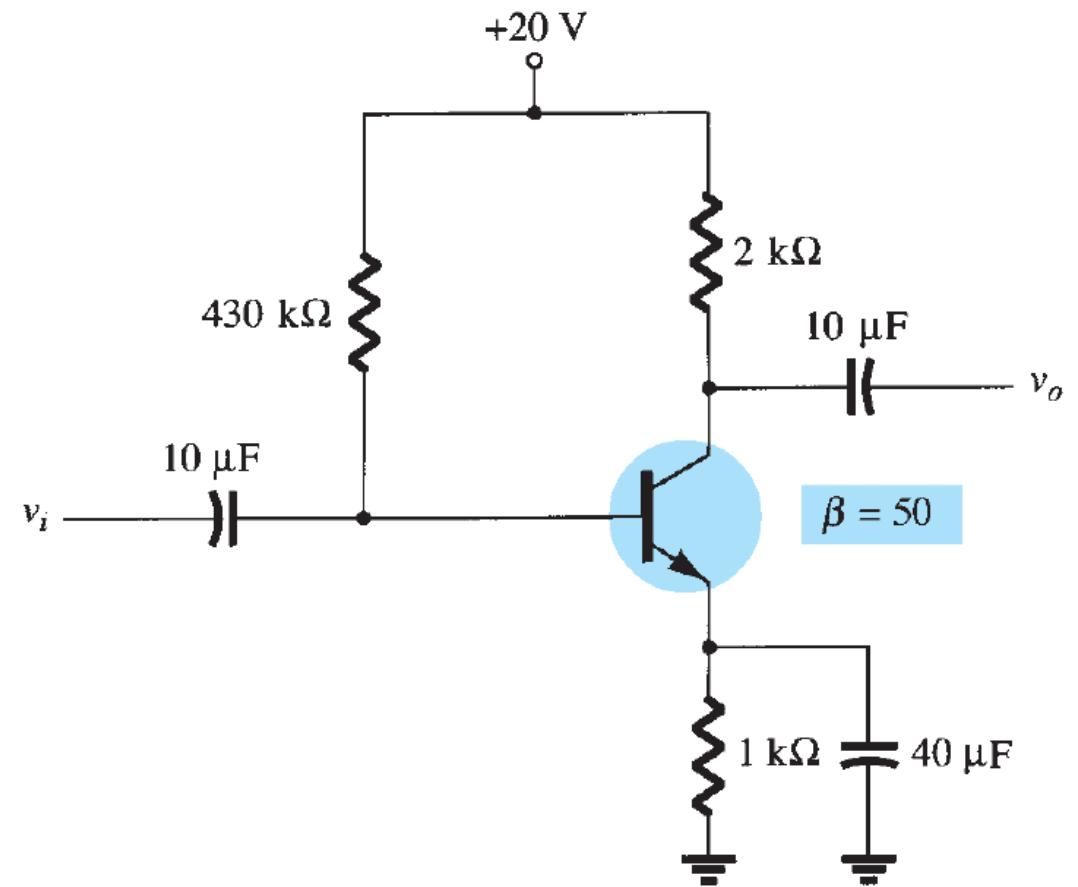
Since $V_{BE} = V_B - V_E = 0.7V$

$$V_B = 0.7V + 2.0464V$$

$$V_B = 2.7464V$$

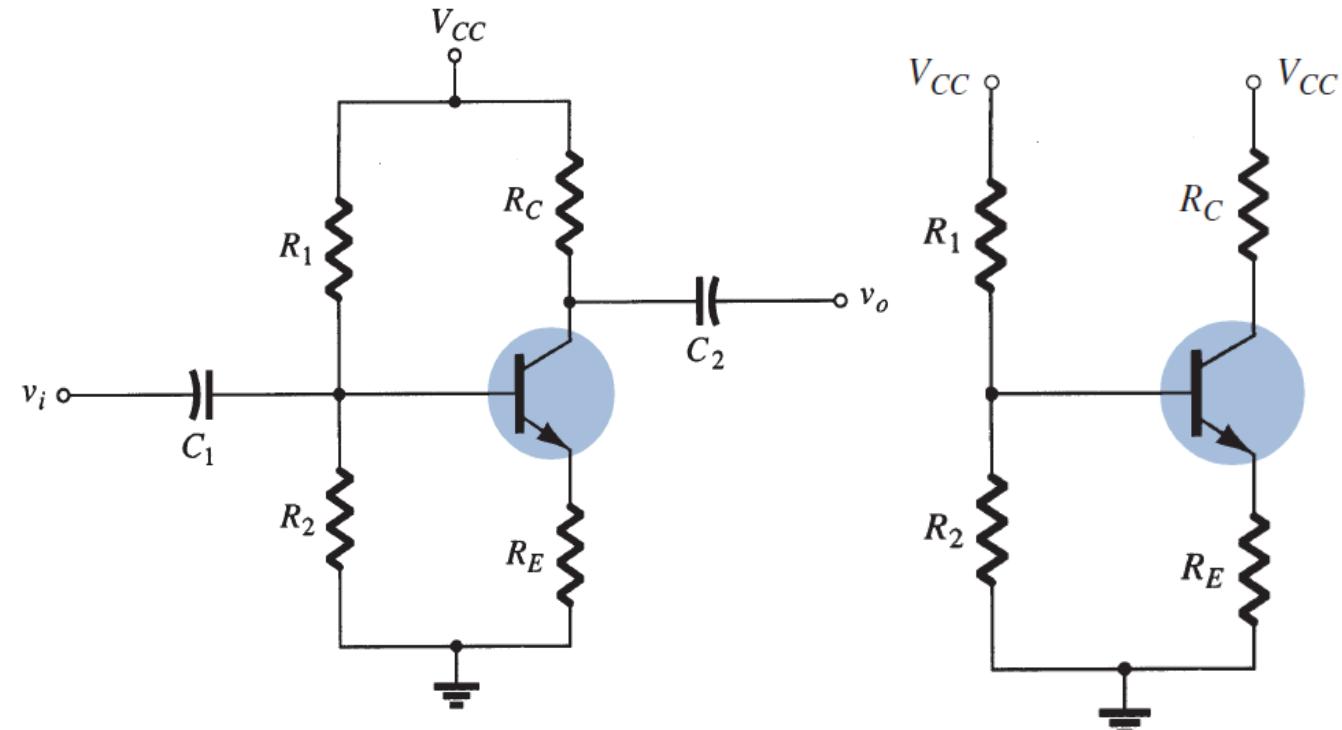
$$\therefore V_{BC} = V_B - V_C$$

$$V_{BC} = -13.2412 V$$



Voltage Divider Bias Circuit

- If circuit parameters are chosen properly, this circuit can make the collector current and collector-emitter voltage stable, though β is varying.
- This is a very stable bias circuit.
- The currents and voltages are almost independent of variations in β
- Can be analyzed using two methods:
 - Exact Method (Thevenin's Analysis)
 - Approximate Method



Voltage Divider Bias Circuit -Exact Method

- For the exact method, the circuit can be analyzed by converting the circuit at the input side into its **Thevenin's equivalent circuit** and then applying **KVL**.

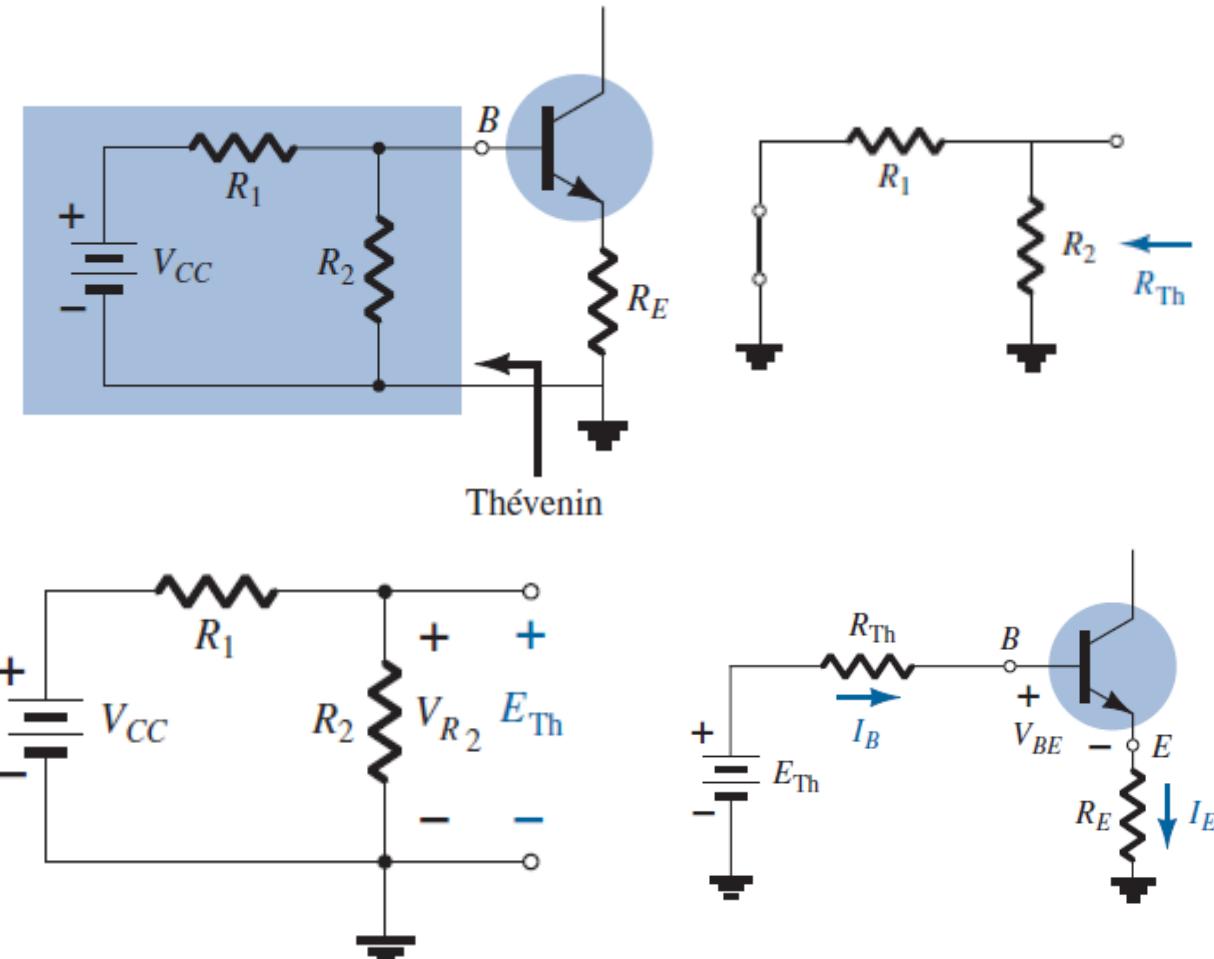
Base-emitter Loop

$$R_{TH} = R_1 \parallel R_2 = \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} = \frac{R_1 R_2}{R_1 + R_2}$$

$$E_{TH} = V_{R_2} = \frac{V_{CC} R_2}{R_1 + R_2}$$

$$E_{TH} - I_B R_{TH} - V_{BE} - I_E R_E = 0 ; I_E = (\beta + 1) I_B$$

$$I_B = \frac{E_{TH} - V_{BE}}{R_{TH} + (\beta + 1) R_E}$$



Voltage Divider Bias Circuit -Exact Method

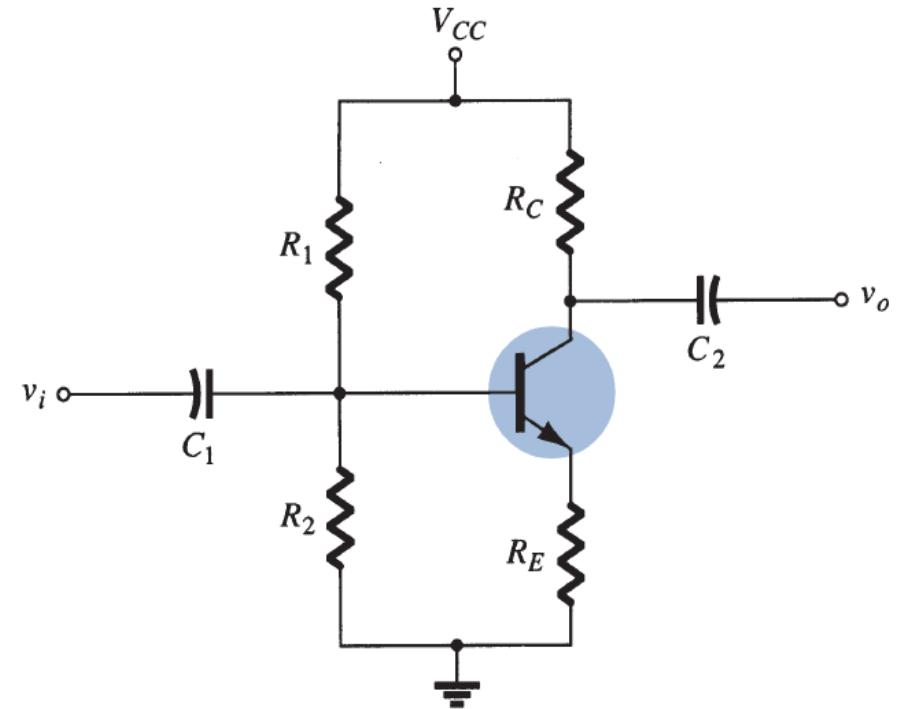
- The Collector emitter loop stays the same:

$$V_{CE} = -I_C R_C + V_{CC} - I_E R_E$$

Since $I_E = I_B + I_C = (\beta + 1)I_B$

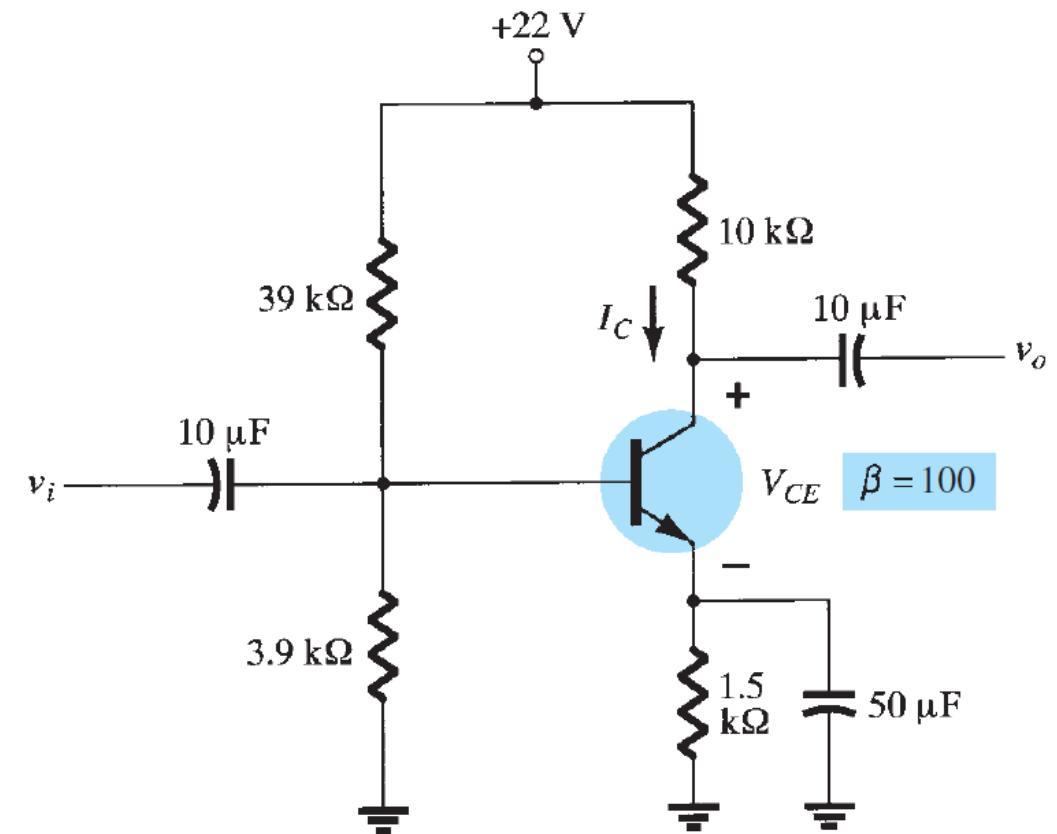
$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C)R_E$$

$$V_{CE} = V_{CC} - \beta I_B R_C - (\beta + 1)I_B R_E$$



Voltage Divider Bias Circuit

- For the circuit shown, using the Exact Method, determine:
 - I_{CQ}
 - V_{CEQ}



Voltage Divider Bias Circuit

- Solution:

$$R_{TH} = \frac{1}{\frac{1}{39k\Omega} + \frac{1}{3.9k\Omega}} = 3.5455 k\Omega$$

$$V_{TH} = \frac{V_{CC} R_{B2}}{R_{B1} + R_{B2}} = \frac{22V (3.9k\Omega)}{39k\Omega + 3.9k\Omega} = 2V$$

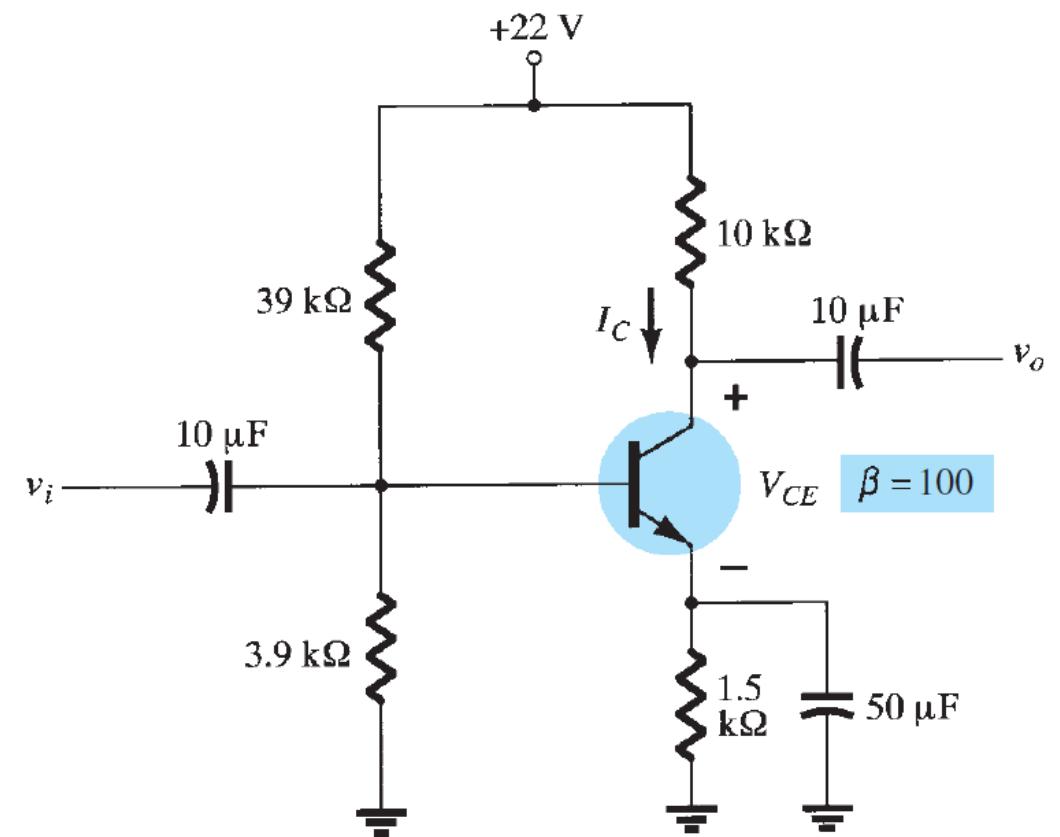
$$I_B = \frac{V_{TH} - 0.7V}{R_{TH} + (\beta + 1)R_E}$$

$$I_B = \frac{2 - 0.7}{3.5455 k\Omega + (100 + 1)(1.5k\Omega)}$$

$$I_B = 8.3846 \mu A$$

$$I_C = \beta I_B = (100)8.3846 \mu A$$

$$I_{CQ} = 838.46 \mu A$$



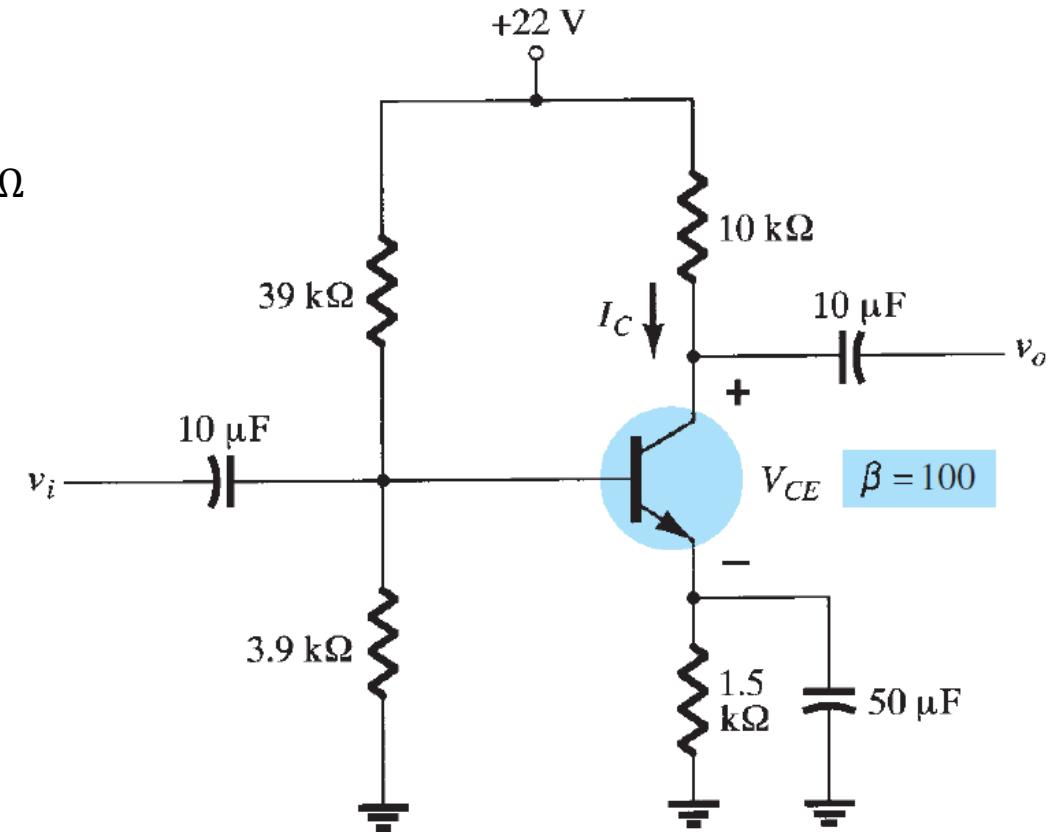
Voltage Divider Bias Circuit

- Solution:

$$V_{CE} = V_{CC} - \beta I_B R_C - (\beta + 1) I_B R_E$$

$$V_{CE} = 22 - 100(8.3846 \mu A)(10 k\Omega) - (100 + 1)(8.3846 \mu A)1.5 k\Omega$$

$$V_{CEQ} = 12.3451V$$



Voltage Divider Bias Circuit -Approximate Method

- For the **approximate approach**, the input side of the circuit can be represented by the circuit as shown
- R_i is the **equivalent resistance** between the base and the ground

$$R_i \cong (\beta + 1)R_E$$

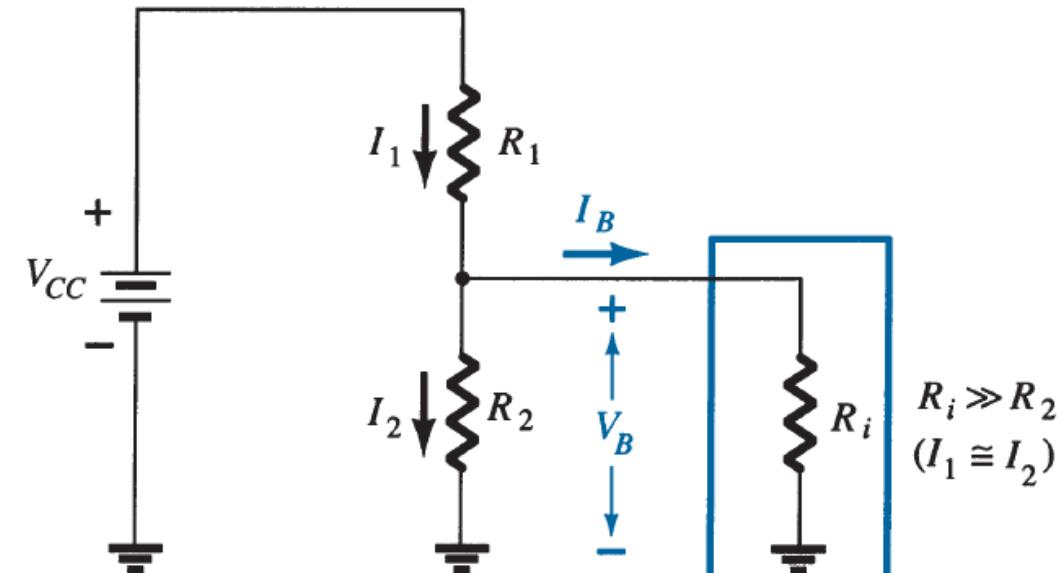
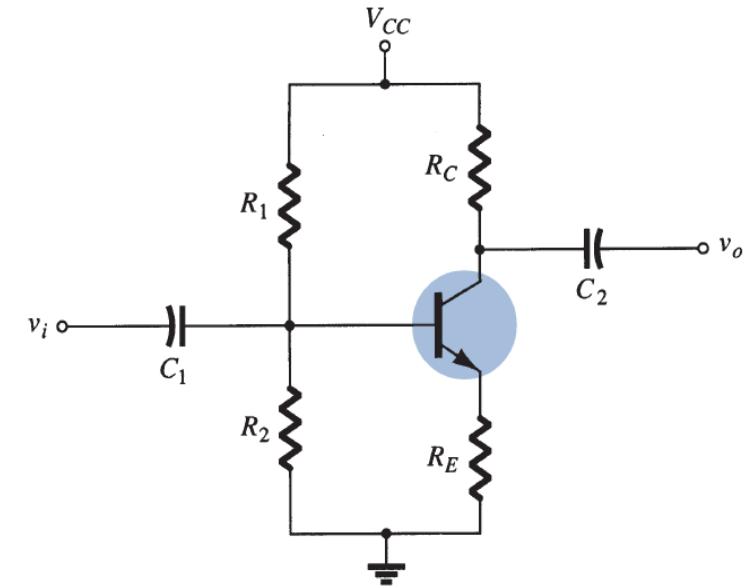
- If $R_i \gg R_2$, I_{R2} is **approximately equal** to I_{R1} because I_B will be **significantly small** compared to I_{R2} . Current always **seeks the path of least resistance**

- If $R_i \geq 10 R_2$ then

$$(\beta + 1)R_E \geq 10 R_2 \text{ then:}$$

$$I_{R2} \cong I_{R1}$$

- With this, we can assume that I_B is **approximately equal to zero**, and R_1 is in series with R_2 .



Voltage Divider Bias Circuit -Approximate Method

- The voltage across R_{B2} can then be computed as:

$$V_{R2} = \frac{V_{CC}R_2}{R_1 + R_2}$$

- The voltage across R_E :

$$V_{RE} = V_{R_{B2}} - V_{BE} = V_{R_{B2}} - 0.7V$$

- The emitter current:

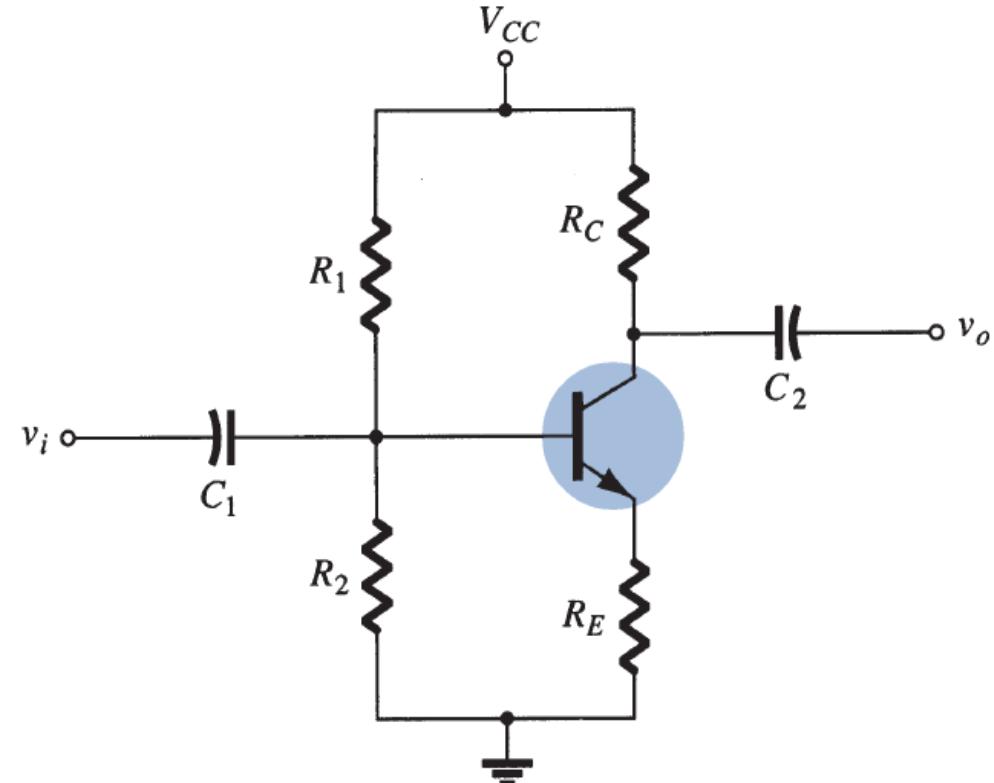
$$I_E = I_{RE} = \frac{V_{RE}}{R_E}$$

- The collector current (approximately equal to the emitter current):

$$I_C \approx I_E$$

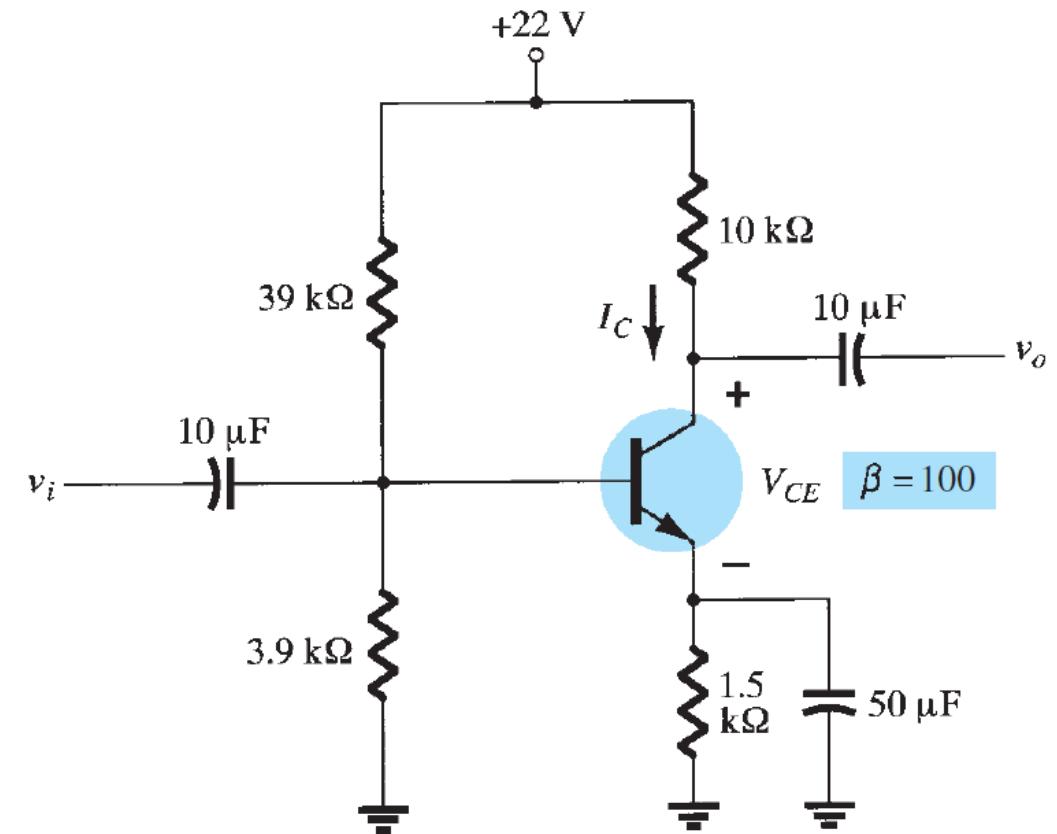
- The collector to emitter voltage:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$



Voltage Divider Bias Circuit

- For the circuit shown, using the Approximate Method, determine:
 - I_{CQ}
 - V_{CEQ}



Voltage Divider Bias Circuit

- Solution:

Testing:

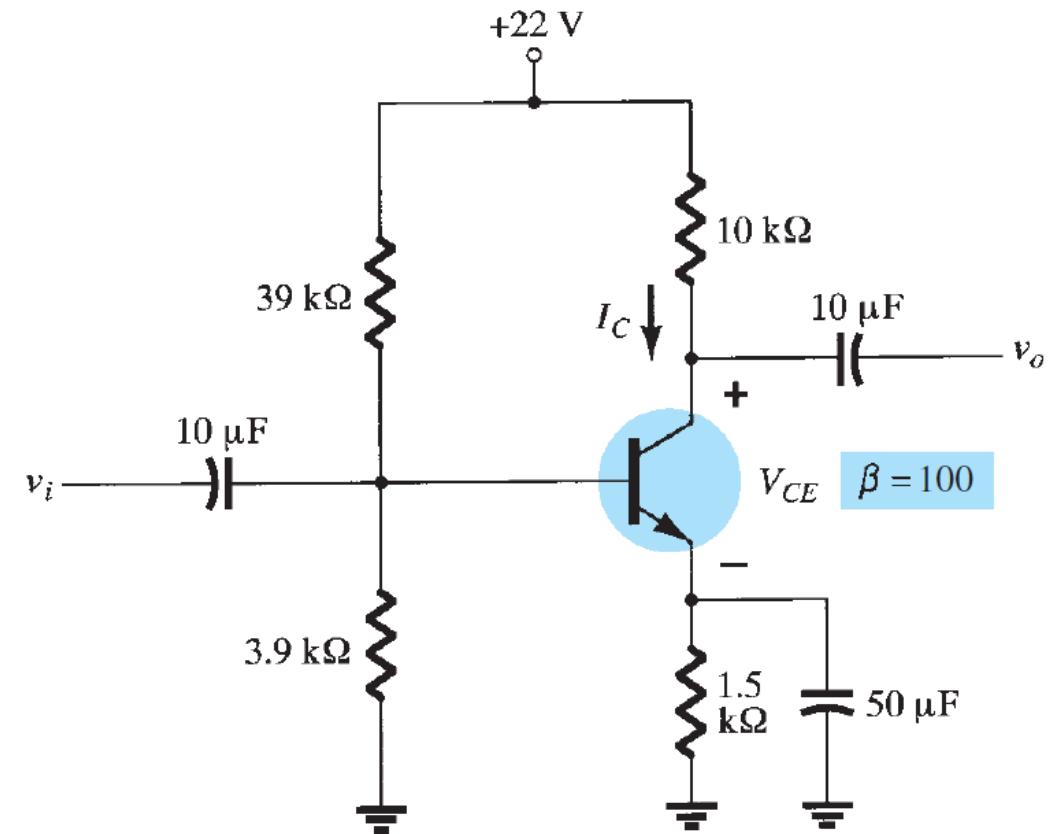
$$\begin{aligned}(\beta + 1)R_E &\stackrel{?}{=} 10R_{B2} \\(101)(1.5 \text{ k}\Omega) &\stackrel{?}{=} 10(3.9 \text{ k}\Omega) \\151.5 \text{ k}\Omega &\geq 39 \text{ k}\Omega \text{ (satisfied)}\end{aligned}$$

$$V_B = \frac{V_{CC}R_{B2}}{R_{B1} + R_{B2}} = \frac{22V(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2V$$

$$V_{BE} = V_B - V_E = 0.7V$$

$$V_E = V_B - V_{BE} = 2V - 0.7V = 1.3V$$

$$I_{CQ} \cong I_E = \frac{V_E}{R_E} = \frac{1.3V}{1.5 \text{ k}\Omega} = 866.6667 \mu A$$

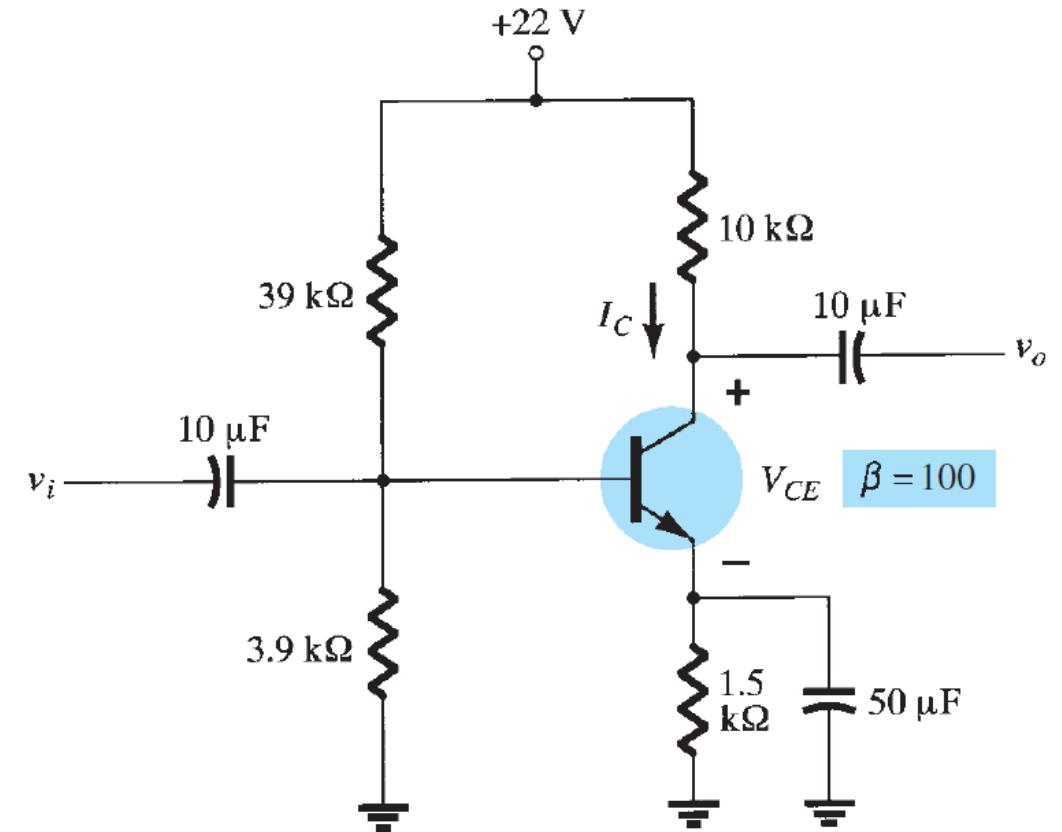


Voltage Divider Bias Circuit

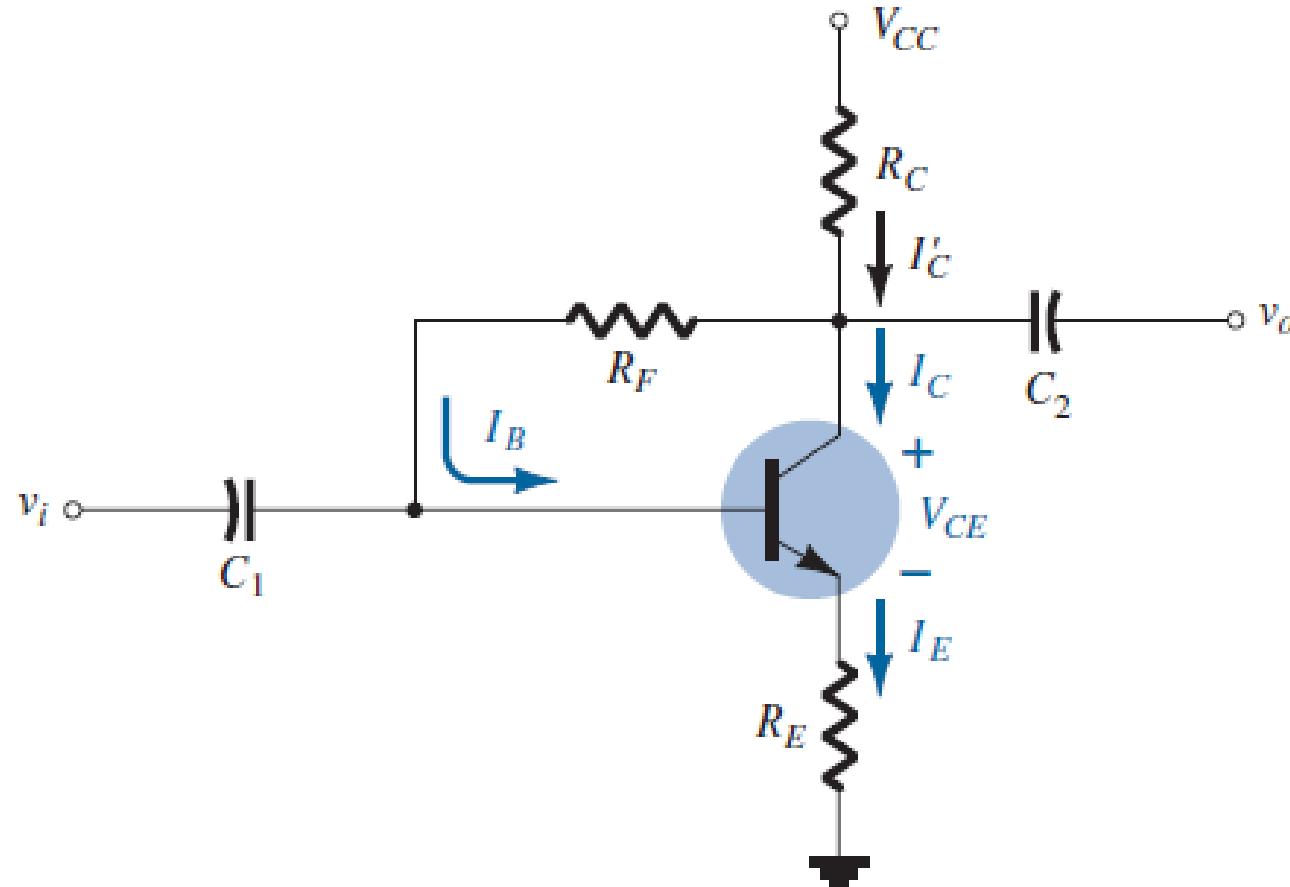
- Solution:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$
$$V_{CE} = 22 - (866.6667 \mu A)(10 k\Omega + 1.5 k\Omega)$$

$$V_{CEQ} = 12.0333 V$$



Collector Feedback Bias Circuit



Collector Feedback Bias Circuit

- The circuit can be analyzed using KVL
- For the base-emitter Loop:

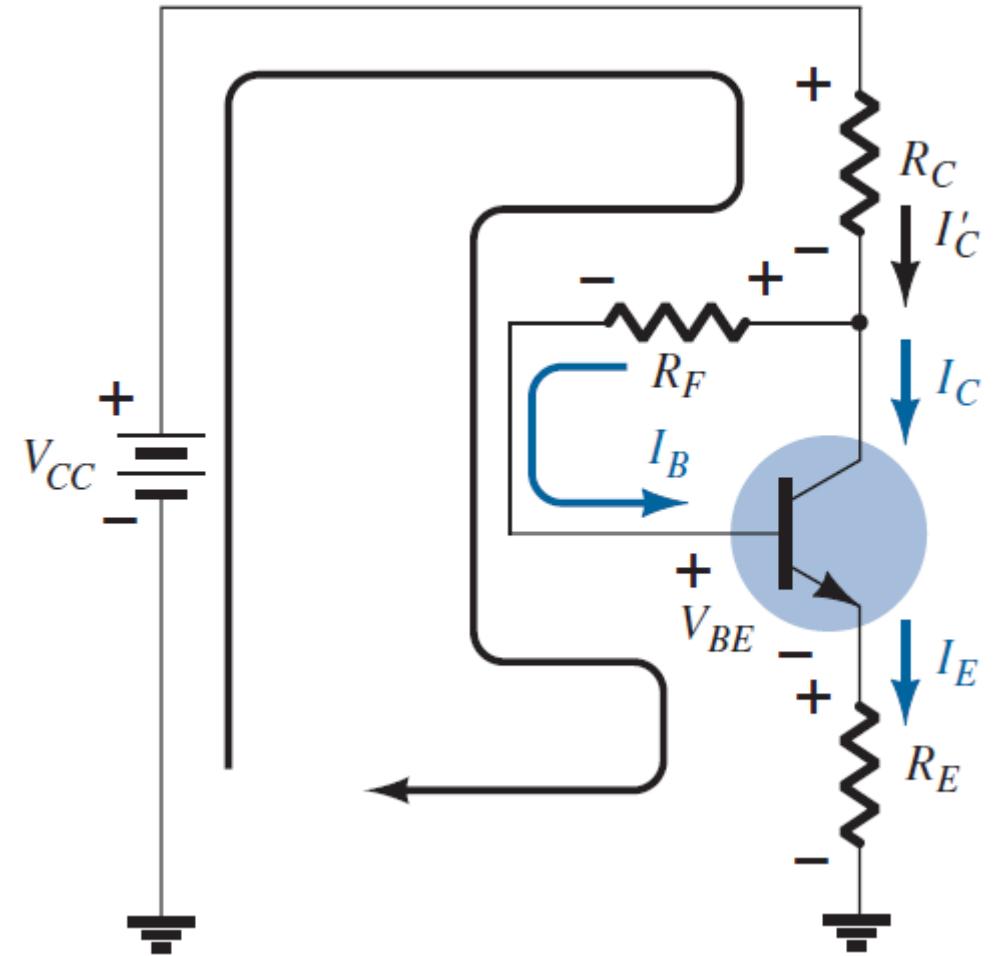
$$V_{CC} - I_C' R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

Where $I_C' = I_C + I_B = I_E$

$$V_{CC} = I_E R_C + I_B R_F + V_{BE} + I_E R_E$$
$$V_{CC} = (\beta + 1)I_B R_C + I_B R_F + V_{BE} + (\beta + 1)I_B R_E$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + (\beta + 1)(R_E + R_C)}$$

$$I_B = \frac{V_{CC} - 0.7V}{R_F + (\beta + 1)(R_E + R_C)}$$

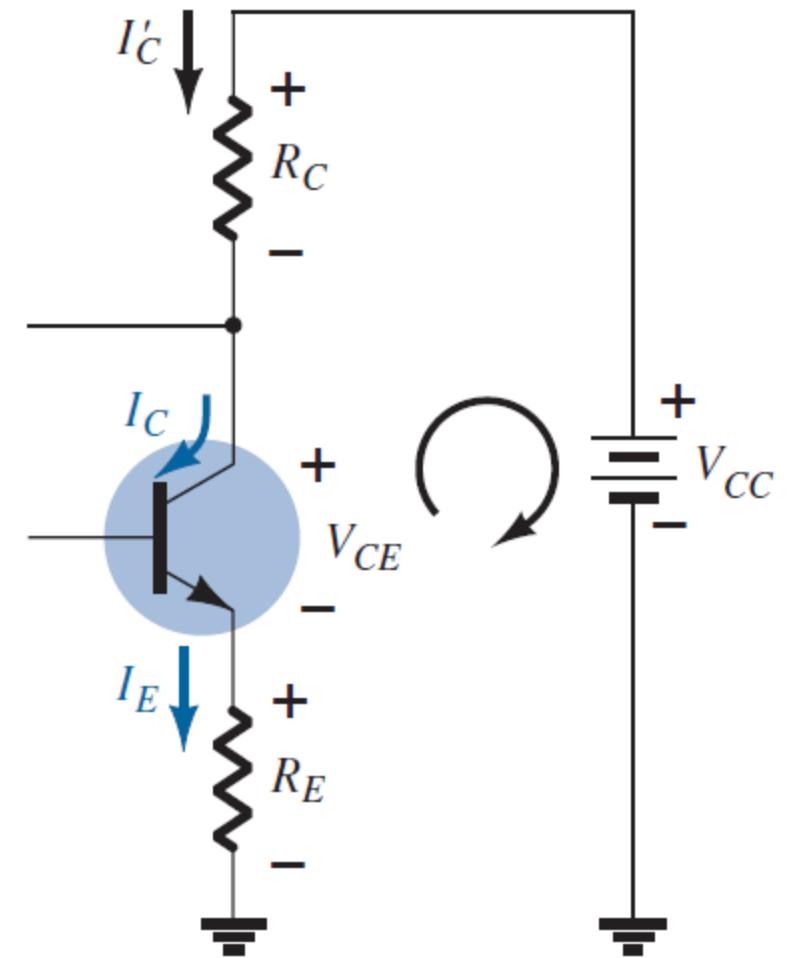


Collector Feedback Bias Circuit

- For the collector-emitter loop:

$$V_{CC} - I_C' R_C - V_{CE} - I_E R_E = 0$$

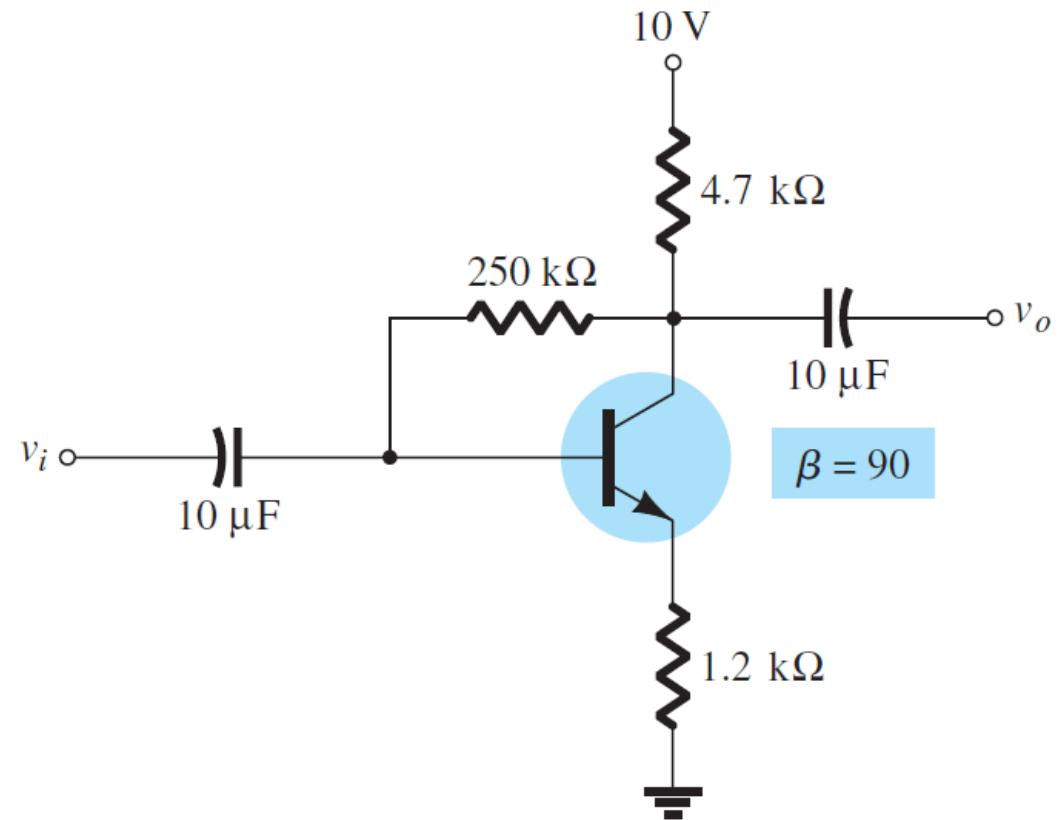
$$V_{CE} = -(I_C + I_B)R_C + V_{CC} - I_E R_E$$
$$V_{CE} = V_{CC} - I_E(R_E + R_C)$$



Collector Feedback Bias Circuit

- For the circuit shown,
determine:

- I_{CQ}
- V_{CEQ}



Collector Feedback Bias Circuit

- Solution:

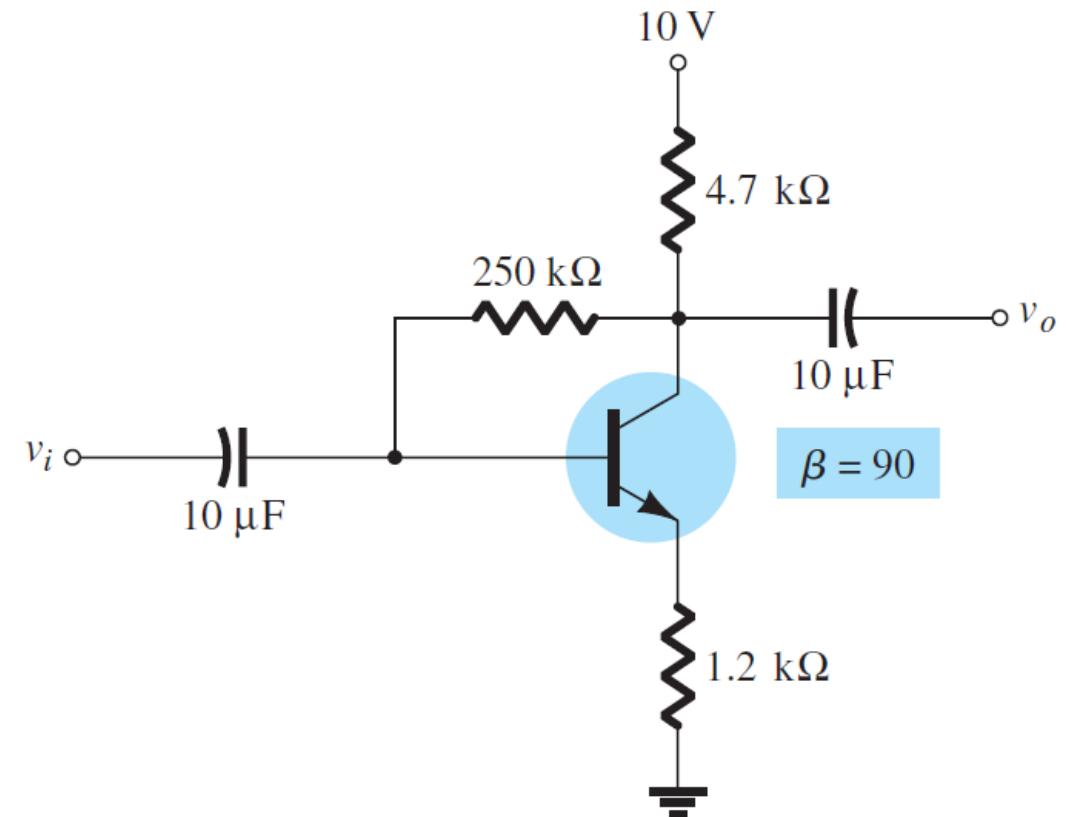
$$I_B = \frac{V_{CC} - 0.7V}{R_F + (\beta + 1)(R_E + R_C)}$$

$$I_B = \frac{10 - 0.7V}{250 \text{ k}\Omega + (90 + 1)(1.2k \Omega + 4.7k\Omega)}$$

$$I_{BQ} = 11.8185 \mu A$$

$$I_C = \beta I_B = 90(11.8185 \mu A)$$

$$I_{CQ} = 1.0637 mA$$



Collector Feedback Bias Circuit

- Solution:

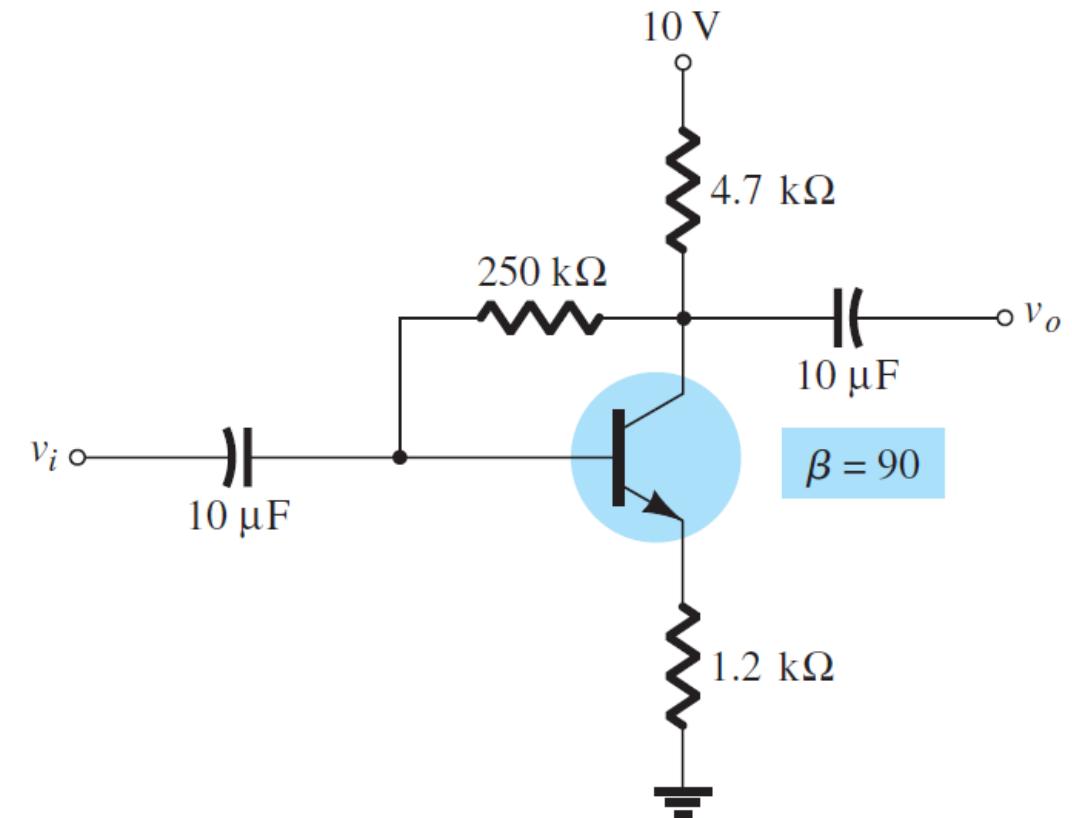
$$V_{CE} = V_{CC} - I_E(R_E + R_C)$$

$$I_E = (\beta + 1)I_B$$

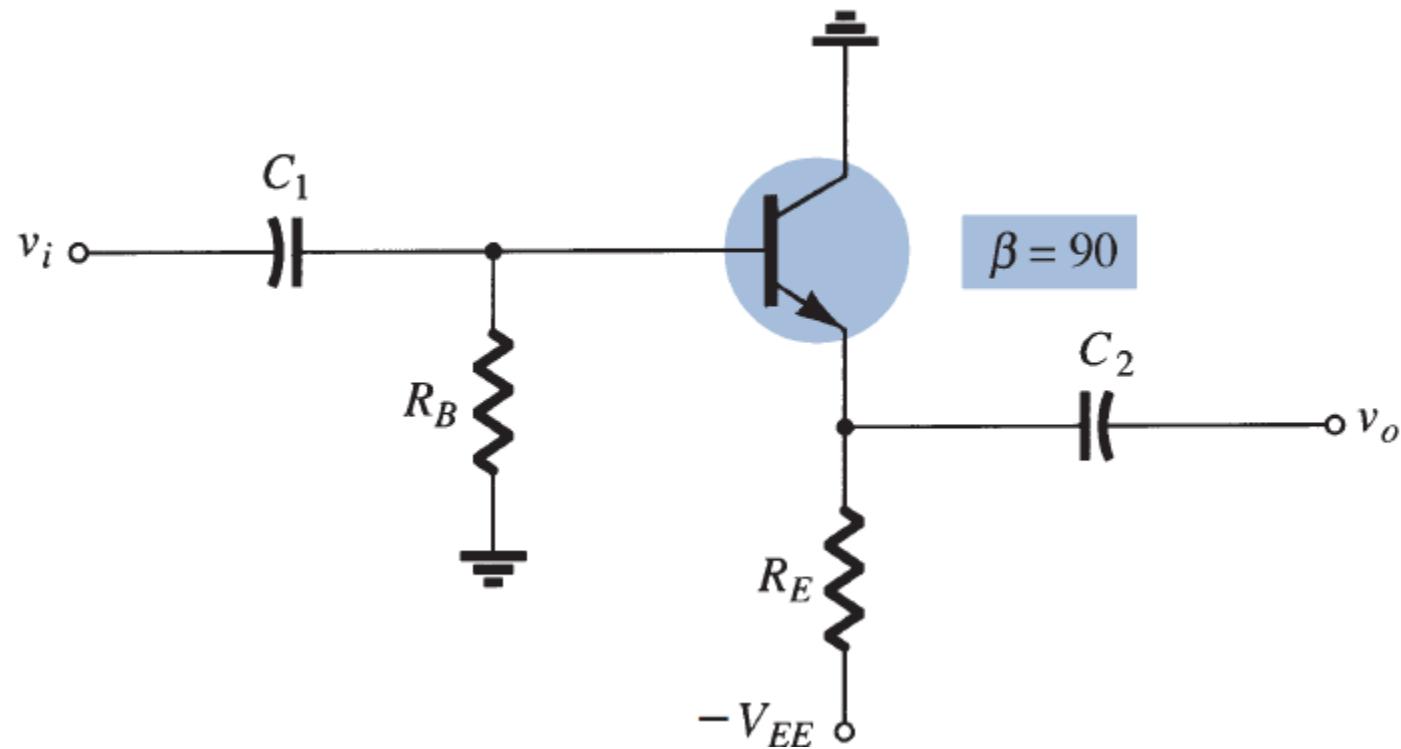
$$I_E = 1.0755 \text{ mA}$$

$$V_{CE} = 10 - 1.0755 \text{ mA} (1.2 \text{ k}\Omega + 4.7 \text{ k}\Omega)$$

$$V_{CEQ} = 3.6546 \text{ V}$$



Emitter-Follower Configuration



Emitter-Follower Configuration

- Applying Kirchhoff's voltage rule to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

and using $I_E = (\beta + 1)I_B$

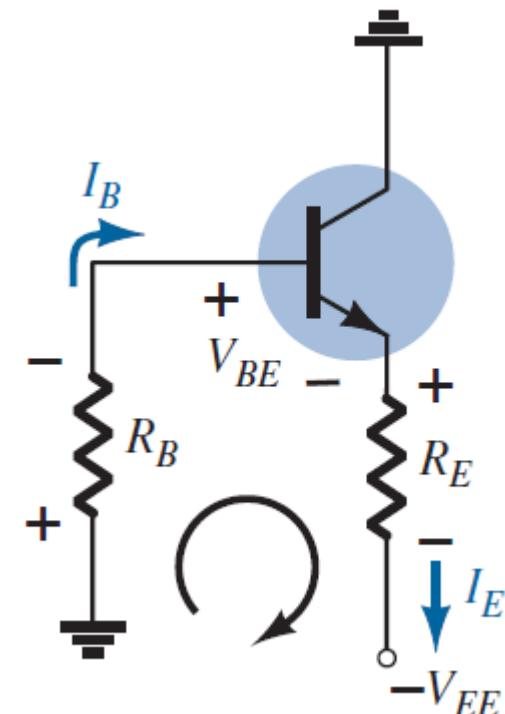
$$I_B R_B + (\beta + 1)I_B R_E = V_{EE} - V_{BE}$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)(R_E)}$$

Output loop

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

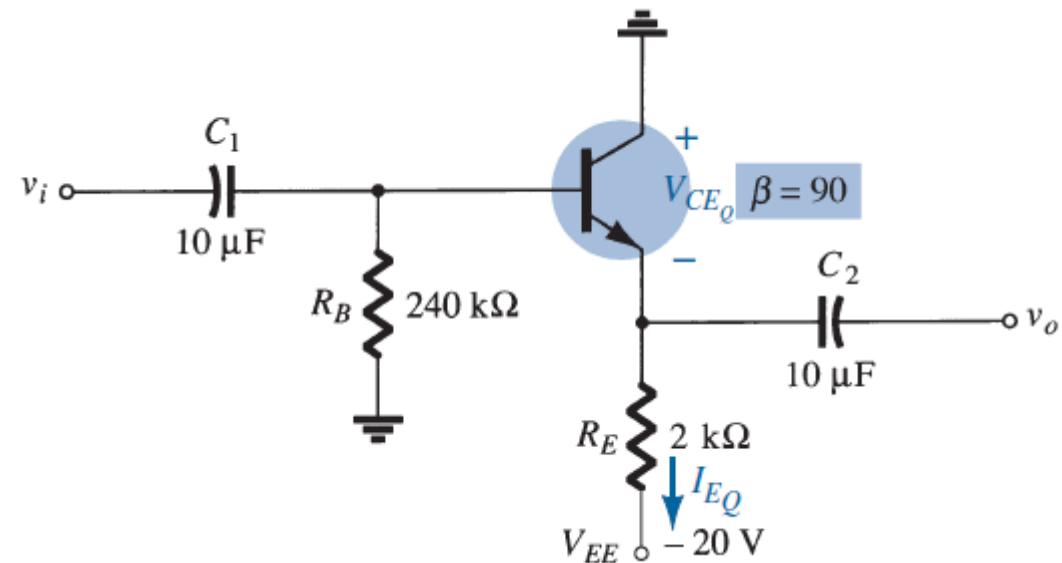
$$V_{CE} = V_{EE} - I_E R_E$$



Emitter-Follower Configuration

- For the circuit shown,
determine:

- I_{EQ}
- V_{CEQ}



Emitter-Follower Configuration

- Solution:

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)(R_E)}$$

$$I_B = \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (90 + 1)(2 \text{ k}\Omega)}$$

$$I_{BQ} = 45.73 \mu\text{A}$$

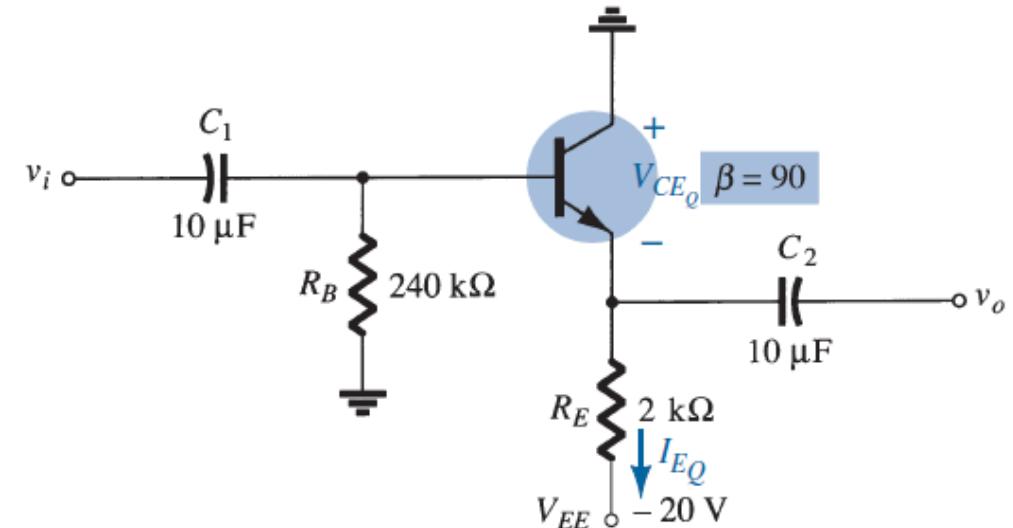
$$V_{CEQ} = V_{EE} - I_E R_E$$

$$V_{CE} = V_{EE} - (\beta + 1) I_B R_E$$

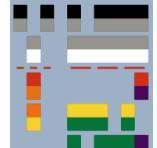
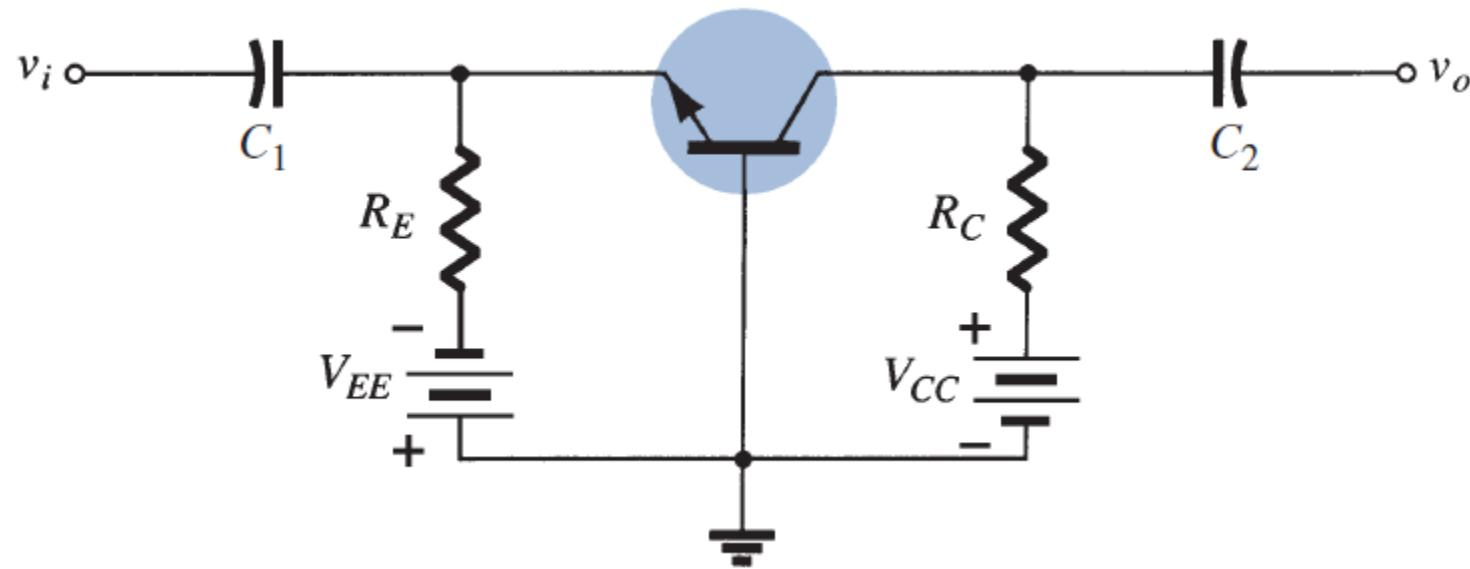
$$V_{CE} = 20 \text{ V} - (90 + 1)(45.73 \mu\text{A})(2 \text{ k}\Omega)$$

$$V_{CEQ} = 20 \text{ V} - 8.32 \text{ V} = 11.68 \text{ V}$$

$$I_{EQ} = (\beta + 1) I_B = (91)(45.73 \mu\text{A}) = 4.16 \text{ mA}$$



Common-base Configuration



Common-base Configuration

- Applying Kirchhoff's voltage law will result in

$$-V_{EE} + V_{BE} + I_E R_E = 0$$

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

- Applying Kirchhoff's voltage law to the entire outside perimeter of the network

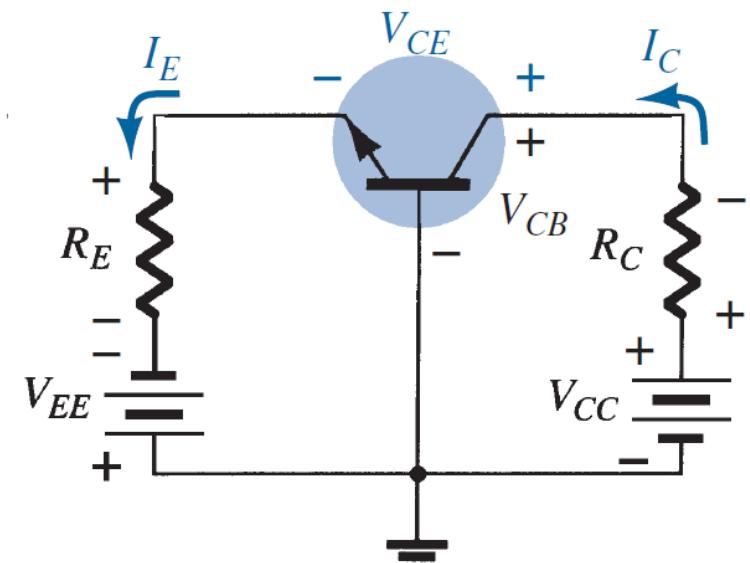
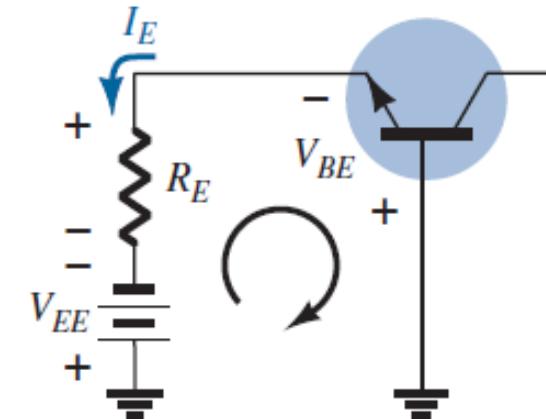
$$-V_{EE} + I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$$

$$V_{CE} = V_{EE} + V_{CC} - I_E R_E - I_C R_C ; I_E \cong I_C$$

$$V_{CE} = V_{EE} + V_{CC} - I_E (R_E + R_C)$$

$$V_{CB} + I_C R_C - V_{CC} = 0$$

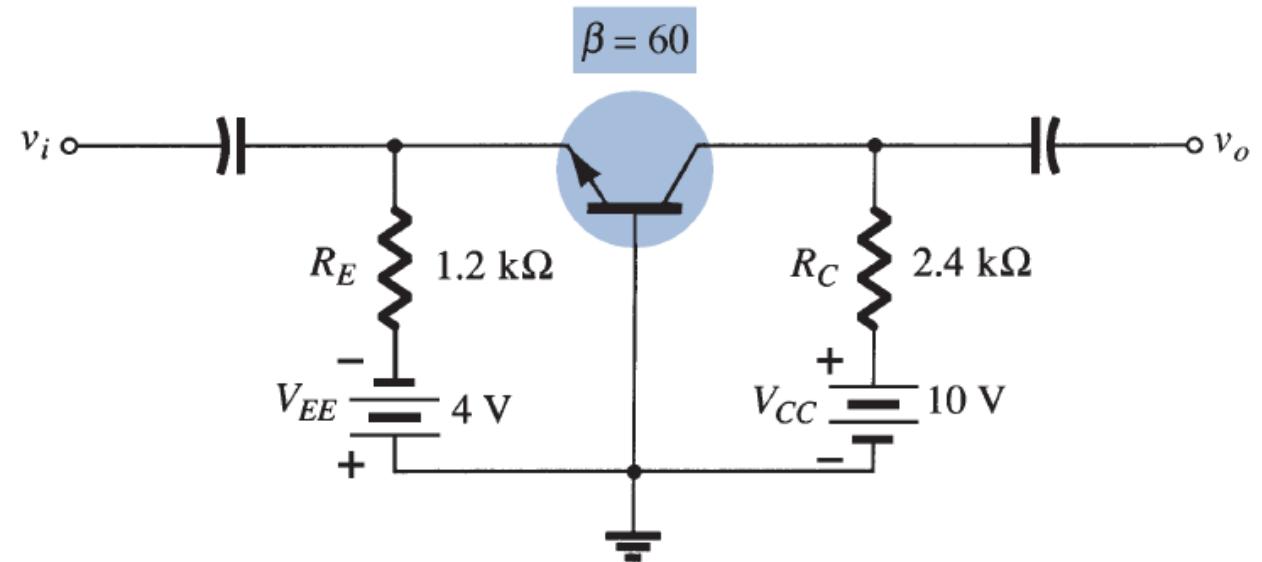
$$V_{CB} = V_{CC} - I_C R_C ; I_E \cong I_C$$



Common-base Configuration

- For the circuit shown,
determine:

- I_E & I_B
- V_{CE} & V_{CB}



Emitter-Follower Configuration

- Solution:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E} = \frac{4V - 0.7V}{1.2k\Omega} = 2.75\text{mA}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75\text{mA}}{60 + 1} = 45.08\mu\text{A}$$

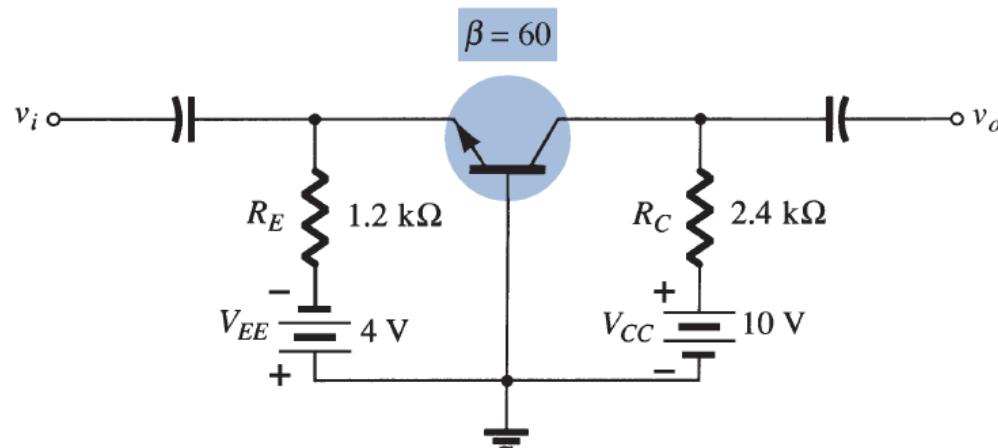
$$V_{CE} = V_{EE} + V_{CC} - I_E (R_E + R_C)$$

$$V_{CE} = 4V + 10V - 2.75\text{mA}(1.2k\Omega + 2.4k\Omega) = 4.1V$$

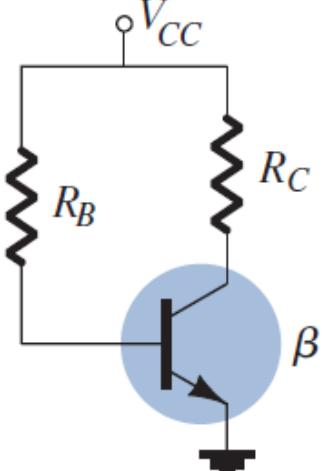
$$V_{CB} = V_{CC} - I_C R_C$$

$$V_{CB} = 10V - (60)(45.08\mu\text{A})(2.4k\Omega)$$

$$V_{CB} = 3.51V$$

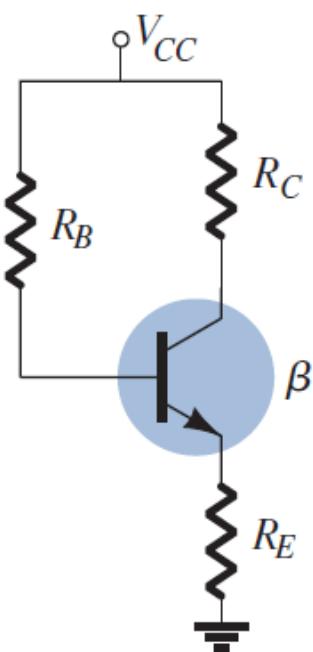


Summary Table

Type	Configuration	Pertinent Equations
Fixed-bias		$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C R_C$

Summary Table

Emitter-bias

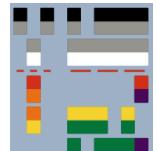


$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

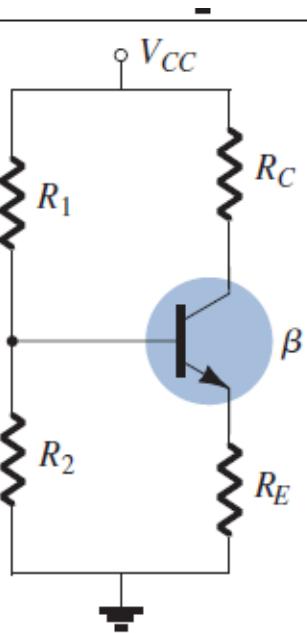
$$I_C = \beta I_B, I_E = (\beta + 1)I_B$$

$$R_i = (\beta + 1)R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

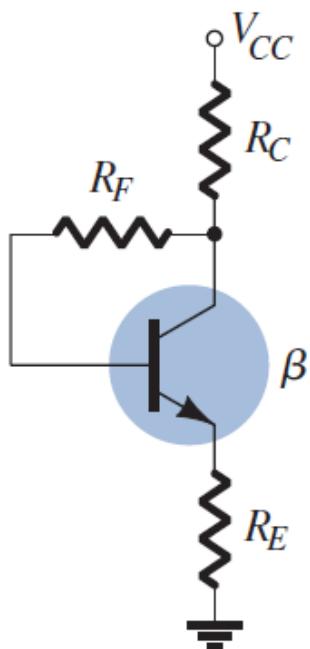


Summary Table

Voltage-divider bias		<p>EXACT: $R_{Th} = R_1 \parallel R_2$, $E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2}$</p> $I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$	<p>APPROXIMATE: $\beta R_E \geq 10R_2$</p> $V_B = \frac{R_2 V_{CC}}{R_1 + R_2}, V_E = V_B - V_{BE}$ $I_E = \frac{V_E}{R_E}, I_B = \frac{I_E}{\beta + 1}$ $V_{CE} = V_{CC} - I_C(R_C + R_E)$
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Summary Table

Collector-feedback

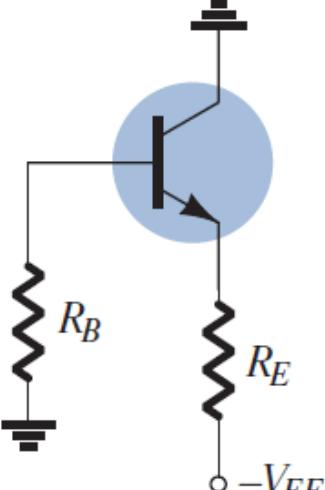


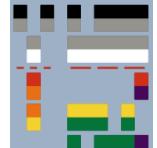
$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta(R_C + R_E)}$$

$$I_C = \beta I_B, I_E = (\beta + 1)I_B$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

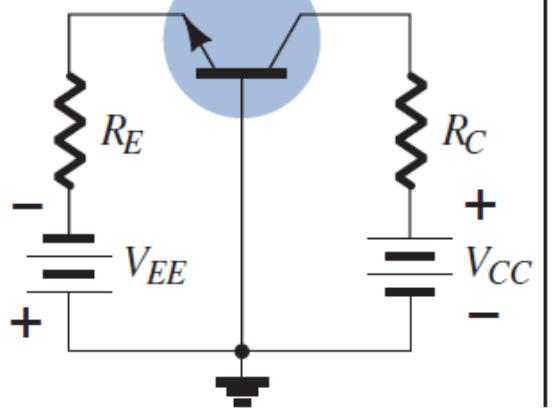
Summary Table

Emitter-follower		$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)}$ $I_C = \beta I_B, I_E = (\beta + 1)I_B$ $V_{CE} = V_{EE} - I_E R_E$
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Summary Table

Common-base



$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$I_B = \frac{I_E}{\beta + 1}, I_C = \beta I_B$$

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$

$$V_{CB} = V_{CC} - I_C R_C$$

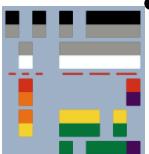
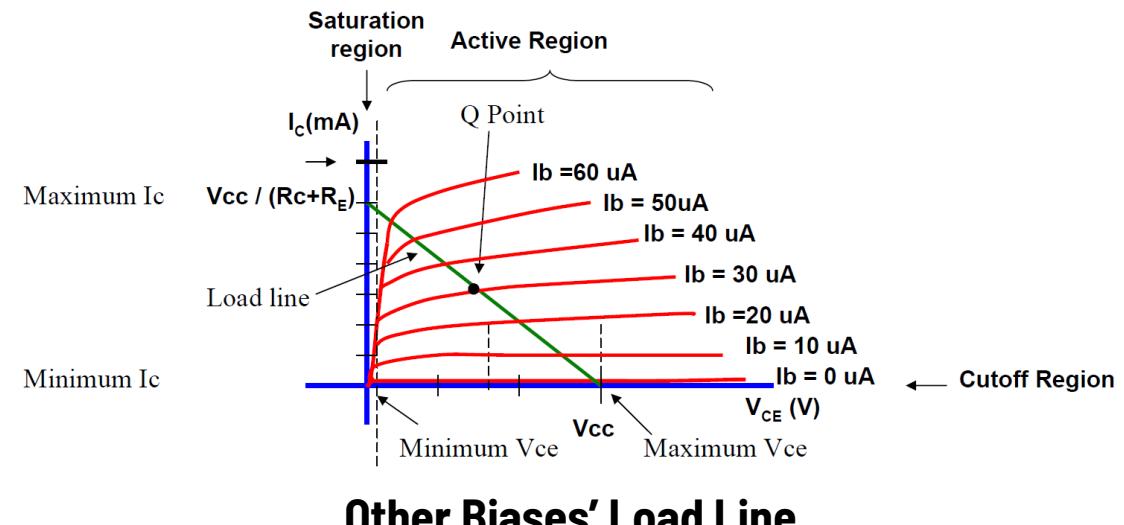
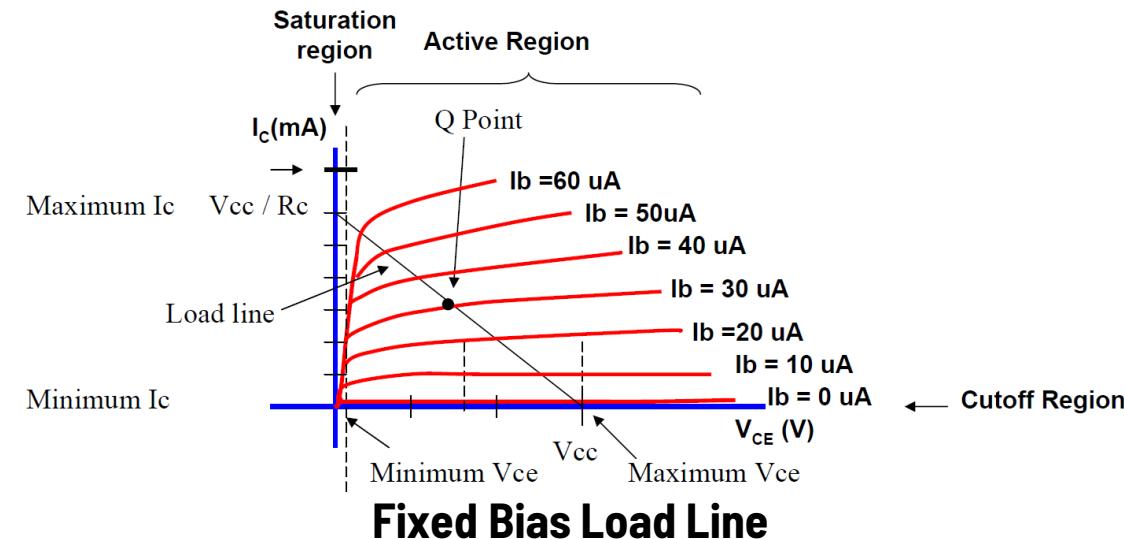
Loadline Analysis

- Loadline – the line drawn over the collector curves to determine all possible operating points.
- At saturation condition:
 1. Set $V_{CE} = 0$ (short circuit V_{CE})
 2. $I_C = I_{CSAT}$ (maximum value that the collector current could have)

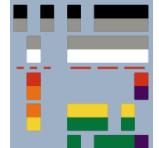
$$I_{CSAT} = \frac{V_{CC}}{R_C} \text{ (Fixed Bias)}$$

$$I_{CSAT} = \frac{V_{CC}}{R_C + R_E} \text{ (all other biasing)}$$

- At cut-off condition:
 1. Open circuit V_{CE} ; $I_C = 0$
 2. $V_{CE} = V_{CC}$ (maximum value that V_{CE} could have)
- Upper end (saturation) of the loadline approximates the value of I_{CSAT}
- Lower end (cut-off) of the loadline approximates the value of V_{CC}

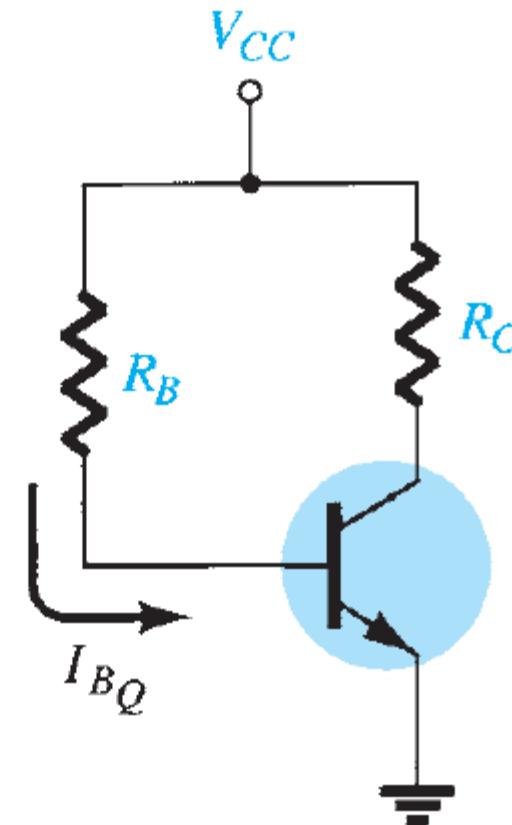
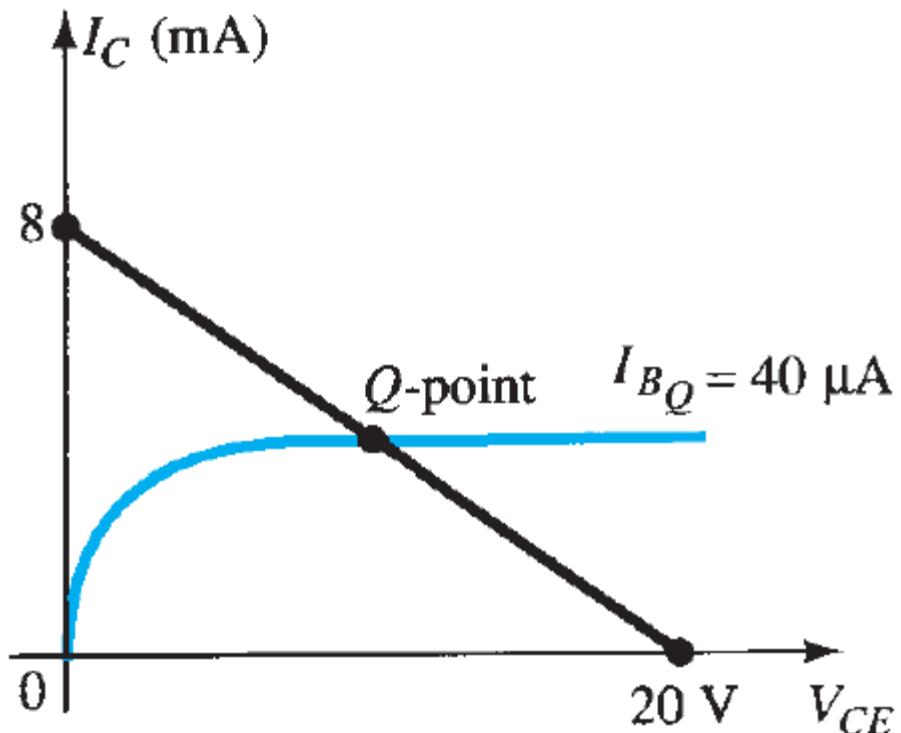


Design Operations



Example #1

- Given the characteristic curve and circuit, determine V_{CC} , R_B and R_C



Example #1

- Solution:

From the load line:

$$V_{CE(cutoff)} \Big|_{I_C=0} = V_{CC} = 20V$$

$$I_{C_{SAT}} = 8mA = \frac{V_{CC}}{R_C}$$

$$R_C = 2.5 k\Omega$$

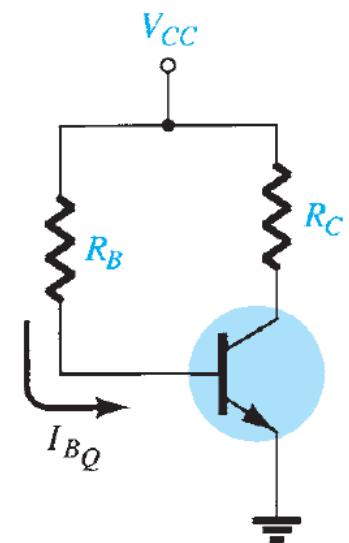
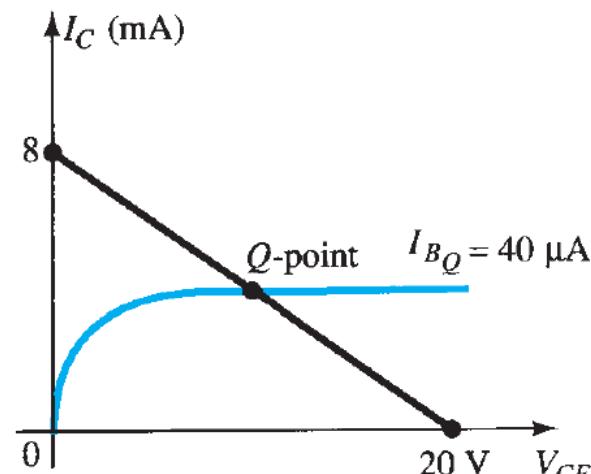
At the input loop:

$$V_{CC} = I_B R_B + V_{BE}$$

$I_B = 40 \mu A$ from the load line

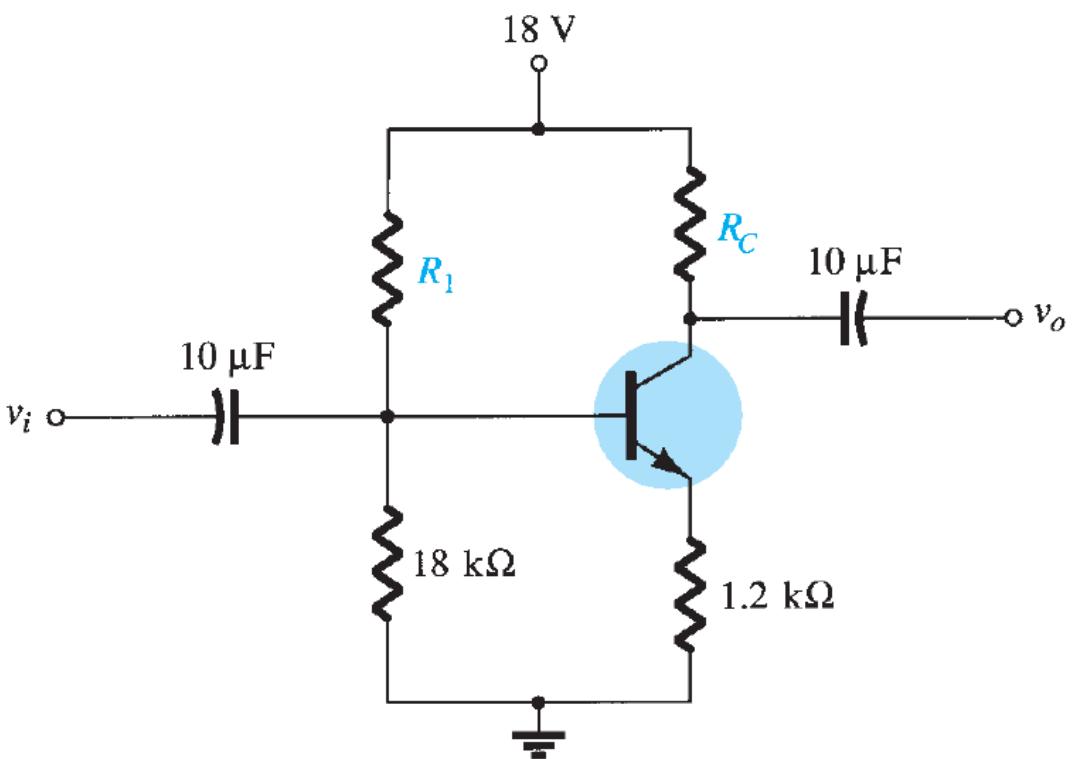
$$20V = 40 \mu A R_B + 0.7V$$

$$R_B = 482.5 k\Omega$$



Example #2

- Given that $I_{CQ} = 2\text{mA}$ and $V_{CEQ} = 10\text{V}$, determine R_{B1} and R_C for the circuit shown



Example #2

- Solution:

$$V_E = I_E R_E$$

From the approximate method:

$$I_E \cong I_C$$

$$V_E = (2mA)(1.2 k\Omega)$$

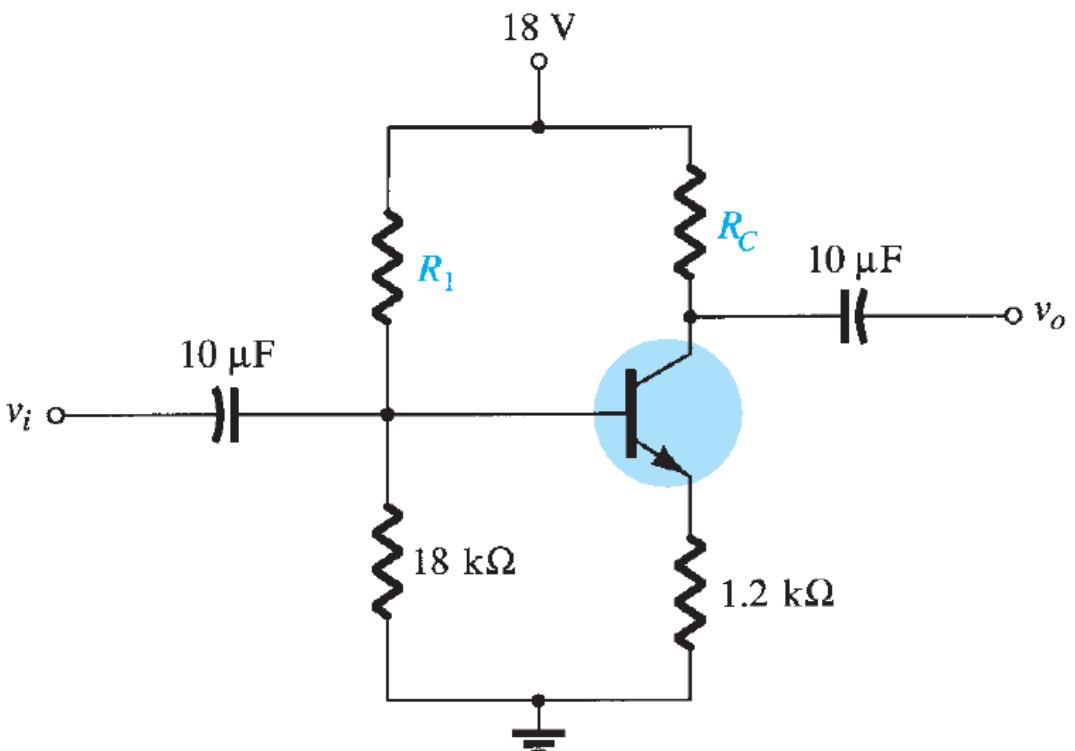
$$V_E = 2.4 V$$

To solve for R_C , at the output loop:

$$V_{CE} = -I_C R_C + V_{CC} - V_E$$

$$10 V = -(2mA)R_C + 18 - 2.4 V$$

$$R_C = 2.8 k\Omega$$



Example #2

- Solution:

For R_{B1} , since $I_B \approx 0$

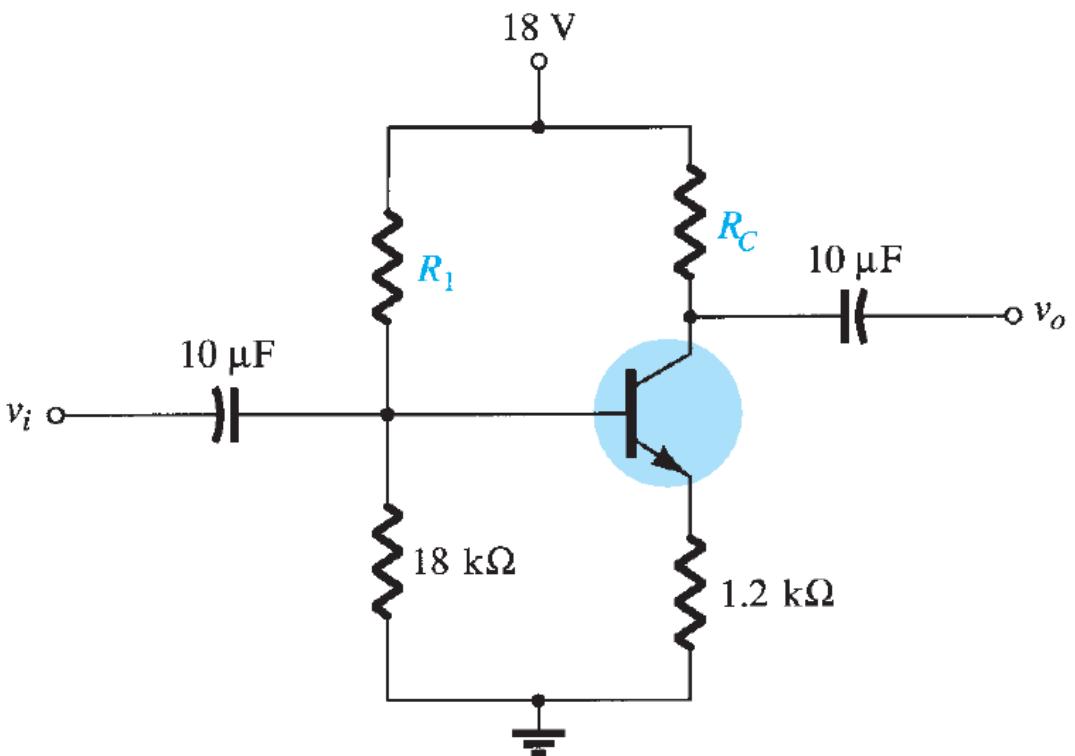
V_{CC} divides its voltage between R_{B1} and R_{B2} . The voltage at the base is the voltage at R_{B2} . We can then use V_B to find R_{B1} .

$$V_{BE} = V_B - V_E = 0.7V$$

$$V_B = V_{BE} + V_E = 0.7V + 2.4V = 3.1V$$

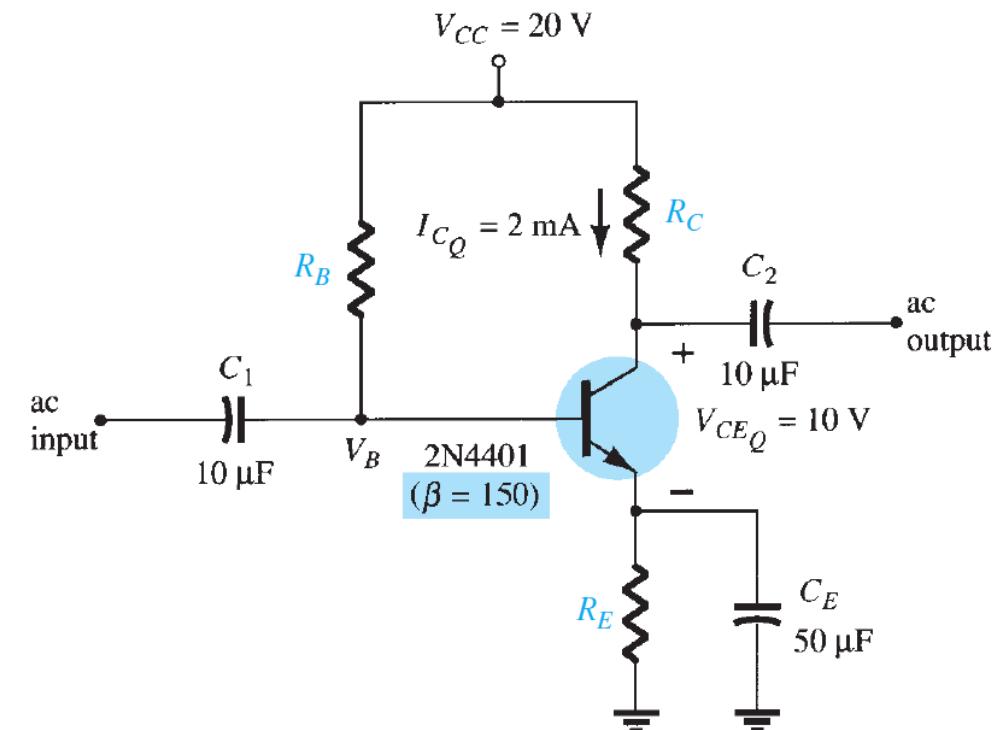
$$3.1V = \frac{18V(18k\Omega)}{18k\Omega + R_{B1}}$$

$$R_{B1} = 86.5161 k\Omega$$



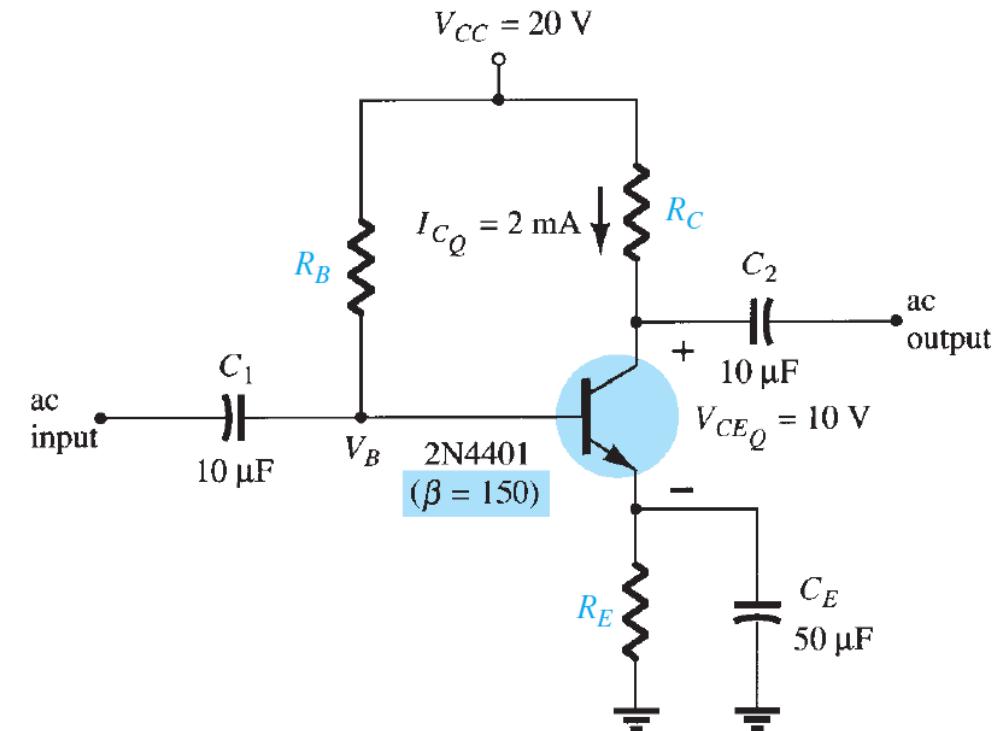
Emitter Stabilized Design

- In the circuit shown, the supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.
- R_C and R_E cannot be determined just from the information given.
- Engineering judgment dictates that the emitter voltage V_E is typically **1/4 to 1/10** of the **supply voltage**.
- Selecting 1/10 will permit calculating R_E and R_C as similar as to those of the previous examples.



Emitter Stabilized Design

- Determine the resistor values (R_B , R_C , and R_E) for the indicated operating point and supply voltage.



Emitter Stabilized Design

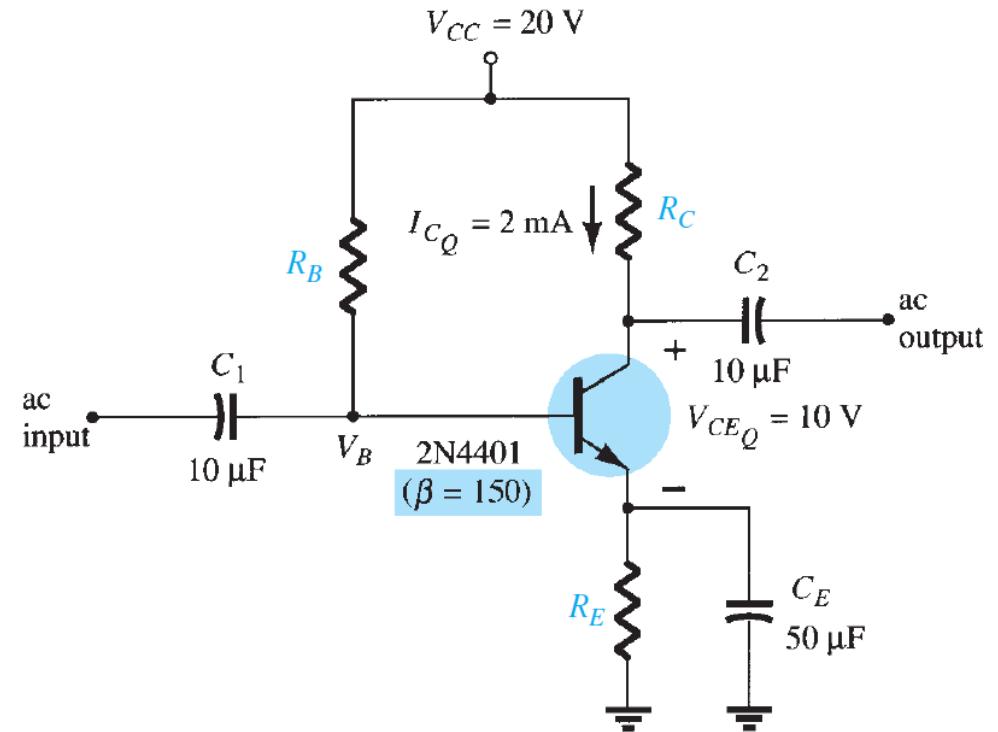
- Solution:

$$V_E = \frac{1}{10} V_{CC} = \frac{1}{10} (20V) = 2V$$

$$I_C = 2mA = \beta I_B$$

$$I_B = \frac{2mA}{150} = 13.3333 \mu A$$

$$R_E = \frac{V_E}{I_E} = \frac{2V}{(\beta + 1)I_B} = \frac{2V}{(151)(13.3333 \mu A)}$$
$$R_E = 993.3774 \Omega$$



Emitter Stabilized Design

- Solution:

$$R_C = \frac{V_{R_C}}{I_C} = \frac{V_{CC} - V_E - V_{CEQ}}{I_C}$$

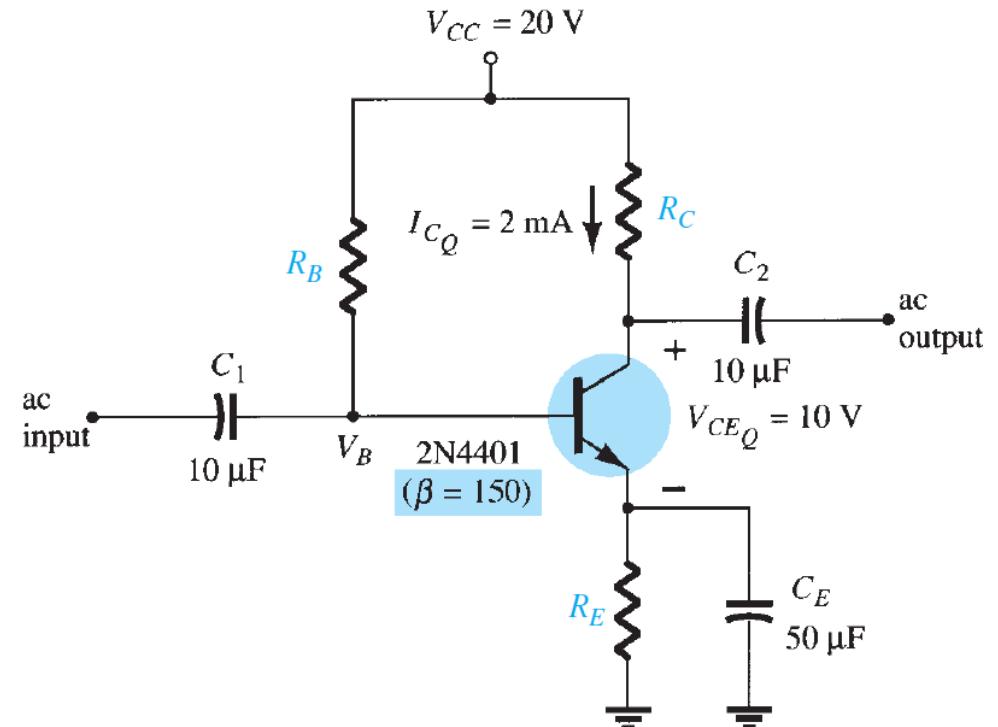
$$R_C = \frac{20V - 2V}{2\text{ mA}} = 10V$$

$$R_C = 4\text{ k}\Omega$$

$$R_B = \frac{V_{R_B}}{I_B} = \frac{V_{CC} - V_E - V_{BE}}{I_B}$$

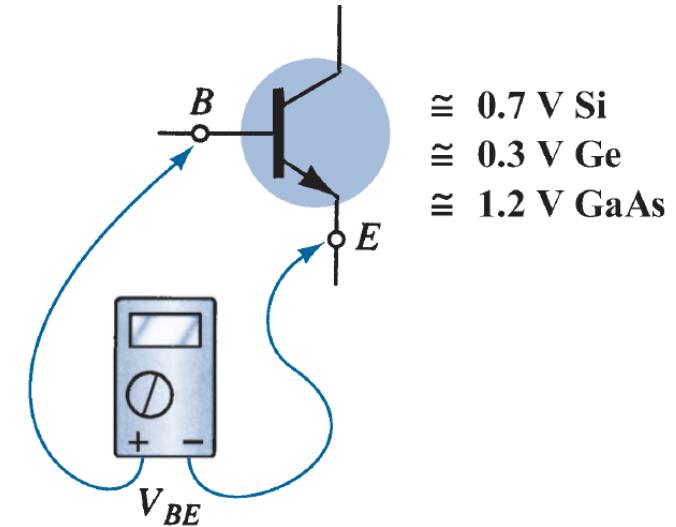
$$R_B = \frac{20V - 2V - 0.7V}{13.3333\mu A} = 1.2975M\Omega$$

$$R_B = 1.2975 M\Omega$$

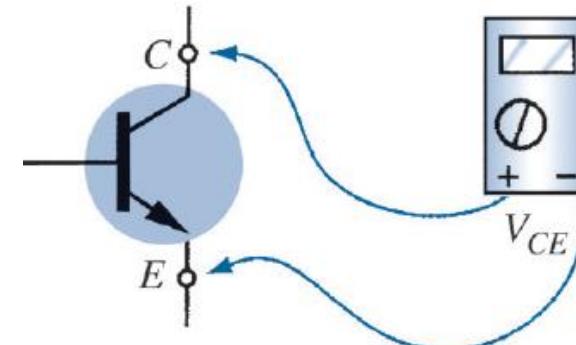


Troubleshooting Techniques

- For an “on” transistor, the voltage VBE should be in the neighborhood of 0.7 V.
- For the typical transistor amplifier in the active region, VCE is usually about 25% to 75% of VCC.



$\approx 0.7 \text{ V Si}$
 $\approx 0.3 \text{ V Ge}$
 $\approx 1.2 \text{ V GaAs}$



0.3 V = saturation
0 V = short-circuit state
or poor connection
Normally a few volts
or more

Troubleshooting Techniques

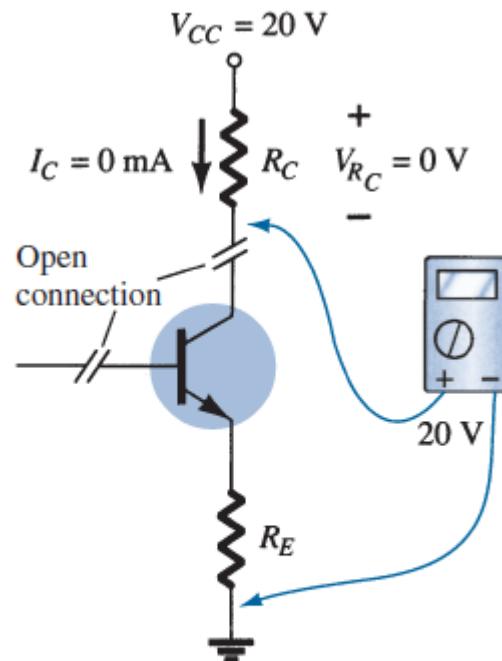


FIG. 94

Effect of a poor connection or damaged device.

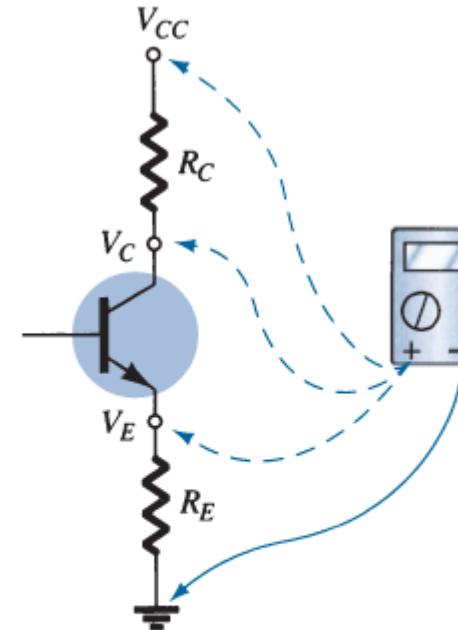
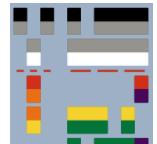


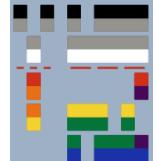
FIG. 95

Checking voltage levels with respect to ground.



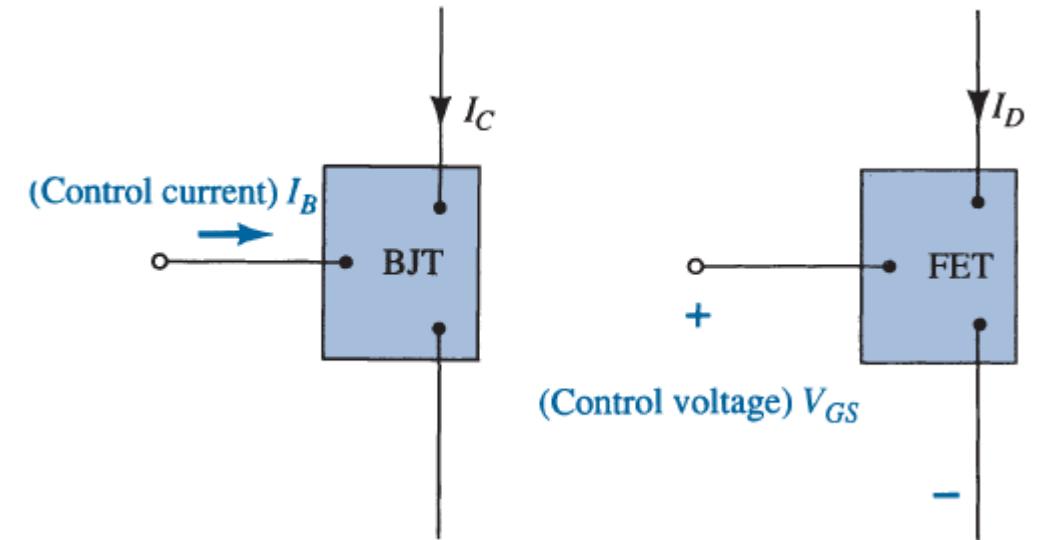


Field Effect Transistors



Field Effect Transistor

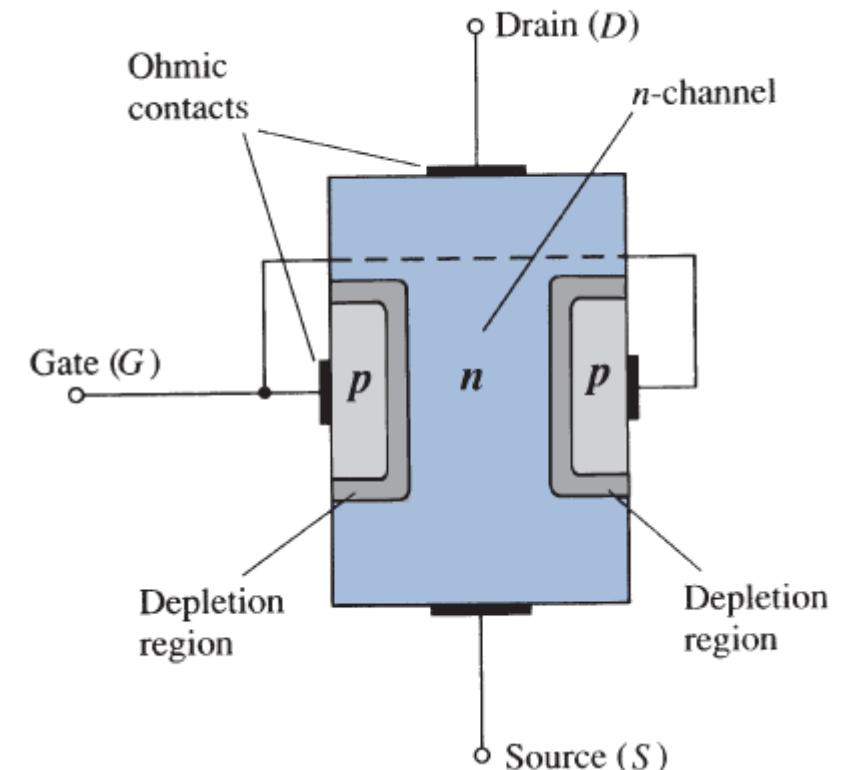
- **Field Effect Transistor (FET)** is generally a three terminal device which could be used in applications wherein bipolar junction transistors are used.
- FETs are the next generation of transistors after BJTs.
- It is a **voltage controlled device** as compared to a BJT which is a current controlled device.
 - Output voltages and currents are controlled by the input voltage rather than by the input current.
- The term **field effect** is used because for FETs, an electric field established by the carriers controls the conduction path of the output current without the need for direct contact between the input signal parameters and the output signal parameters.



It is a **unipolar device** because current flow is only dependent on either **electron flow** (n channel) or **hole flow** (p channel). **BJT is a bipolar device** because current flow is always dependent on electron flow (n material) and hole flow (p material).

Field Effect Transistor

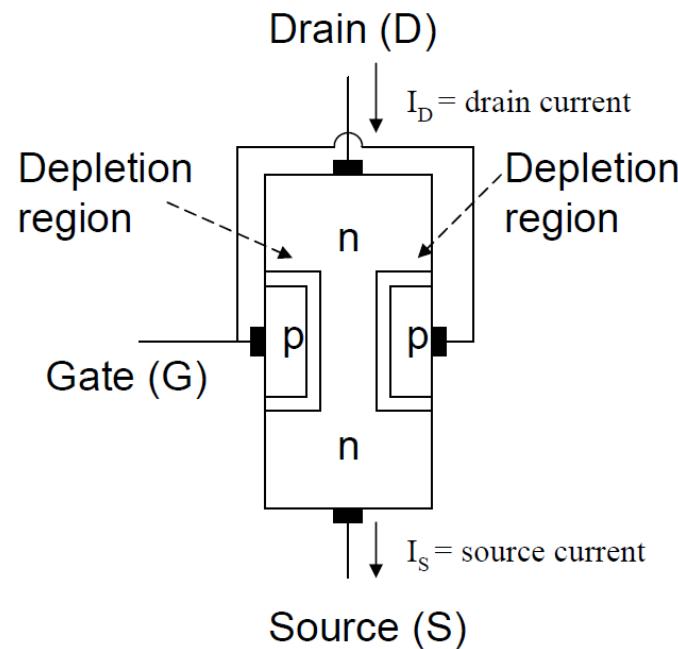
- A FET has three terminals: the **drain (D)**, the **gate (G)**, and the **source (S)**. The output current of an FET **depends on an electric field that depends on a gate control voltage**.
- Since a FET operates as a voltage-dependent device, the **drain (output) current** depends on the **input gate voltage**.
- One **major characteristic** of field effect transistors is its **very high input impedance**, which make it **ideal** as an **input stage device**.
- There are three types of FETs: enhancement metal oxide semiconductor field-effect transistors (**enhancement MOSFETs**), depletion metal oxide semiconductor field-effect transistors (**depletion MOSFETs**), and junction field-effect transistors (**JFETs**).



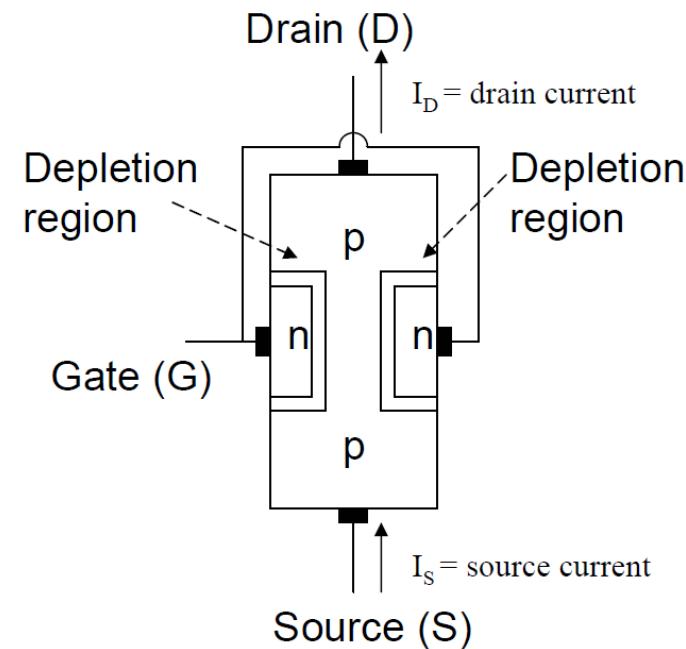
Junction Field Effect Transistor

Junction Field Effect Transistor

- JFETs are either **n-channel** or **p-channel** depending on its construction. The basic construction of an n-channel and p-channel JFET is shown below.
- There exists a p-n junction between the gate and the channel, thus, the name junction FET.



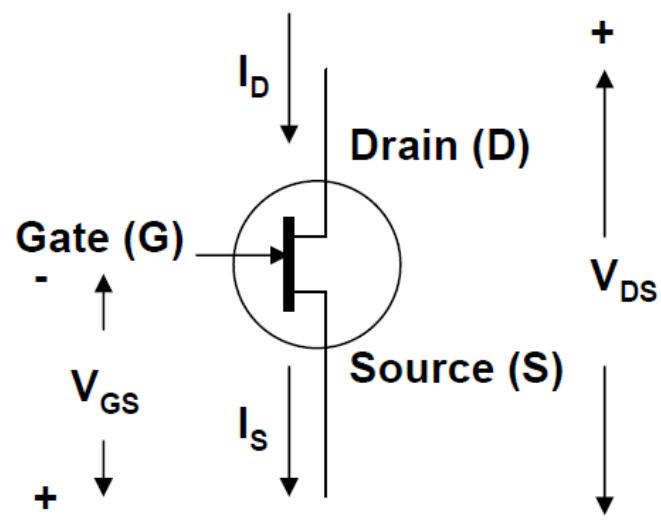
N-Channel JFET



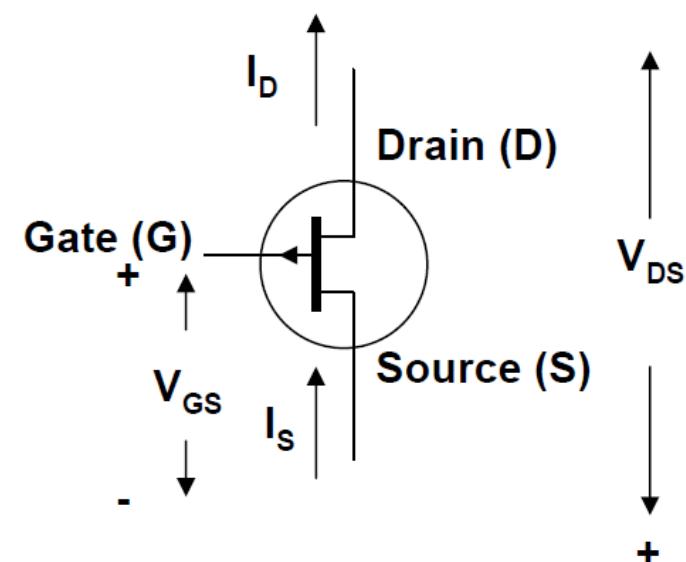
P-Channel JFET

Junction Field Effect Transistor

- The schematic symbol for the JFET is shown below.



N-Channel JFET



P-Channel JFET

Junction Field Effect Transistor

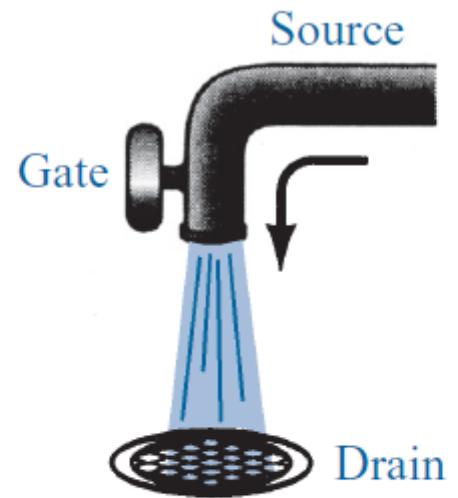
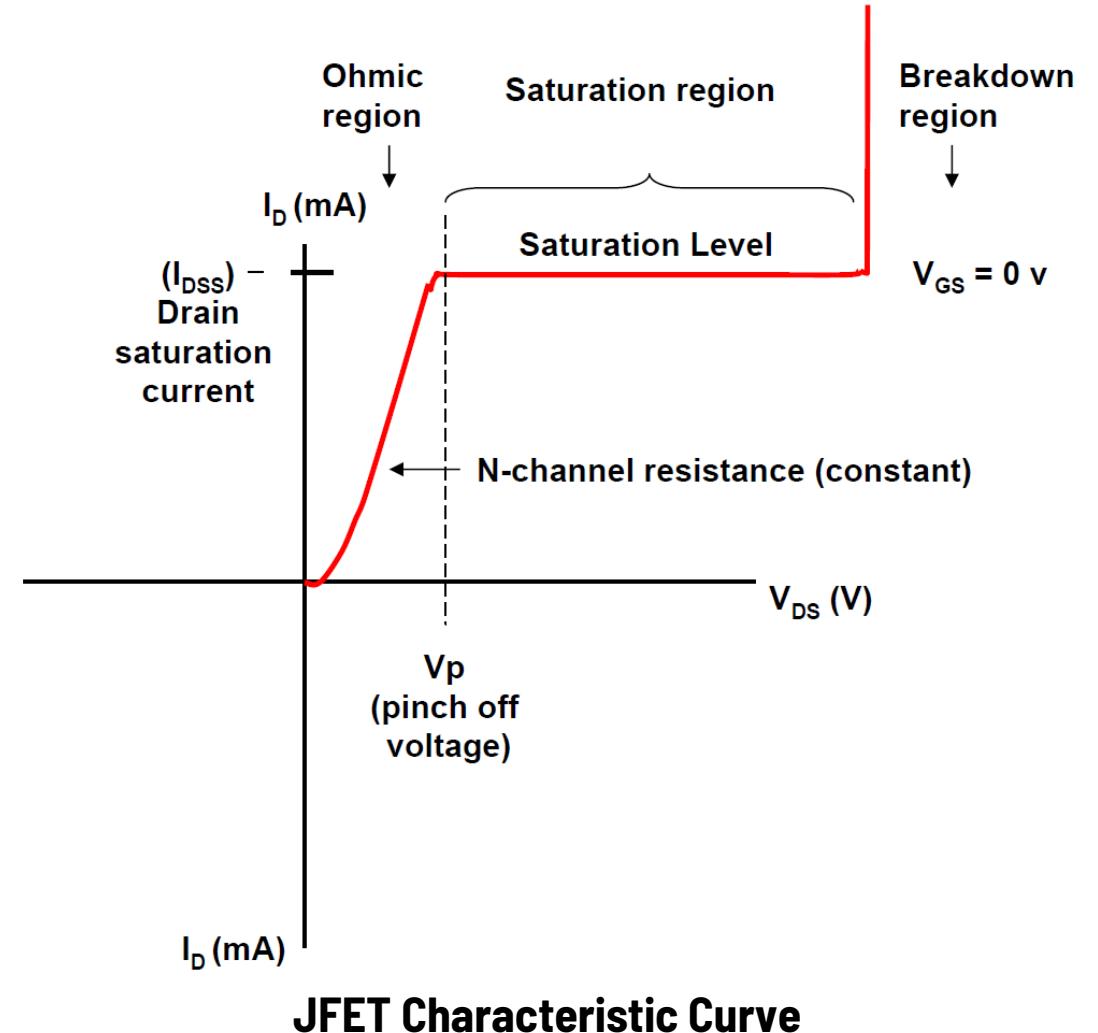


FIG. 4
Water analogy for the JFET control mechanism.

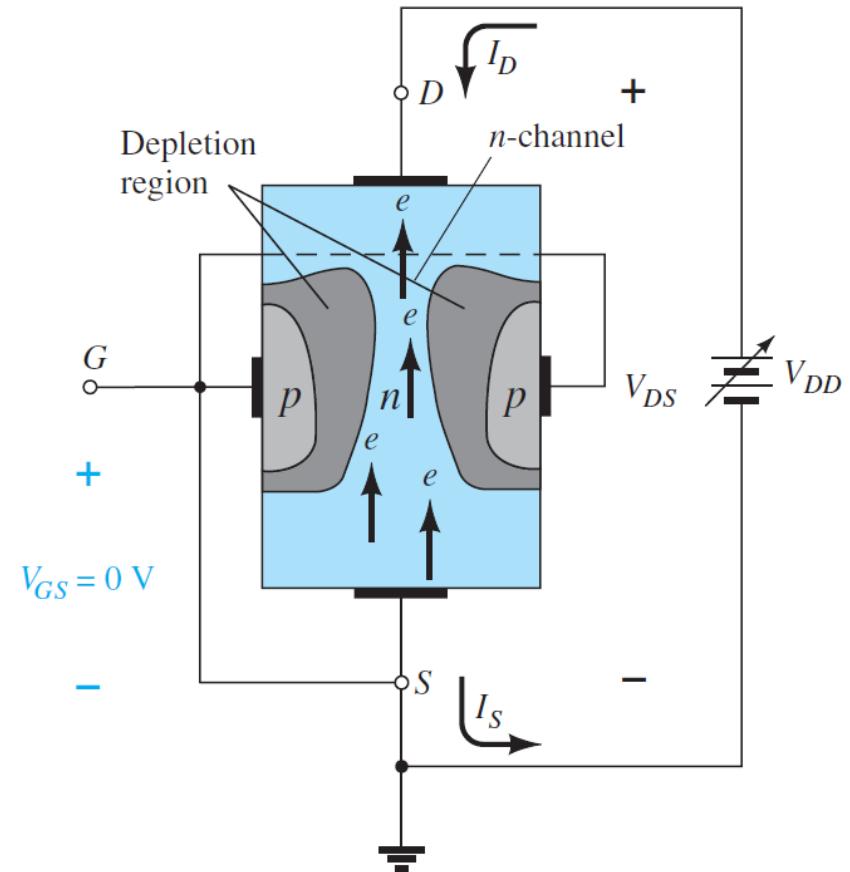
Junction Field Effect Transistor

- The JFET output has three regions of operation: **ohmic**, **saturation** and **breakdown**.
- In the **ohmic region** the JFET output acts like a **voltage controlled resistance**, while in the **saturation** the **current** across the transistor appears to be **constant** and the **breakdown** region is where the transistor starts to **fail** and be destroyed.



Junction Field Effect Transistor

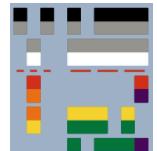
- The JFET input **must be reverse biased** so that **no current** will flow back to the gate.
- The simplest biasing arrangement to explain the operating regions of a JFET is by providing a zero volt input (gate) at the transistor and a bias voltage from the drain to the source.



JFET at $V_{GS} = 0\text{V}$ and $V_{DS} > 0\text{V}$

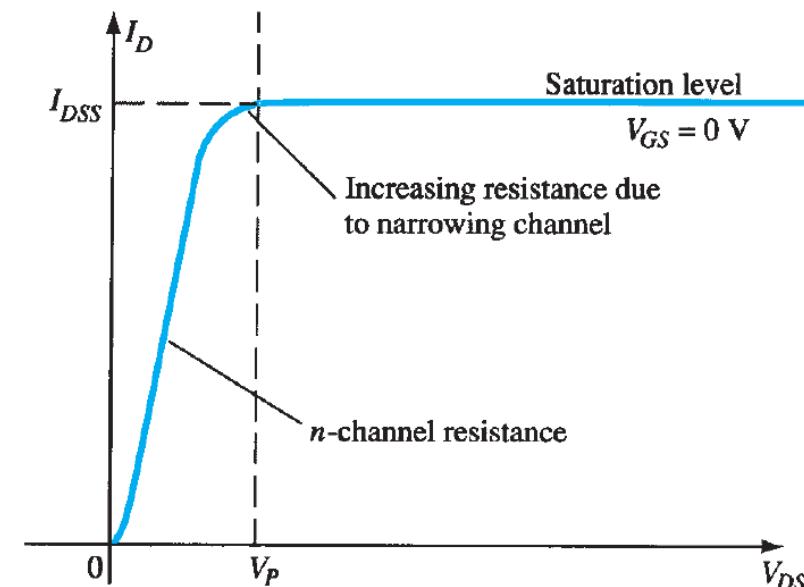
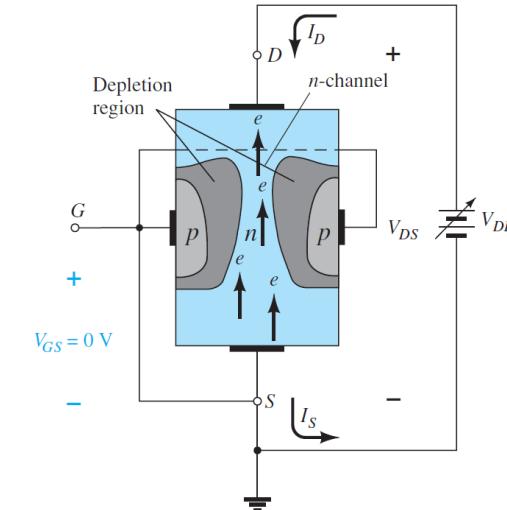
Junction Field Effect Transistor

- V_{DD} – Drain biasing voltage – Voltage input supply for the Drain junction
- V_{GG} – Gate biasing voltage – Voltage input supply for the Gate junction
- V_{GS} – Gate to Source voltage
- V_{DS} – Drain to Source voltage
- V_P – Pinch-off Voltage
- I_G – Gate Current
- I_D – Drain Current
- I_{DSS} – maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.
- r_D – resistance at a particular level of V_{GS}
- r_o – resistance with $V_{GS} = 0$ V



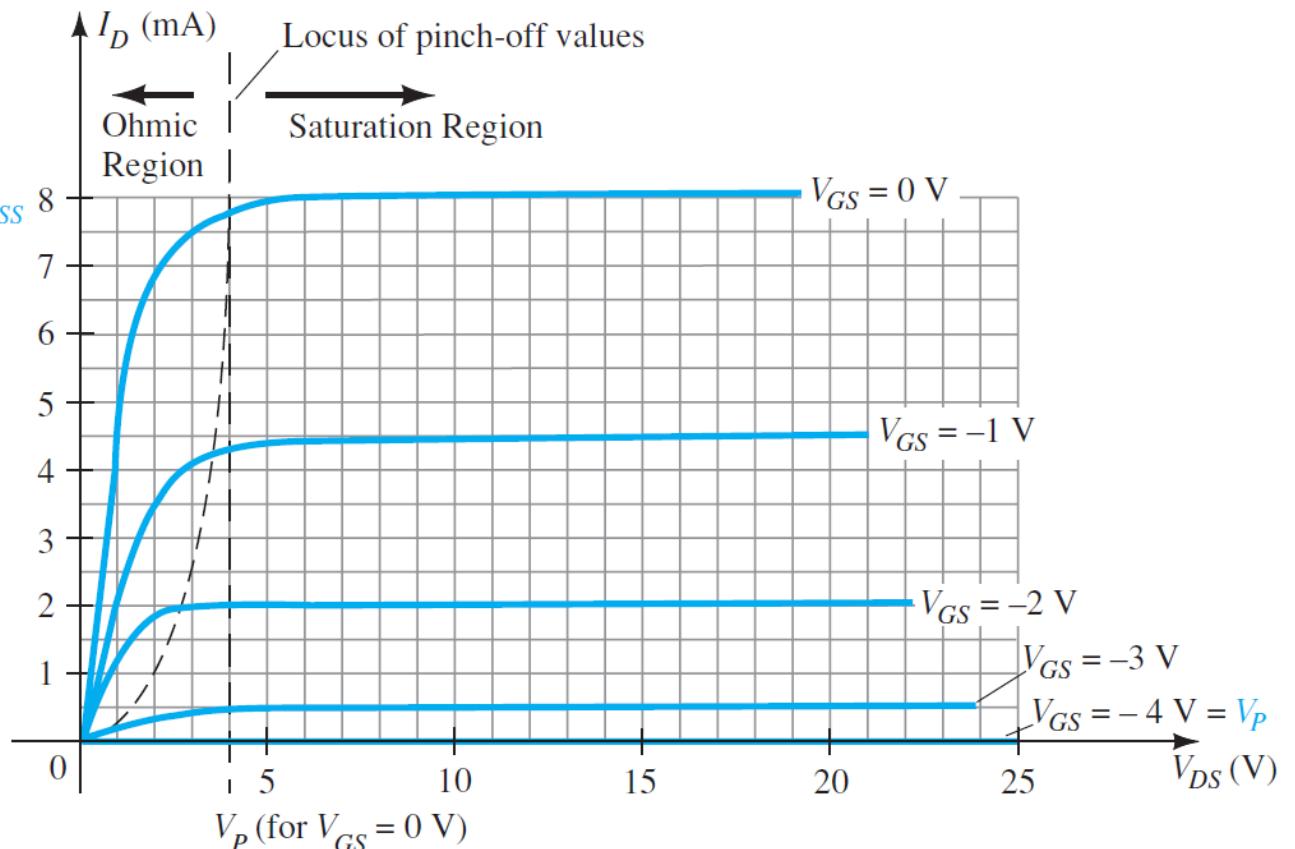
Junction Field Effect Transistor

- In this arrangement ($V_{GS} = 0V$), when $V_{DD} = 0V$, the junction creates a depletion region and from here the first approximation for the FET is that $I_G = 0$ and also $I_D = I_{DD}$.
- When V_{dd} is gradually increased the current will also increase according to Ohm's Law
- The transistor is now working in the ohmic region. As V_{dd} increases, the depletion region widens, thus making the output resistance larger until it reached a point called the pinch-off voltage, V_P , where the resistance of the channel increased and the channel current stops increasing reaching a saturation point, entering the saturation region.
- The current at this saturation point, $V_{GS} = 0$ and $V_{DS} > V_P$ is called the drain-to-source saturation current, I_{DSS} . This is the region where the transistor can act as an amplifier.



Junction Field Effect Transistor

- V_{GS} (gate-to-source voltage) is used to **control** the current of the transistor.
- When a negative voltage, V_{GS} is applied to the transistor it establishes **depletion regions similar** to those obtained with $V_{GS} = 0V$ but **at lower levels of V_{DS}** .
- The result of **applying a negative bias** to the gate is to **reach the saturation level at a lower level of V_{DS}** . The resulting **saturation level for I_D has been reduced** and in fact will **continue to decrease** as V_{GS} is made more and **more negative**.
- Eventually, V_{GS} , when $V_{GS} = -V_P$, will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes, the device has been turned off.
- The level of V_{GS} that results in $I_D = 0\text{mA}$ is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel and positive for p-channel JFETs.



Junction Field Effect Transistor

- The transfer characteristic of a JFET is determined by **Shockley's equation**.
- The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

For BJT, $I_C = \beta I_B$ where β is the constant and I_B is the control element

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Where:

I_{DSS} = Saturation Drain current when $V_{GS} = 0V$

V_{GS} = Gate to source voltage

$V_P = V_{P(OFF)} = V_{GS(OFF)}$ = Pinch off voltage

Junction Field Effect Transistor

- The transfer characteristic of a JFET is determined by **Shockley's equation**.
- The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

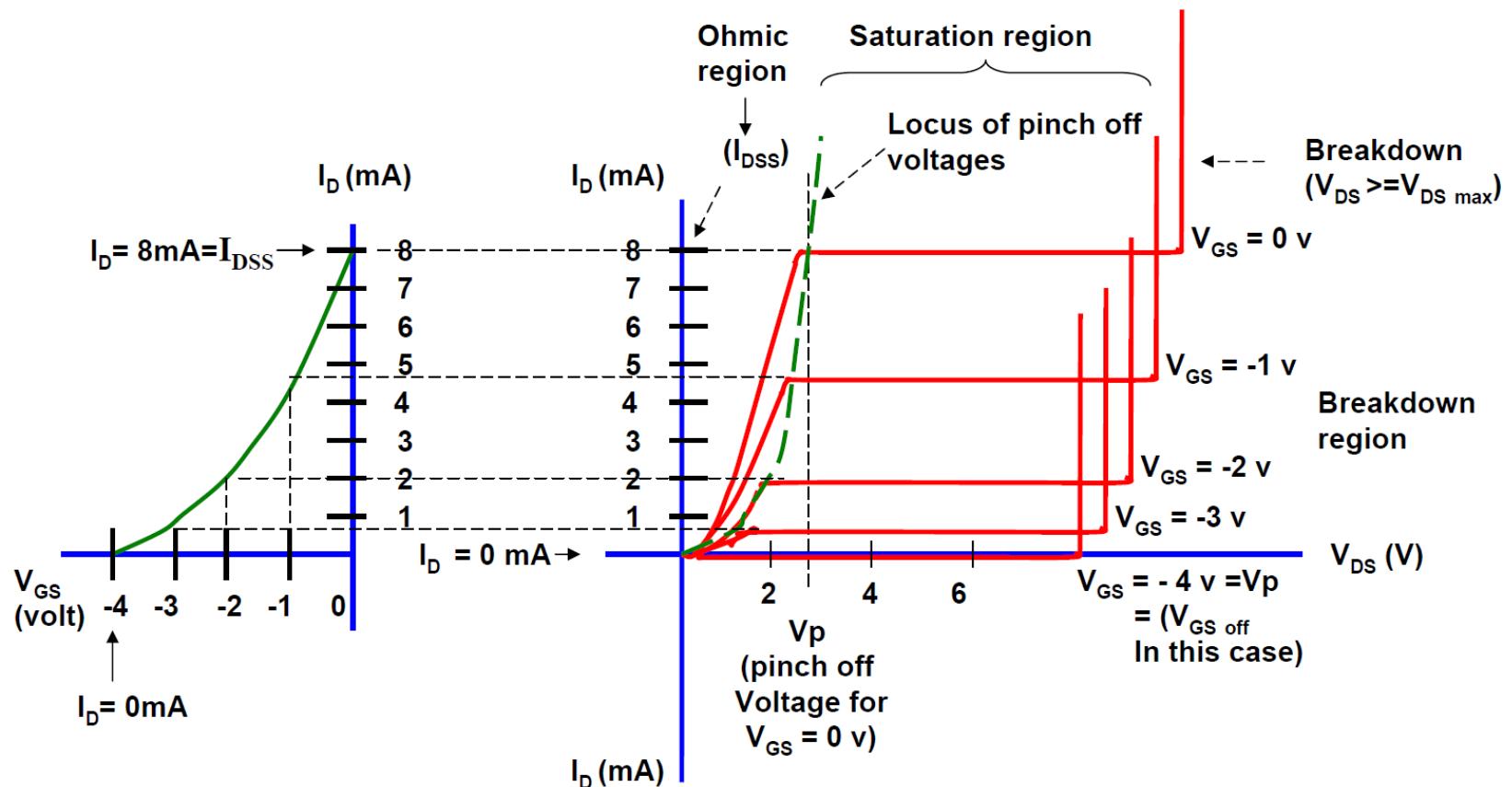
When $V_{GS} = 0 \text{ V}$, $I_D = I_{DSS}$.

When $V_{GS} = V_P$, $I_D = 0 \text{ mA}$.

$$V_{GS} = V_P \left[1 - \sqrt{\frac{I_D}{I_{DSS}}} \right]$$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

Junction Field Effect Transistor



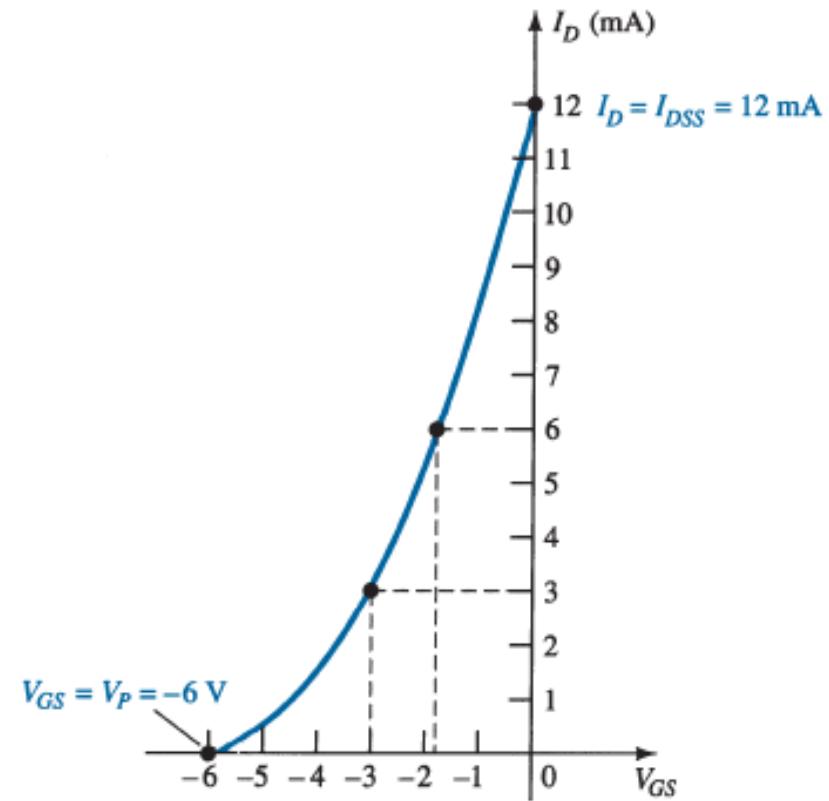
Junction Field Effect Transistor

- Sketch the transfer curve defined by $IDSS = 12 \text{ mA}$ and $V_P = -6 \text{ V}$.

Junction Field Effect Transistor

- Sketch the transfer curve defined by $ID_{SS} = 12 \text{ mA}$ and $V_P = -6 \text{ V}$.

- $ID_{SS} = 12 \text{ mA}$ and $V_{GS} = 0 \text{ V}$
- $ID = 0 \text{ mA}$ and $V_{GS} = V_P$
- $V_{GS} = V_P/2 = -6 \text{ V}/2 = -3 \text{ V}$
- $ID = ID_{SS}/4 = 12 \text{ mA}/4 = 3 \text{ mA}$.
- At $ID = ID_{SS}/2 = 12 \text{ mA}/2 = 6 \text{ mA}$
- $V_{GS} \approx 0.3V_P = 0.3(-6 \text{ V}) = -1.8 \text{ V}$



Junction Field Effect Transistor

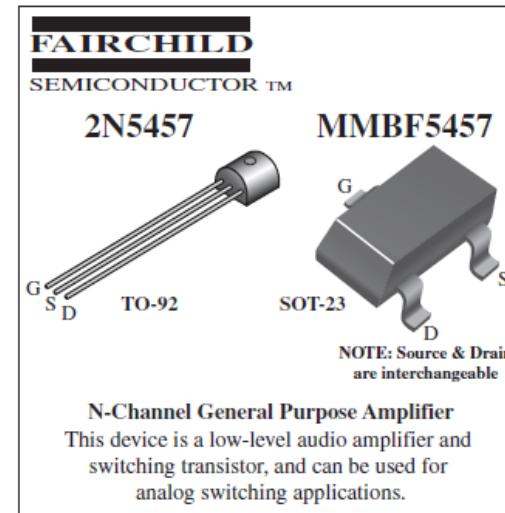
- Specification sheets (JFETS)

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source Voltage	25	V
V_{DG}	Drain-Gate Voltage	25	V
V_{GS}	Gate-Source Voltage	-25	V
I_{GF}	Forward Gate Current	10	mA
T_j, T_{stg}	Operating and Storage Junction Temperature Range	-55 to +150	°C

THERMAL CHARACTERISTICS

Symbol	Characteristic	Max		Units
		2N5457	*MMBF5457	
P_D	Total Device Dissipation Derate above 25°C	625 5.0	350 2.8	mW mW/°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	°C/W



Junction Field Effect Transistor

- Specification sheets (JFETS)

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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OFF CHARACTERISTICS

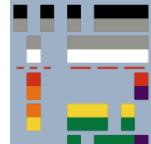
$V_{(\text{BR})\text{GSS}}$	Gate-Source Breakdown Voltage	$I_G = 10 \mu\text{A}, V_{DS} = 0$	-25			V
I_{GSS}	Gate Reverse Current	$V_{GS} = -15 \text{ V}, V_{DS} = 0$ $V_{GS} = -15 \text{ V}, V_{DS} = 0, T_A = 100^\circ\text{C}$		-1.0 -200	nA nA	
$V_{GS(\text{off})}$	Gate-Source Cutoff Voltage	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ nA}$	5457	-0.5	-6.0	V
V_{GS}	Gate-Source Voltage	$V_{DS} = 15 \text{ V}, I_D = 100 \mu\text{A}$	5457	-2.5		V

ON CHARACTERISTICS

I_{DSS}	Zero-Gate Voltage Drain Current	$V_{DS} = 15 \text{ V}, V_{GS} = 0$	5457	1.0	3.0	5.0	mA
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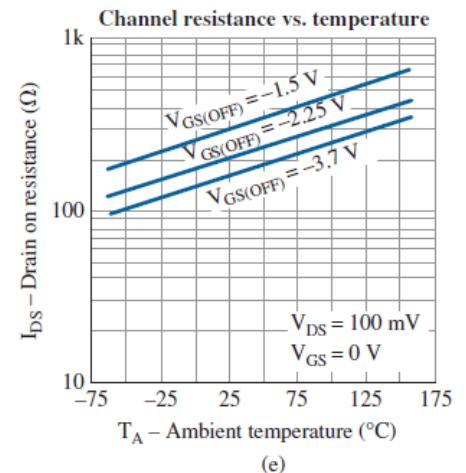
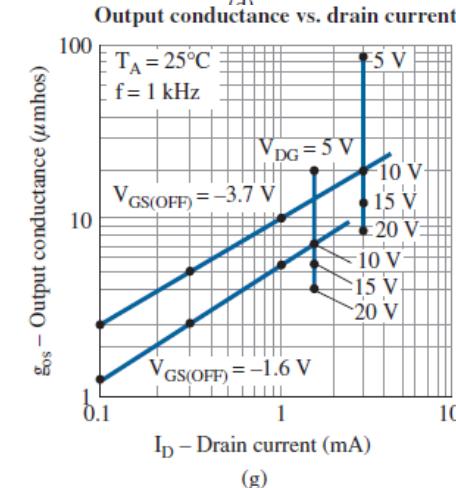
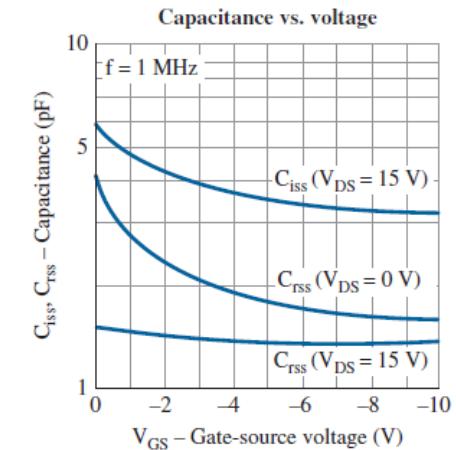
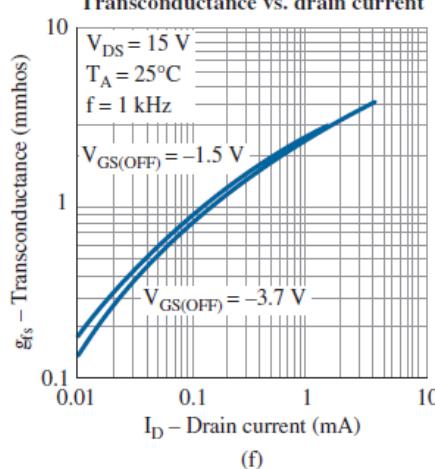
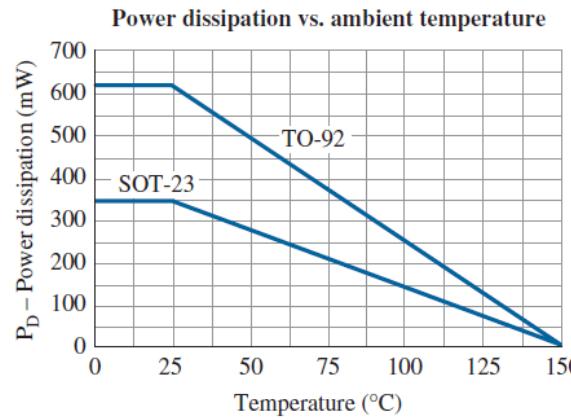
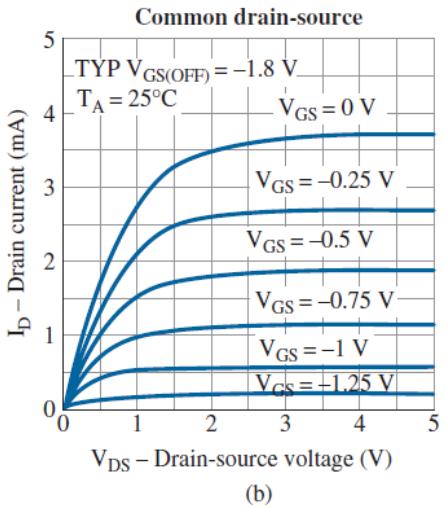
SMALL SIGNAL CHARACTERISTICS

g_{fs}	Forward Transfer Conductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}$	5457	1000		5000	μmhos
g_{os}	Output Conductance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		10	50		μmhos
C_{iss}	Input Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		4.5	7.0		pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$		1.5	3.0		pF
NF	Noise Figure	$V_{DS} = 15 \text{ V}, V_{GS} = 0, f = 1.0 \text{ kHz}, R_G = 1.0 \text{ megohm}, \text{BW} = 1.0 \text{ Hz}$			3.0		dB



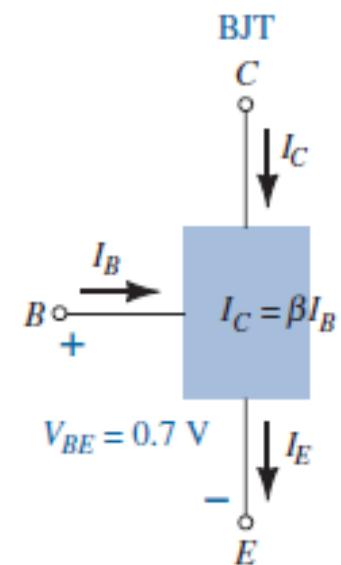
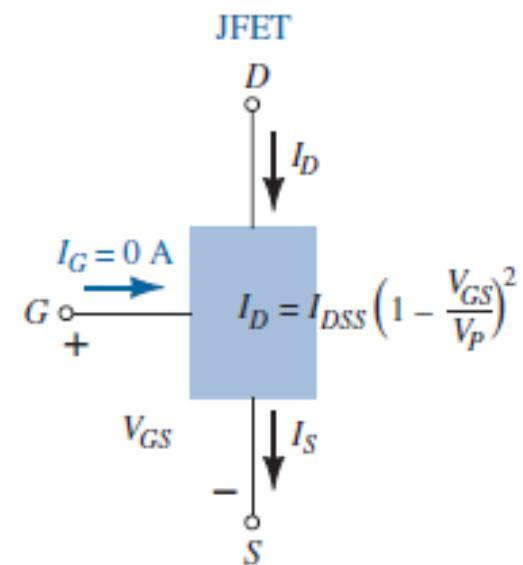
Junction Field Effect Transistor

- Specification sheets (JFETS)



Important Relationships

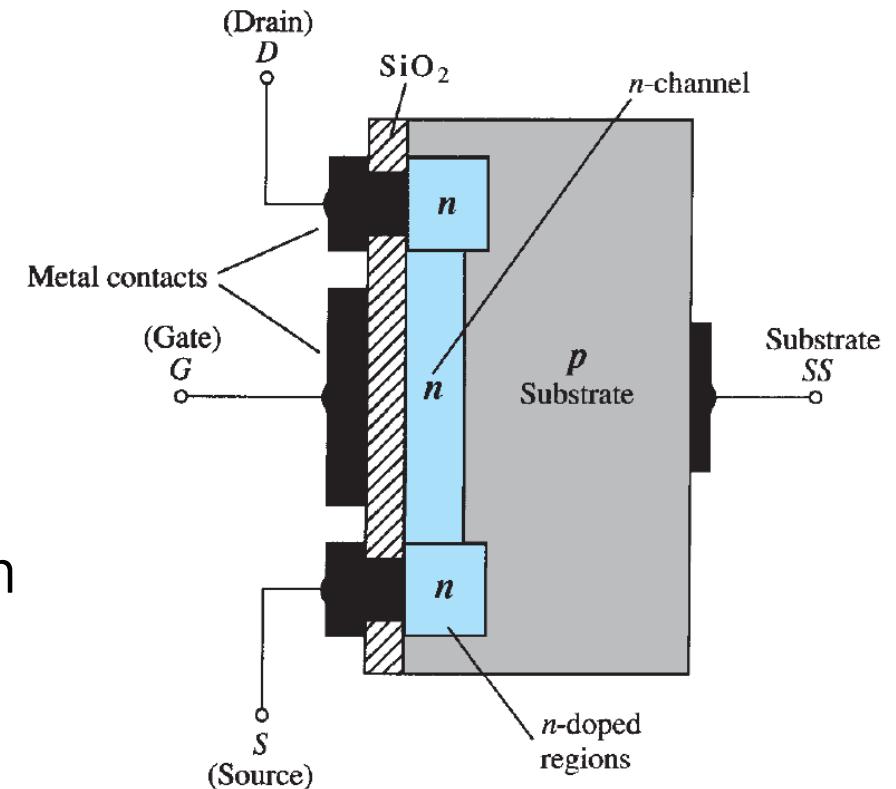
JFET	BJT	
$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$	\Leftrightarrow	$I_C = \beta I_B$
$I_D = I_S$	\Leftrightarrow	$I_C \approx I_E$
$I_G \approx 0 \text{ A}$	\Leftrightarrow	$V_{BE} \approx 0.7 \text{ V}$



Depletion-Type Metal Oxide Semiconductor FET (D-MOSFET)

D-MOSFET

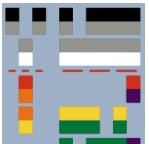
- Depletion type MOSFET has **the same** characteristics as JFET **between cutoff and saturation at I_{DSS}** .
- Another name for D-MOSFET is **Insulated Gate FET (IGFET)**.
- Note that There is no direct electrical connection between the gate terminal and the channel of a MOSFET.
- It is the insulating later of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.



N-channel D-MOSFET

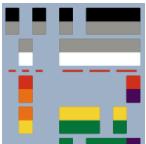
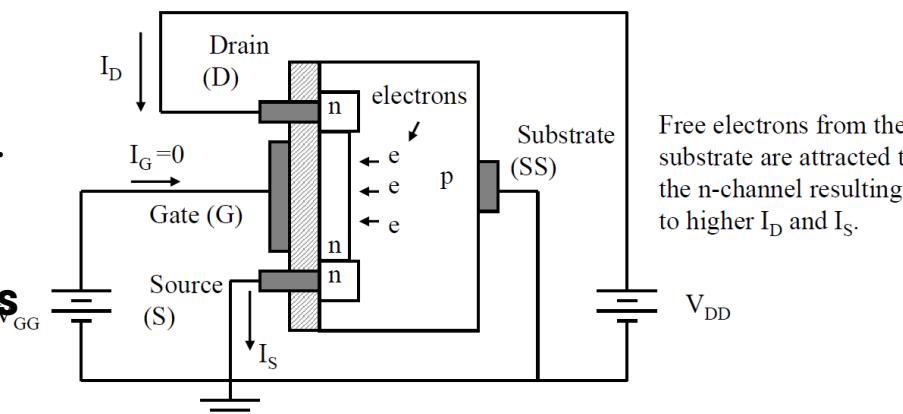
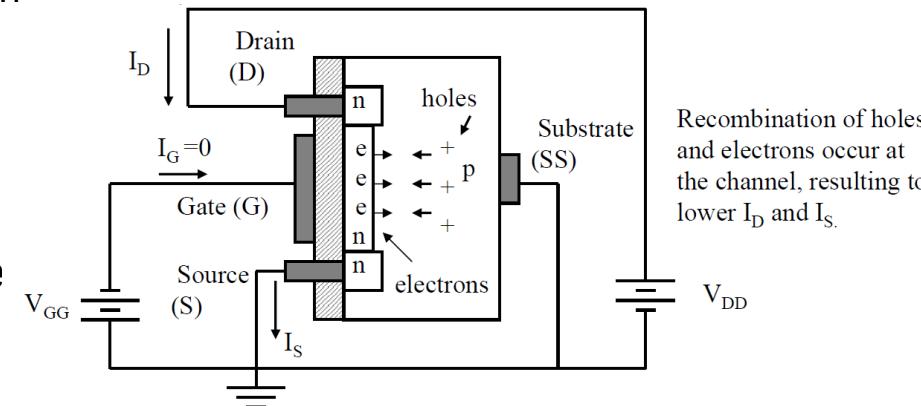
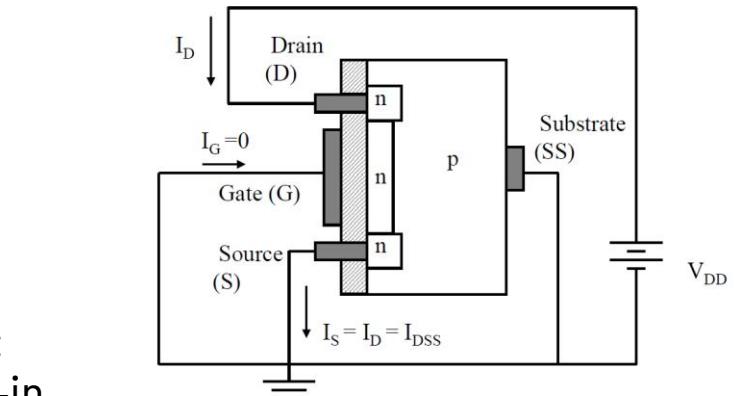
D-MOSFET

- The reason for the label metal-oxide-semiconductor FET is fairly obvious: metal for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the oxide for the silicon dioxide insulating layer, and the semiconductor for the basic structure on which the n- and p-type regions are diffused.
- The D-MOSFET almost works the same way as the JFET. When $V_{GS} = 0$, the drain current is designated as I_{DSS} . If V_{GS} is decreased, a lower V_{DD} is required to saturate the transistor.
- Also if V_{GS} is made less than zero and gradually decreased, the channel depletes and this is called the depletion-mode of the transistor.
- This depletion of channel and will stop until it reach its pinch-off voltage.
- Shockley's equation is the transfer equation of a D-MOSFET.
- When V_{GS} is made greater than zero, the channel of the transistor widens thus increasing the V_{DS} required to saturate the transistor. This mode is called the enhancement mode of operation.

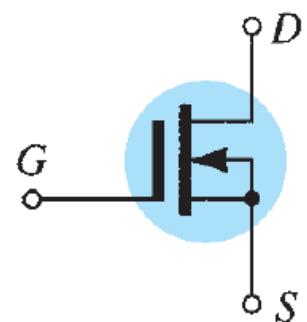
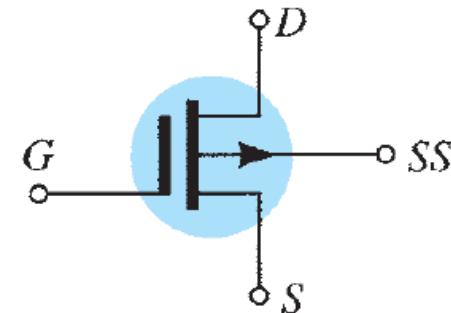
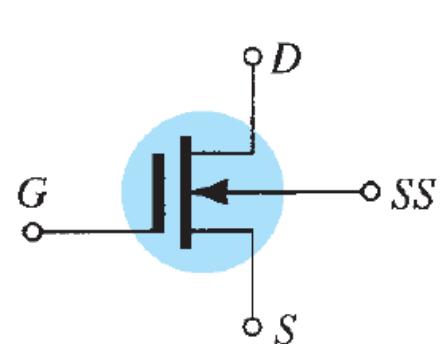


D-MOSFET

- The reason for the label metal-oxide-semiconductor FET is fairly obvious: **metal** for the **drain**, **source**, and **gate** connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the **oxide** for the **silicon dioxide** insulating layer, and the semiconductor for the basic structure on which the n- and p-type regions are diffused.
- The **D-MOSFET** almost works the **same way** as the **JFET**. When $V_{GS} = 0$, the **drain current** is designated as I_{DSS} . If V_{GS} is decreased, a lower V_{DD} is required to **saturate the transistor**.
- Also if V_{GS} is **made less than zero** and **gradually decreased**, the **channel depletes** and this is called the **depletion-mode** of the transistor.
- This **depletion of channel** and will stop **until it reach its pinch-off voltage**.
- Shockley's equation is the transfer equation of a D-MOSFET.
- When V_{GS} is made greater than zero, the **channel of the transistor widens** thus **increasing the V_{DS}** required to **saturate the transistor**. This mode is called the **enhancement mode** of operation.

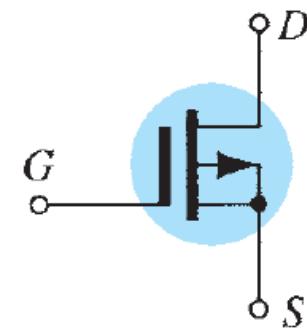


D-MOSFET



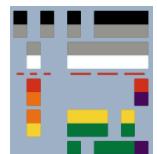
(a)

N-Channel



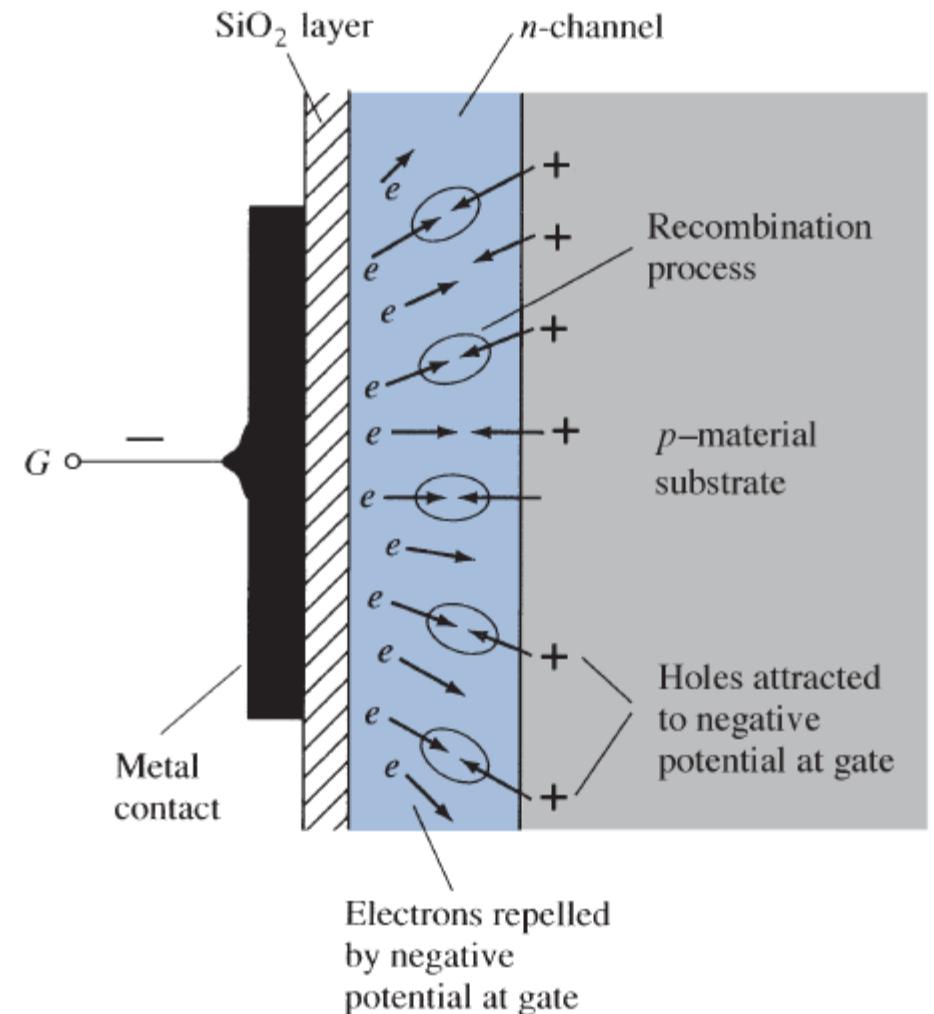
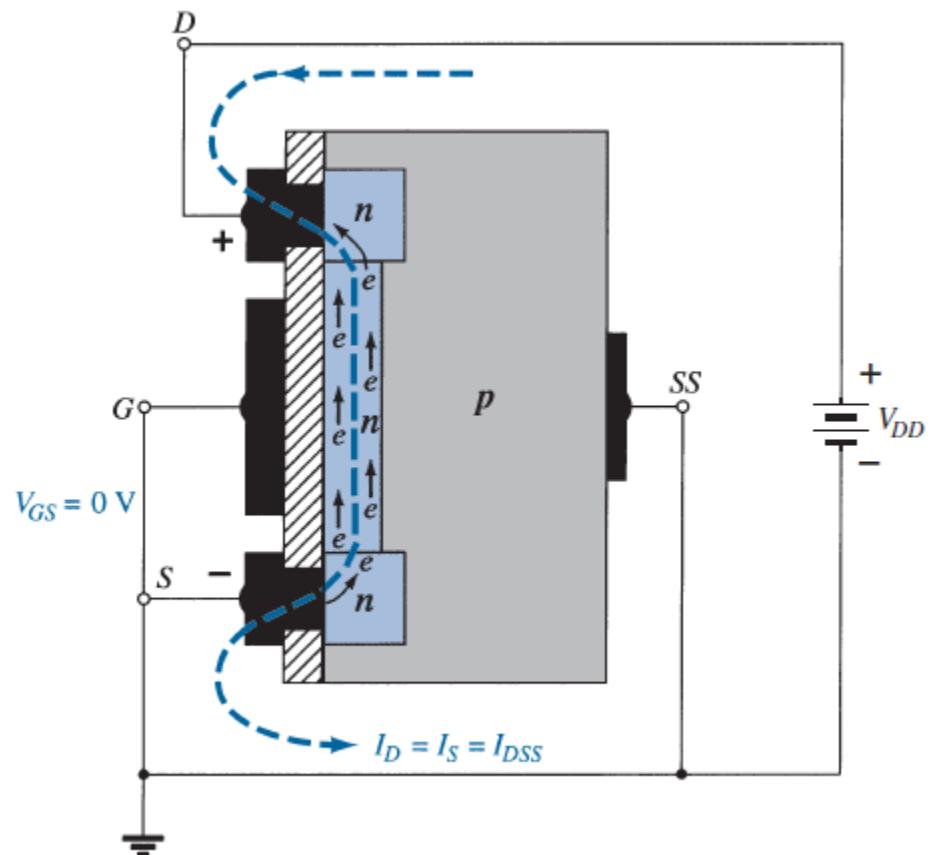
(b)

P-Channel

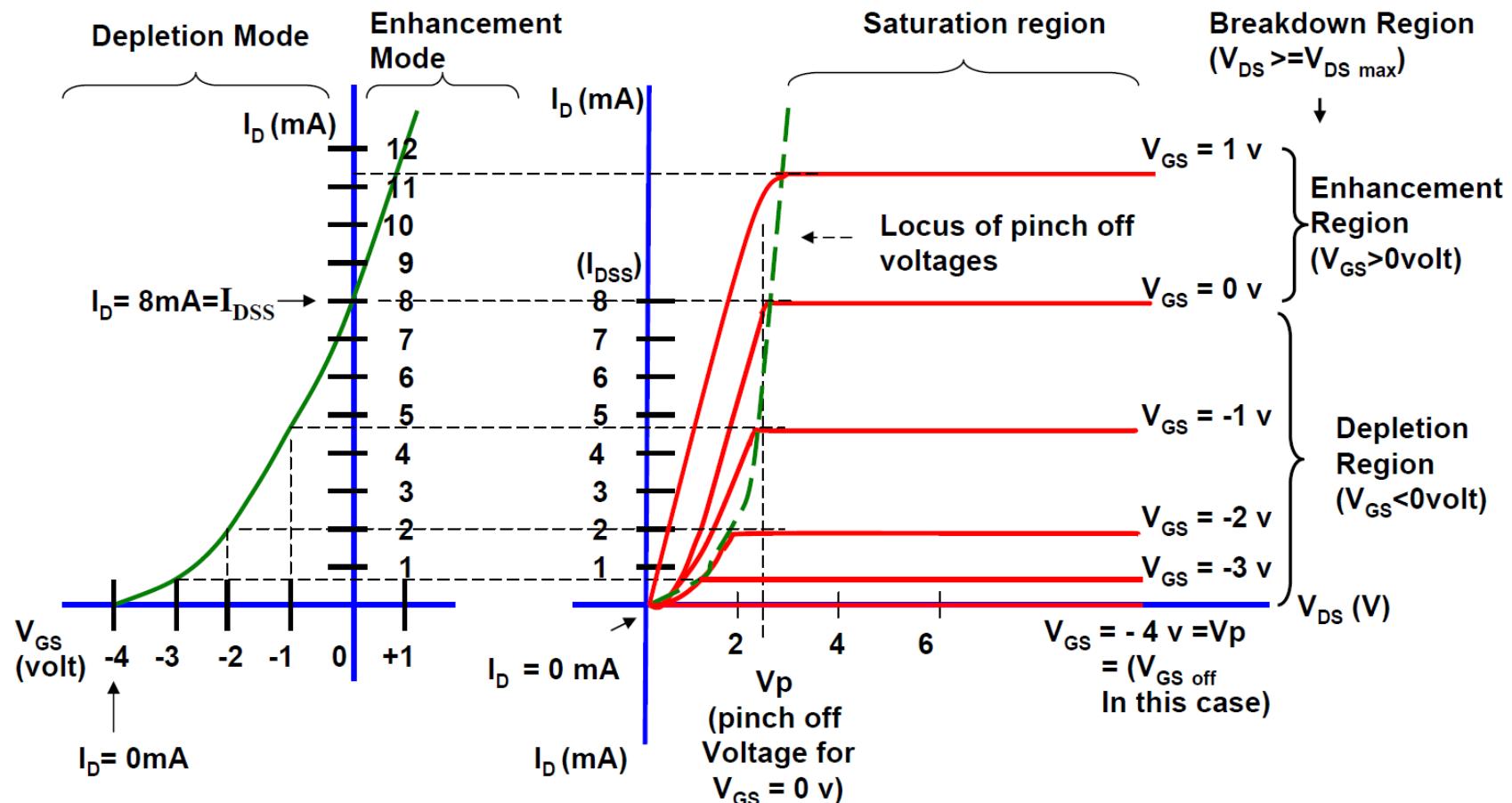


D-MOSFET

- Basic Operation and Characteristics



D-MOSFET



The region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region*.

D-MOSFET

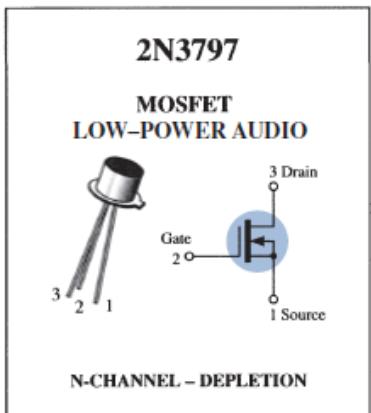
- Specification sheets

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage 2N3797	V_{DS}	20	Vdc
Gate-Source Voltage	V_{GS}	± 10	Vdc
Drain Current	I_D	20	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	200 1.14	mW mW/C
Junction Temperature Range	T_J	+175	°C
Storage Channel Temperature Range	T_{sg}	-65 to +200	°C

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain Source Breakdown Voltage ($V_{GS} = -7.0 \text{ V}$, $I_D = 5.0 \mu\text{A}$)	$V_{(BR)DSX}$	20	25	—	Vdc
Gate Reverse Current (1) ($V_{GS} = -10 \text{ V}$, $V_{DS} = 0$) ($V_{GS} = -10 \text{ V}$, $V_{DS} = 0$, $T_A = 150^\circ\text{C}$)	I_{GSS}	—	—	1.0 200	pAdc
Gate Source Cutoff Voltage ($I_D = 2.0 \mu\text{A}$, $V_{DS} = 10 \text{ V}$)	$V_{GS(off)}$	—	-5.0	-7.0	Vdc
Drain-Gate Reverse Current (1) ($V_{DG} = 10 \text{ V}$, $I_S = 0$)	I_{DGO}	—	—	1.0	pAdc
ON CHARACTERISTICS					
Zero-Gate-Voltage Drain Current ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$)	I_{DSS}	2.0	2.9	6.0	mAdc
On-State Drain Current ($V_{DS} = 10 \text{ V}$, $V_{GS} = +3.5 \text{ V}$)	$I_{D(on)}$	9.0	14	18	mAdc



ON CHARACTERISTICS

Zero-Gate-Voltage Drain Current
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$)

2N3797	I_{DSS}	2.0	2.9	6.0	mAdc
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On-State Drain Current
($V_{DS} = 10 \text{ V}$, $V_{GS} = +3.5 \text{ V}$)

2N3797	$I_{D(on)}$	9.0	14	18	mAdc
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SMALL-SIGNAL CHARACTERISTICS

Forward Transfer Admittance
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)

2N3797	$ y_{fs} $	1500	2300	3000	μmhos
--------	------------	------	------	------	------------------

($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)

2N3797	$ y_{fs} $	1500	—	—	μmhos
--------	------------	------	---	---	------------------

Output Admittance
($I_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$)

2N3797	$ y_{os} $	—	27	60	μmhos
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Input Capacitance
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)

2N3797	C_{iss}	—	6.0	8.0	pF
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Reverse Transfer Capacitance
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ MHz}$)

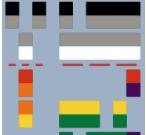
2N3797	C_{rss}	—	0.5	0.8	pF
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FUNCTIONAL CHARACTERISTICS

Noise Figure
($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1.0 \text{ kHz}$, $R_S = 3 \text{ megohms}$)

NF	—	3.8	—	dB
----	---	-----	---	----

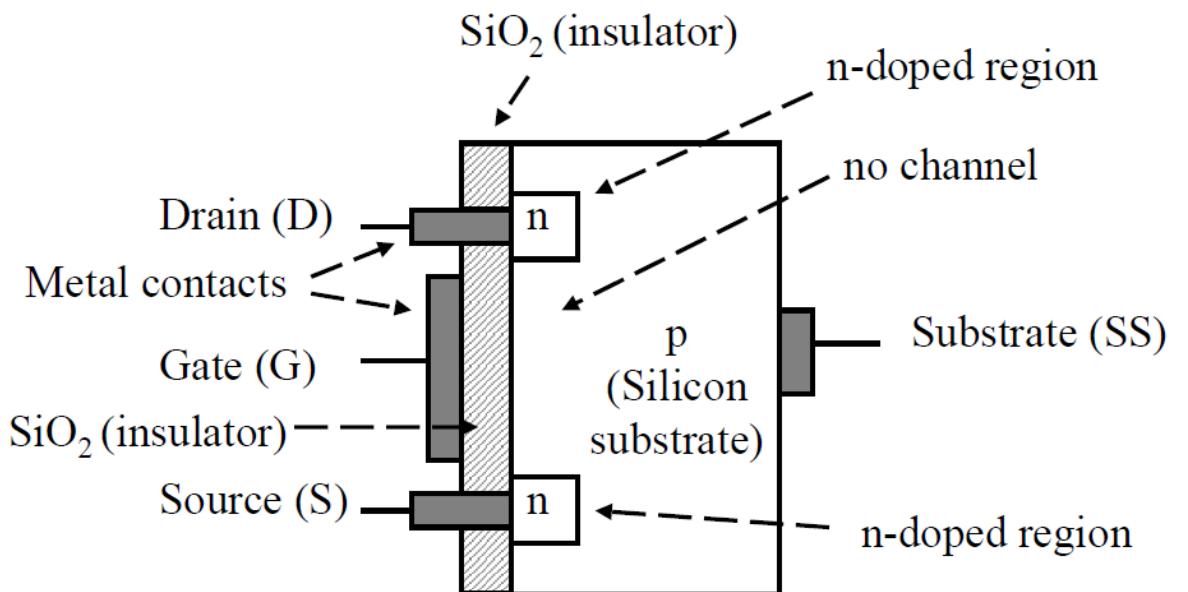
(1) This value of current includes both the FET leakage current as well as the leakage current associated with the test socket and fixture when measured under best attainable conditions.



Enhancement-Type MOSFET

Enhancement-Type MOSFET

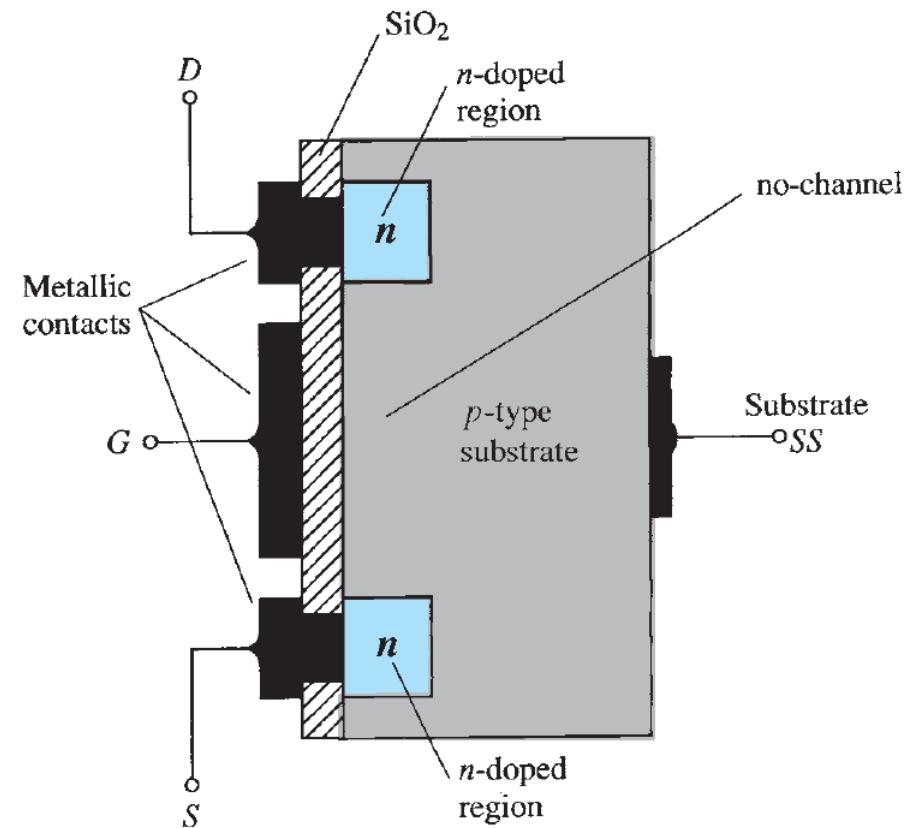
- Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far.
- The transfer curve is **not defined by Shockley's equation**, and the **drain current is now cut off until the gate-to-source voltage reaches a specific magnitude**.
- The construction of an enhancement-type MOSFET is quite **similar** to that of the depletion-type MOSFET, **except for the absence of a channel** between the drain and source terminals.



N-channel Enhancement Type MOSFET

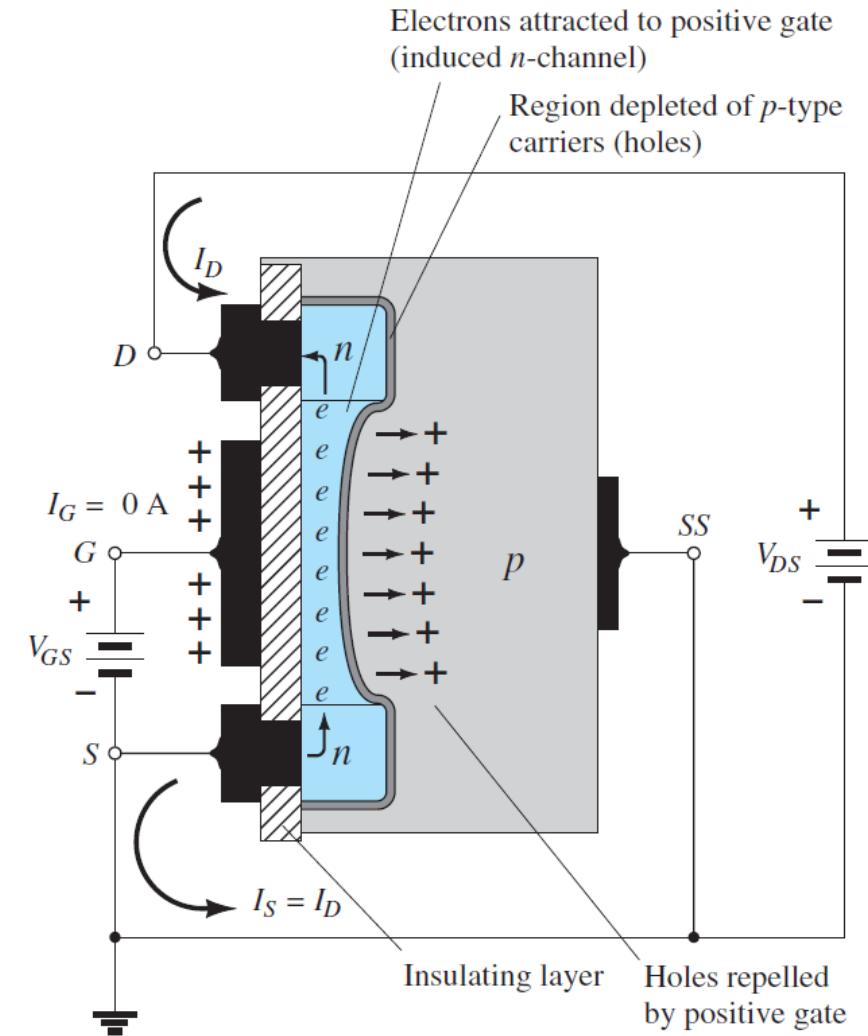
Enhancement-Type MOSFET

- If V_{GS} is set at 0 V and a voltage applied between the drain and the source of the device in the figure, the **absence of an n-channel** (with its generous number of free carriers) **will result in a current of effectively 0 A**—quite different from the depletion-type MOSFET and JFET, where $I_D = I_{DSS}$.
- It is **not sufficient** to have a **large accumulation** of carriers (**electrons**) at the **drain** and the **source** (due to the n-doped regions) **if a path fails to exist between the two**.
- With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal SS directly connected to the source, there are in fact two reverse-biased p-n junctions between the n-doped regions and the p-substrate to oppose any significant flow between drain and source.



Enhancement-Type MOSFET

- In the figure, both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and the gate at a positive potential with respect to the source.
- The positive potential at the gate will pressure the holes (since like charges repel) in the p-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the p-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the p-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer.



Enhancement-Type MOSFET

- The saturation of the transistor is related to V_{GS} by:

$$V_{DS_{SAT}} = V_{GS} - V_T$$

- The transfer characteristic is given by:

$$I_D = k (V_{GS} - V_T)^2$$
$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

Where:

V_{DSAT} = Gate to source saturation voltage

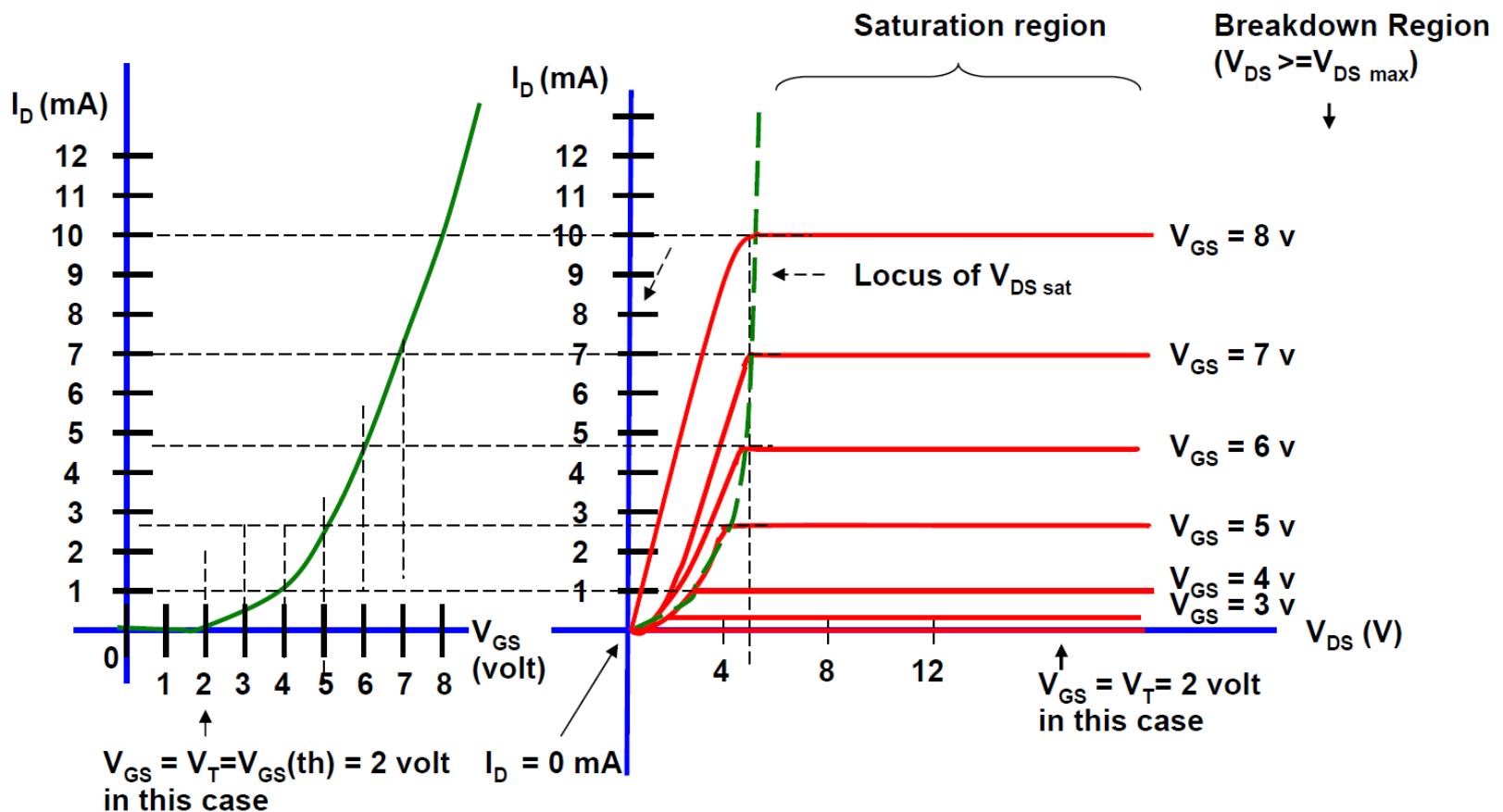
V_{GS} = Gate to source voltage

V_T = Gate to source threshold voltage

k = constant and a function of a particular device (A/V^2)

For values of V_{GS} less than the threshold level, the drain current of an enhancement type MOSFET is 0 mA.

Enhancement-Type MOSFET



Enhancement-Type MOSFET

- Specification sheets

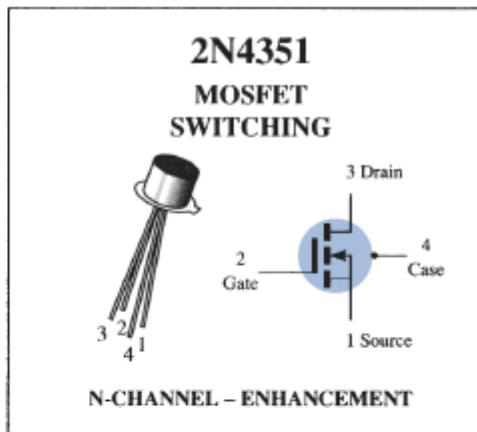
MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	30	Vdc
Gate-Source Voltage*	V_{GS}	30	Vdc
Drain Current	I_D	30	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	300 1.7	mW mW/ $^\circ\text{C}$
Junction Temperature Range	T_J	175	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +175	$^\circ\text{C}$

* Transient potentials of ± 75 Volt will not cause gate-oxide failure.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage ($I_D = 10 \mu\text{A}$, $V_{GS} = 0$)	$V_{(BR)DSX}$	25	-	Vdc
Zero-Gate-Voltage Drain Current ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$) $T_A = 25^\circ\text{C}$ $T_A = 150^\circ\text{C}$	I_{DSS}	- -	10 10	nAdc μAdc
Gate Reverse Current ($V_{GS} = \pm 15 \text{ Vdc}$, $V_{DS} = 0$)	I_{GSS}	-	± 10	pAdc



ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = 10 \text{ V}$, $I_D = 10 \mu\text{A}$)	$V_{GS(\text{Th})}$	1.0	5	Vdc
Drain-Source On-Voltage ($I_D = 2.0 \text{ mA}$, $V_{GS} = 10 \text{ V}$)	$V_{DS(\text{on})}$	-	1.0	V
On-State Drain Current ($V_{GS} = 10 \text{ V}$, $V_{DS} = 10 \text{ V}$)	$I_{D(\text{on})}$	3.0	-	mAdc

SMALL-SIGNAL CHARACTERISTICS

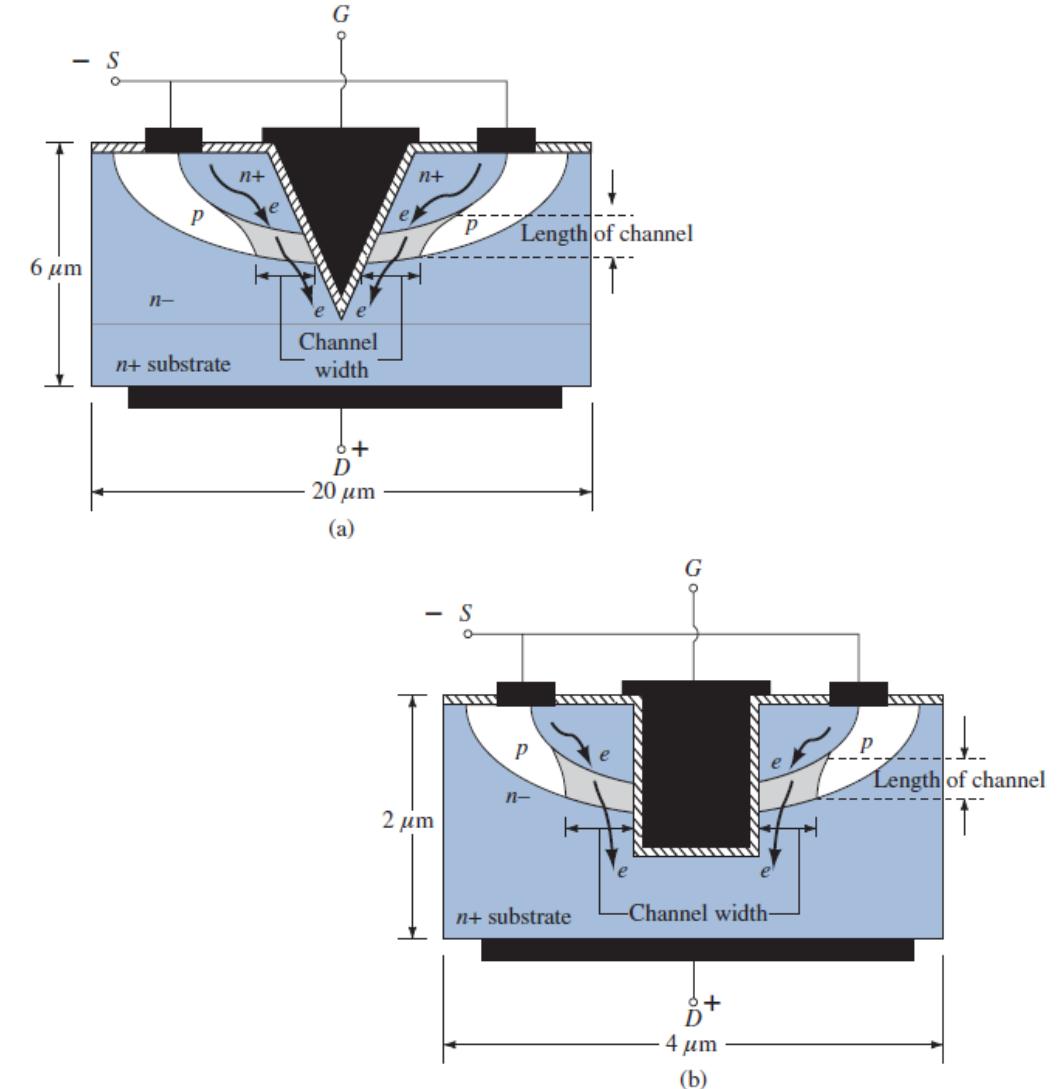
Forward Transfer Admittance ($V_{DS} = 10 \text{ V}$, $I_D = 2.0 \text{ mA}$, $f = 1.0 \text{ kHz}$)	$ y_{fs} $	1000	-	μmho
Input Capacitance ($V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 140 \text{ kHz}$)	C_{iss}	-	5.0	pF
Reverse Transfer Capacitance ($V_{DS} = 0$, $V_{GS} = 0$, $f = 140 \text{ kHz}$)	C_{rss}	-	1.3	pF
Drain-Substrate Capacitance ($V_{D(\text{SUB})} = 10 \text{ V}$, $f = 140 \text{ kHz}$)	$C_{d(\text{sub})}$	-	5.0	pF
Drain-Source Resistance ($V_{GS} = 10 \text{ V}$, $I_D = 0$, $f = 1.0 \text{ kHz}$)	$r_{ds(\text{on})}$	-	300	ohms

SWITCHING CHARACTERISTICS

Turn-On Delay (Fig. 5)	$I_D = 2.0 \text{ mA}, V_{DS} = 10 \text{ Vdc}, (V_{GS} = 10 \text{ Vdc})$ (See Figure 9; Times Circuit Determined)	t_{d1}	-	45	ns
Rise Time (Fig. 6)		t_r	-	65	ns
Turn-Off Delay (Fig. 7)		t_{d2}	-	60	ns
Fall Time (Fig. 8)		t_f	-	100	ns

VMOS And UMOS Power Mosfets

- **VMOS** (Vertical MOSFET) and **UMOS** (Trench MOSFET) are both types of power MOSFETs used in power electronics applications. VMOS has a lateral structure with the gate located on top of the device and the source and drain on opposite sides of the wafer. UMOS has a vertical structure with a trench etched into the silicon substrate, with the gate located in the trench and the source and drain on opposite sides of the trench. UMOS has a lower gate capacitance, faster switching speed, and lower on-resistance compared to VMOS, making it more suitable for high-frequency applications. However, VMOS has a higher current handling capability due to its lateral structure.



CMOS

CMOS (Complementary Metal-Oxide-Semiconductor) is a type of semiconductor technology widely used in digital circuits, such as microprocessors and memory chips. It utilizes both n-type and p-type MOSFETs to create low-power, high-performance digital circuits with high noise immunity and high integration density. This technology is based on the use of a combination of metal-oxide-semiconductor field-effect transistors (MOSFETs), which work in complementary pairs to allow for efficient switching between on and off states. CMOS technology is known for its low power consumption and compatibility with modern semiconductor manufacturing processes, making it a popular choice in many applications.

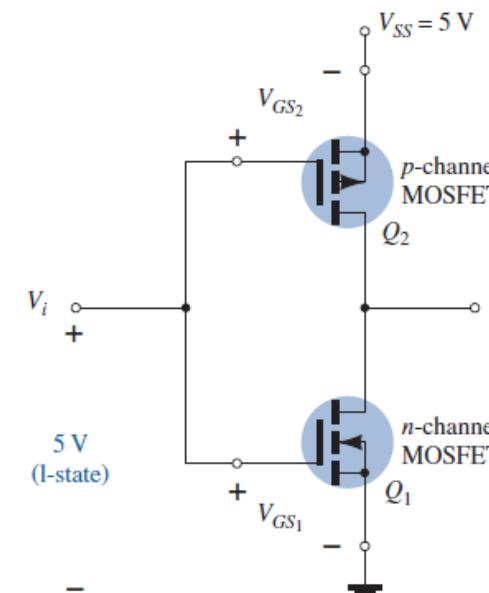
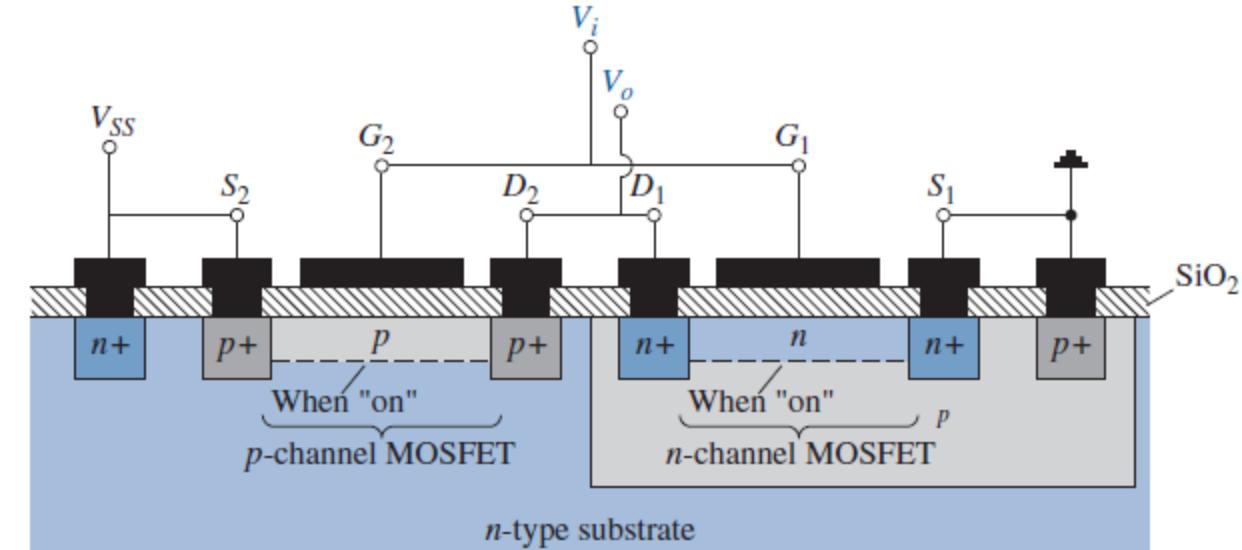


FIG. 45
CMOS inverter.

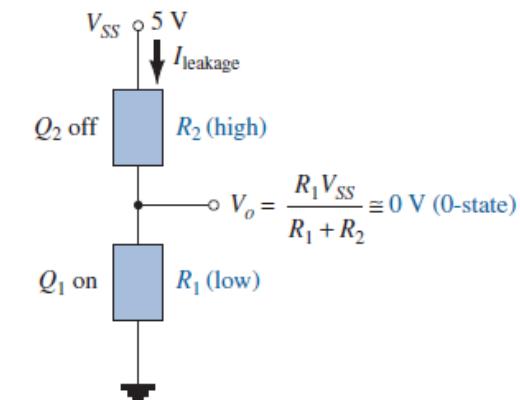


FIG. 46
Relative resistance levels for $V_i = 5 \text{ V}$ (I-state).

MESFETs

- MESFET stands for Metal Semiconductor Field Effect Transistor, which is a type of field-effect transistor that uses a metal-semiconductor junction for the gate. It is widely used in high-frequency electronic applications such as amplifiers and microwave devices.

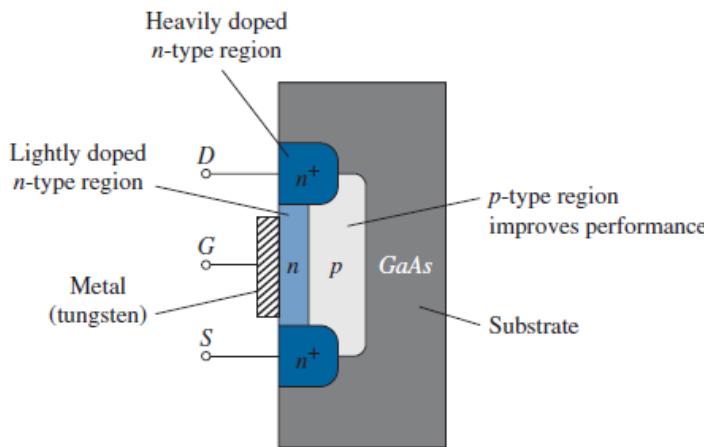


FIG. 47
Basic construction of an n-channel MESFET.

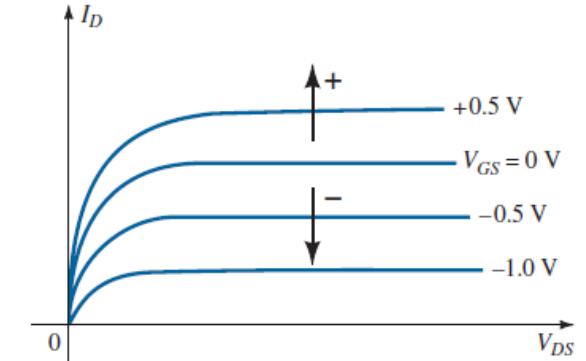


FIG. 48
Characteristics of an n-channel MESFET.

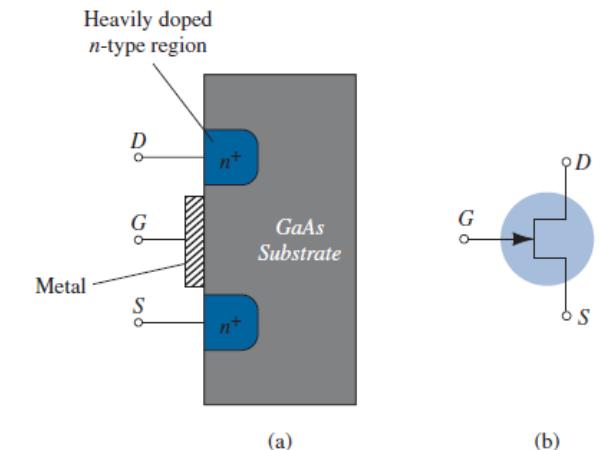
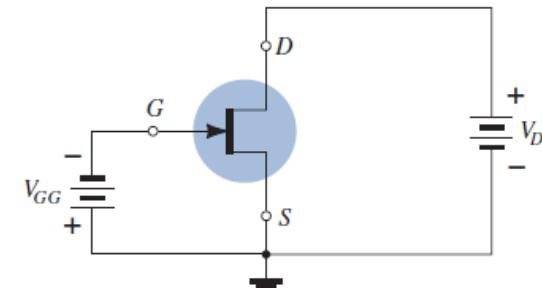
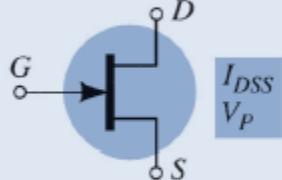
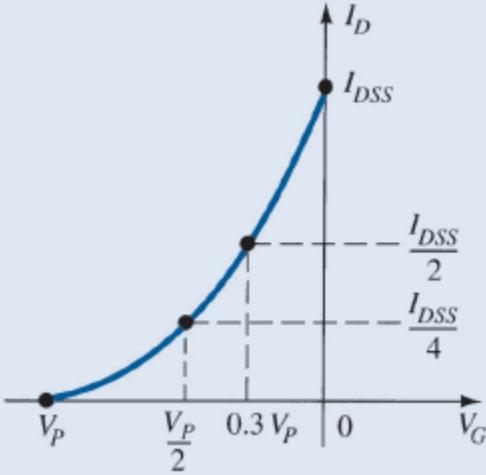
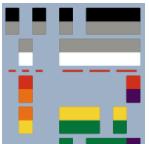


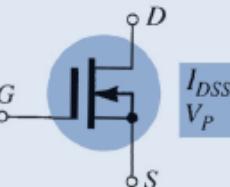
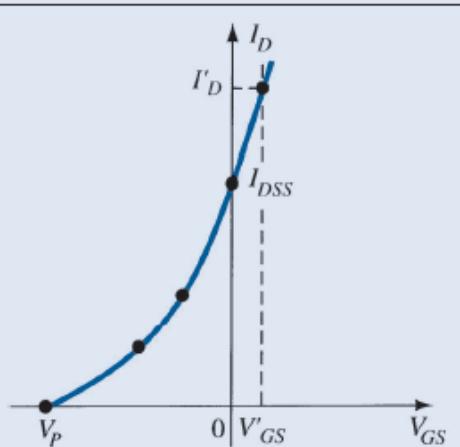
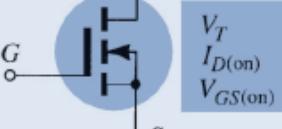
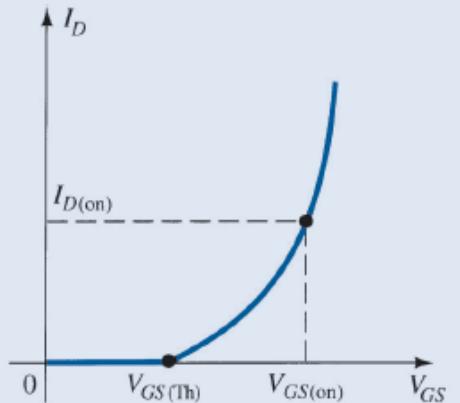
FIG. 50
Enhancement-type MESFET: (a) construction; (b) symbol.

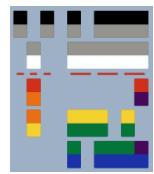
Summary Table

Type	Symbol and Basic Relationships	Transfer Curve	Input Resistance and Capacitance
JFET (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 100 \text{ M}\Omega$ $C_i: (1 - 10) \text{ pF}$

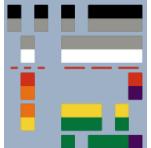


Summary Table

MOSFET depletion type (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$		$R_i > 10^{10} \Omega$ $C_i: (1 - 10) \text{ pF}$
MOSFET enhancement type (n-channel)	$I_G = 0 \text{ A}, I_D = I_S$  $I_D = k (V_{GS} - V_{GS(\text{Th})})^2$ $k = \frac{I_{D(\text{on})}}{(V_{GS(\text{on})} - V_{GS(\text{Th})})^2}$		$R_i > 10^{10} \Omega$ $C_i: (1 - 10) \text{ pF}$



FET Biasing



Introduction

- The controlling variable for a BJT transistor is a current level, whereas for the FET a voltage is the controlling variable.
- The general relationships that can be applied to the dc analysis of all FET amplifiers are

$$I_G \approx 0 \text{ A}$$

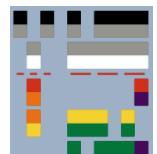
$$I_D = I_S$$

- JFET and D-MOSFET

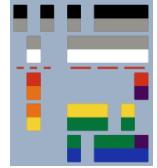
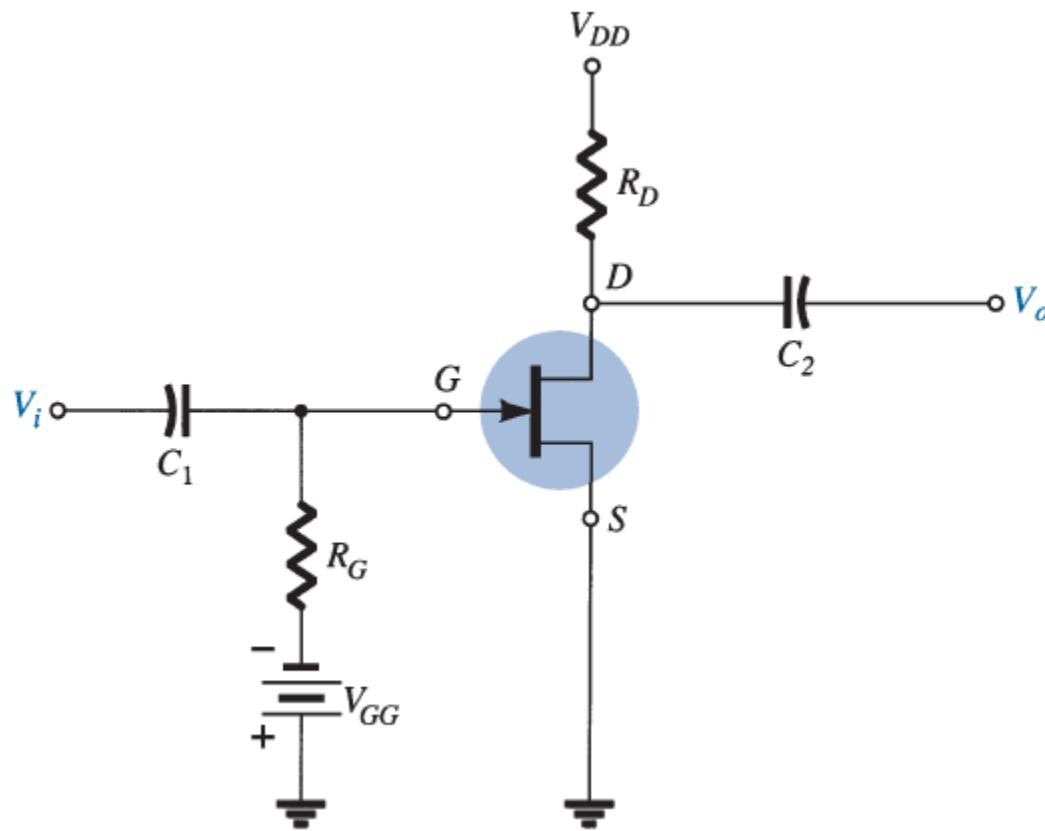
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

- E-MOSFET

$$I_D = k(V_{GS} - V_T)^2$$



Fixed Bias Configuration



Fixed Bias Configuration

- The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis.

$$I_G \approx 0A$$

$$V_{RG} = I_G R_G = (0 A) R_G = 0 V$$

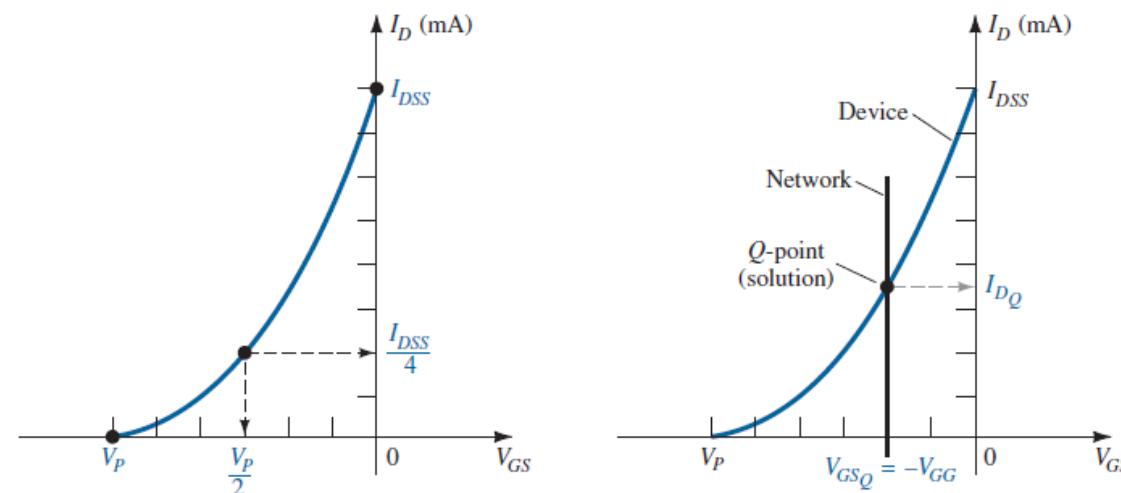
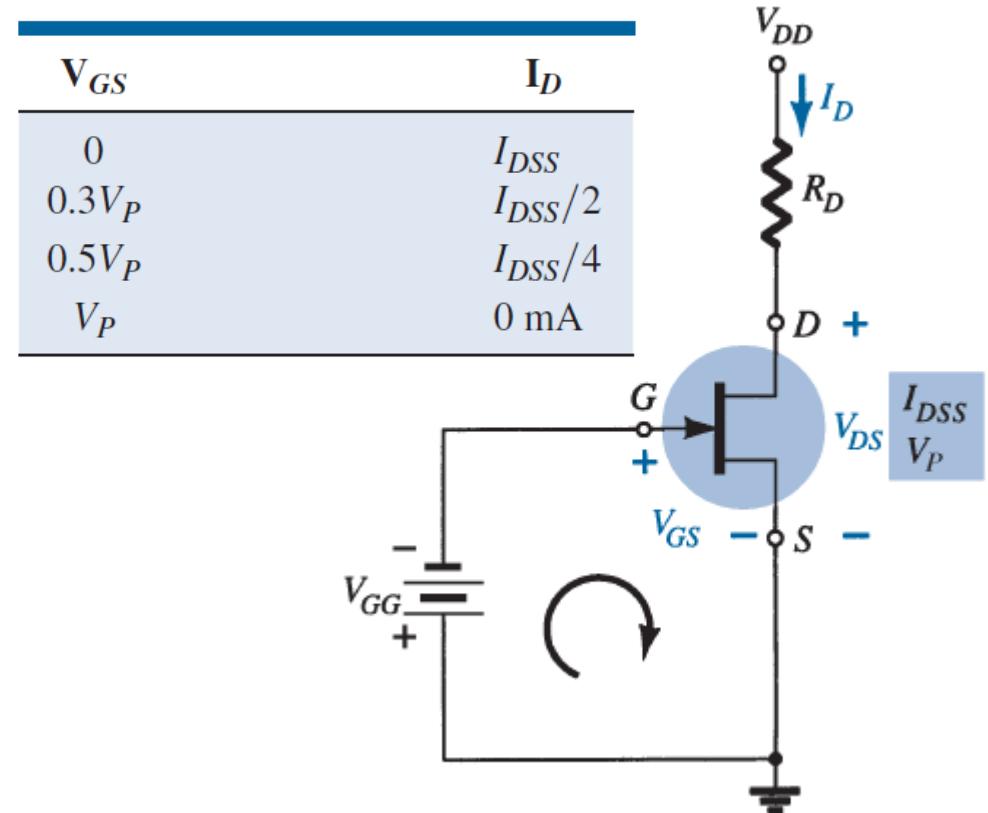
Applying Kirchhoff's voltage law in the clockwise direction gate source loop:

$$-V_{GG} - V_{GS} = 0 ; V_{GS} = -V_{GG}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the designation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$



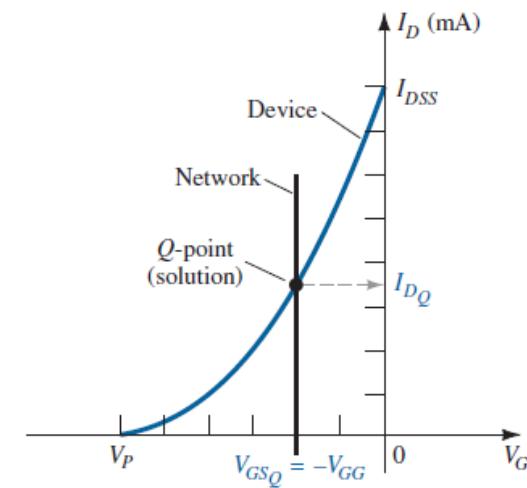
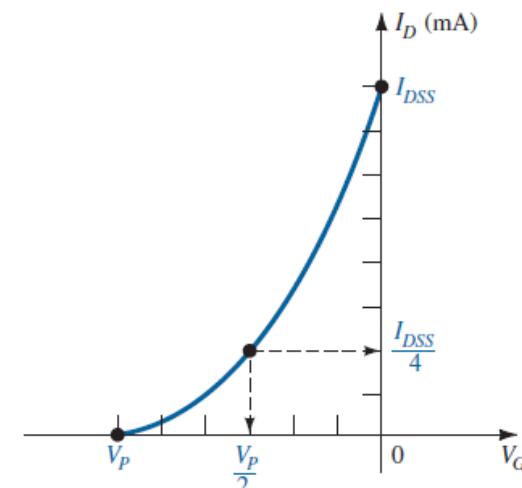
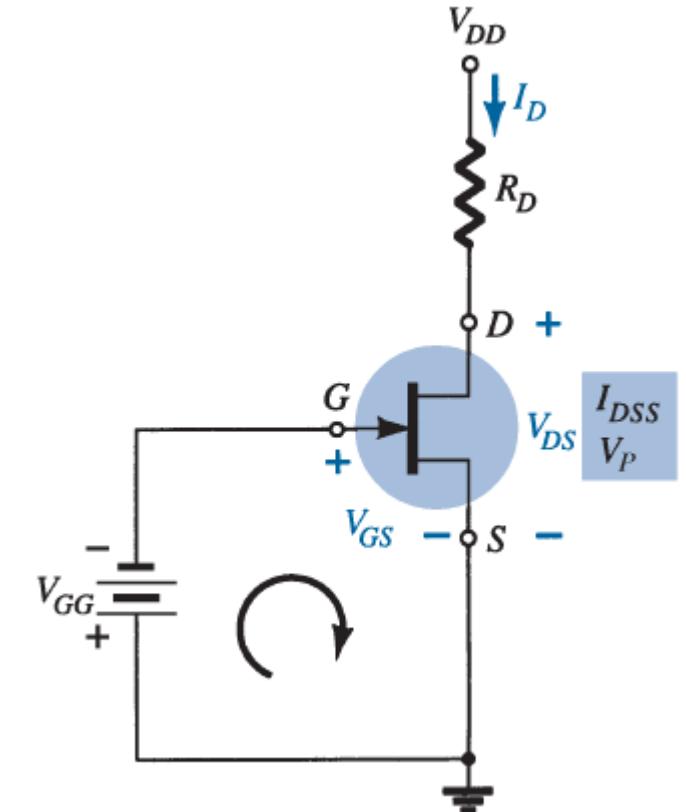
Fixed Bias Configuration

- The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

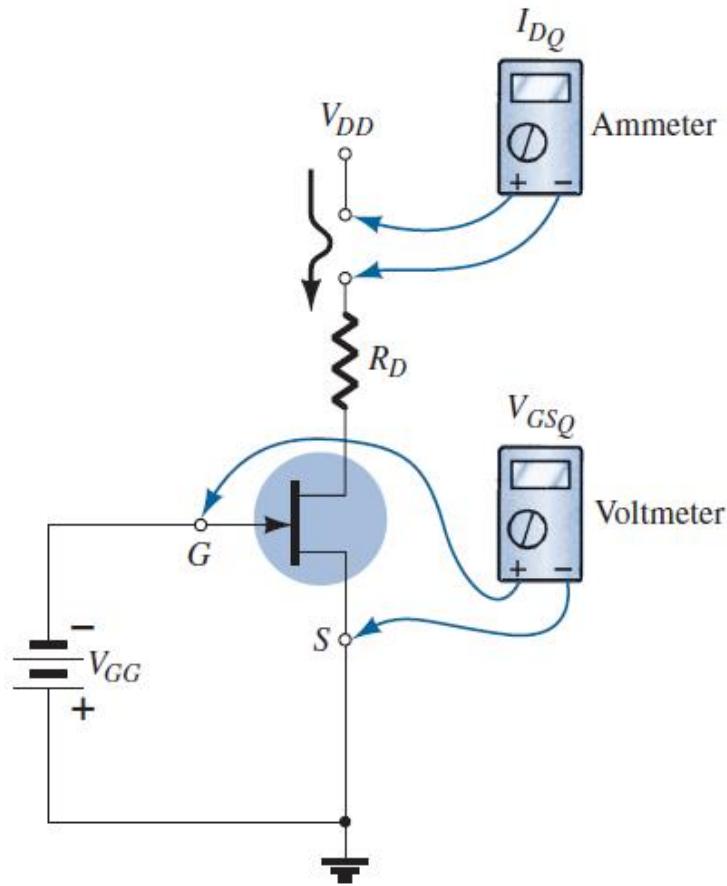
$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0; V_D = V_{DS}; V_G = V_{GS}$$

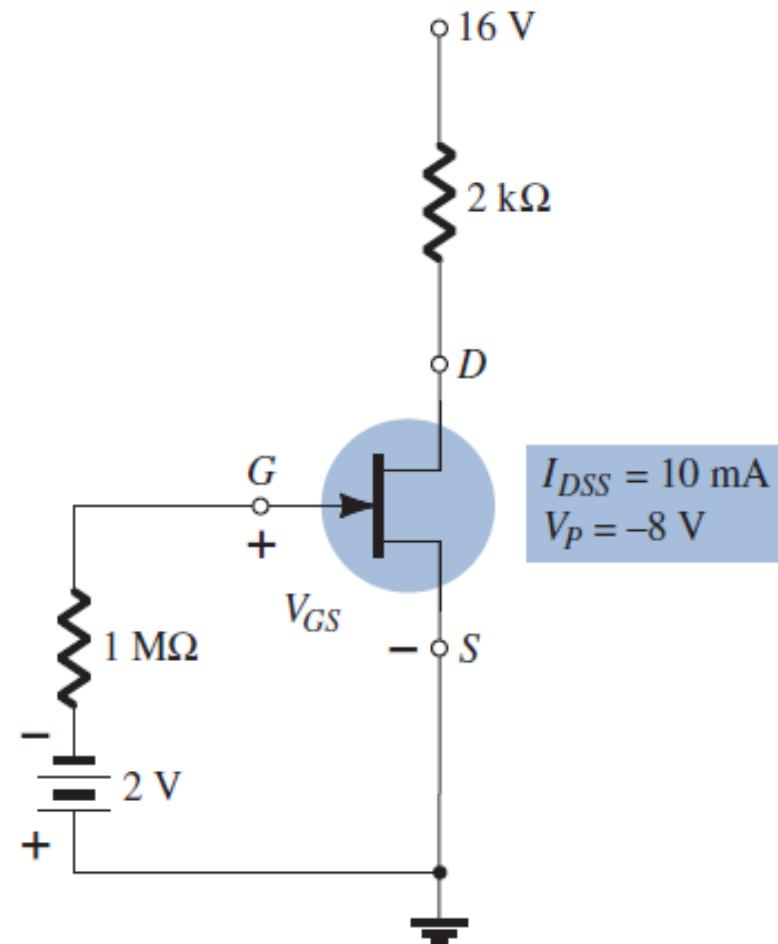


Fixed Bias Configuration



Fixed Bias Configuration

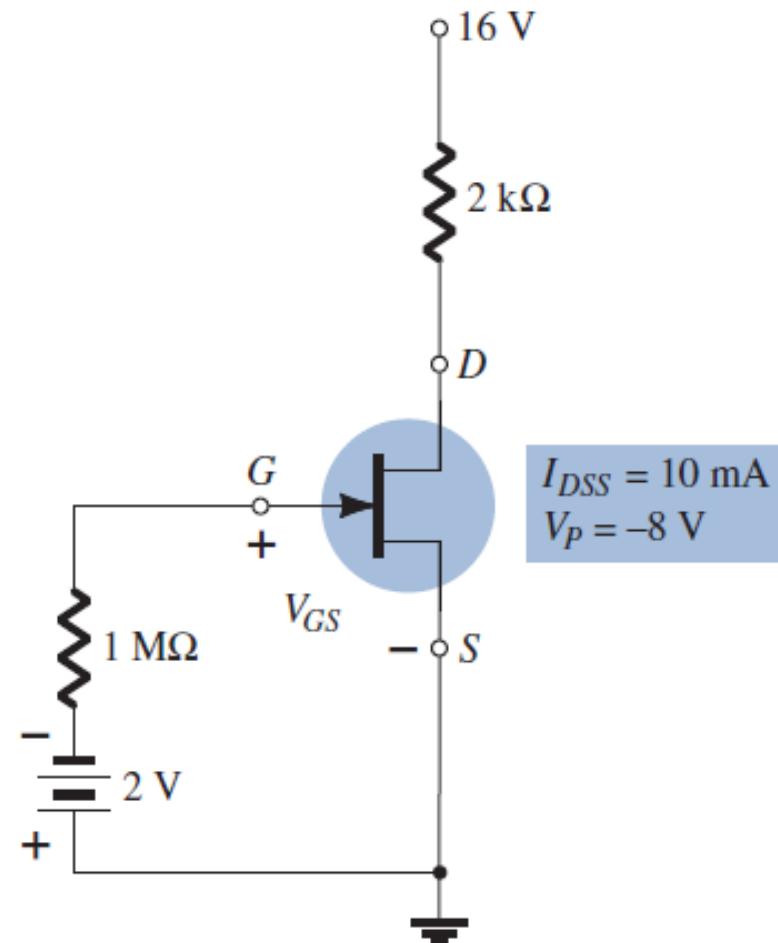
- Example Determine the following for the network
- a. V_{GSQ} .
- b. I_{DQ} .
- c. V_{DS} .
- d. V_D .
- e. V_G .
- f. V_S .



Fixed Bias Configuration

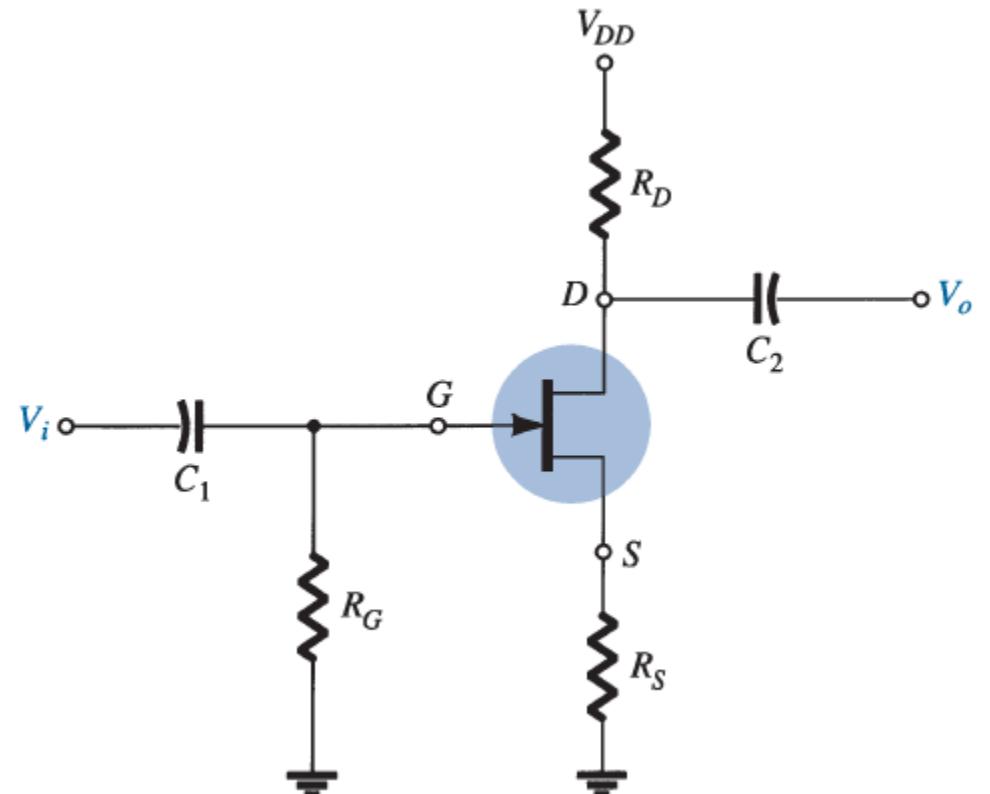
Solution

- a. $V_{GSQ} = -V_{GG} = -2V$
- b. $I_{DQ} = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 = 10mA \left[1 - \frac{-2V}{-8V} \right]^2 = 5.625mA$
- c. $V_{DS} = V_{DD} - I_D R_D = 16V - (5.625mA)(2k\Omega) = 4.75V$
- d. $V_D = V_{DS} = 4.75V$
- e. $V_G = V_{GS} = -2V$
- f. $V_S = 0V$



Self-bias Configuration

The self-bias configuration eliminates the need for two dc supplies. The controlling gate to source voltage is now determined by the voltage across a resistor RS introduced in the source leg of the configuration



Self-bias Configuration

- The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis.

$$I_G \approx 0A ; V_{RG} = 0V$$

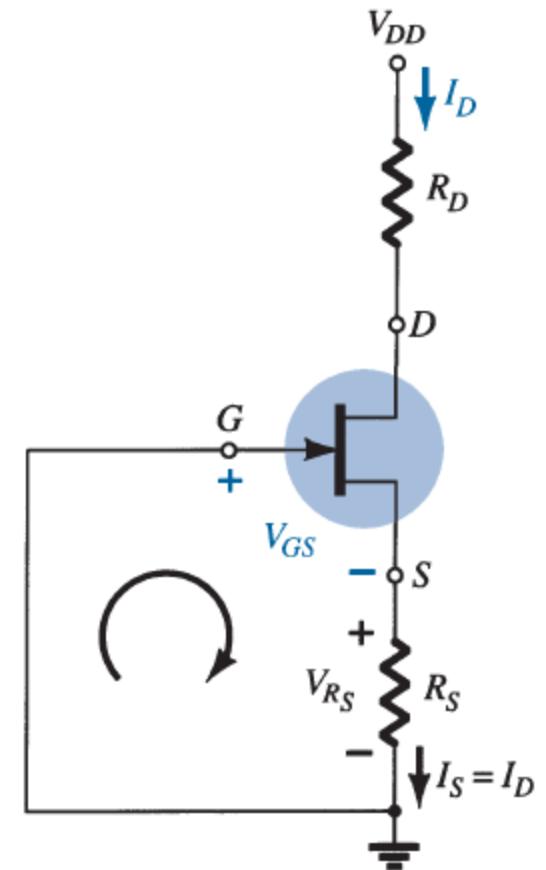
The current through R_S is the source current I_S , but $I_S = I_D$ and $V_{RS} = I_D R_S$

Applying Kirchhoff's voltage law in the clockwise direction gate source loop:

$$-V_{GS} - V_{RS} = 0 ; V_{GS} = -V_{RS} = V_{GS} = -I_D R_S$$

The resulting level of drain current I_D is now controlled by Shockley's equation:

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 ; I_D = I_{DSS} \left[1 + \frac{I_D R_S}{V_P} \right]^2$$



Self-bias Configuration

- The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

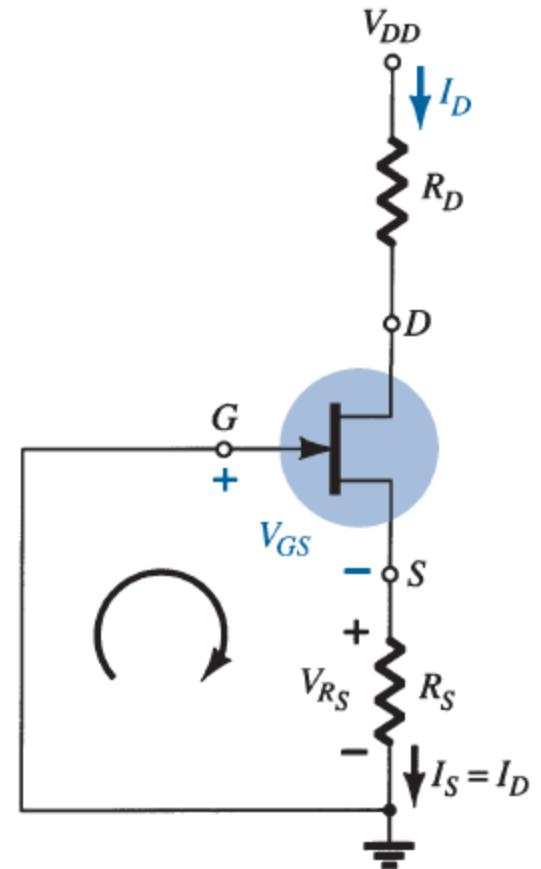
$$V_{DD} - I_D R_D - V_{DS} - V_{RS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

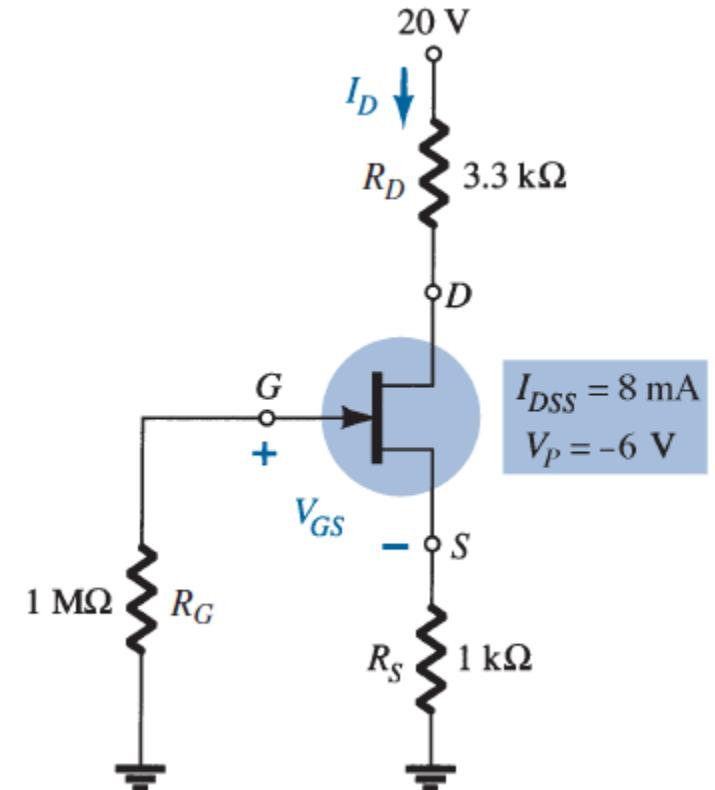
$$V_S = I_D R_S; V_G = 0$$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$



Self-bias Configuration

- Example Determine the following for the network
- a. V_{GSQ} .
- b. I_{DQ}
- c. V_{DS} .
- d. V_S .
- e. V_G .
- f. V_D .



Self-bias Configuration

- Example Determine the following for the network
- a. V_{GSQ} .
- b. I_{DQ}
- c. V_{DS} .
- d. V_S .
- e. V_G .
- f. V_D .

Solution: Using pure computation:

$$\begin{aligned} -V_{GS} - V_{RS} &= 0 \\ V_{GS} &= -V_{RS} = -I_D R_S \\ V_{GS} &= -I_D (1k\Omega) \\ I_D &= I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 \end{aligned}$$

Substitute the eq. of V_{GS}

$$I_D = 8mA \left[1 - \frac{-I_D(1k\Omega)}{-6V} \right]^2$$

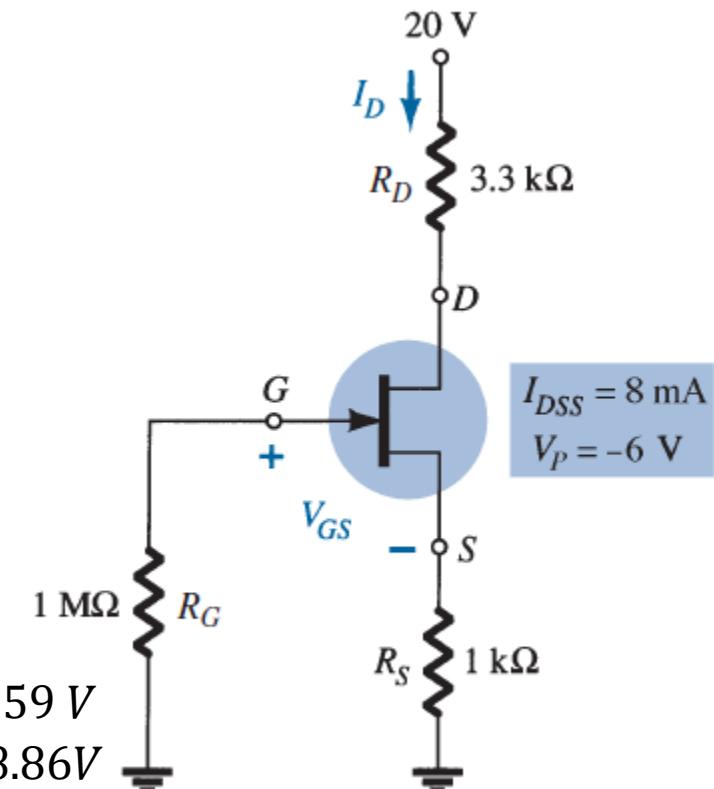
Using calculator:

$$\begin{aligned} I_D &= 2.59 \text{ mA} \\ V_{GS} &= -I_D (1k\Omega) = -2.59mA(1k\Omega) = -2.59 \text{ V} \\ V_{DS} &= 20V - (2.59mA)(3.3k\Omega + 1k\Omega) = 8.86V \end{aligned}$$

$$V_S = I_D R_S = 2.59V$$

$$V_G = 0V$$

$$V_D = V_{DS} + V_S = 8.86V + 2.59V = 11.45V$$



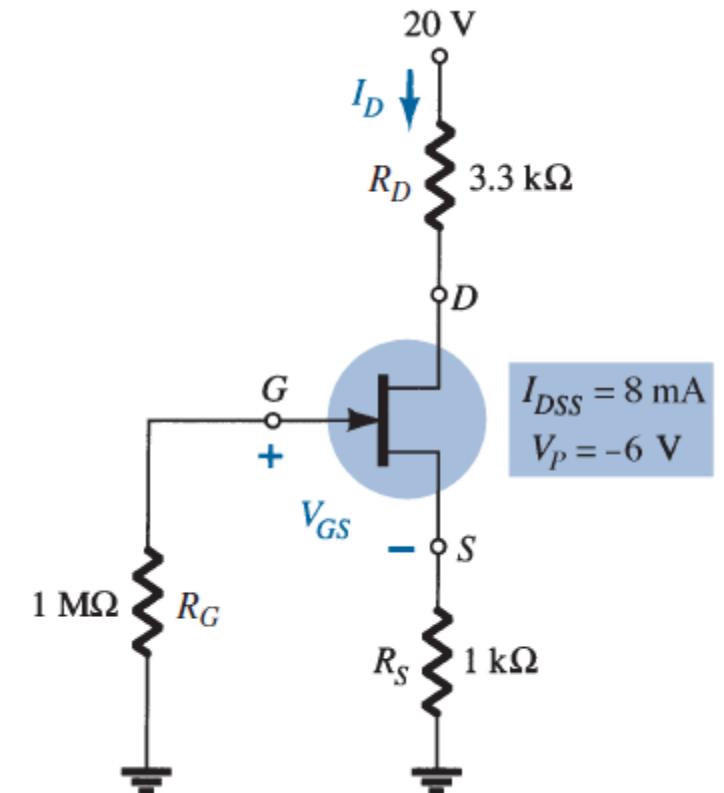
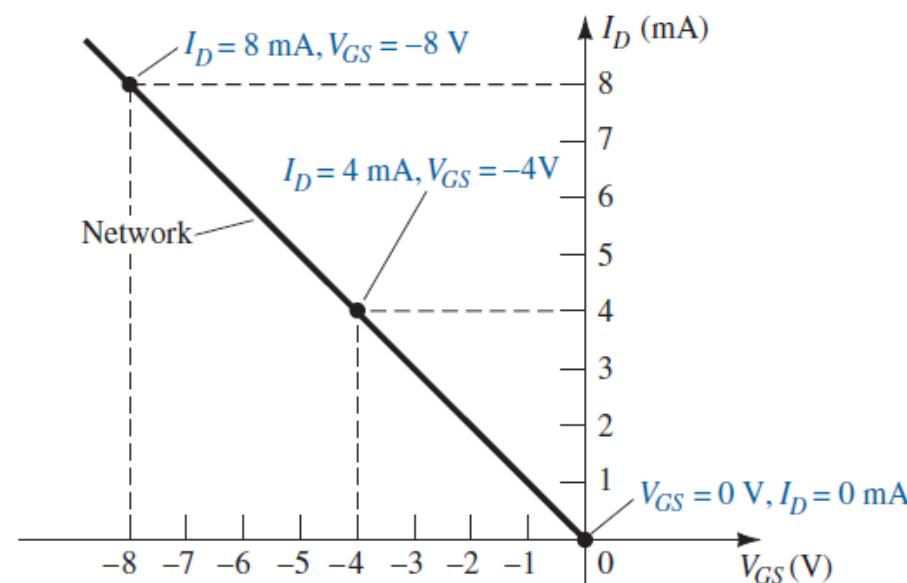
Self-bias Configuration

Solution

- a. $V_{GS0} = -I_D R_S$;

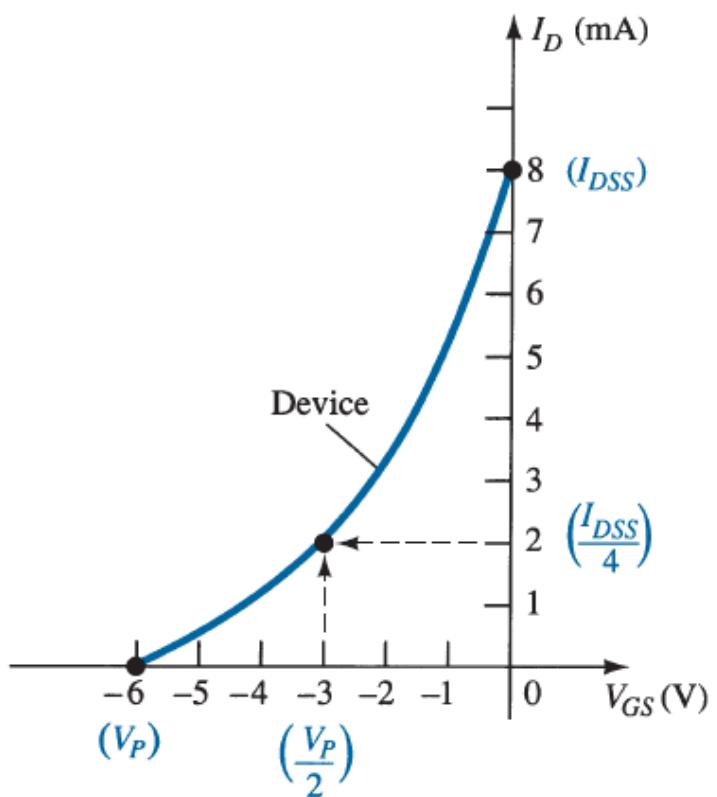
Choosing $I_D = 4 \text{ mA}$, we obtain $V_{GS} = -(4 \text{ mA})(1 \text{ k}\Omega) = -4 \text{ V}$

Choosing $I_D = 8 \text{ mA}$, we obtain $V_{GS} = -(8 \text{ mA})(1 \text{ k}\Omega) = -8 \text{ V}$

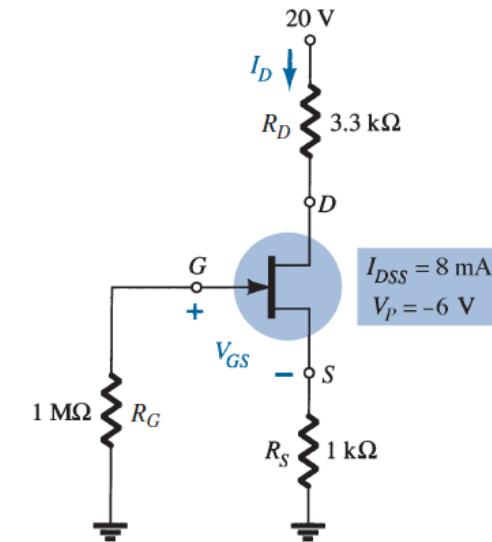
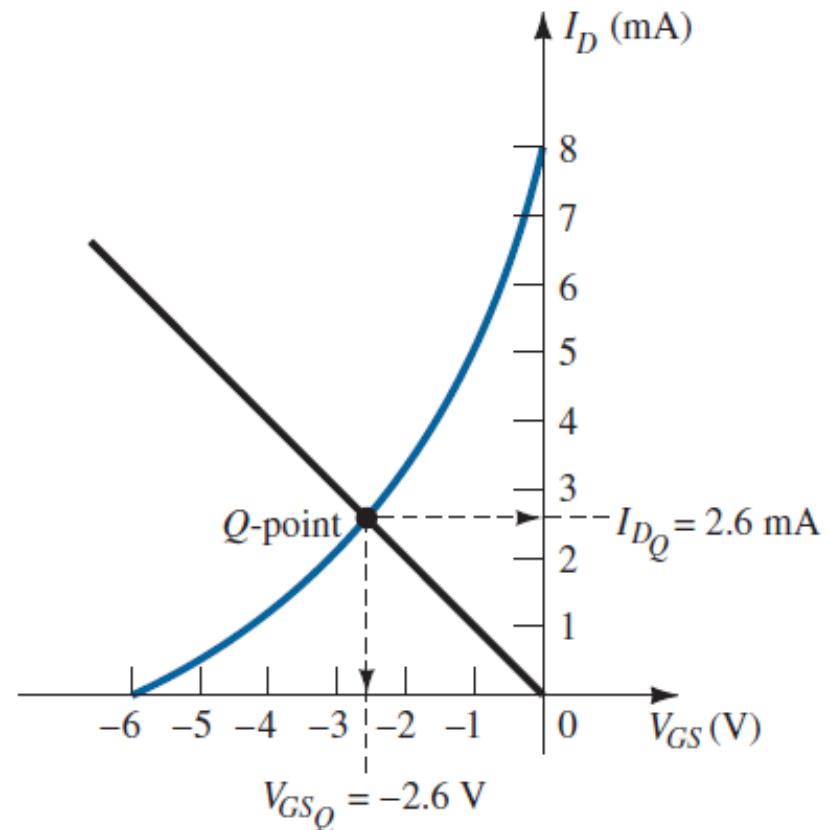


Self-bias Configuration

- $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$
- a. $V_{GSQ} = -2.6\text{V}$
- b. $I_{DQ} = 2.6\text{mA}$



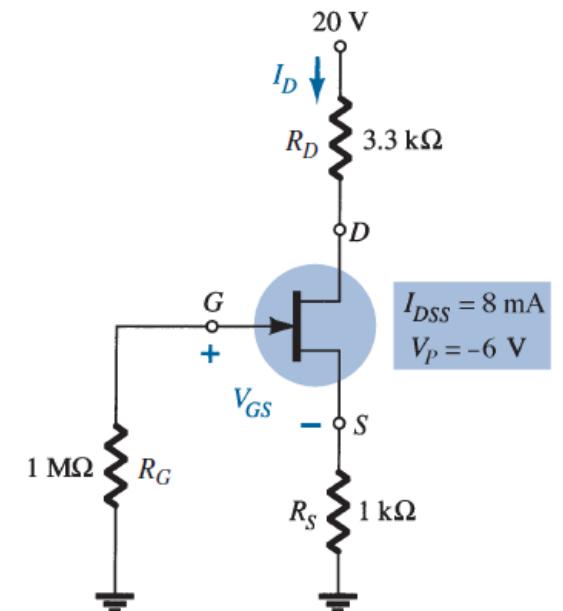
V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA



Self-bias Configuration

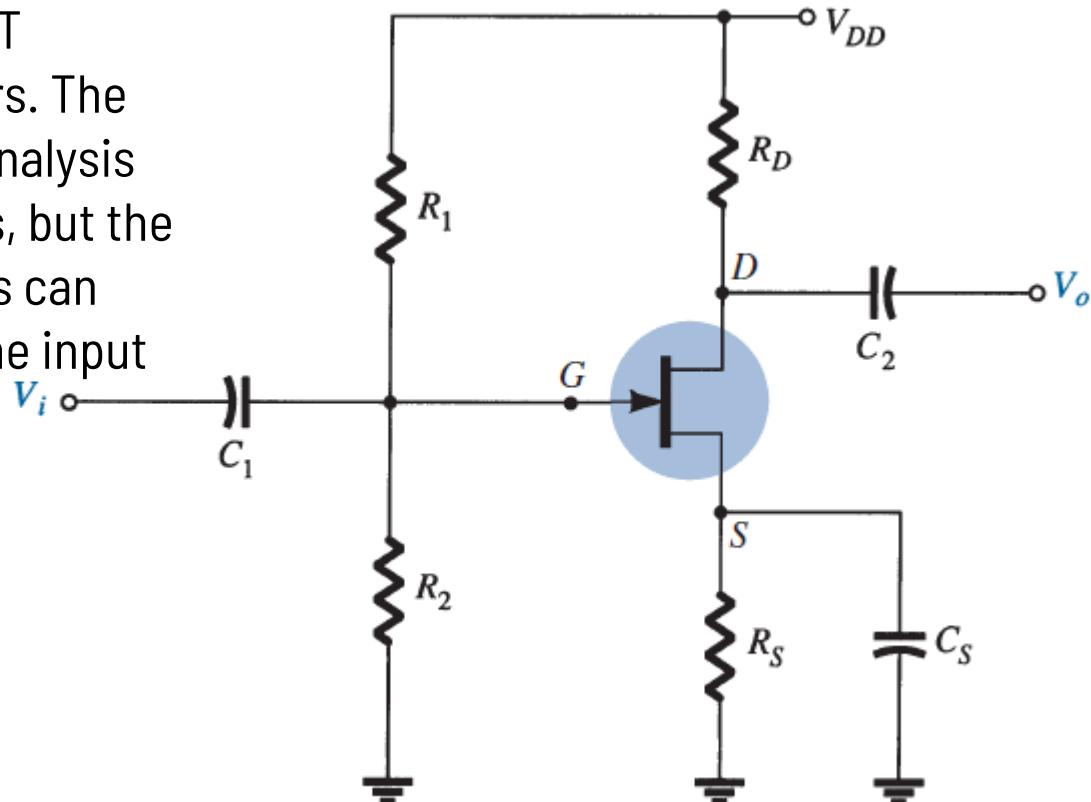
Solution

- c. $V_{DS} = V_{DD} - I_D(R_s + R_D) = 20V - (2.6mA)(1k\Omega + 3.3k\Omega) = 8.82V$
- d. $V_S = I_D R_S = (2.6mA)(1k\Omega) = 2.6V$
- e. $V_G = 0V$
- f. $V_D = V_{DS} + V_S = 8.82V + 2.6V = 11.42V$



Voltage-divider Biasing

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0 \text{ A}$ for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits.



Voltage-divider Biasing

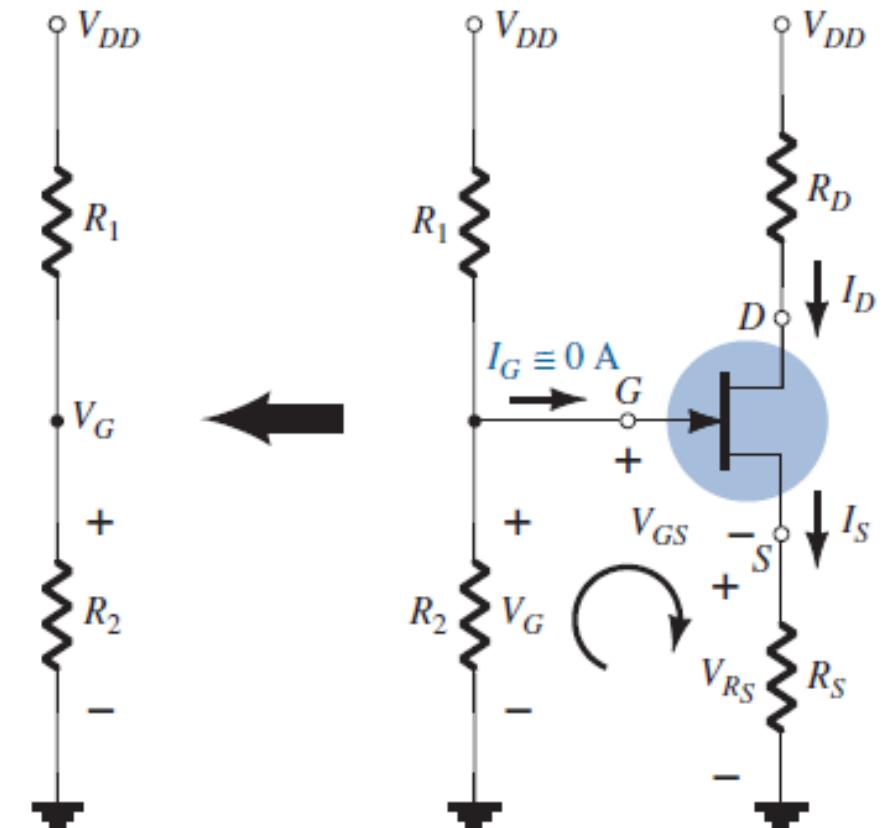
Since $I_G = 0 \text{ A}$, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$, and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G . The voltage V_G , equal to the voltage across R_2 , can be found using the voltage-divider rule

$$I_G \approx 0 \text{ A} ; V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law in the clockwise direction gate source loop:

$$\begin{aligned} V_G - V_{GS} - V_{RS} &= 0 ; V_{GS} = V_G - V_{RS} \\ &= V_{GS} = V_G - I_D R_S \end{aligned}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D .



Voltage-divider Biasing

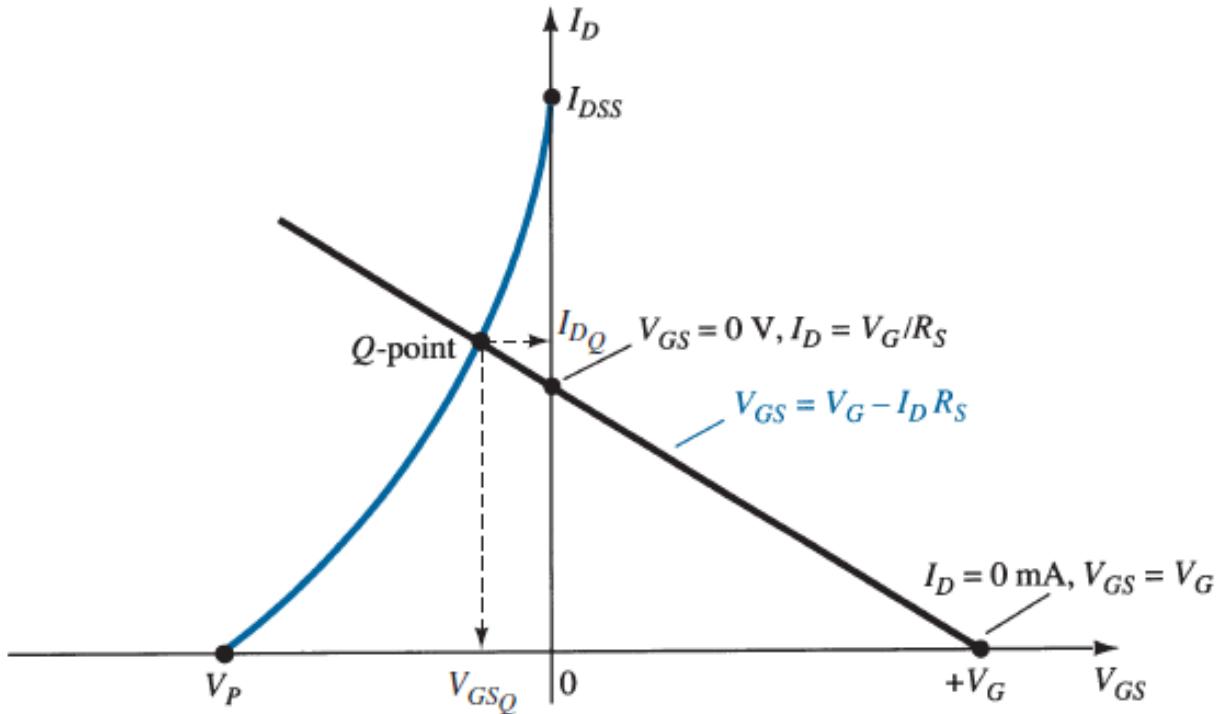
- $V_{GS} = V_G - I_D R_S = V_G - (0 \text{ mA})R_S$

$$V_{GS} = V_G \Big|_{I_D=0 \text{ mA}}$$

- $0V = V_G - I_D R_S$

$$I_D = \frac{V_G}{R_S} \Big|_{V_{GS}=0 \text{ V}}$$

- Increasing values of R_S result in lower quiescent values of I_D and declining values of V_{GS} .



Voltage-divider Biasing

- The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

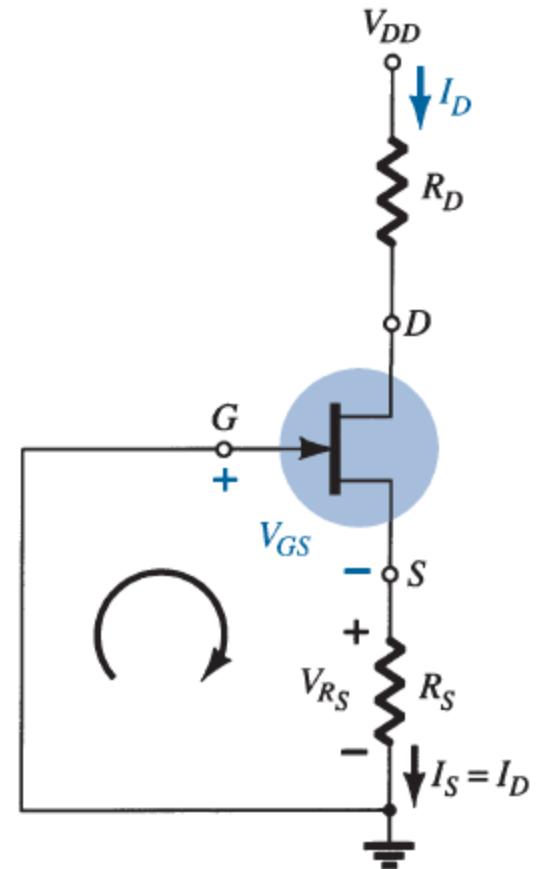
$$V_{DD} - I_D R_D - V_{DS} - V_{RS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

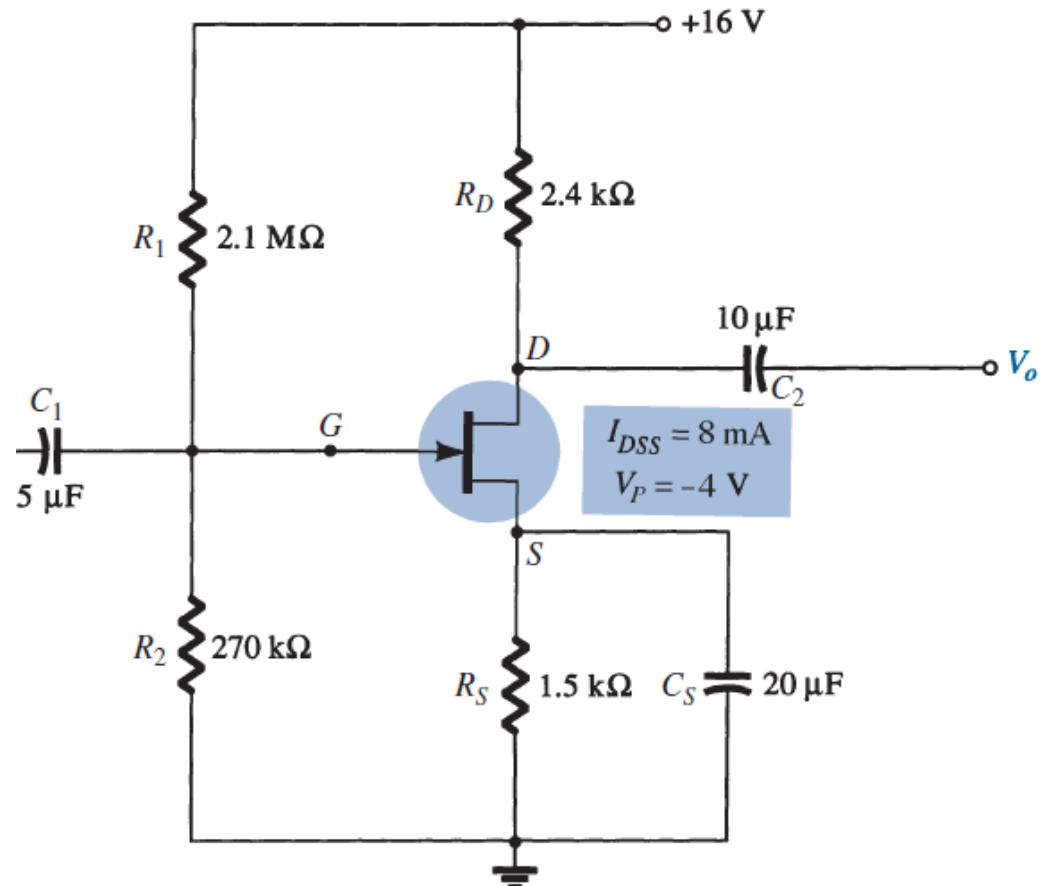
$$V_S = I_D R_S; \quad V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$V_D = V_{DS} + V_S = V_{DD} - I_D R_D$$



Voltage-divider Biasing

- Determine the following for the network
- a. I_{DQ} and V_{GSQ} .
- b. V_D .
- c. V_S .
- d. V_{DS} .
- e. V_{DG} .



Voltage-divider Biasing

- Determine the following for the network
- a. I_{DQ} and V_{GSQ} .
- b. V_D .
- c. V_S .
- d. V_{DS} .
- e. V_{DG} .

Solution: Using pure computation:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{16V(270k\Omega)}{2.1M\Omega + 270k\Omega} = 1.823V$$

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS} = V_G - I_D R_S$$

$$V_{GS} = 1.823V - I_D (1.5k\Omega)$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Substitute the eq. of V_{GS}

$$I_D = 8mA \left[1 - \frac{1.823V - I_D (1.5k\Omega)}{-4V} \right]^2$$

Using calculator:

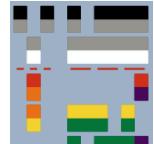
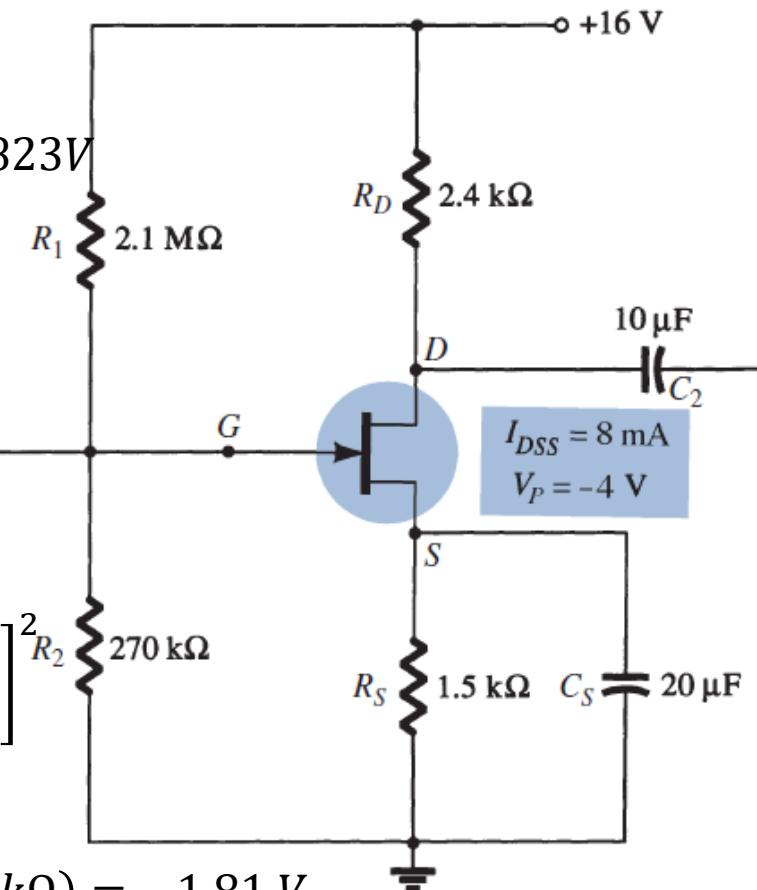
$$I_D = 2.42 \text{ mA}$$

$$V_{GS} = 1.822 - I_D (1.5k\Omega) = 1.822 - 2.42mA (1.5k\Omega) = -1.81V$$

$$V_D = V_{DD} - I_D R_D = 16V - I_D (2.4k\Omega) = 10.19V$$

$$V_S = I_D R_S = 2.42mA (1.5k\Omega) = 3.63V$$

$$V_{DS} = V_D - V_S = 10.19V - 3.63V = 8.37V$$



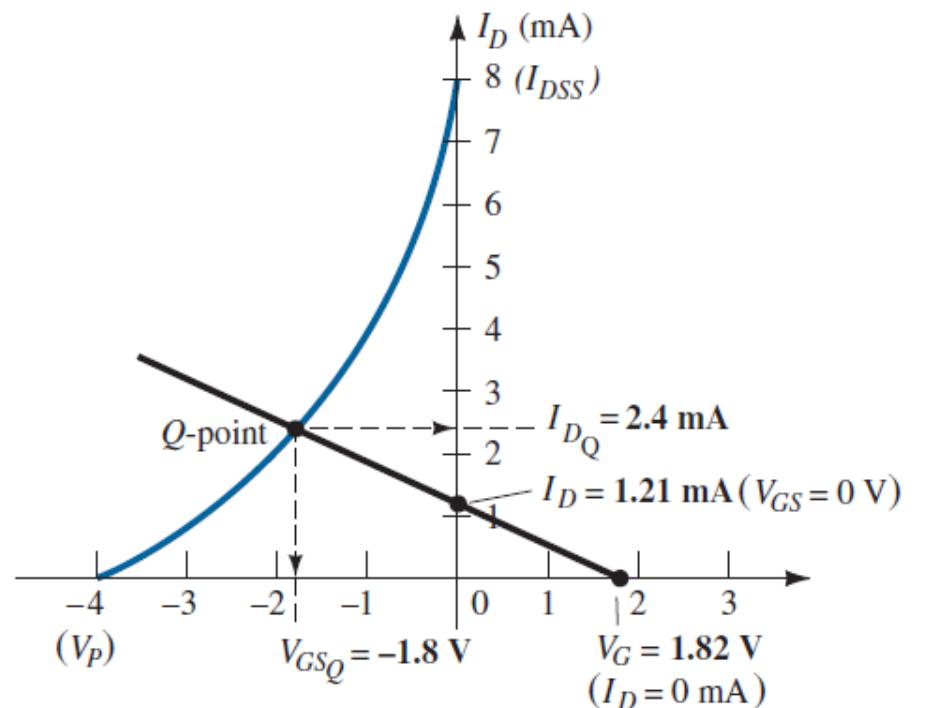
Voltage-divider Biasing

- For the transfer characteristics, if $I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA}$, then $V_{GS} = V_P/2 = -4 \text{ V}/2 = -2 \text{ V}$. The resulting curve representing Shockley's equation
The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(270 \text{ k}\Omega)(16 \text{ V})}{2.1 \text{ M}\Omega + 0.27 \text{ M}\Omega} = 1.82 \text{ V}$$

- $V_{GS} = V_G - I_D R_S = 1.82 \text{ V} - I_D(1.5 \text{ k}\Omega)$
- When $I_D = 0 \text{ mA}$, $V_{GS} = +1.82 \text{ V}$
- When $V_{GS} = 0 \text{ V}$, $\frac{1.82 \text{ V}}{1.5 \text{ k}\Omega} = 1.21 \text{ mA}$
- $I_{DQ} = 2.4 \text{ mA}$ and $V_{GSQ} = -1.8 \text{ V}$

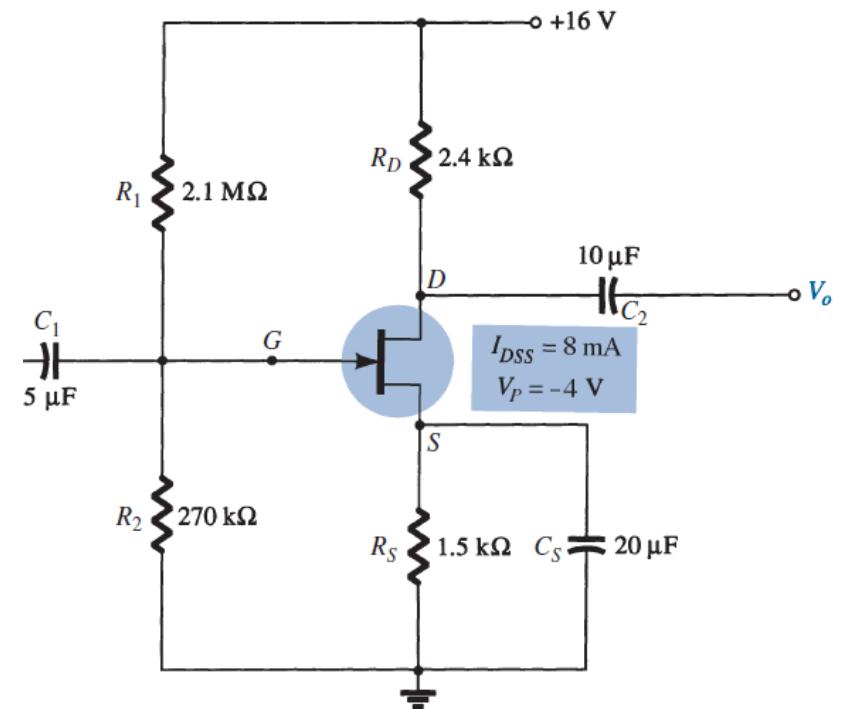
V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA



Voltage-divider Biasing

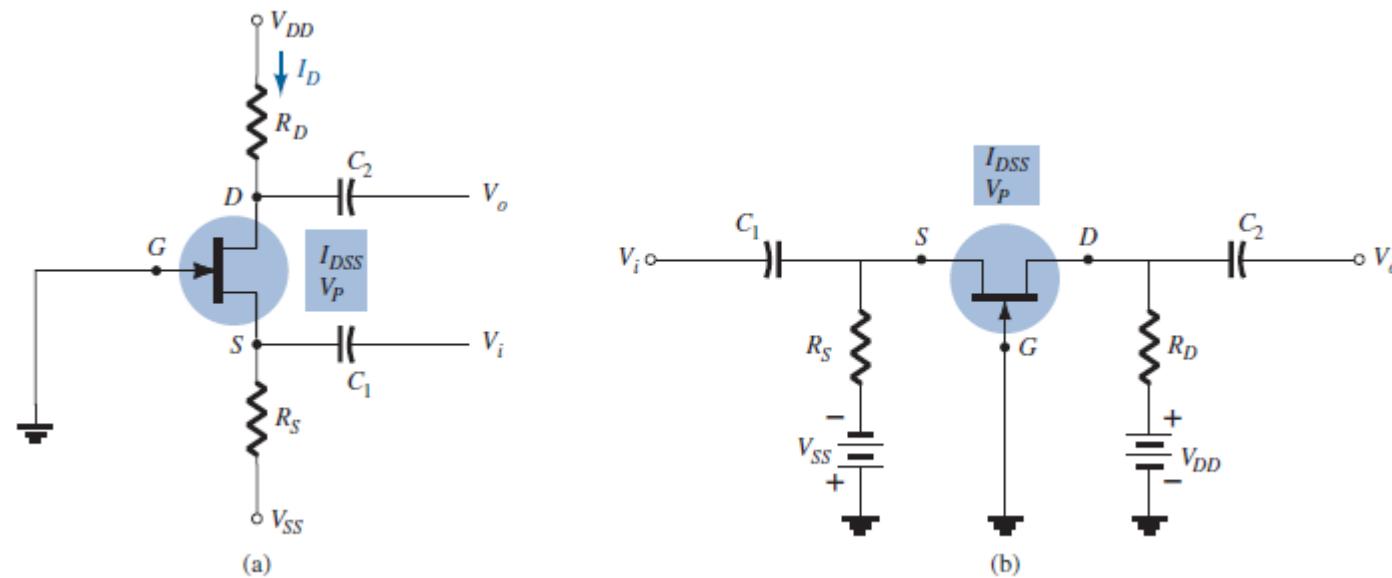
Solution

- c. $V_D = V_{DD} - I_D R_D = 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega) = 10.24 \text{ V}$
- d. $V_S = I_D R_S = (2.4 \text{ mA})(1.5 \text{ k}\Omega) = 3.6 \text{ V}$
- e. $V_{DS} = V_{DD} - I_D(R_s + R_D)$
 $= 16 \text{ V} - (2.4 \text{ mA})(2.4 \text{ k}\Omega + 1.5 \text{ k}\Omega) = 6.64 \text{ V}$
- F. $VDG = VD - VG = 10.24 \text{ V} - 1.82 \text{ V} = 8.42 \text{ V}$



Common-gate Configuration

- The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal



Common-gate Configuration

- Applying Kirchhoff's voltage law:

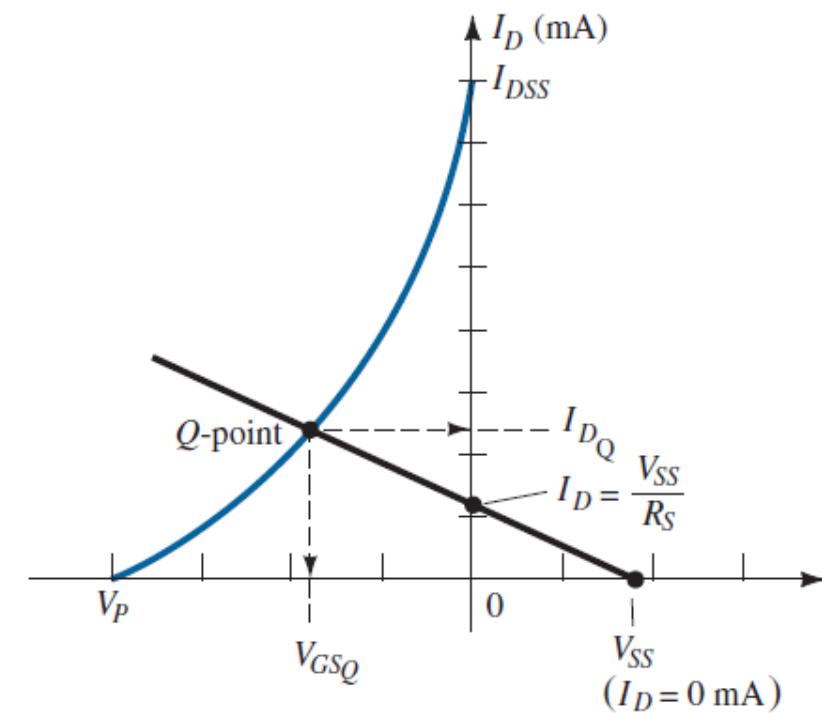
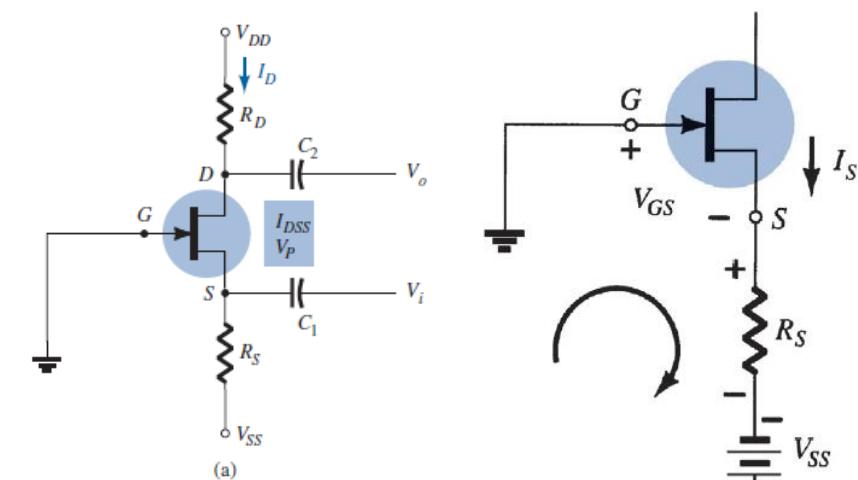
$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S ; \quad I_s = I_D ; \quad V_{GS} = V_{SS} - I_D R_S$$

Applying the condition $I_D = 0 \text{ mA}$, $V_{GS} = V_{SS}$

Applying the condition $V_{GS} = 0 \text{ V}$, $I_D = \frac{V_{SS}}{R_S}$

The resulting load-line appears intersecting the transfer curve for the JFET. The resulting intersection defines the operating current I_{DQ} and voltage V_{DQ} for the network as also indicated in the network.



Common-gate Configuration

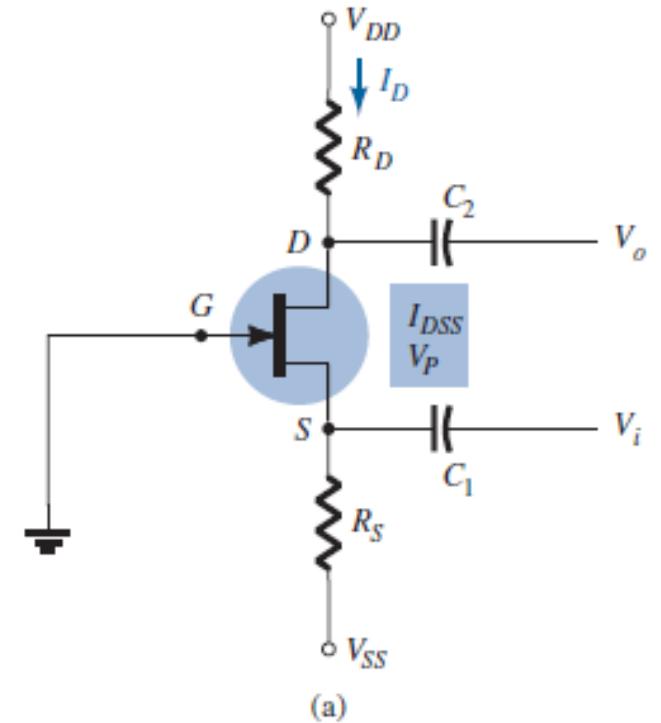
- Applying Kirchhoff's voltage law around the loop containing the two sources, the JFET and the resistors RD and RS:

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0 ; I_S = I_D$$

$$V_D = V_{DD} - I_D R_D$$

$$V_S = -V_{SS} + I_D R_S$$

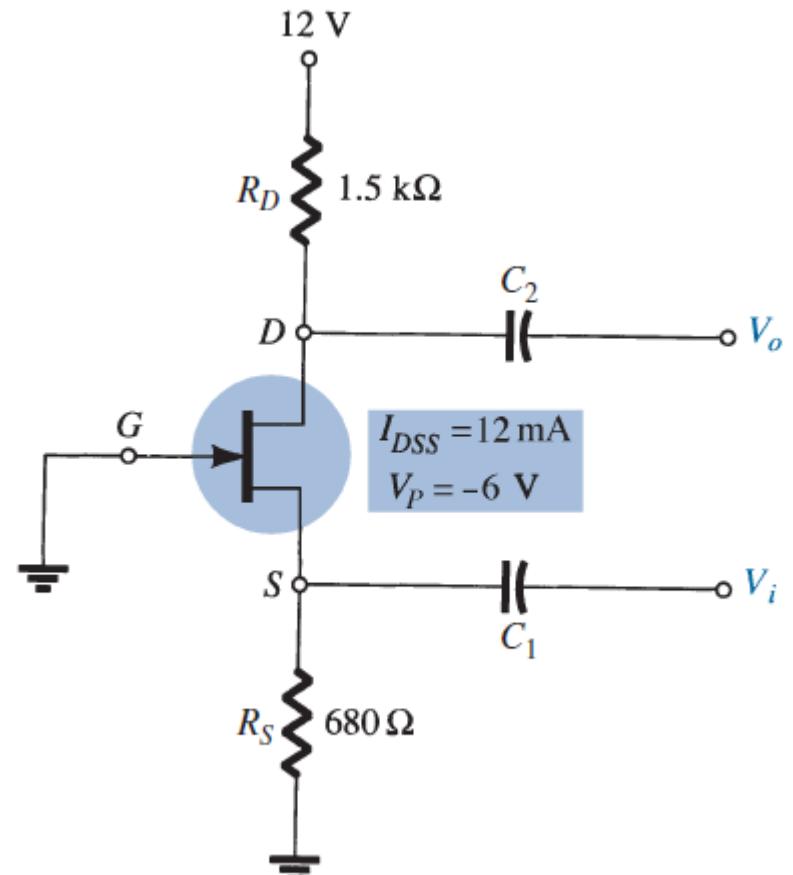
$$V_{DS} = V_D - V_S$$



(a)

Common-gate Configuration

- Determine the following for the network
- a. I_{DQ} and V_{GSQ} .
- b. V_D .
- c. V_S .
- d. V_G .
- e. V_{DS} .



Common-gate Configuration

- Determine the following for the network
- a. I_{DQ} and V_{GSQ} .
- b. V_D .
- c. V_S .
- d. V_G .
- e. V_{DS} .

Solution: Using pure computation:

$$-V_{GS} - V_{RS} = 0$$

$$V_{GS} = -V_{RS} = -I_D R_S$$

$$V_{GS} = -I_D (0.68k\Omega)$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Substitute the eq. of V_{GS}

$$I_D = 12mA \left[1 - \frac{-I_D(0.68k\Omega)}{-6V} \right]^2$$

Using calculator:

$$I_D = 3.84 \text{ mA}$$

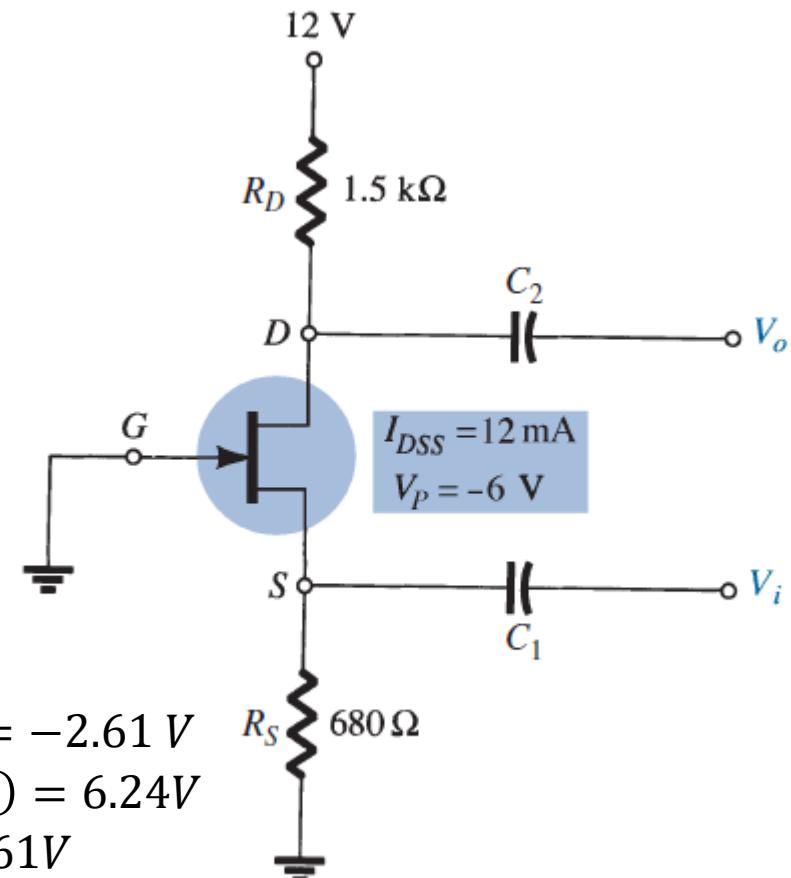
$$V_{GS} = -I_D (0.68k\Omega) = -3.84mA(0.68k\Omega) = -2.61 \text{ V}$$

$$V_D = V_{DD} - I_D R_D = 12 - (3.84mA)(1.5k\Omega) = 6.24V$$

$$V_S = I_D R_S = (3.84mA)(0.68k\Omega) = 2.61V$$

$$V_G = 0V$$

$$V_{DS} = V_D - V_S = 6.24V - 2.61V = 3.63V$$



Common-gate Configuration

$V_{SS} = 0 \text{ V}$; $V_{GS} = 0\text{V}$ if $I_D = 0\text{mA}$

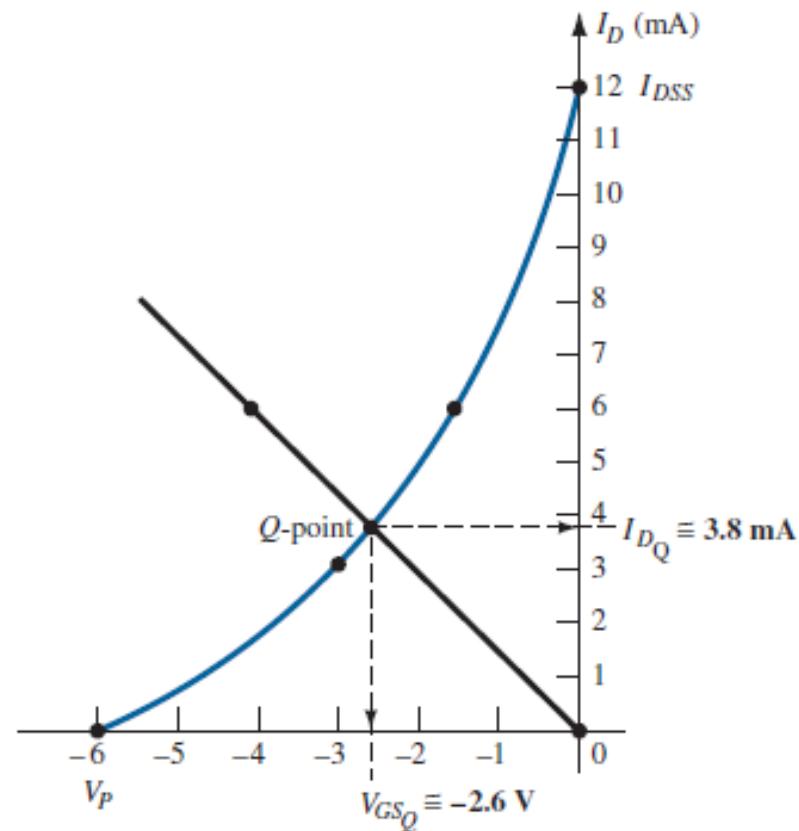
- $V_{GS} = -I_D R_S$
- For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing $I_D = 6 \text{ mA}$ and solving for V_{GS} will result in the following:

$$V_{GS} = -I_D R_S = -(6\text{mA})(680\Omega) = -4.08\text{V}$$

$I_D = I_{DSS}/4 = 12 \text{ mA} / 4 = 3 \text{ mA}$ (at $V_P > 2$) and $V_{GS} \cong 0.3V_P$
 $= 0.3(-6 \text{ V}) = -1.8 \text{ V}$ (at $I_D = I_{DSS}/2$)

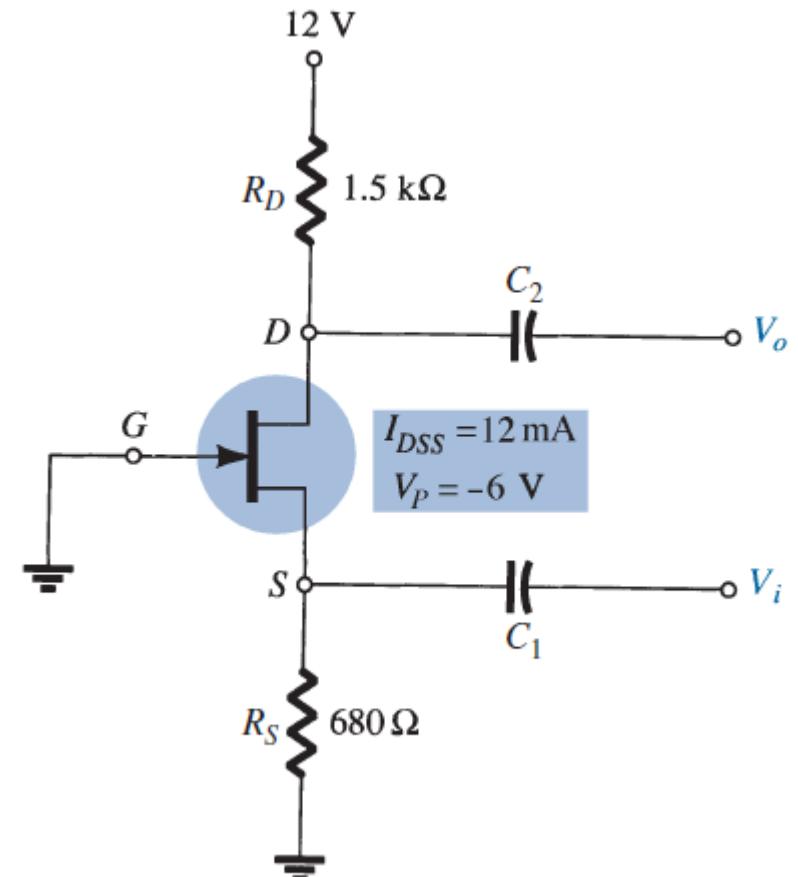
- The resulting solution is: $I_{DQ} = 3.8\text{mA}$ and $V_{GSQ} = -2.6\text{V}$

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA



Common-gate Configuration

- b. $V_D = V_{DD} - I_D R_D = 12V - (3.8mA)(1.5k\Omega) = 6.3V$
- c. $V_S = I_D R_S = (3.8mA)(680\Omega) = 2.58V$
- d. $V_G = 0V$
- e. $V_{DS} = V_D - V_S = 6.3V - 2.58V = 3.72V$



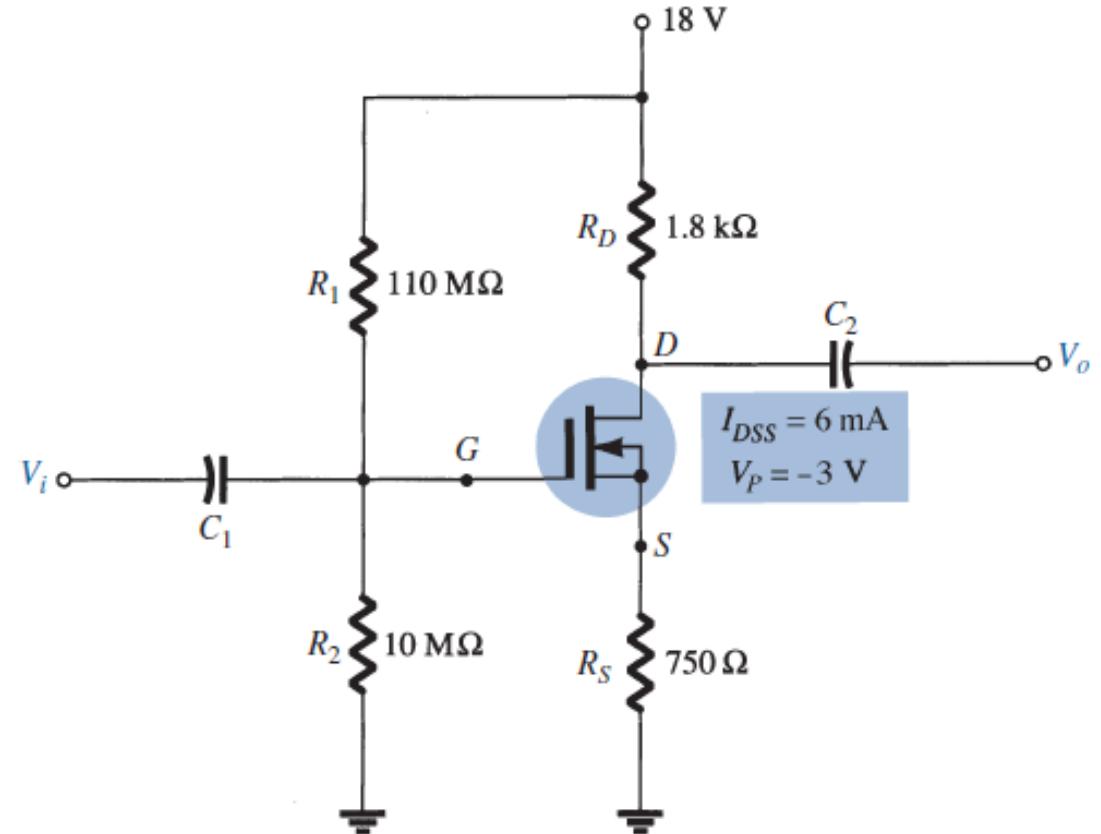
Depletion-Type MOSFETs

- The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS} . In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

Depletion-Type MOSFETs

For the n-channel depletion-type MOSFET,
determine:

- I_{DQ} and V_{GSQ}
- V_{DS}



Depletion-Type MOSFETs

Solution: Using pure computation:

For the n-channel depletion-type MOSFET, determine:

- I_{DQ} and V_{GSQ}
 - V_{DS}
- Substitute the eq. of V_{GS}

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{18V(10M\Omega)}{110M\Omega + 10M\Omega} = 1.5V$$

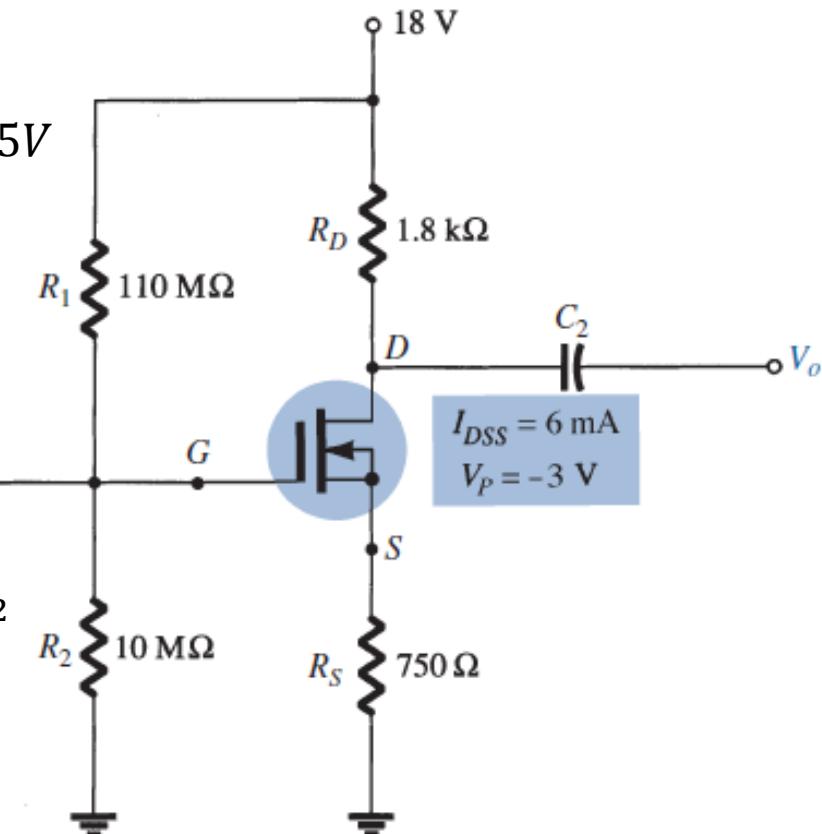
$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS} = V_G - I_D R_S$$

$$V_{GS} = 1.5V - I_D (0.75k\Omega)$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$I_D = 6mA \left[1 - \frac{1.5V - I_D (0.75k\Omega)}{-3V} \right]^2$$



Using calculator:

$$I_D = 3.12 \text{ mA}$$

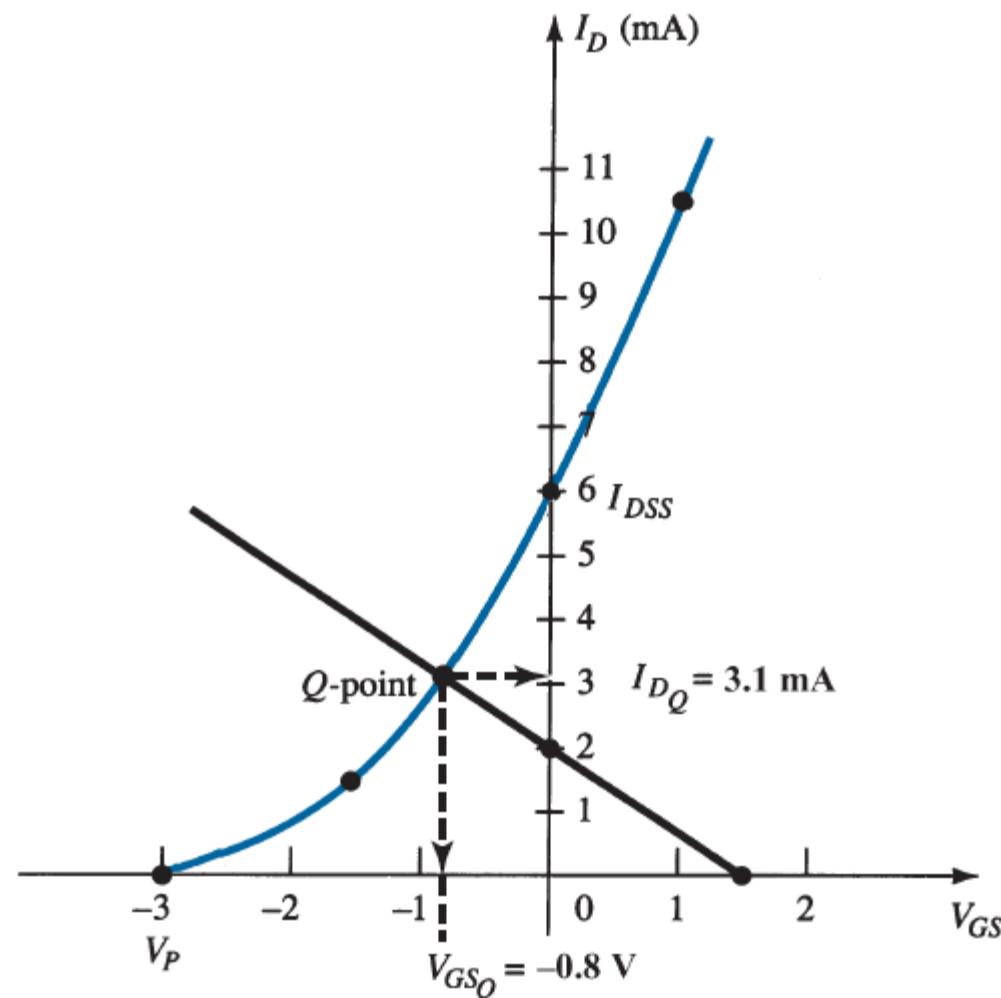
$$V_{GS} = 1.5 - I_D (0.75k\Omega) = 1.5V - 3.12mA(0.75k\Omega) = -0.84 V$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 18V - (3.12mA)(1.8k\Omega + 0.75k\Omega) = 10.04V$$

Depletion-Type MOSFETs

For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6 \text{ mA}/4 = 1.5 \text{ mA}$ and $V_{GS} = V_P/2 = -3 \text{ V}/2 = -1.5 \text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1 \text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$
$$I_D = 6 \text{ mA} \left[1 - \frac{+1 \text{ V}}{-3 \text{ V}} \right]^2 = 6 \text{ mA} (1.778)$$
$$= 10.67 \text{ mA}$$



Depletion-Type MOSFETs

To get the Q-point:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{10M\Omega(18V)}{10M\Omega + 110M\Omega} = 1.5V$$
$$V_{GS} = V_G - I_D R_S = 1.5V - I_D(750\Omega)$$

Setting $I_D = 0$ mA results in $V_{GS} = V_G = 1.5V$

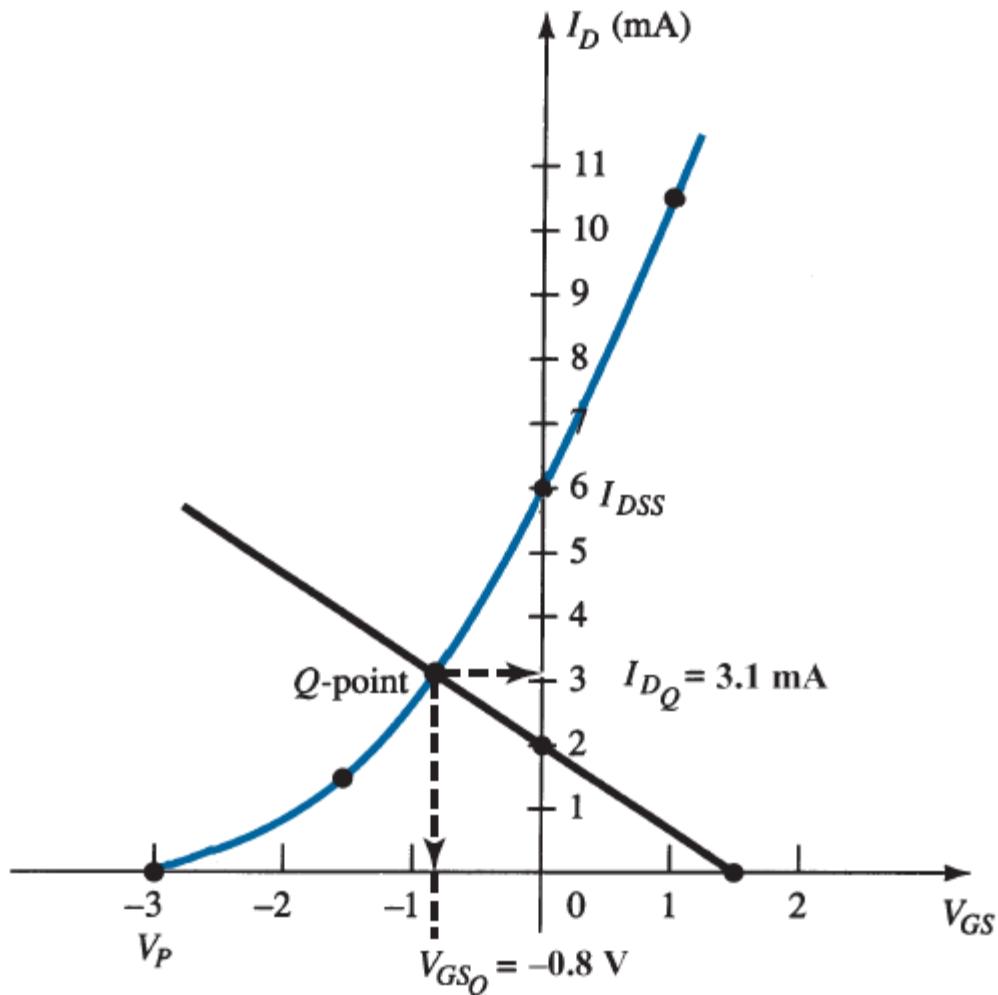
Setting $V_{GS} = 0$ V yields $I_D = \frac{V_G}{R_S} = \frac{1.75V}{750\Omega} = 2mA$

Upon plotting points and resulting bias line, the resulting operating point is given by

$$I_{DQ} = 3.1mA \text{ and } V_{GSQ} = -0.8V$$

b.

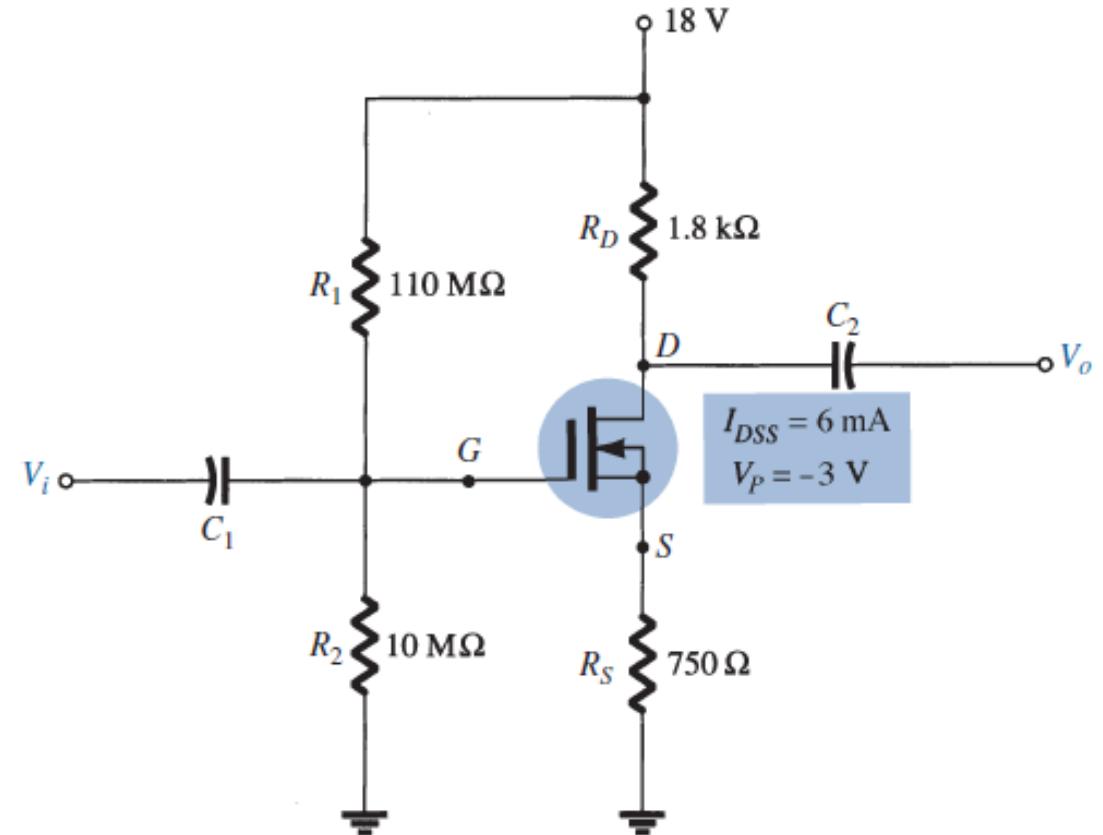
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18V - (3.1\text{mA})(1.8k\Omega + 750\Omega) = 10.1V$$



Depletion-Type MOSFETs

Repeat, if $R_S=150 \Omega$

- I_{DQ} and V_{GSQ}
- V_{DS}



Depletion-Type MOSFETs

Solution: Using pure computation:

Repeat, if $R_S=150 \Omega$ $V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{18V(10M\Omega)}{110M\Omega + 10M\Omega} = 1.5V$

- I_{DQ} and V_{GSQ}
- V_{DS}

$$\begin{aligned} V_G - V_{GS} - V_{RS} &= 0 \\ V_{GS} &= V_G - V_{RS} = V_G - I_D R_S \\ V_{GS} &= 1.5V - I_D (0.15k\Omega) \end{aligned}$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

Substitute the eq. of V_{GS}

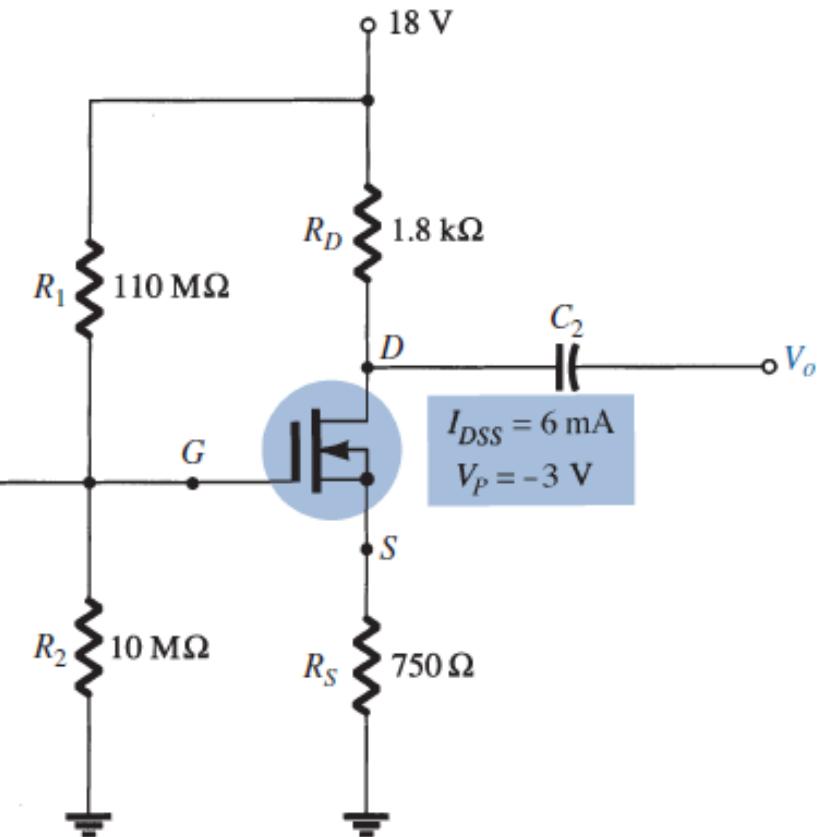
$$I_D = 6mA \left[1 - \frac{1.5V - I_D (0.15k\Omega)}{-3V} \right]^2$$

Using calculator:

$$I_D = 7.56mA$$

$$V_{GS} = 1.5 - I_D (0.15k\Omega) = 1.5V - 7.56mA(0.15k\Omega) = 0.29 V$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 18V - (7.56mA)(1.8k\Omega + 0.15k\Omega) = 3.26V$$

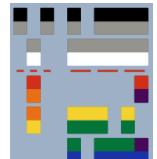
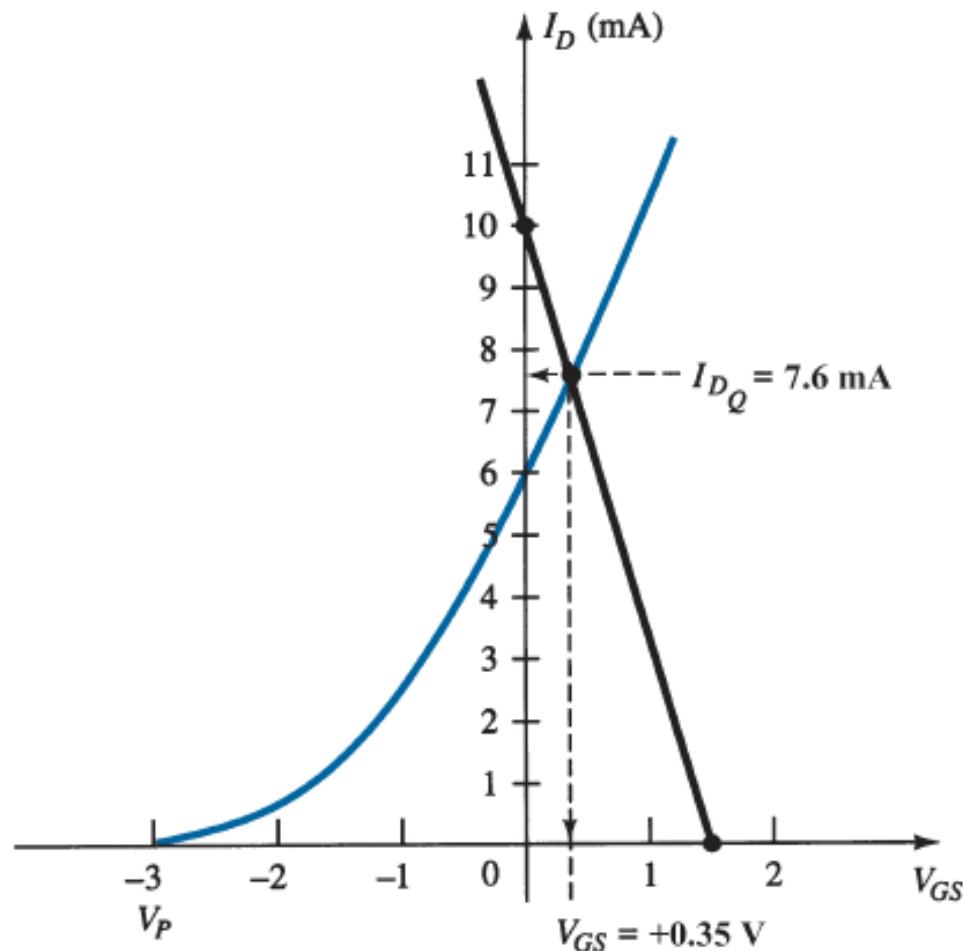


Depletion-Type MOSFETs

For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6 \text{ mA}/4 = 1.5 \text{ mA}$ and $V_{GS} = V_P/2 = -3 \text{ V}/2 = -1.5 \text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1 \text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

$$I_D = 6 \text{ mA} \left[1 - \frac{+1 \text{ V}}{-3 \text{ V}} \right]^2 = 6 \text{ mA}(1.778) = 10.67 \text{ mA}$$



Depletion-Type MOSFETs

To get the Q-point:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{10M\Omega(18V)}{10M\Omega + 110M\Omega} = 1.5V$$
$$V_{GS} = V_G - I_D R_S = 1.5V - I_D(250\Omega)$$

Setting $I_D = 0$ mA results in $V_{GS} = V_G = 1.5V$

Setting $V_{GS} = 0$ V yields $I_D = \frac{V_G}{R_S} = \frac{1.75V}{750\Omega} = 10mA$

Upon plotting points and resulting bias line, the resulting operating point is given by

$$I_{DQ} = 7.6mA \text{ and } V_{GSQ} = +0.35V$$

b.

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18V - (7.6mA)(1.8k\Omega + 150\Omega) = 3.18V$$

To get the Q-point:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{10M\Omega(18V)}{10M\Omega + 110M\Omega} = 1.5V$$
$$V_{GS} = V_G - I_D R_S = 1.5V - I_D(250\Omega)$$

Setting $I_D = 0$ mA results in $V_{GS} = V_G = 1.5V$

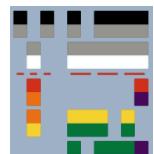
Setting $V_{GS} = 0$ V yields $I_D = \frac{V_G}{R_S} = \frac{1.75V}{750\Omega} = 10mA$

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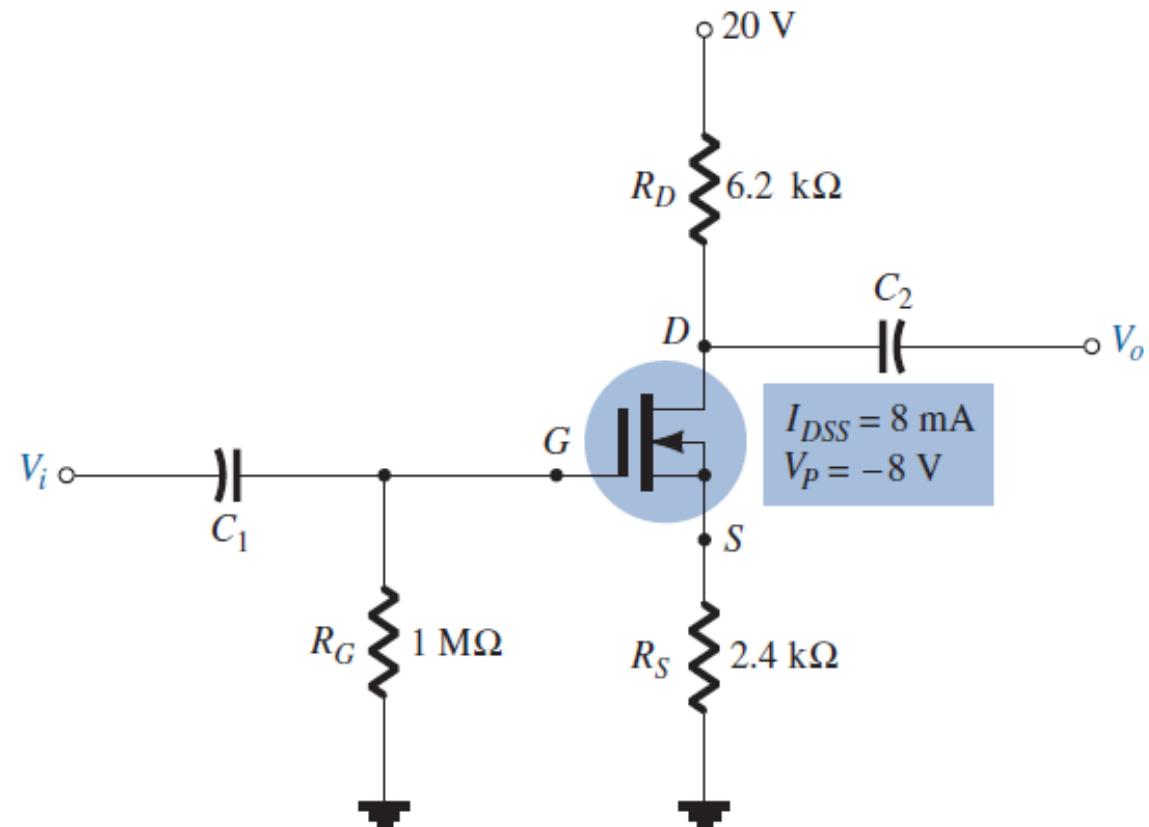
$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18V - (7.6mA)(1.8k\Omega + 150\Omega) = 3.18V$$



Depletion-Type MOSFETs

Determine the following for the network

- I_{DQ} and V_{GSQ}
- V_{DS}



Depletion-Type MOSFETs

Determine the following for the network

- I_{DQ} and V_{GSQ}
- V_{DS}

Substitute the eq. of V_{GS}

$$V_{GS} = -V_{RS} = -I_D R_S$$

$$V_{GS} = -I_D (2.4 \text{ k}\Omega)$$

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2$$

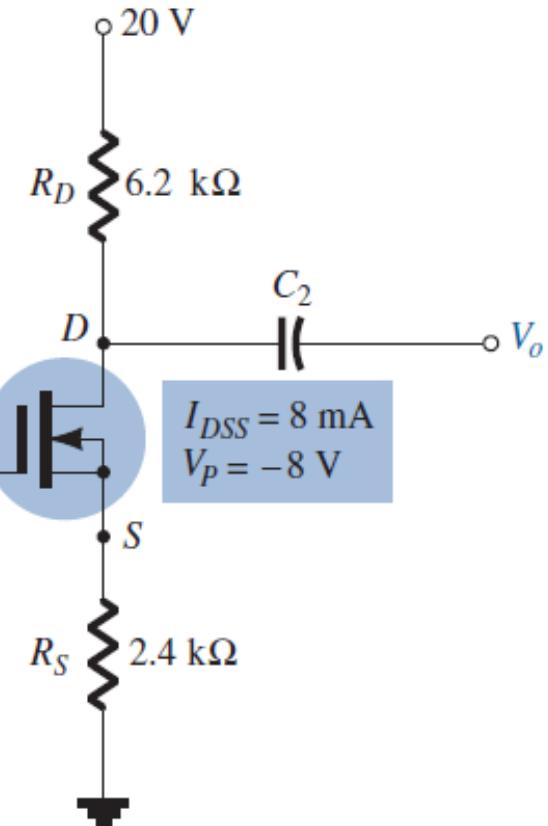
$$I_D = 8 \text{ mA} \left[1 - \frac{-I_D (2.4 \text{ k}\Omega)}{-8 \text{ V}} \right]^2$$

Using calculator:

$$I_D = 1.77 \text{ mA}$$

$$V_{GS} = -I_D (2.4 \text{ k}\Omega) = -1.77 \text{ mA} (2.4 \text{ k}\Omega) = -4.25 \text{ V}$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S) = 12 - (3.84 \text{ mA}) (6.2 \text{ k}\Omega + 2.4 \text{ k}\Omega) = 4.78 \text{ V}$$



Depletion-Type MOSFETs

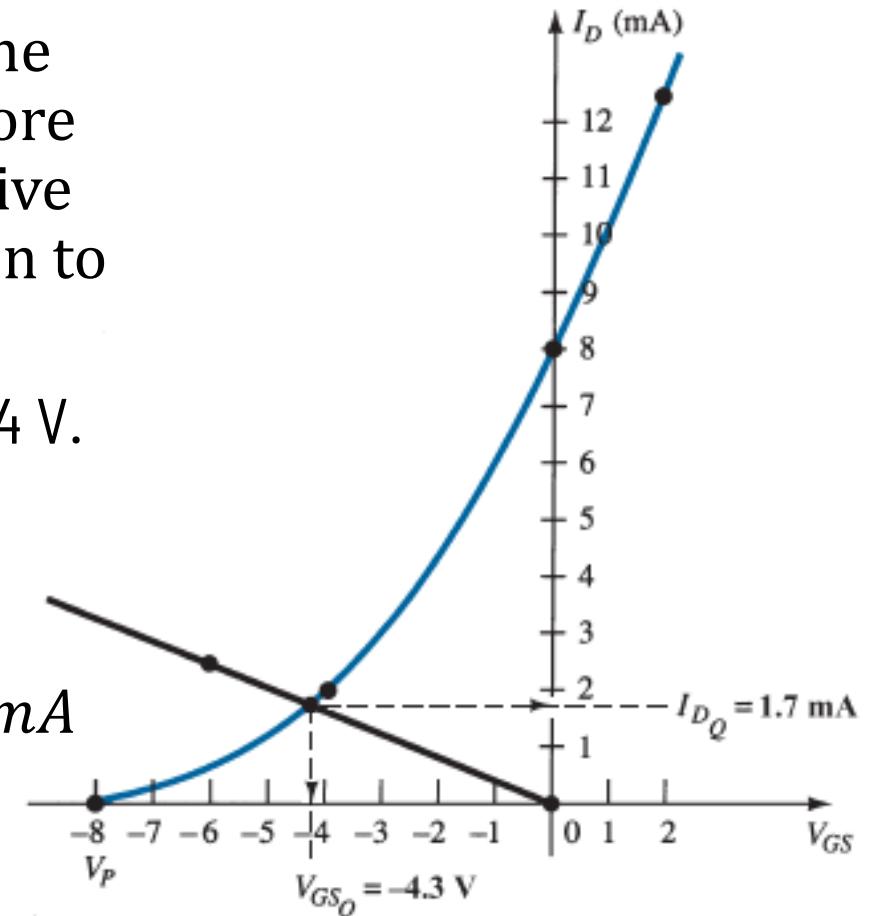
The self-bias configuration results in $V_{GS} = -I_D R_S$ as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS} , although it was done on this occasion to complete the transfer characteristics.

$$I_D = I_{DSS}/4 = 8 \text{ mA}/4 = 2 \text{ mA} \text{ and } V_{GS} = V_P/2 = -8 \text{ V}/2 = -4 \text{ V}.$$

$$I_D =$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_P} \right]^2 = 8mA \left[1 - \frac{+2V}{-8V} \right]^2 = 12.5mA$$



Depletion-Type MOSFETs

To get the Q-point:

Setting $I_D = 0 \text{ mA}$ results in $V_{GS} = 0V$

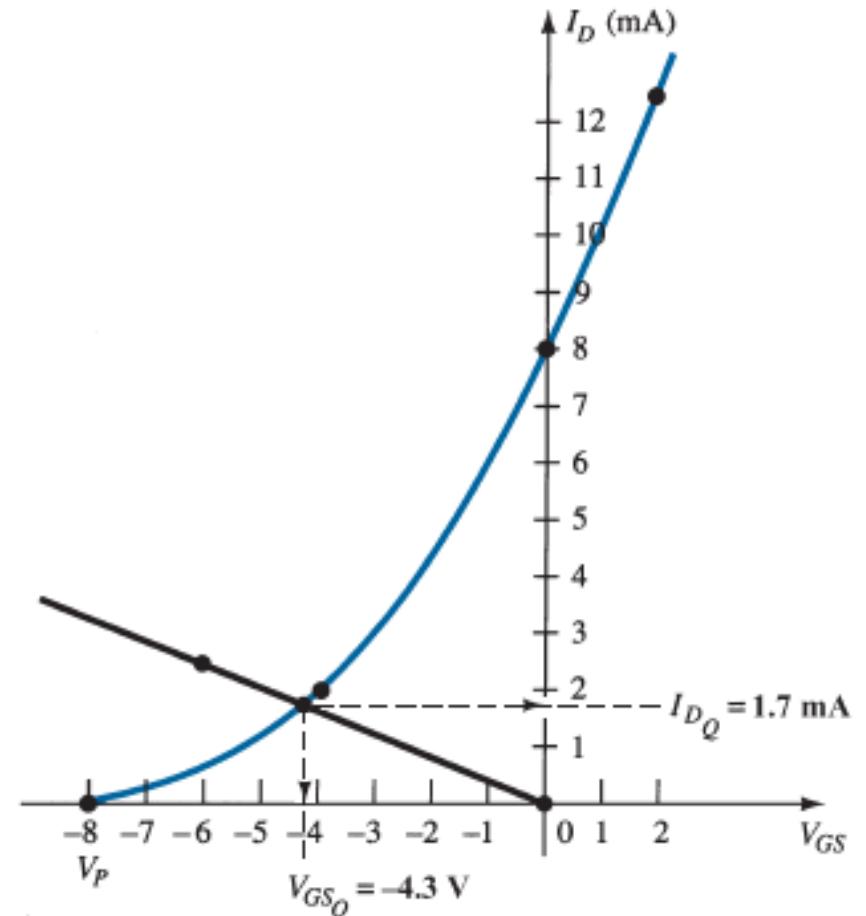
Setting $V_{GS} = -6 \text{ V}$ yields $I_D = \frac{-V_{GS}}{R_S} = \frac{-6 \text{ V}}{2.4 \text{ k}\Omega} = 2.5 \text{ mA}$

The resulting Q-point is given by $I_{DQ} = 1.7 \text{ mA}$; $V_{GSQ} = -4.3 \text{ V}$

Upon plotting points and resulting bias line, the resulting operating point is given by

$I_{DQ} = 1.7 \text{ mA}$ and $V_{GSQ} = -4.3 \text{ V}$

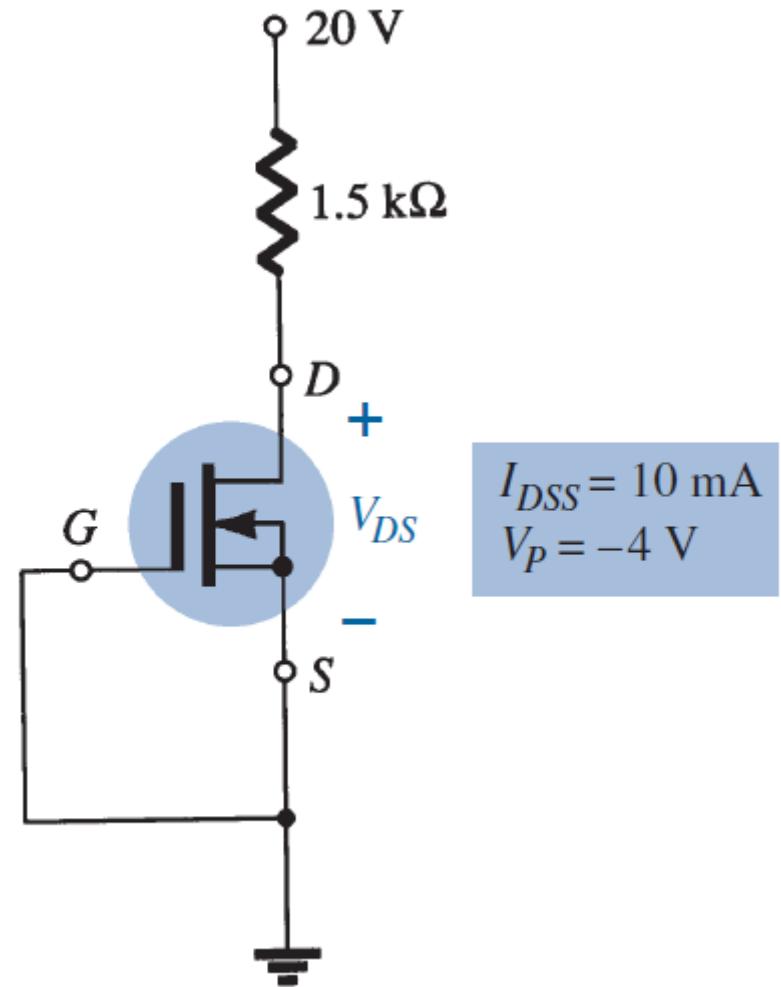
b. $V_D = V_{DD} - I_D R_D = 20 \text{ V} - (1.7 \text{ mA})(6.2 \text{ k}\Omega) = 9.46 \text{ V}$



Depletion-Type MOSFETs

Determine the following for the network

- V_{DS}



Depletion-Type MOSFETs

Determine the following for the network

- V_{DS}

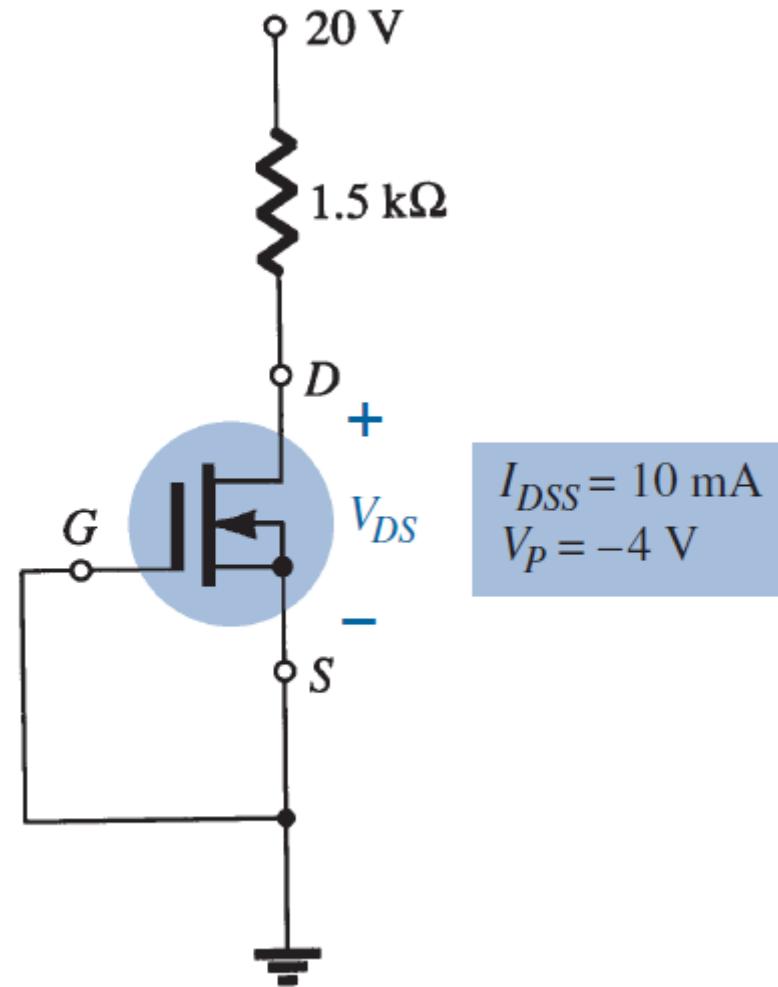
Solution: Using pure computation:

If $V_{GS} = 0$; $I_D = I_{DSS}$

$$I_D = 10 \text{ mA}$$

$$I_D = 1.77 \text{ mA}$$

$$V_{DS} = V_{DD} - I_D R_D = 12 - (10 \text{ mA})(1.5 \text{ k}\Omega) = 5V$$



Depletion-Type MOSFETs

The direct connection between the gate and source terminals requires that

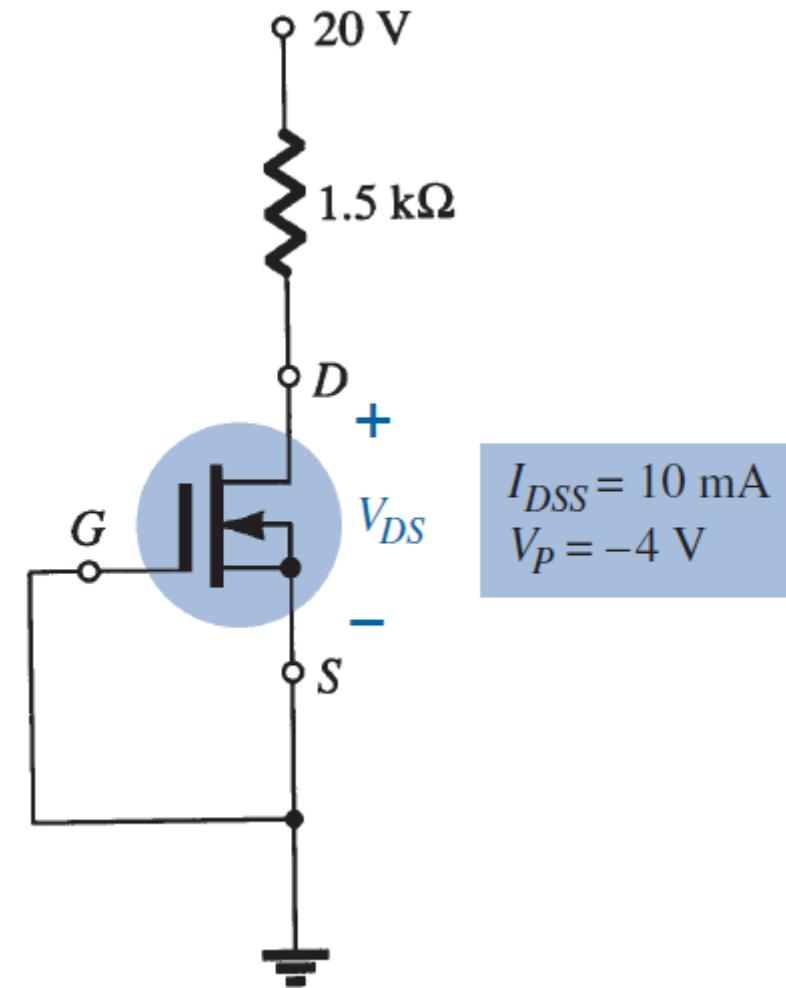
$$V_{GS} = 0 \text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS0} = 0 \text{ V} \text{ and } I_{D0} = 10 \text{ mA}$$

There is therefore no need to draw the transfer curve, and

$$V_D = V_{DD} - I_D R_D = 20 \text{ V} - (10 \text{ mA})(1.5 \text{ k}\Omega) = 20 \text{ V} - 15 \text{ V} = 5 \text{ V}$$



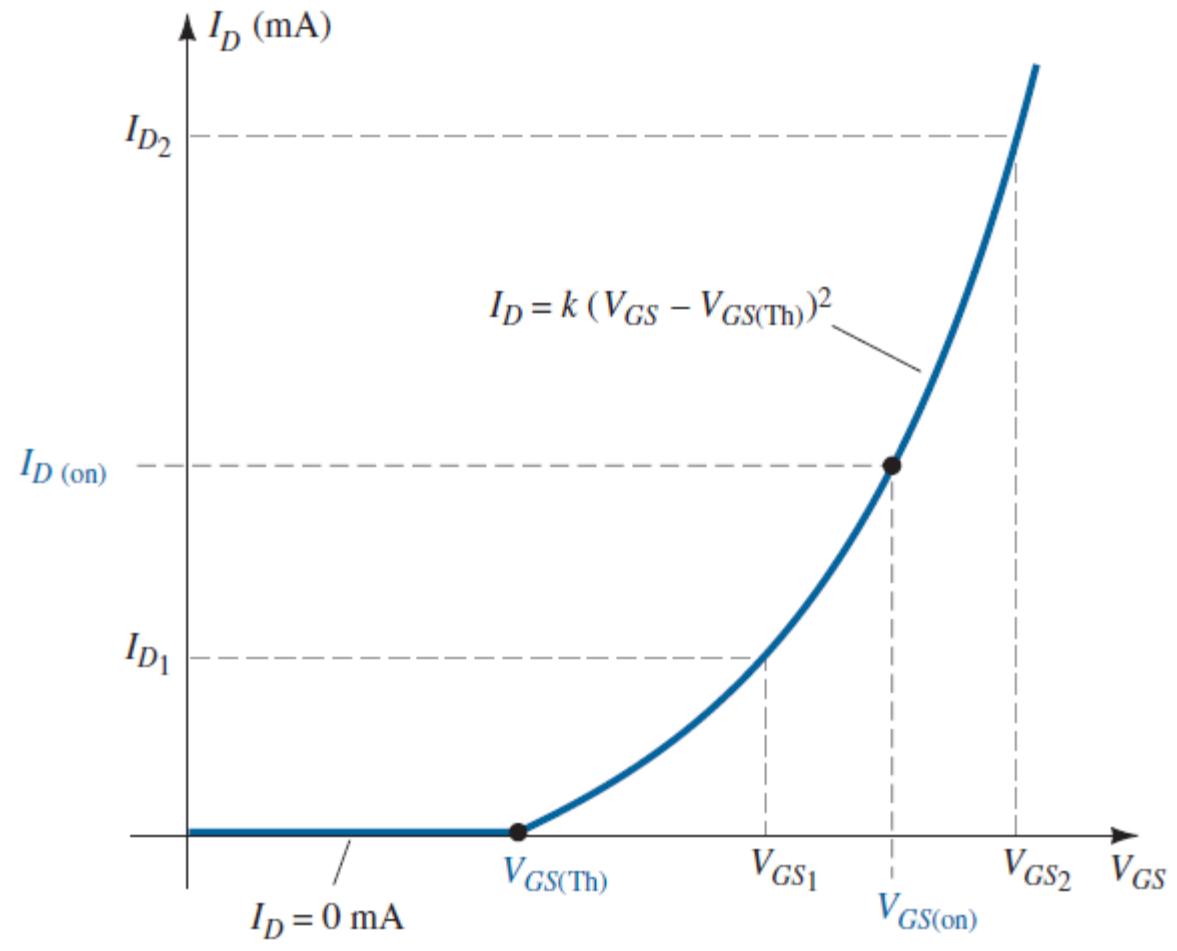
Enhancement-type Mosfets

Enhancement-type Mosfets

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the n-channel enhancement-type MOSFET, the drain current is zero for levels of gate to- source voltage less than the threshold level $V_{GS(Th)}$. For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$I_D = k (V_{GS} - V_T)^2$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$



Feedback biasing arrangement

- The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since
- $I_G = 0 \text{ mA}$, $V_{RG} = 0 \text{ V}$ and the dc equivalent network appears as shown
- A direct connection now exists between drain and gate, resulting in

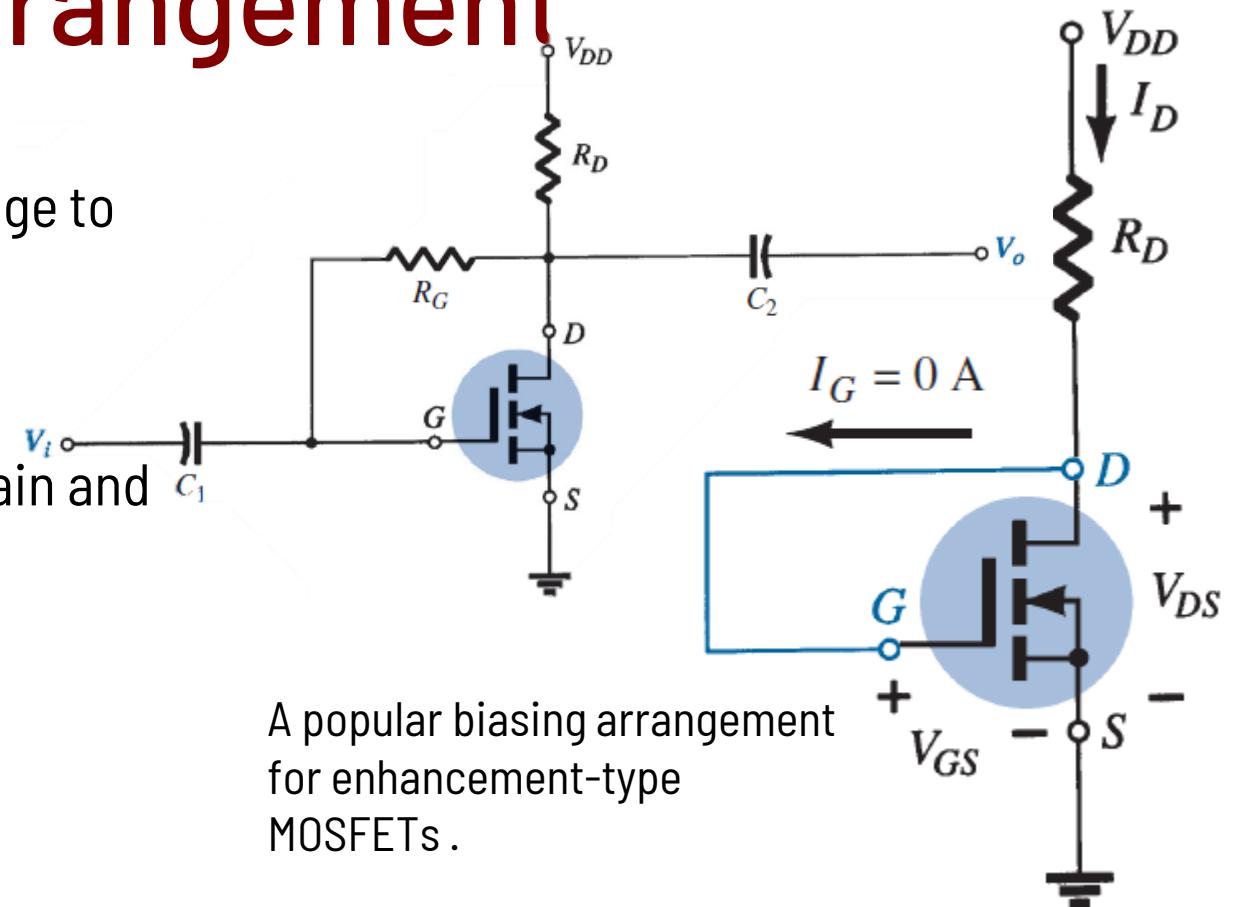
$$V_D = V_G ; V_{DS} = V_{GS}$$

For the output circuit,

$$V_{DS} = V_{DD} - I_D R_D ; V_{GS} = V_{DD} - I_D R_D$$

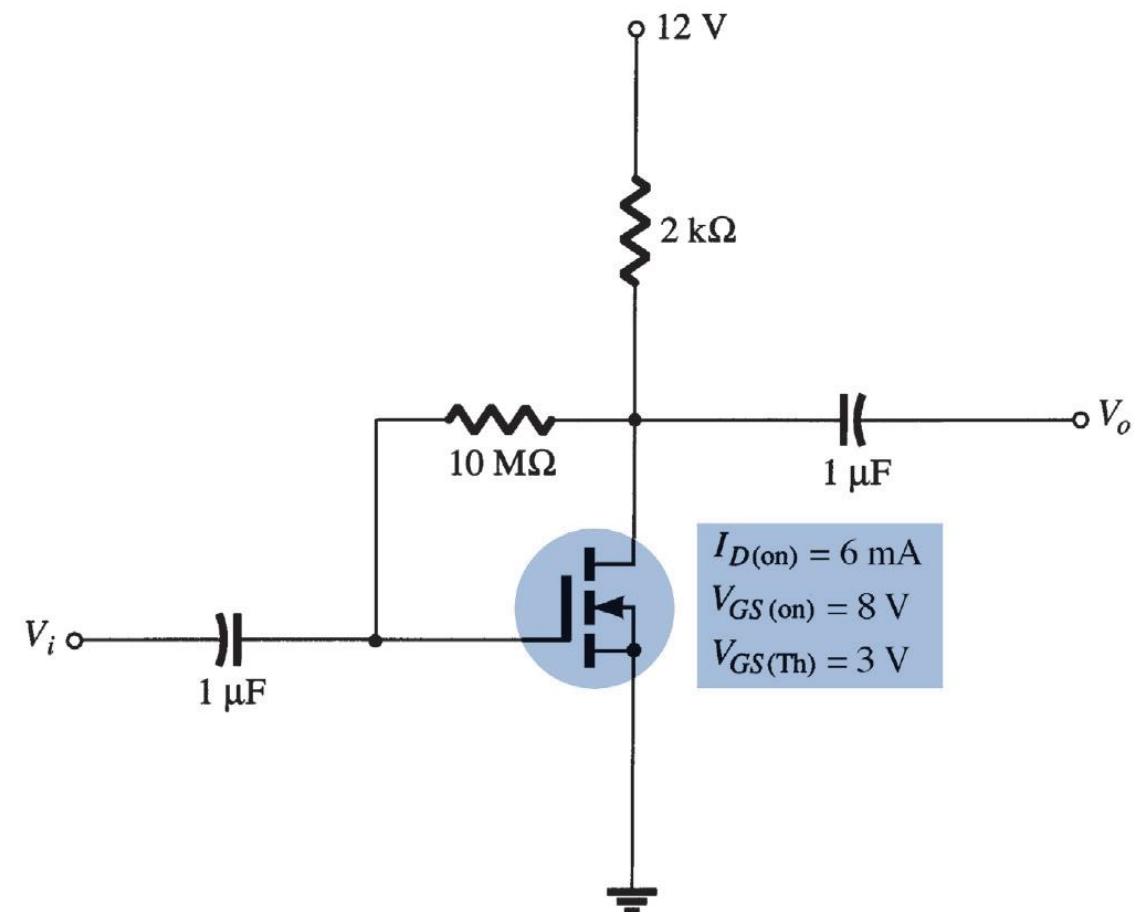
If $I_D = 0 \text{ mA}$, $V_{GS} = V_{DD}$

Substituting $V_{GS} = 0 \text{ V}$, $I_D = \frac{V_{DD}}{R_D}$



Feedback biasing arrangement

Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET.



Feedback biasing arrangement

Determine I_{DQ} and V_{DSQ} for the enhancement-type MOSFET.

Solution: Using pure computation:

Solving for k , we obtain

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} = \frac{6mA}{(8V - 3V)^2} = 240 \times 10^{-6} \frac{A}{V^2}$$

$$V_{DS} = V_{GS} = V_{DD} - I_D R_D = 12 - I_D (2k\Omega)$$

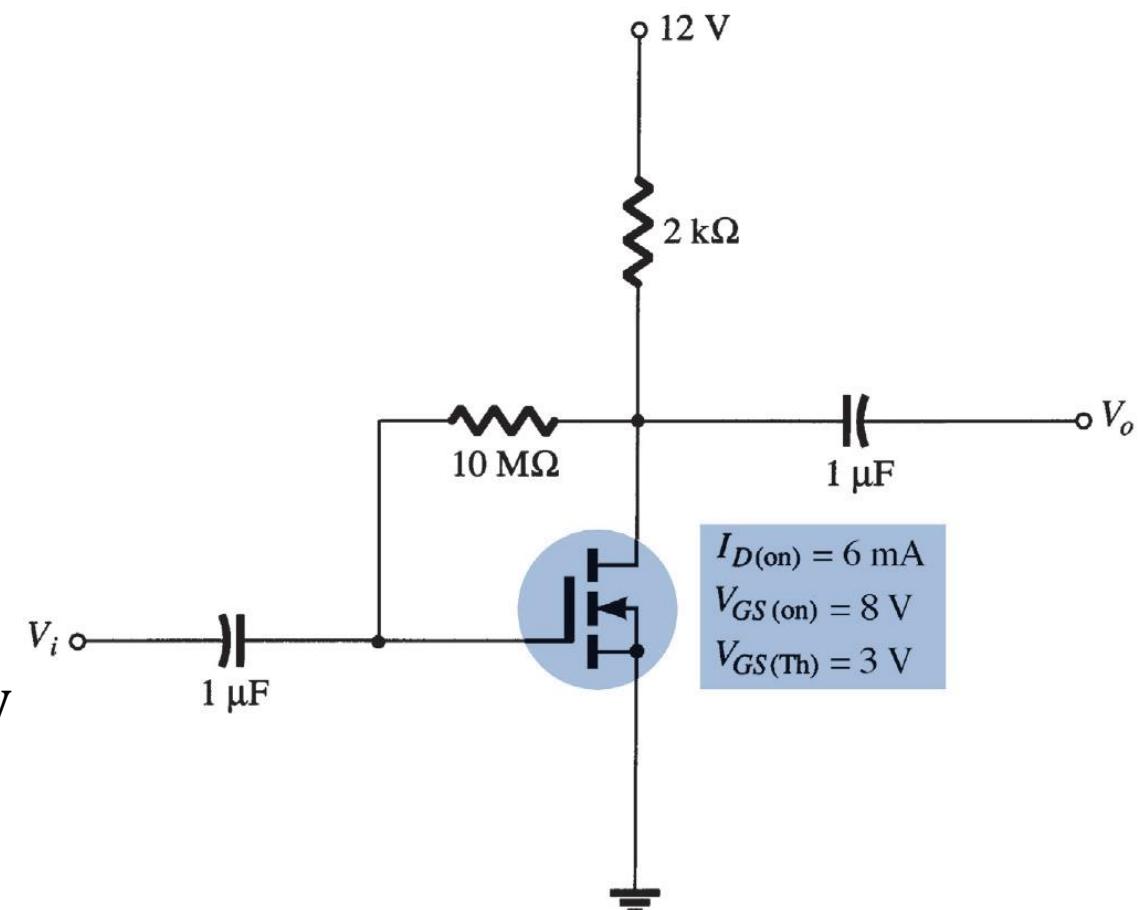
$$I_D = k (V_{GS} - V_T)^2$$

$$I_D = 240 \times 10^{-6} (12 - I_D (2k\Omega) - 3)^2$$

Using Calculator:

$$I_D = 2.79mA$$

$$V_{DS} = V_{GS} = V_{DD} - I_D R_D = 12 - 2.79mA (2k\Omega) = 6.24V$$



Feedback biasing arrangement

Two points are defined immediately

Solving for k, we obtain

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} = \frac{6mA}{(8V - 3V)^2}$$
$$= 0.24 \times 10^{-3} \frac{A}{V^2}$$

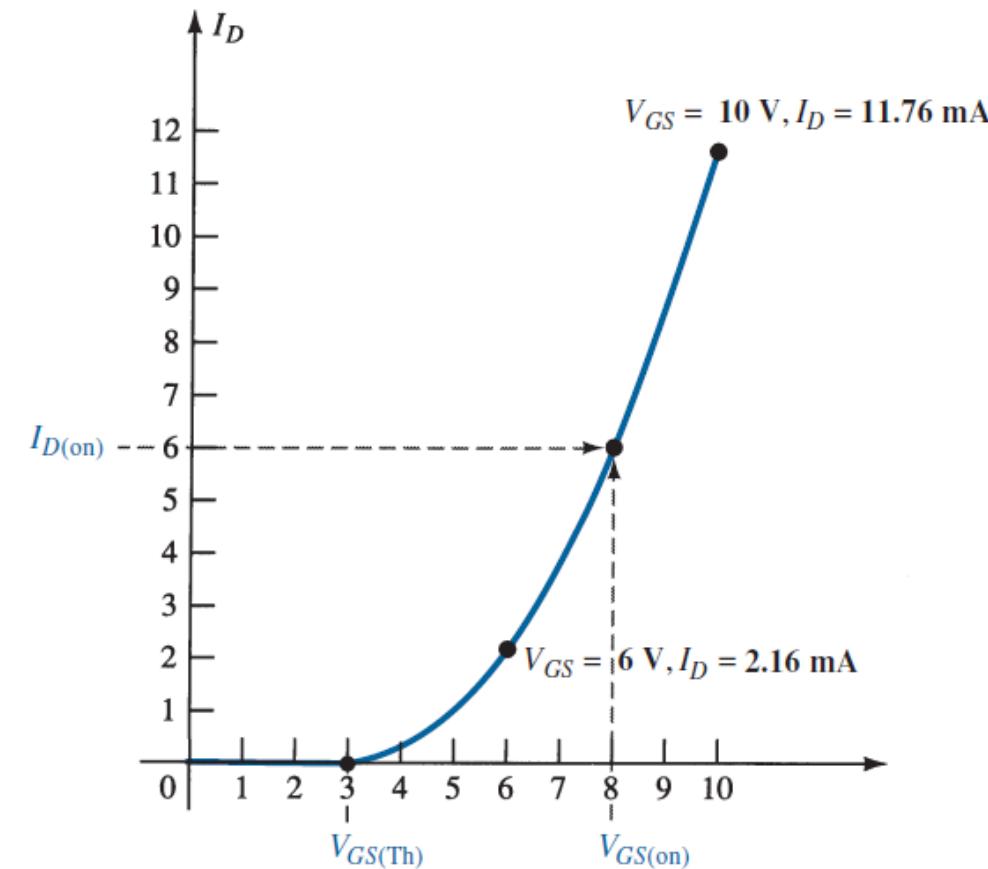
For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6 V - 3 V)^2 = 0.24 \times 10^{-3}(9) = 2.16 mA$$

For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$),

$$I_D = 0.24 \times 10^{-3}(10 V - 3 V)^2 = 0.24 * 10^{-3}(49) = 11.76 mA$$

The four points are sufficient to plot the full curve for the range of interest.



Feedback biasing arrangement

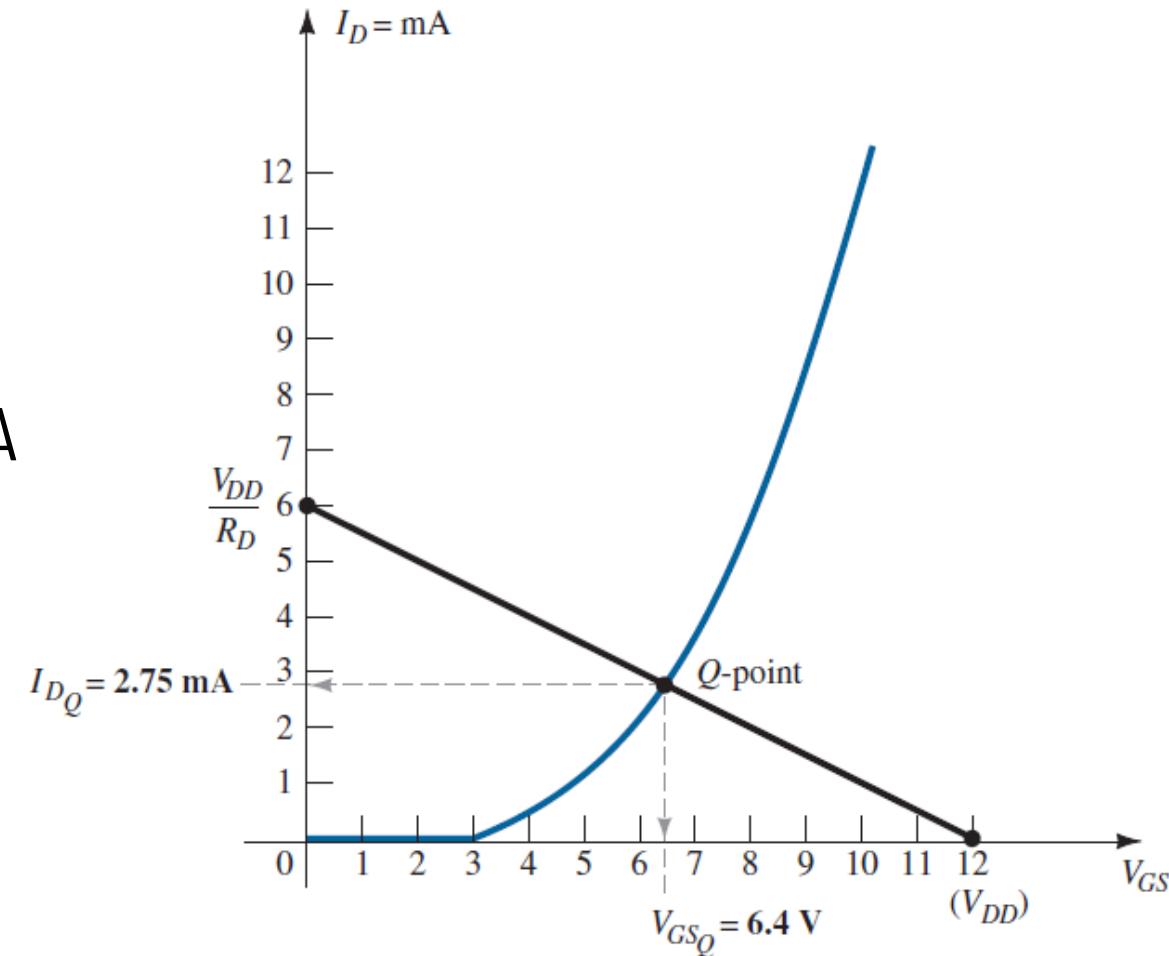
For the network bias Line

$$V_{GS} = V_{DD} - I_D R_D = 12 \text{ V} - I_D(2\text{k}\Omega)$$

If $I_D = 0 \text{ mA}$, $V_{GS} = V_{DD} = 12 \text{ V}$

If $V_{GS} = 0 \text{ V}$, $I_D = V_{DD} / R_D = 12 \text{ V} / (2\text{k}\Omega) = 6 \text{ mA}$

$$I_{DQ} = 2.75 \text{ mA} \text{ and } V_{DSQ} = 6.4 \text{ V}$$



Voltage-divider Biasing Arrangement

- A second popular biasing arrangement for the enhancement-type MOSFET appears. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

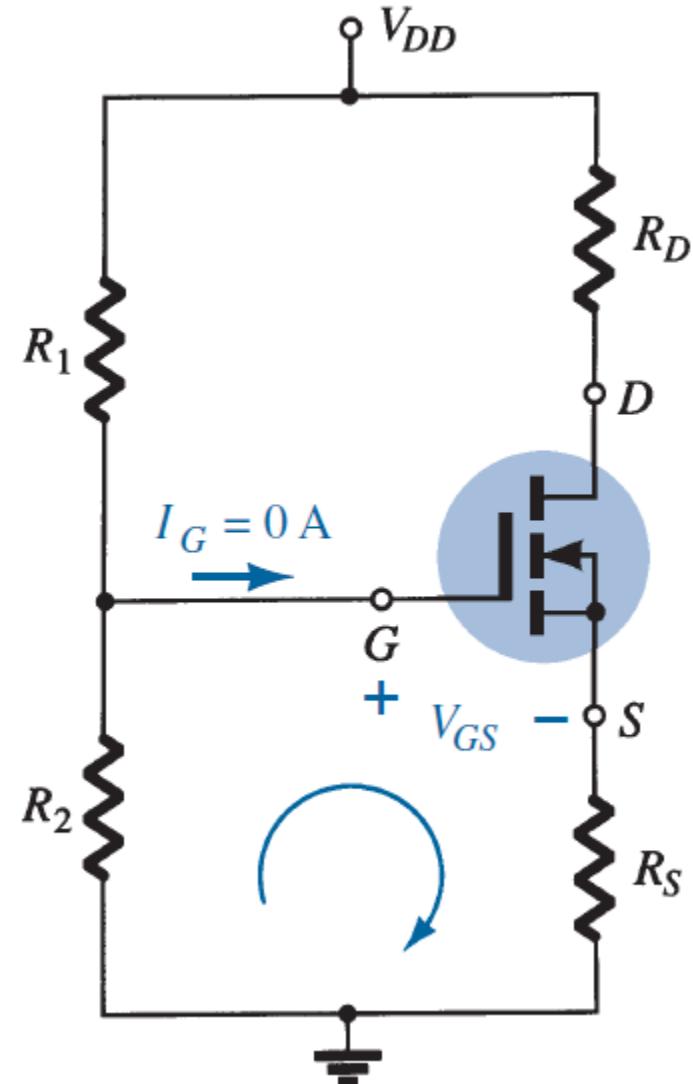
$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Applying Kirchhoff's voltage law around the indicated loop results in

$$+V_G - V_{GS} - V_{RS} = 0 ; V_{GS} = V_G - V_{RS}$$
$$V_{GS} = V_G - I_D R_S$$

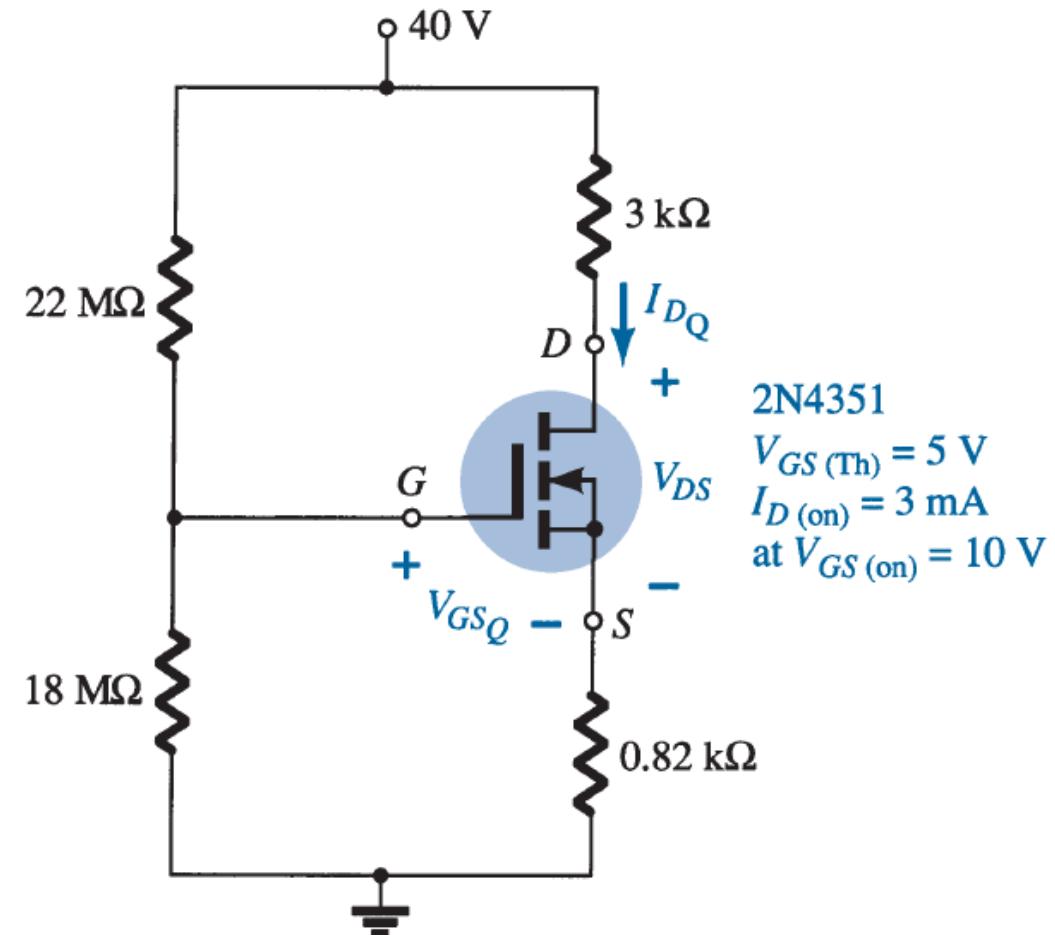
For the output section,

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0; V_{DS} = V_{DD} - V_{RS} - V_{RD}$$
$$V_{DS} = V_{DD} - I_D (R_S + R_D)$$



Voltage-divider Biasing Arrangement

Determine I_{DQ} , V_{GSQ} , and V_{DS} for the network.



Voltage-divider Biasing Arrangement

Determine I_{DQ} , V_{GSQ} , and V_{DS} for the network.

Solution: Using pure computation:

Solving for k , we obtain

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} = \frac{3mA}{(10V - 5V)^2} = 120 \times 10^{-6} \frac{A}{V^2}$$

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18M\Omega)(40V)}{22M\Omega + 18M\Omega} = 18V$$

$$V_{GS} = V_G - I_D R_S = 18 - I_D (0.82k\Omega)$$

$$I_D = k (V_{GS} - V_T)^2$$

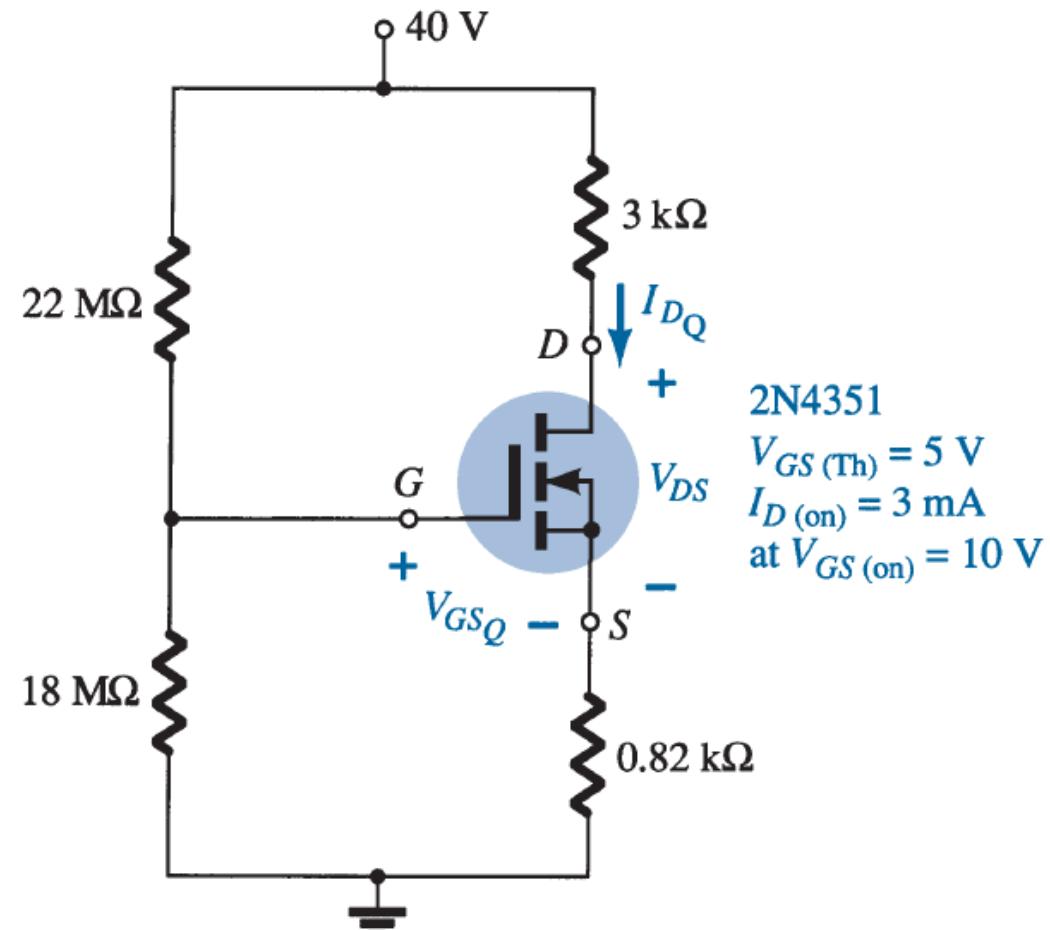
$$I_D = 120 \times 10^{-6} (18 - I_D (0.82k\Omega) - 5)^2$$

Using Calculator:

$$I_D = 6.72mA$$

$$V_{GS} = V_G - I_D R_S = 18 - 6.72mA(0.82k\Omega) = 12.49V$$

$$V_{DS} = 40V - 6.72mA(0.82k\Omega + 3k\Omega) = 14.33V$$



Voltage-divider Biasing Arrangement

Solving for k, we obtain

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} = \frac{3mA}{(10V - 5V)^2}$$
$$= 0.12 \times 10^{-3} \frac{A}{V^2}$$

For $V_{GS} = 10$ V

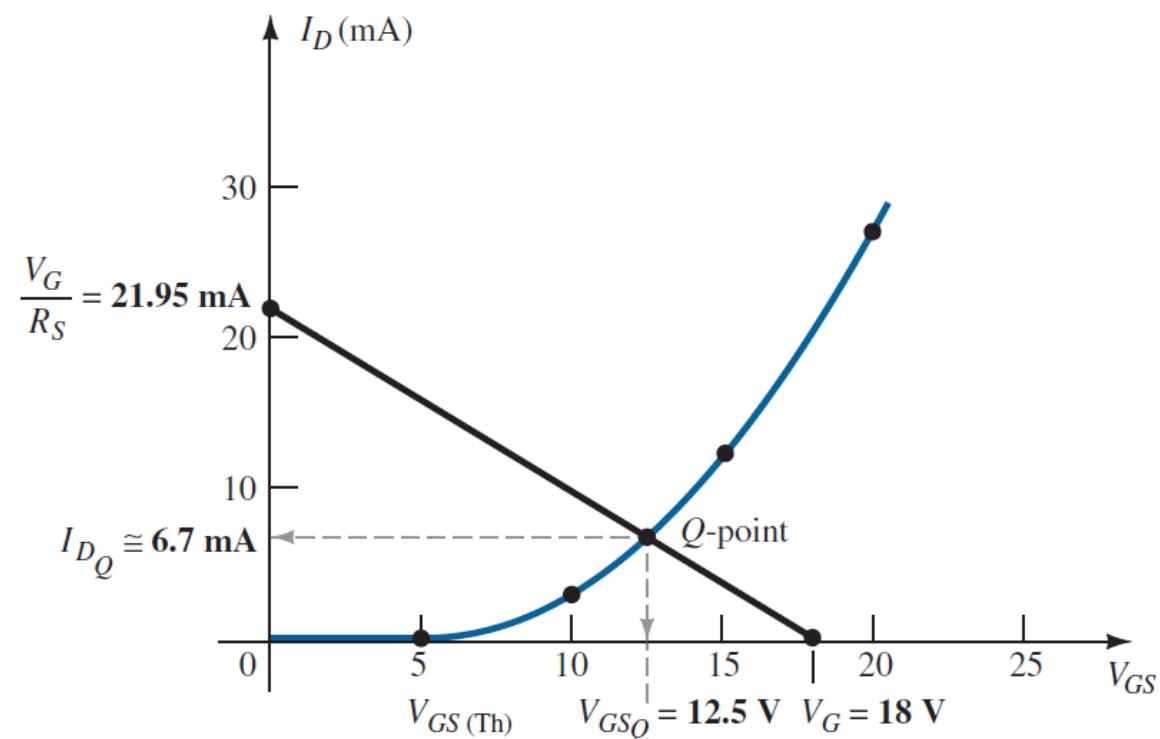
$$I_D = 0.12 \times 10^{-3}(10\text{ V} - 5\text{ V})^2 = 0.12 \times 10^{-3}(25) = 3 \text{ mA}$$

For $V_{GS} = 15$ V

$$I_D = 0.12 \times 10^{-3}(15\text{ V} - 5\text{ V})^2 = 0.12 \times 10^{-3}(100) = 12 \text{ mA}$$

For $V_{GS} = 20$ V

$$I_D = 0.12 \times 10^{-3}(20\text{ V} - 5\text{ V})^2 = 0.12 \times 10^{-3}(225) = 27 \text{ mA}$$



Voltage-divider Biasing Arrangement

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18M\Omega)(40V)}{22M\Omega + 18M\Omega} = 18V$$

$$V_{GS} = V_G - I_D R_S = 18 - I_D(0.82k\Omega)$$

When $I_D = 0$ mA,

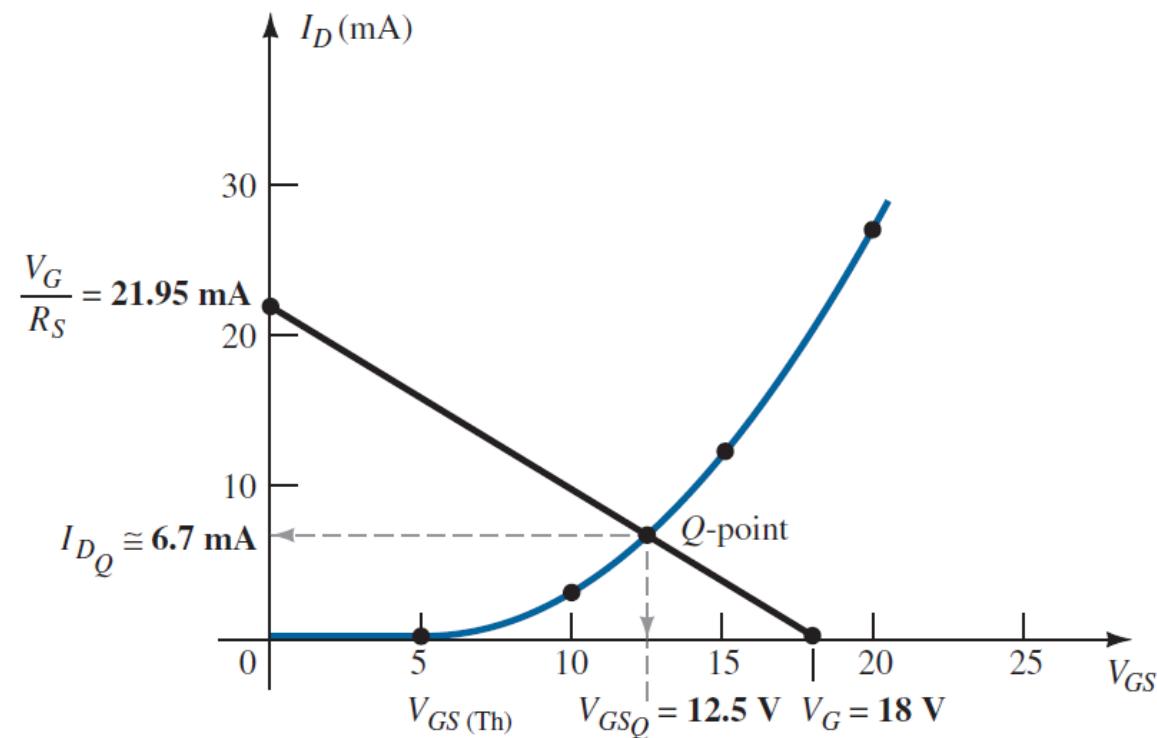
$$V_{GS} = V_G = 18V$$

When $V_{GS} = 0$ V,

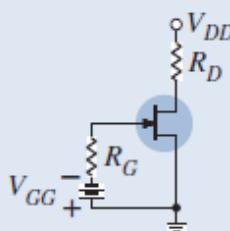
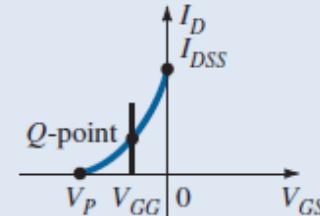
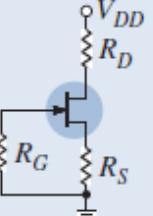
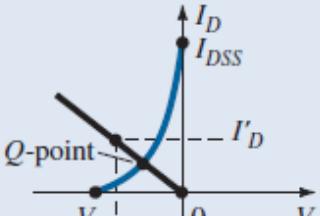
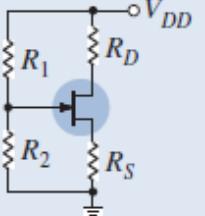
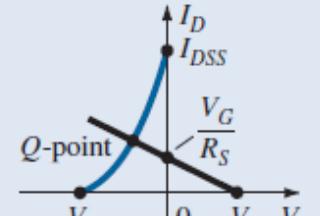
$$0 = 18 - I_D(0.82k\Omega) = 21.95mA$$

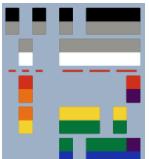
Plotted in Graph: $I_{DQ} = 6.7$ mA and $V_{GSQ} = 12.5$ V

$$\begin{aligned} V_{DS} &= V_{DD} - I_D(R_S + R_D) \\ V_{DS} &= 40V - 6.7\text{mA}(0.82k\Omega + 3k\Omega) \\ &= 14.4V \end{aligned}$$



FET Bias Configurations

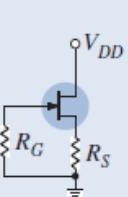
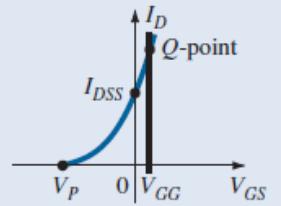
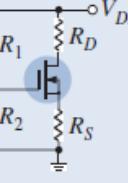
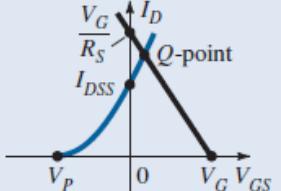
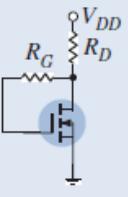
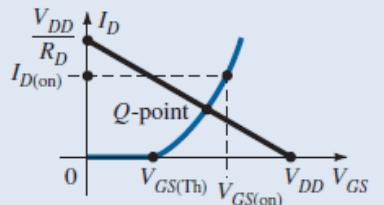
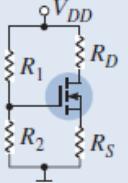
Type	Configuration	Pertinent Equations	Graphical Solution
JFET Fixed-bias		$V_{GSQ} = -V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
JFET Self-bias		$V_{GS} = -I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
JFET Voltage-divider bias		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	



FET Bias Configurations

JFET Common-gate		$V_{GS} = V_{SS} - I_D R_S$ $V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)$	
JFET ($R_D = 0 \Omega$)		$V_{GS} = -I_D R_S$ $V_D = V_{DD}$ $V_S = I_D R_S$ $V_{DS} = V_{DD} - I_S R_S$	
JFET Special case ($V_{GSQ} = 0 \text{ V}$)		$V_{GSQ} = 0 \text{ V}$ $I_{DQ} = I_{DSS}$	

FET Bias Configurations

Depletion-type MOSFET Fixed-bias (and MESFETs)		$V_{GSQ} = +V_{GG}$ $V_{DS} = V_{DD} - I_D R_S$	
Depletion-type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_S R_S$ $V_{DS} = V_{DD} - I_D(R_D + R_S)$	
Enhancement type MOSFET Feedback configuration (and MESFETs)		$V_{GS} = V_{DS}$ $V_{GS} = V_{DD} - I_D R_D$	
Enhancement type MOSFET Voltage-divider bias (and MESFETs)		$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$ $V_{GS} = V_G - I_D R_S$	