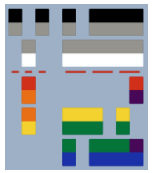
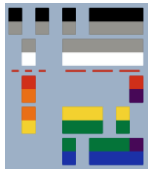
Transistor Amplifier Circuit Analysis



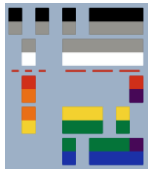
Introduction

- In the previous section we only determined the gain of transistor amplifier with input and output connected directly to the terminal of the transistor. In this module we will analyze the effects of our source resistor and load resistor to the single stage and multiple stage amplifier. Also the calculation of the individual effects of load resistor and source resistor, and both to the no-load gain will cover by this module.
- After finishing this topic, the students will learn the effect of RL and RS to amplifier circuit and can calculate the voltage-gain affected by the said resistances.

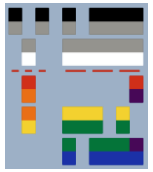


Topic Outcome

- 1. Analyze the effects of source resistor and Load resistor on the input and output impedance and overall gain of the Transistor Bias Circuit.
- 2. Discuss cascaded configurations with transistor amplifiers.

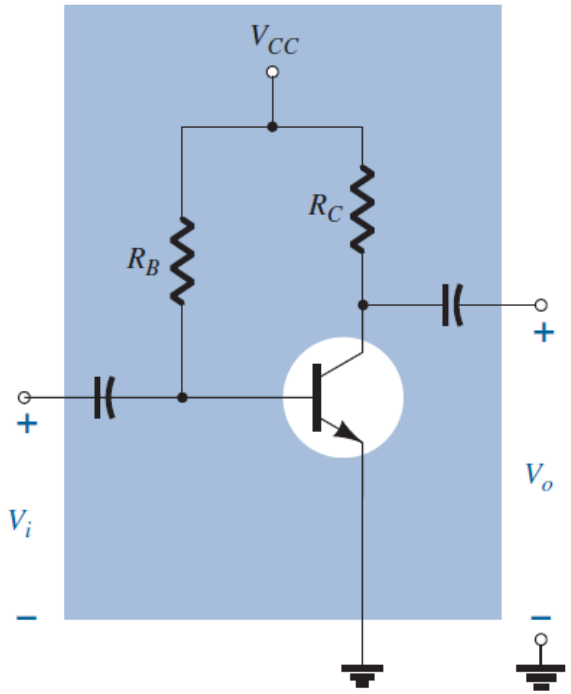


Effects of Source and Load Resistance

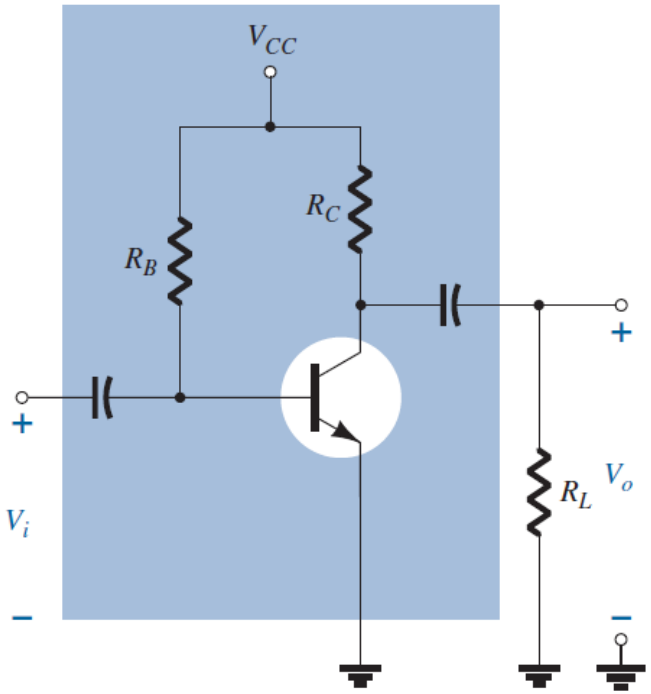


Effect of Source and Load Resistors

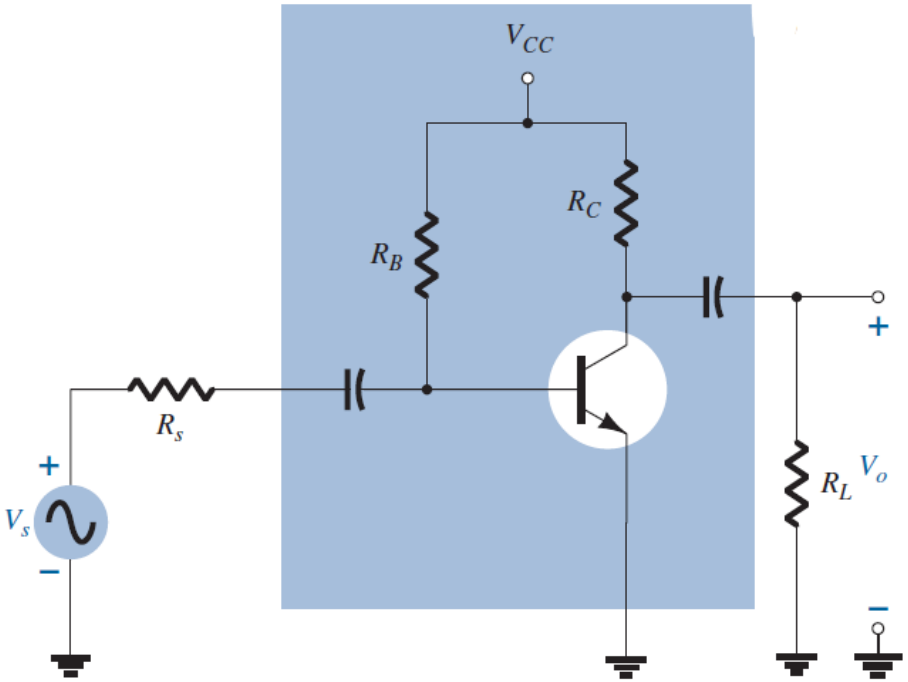
- All parameters determined in the previous lecture are for the unloaded amplifier whose input voltage is connected directly to the transistor.
- The circuit shown is a typical network with unloaded voltage gain specified in the previous lecture.



$$A_{v_{NL}} = \frac{V_o}{V_i}$$



$$A_{v_L} = \frac{V_o}{V_i}$$



$$A_{v_s} = \frac{V_o}{V_s}$$

Effect of Source and Load Resistors

- When source is added to the circuit, we can now derive the new voltage gain by simplifying the circuit.

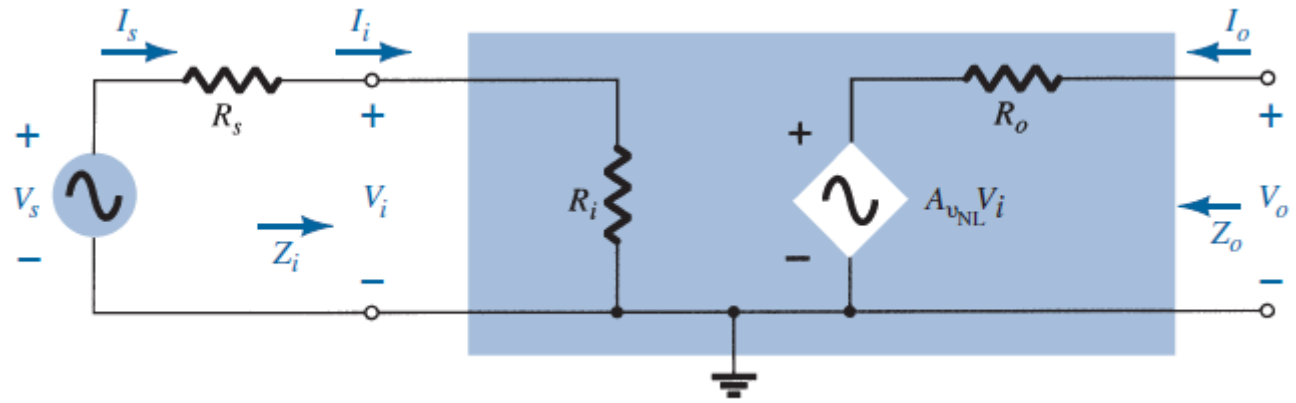
Where:

V_S = source voltage

$Z_i = R_i$

$Z_0 = R_0$

A_{VNL} = unloaded voltage gain/voltage gain at No-Load



Effect of Source and Load Resistors

- The voltage gain for this configuration is the ratio of the output voltage and the source voltage.

$$A_{VSO} = \frac{V_O}{V_S}$$

- The general term for voltage gain:

$$A_{VNL} = \frac{V_O}{V_I}$$

- Using voltage divider theorem at the input:, Vi wrt V_s

$$V_i = \frac{R_i}{R_i + R_s} V_s$$

- From the general term for voltage gain:

$$V_o = A_{VNL} V_i$$

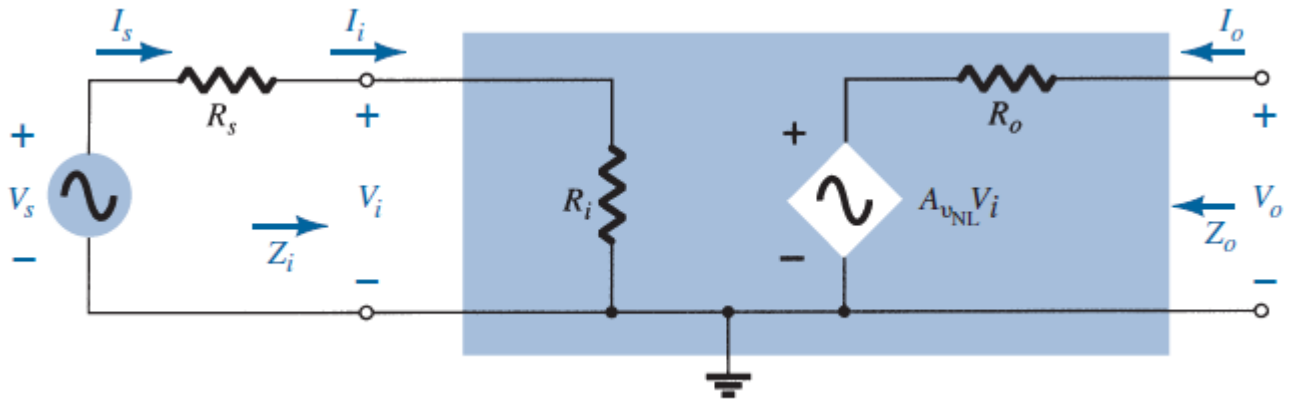
- Substituting the equation for V_i :

$$V_O = A_{VNL} V_s \frac{R_i}{R_i + R_s}$$

- Getting the equation for $A_{VSO} = \frac{V_O}{V_S}$

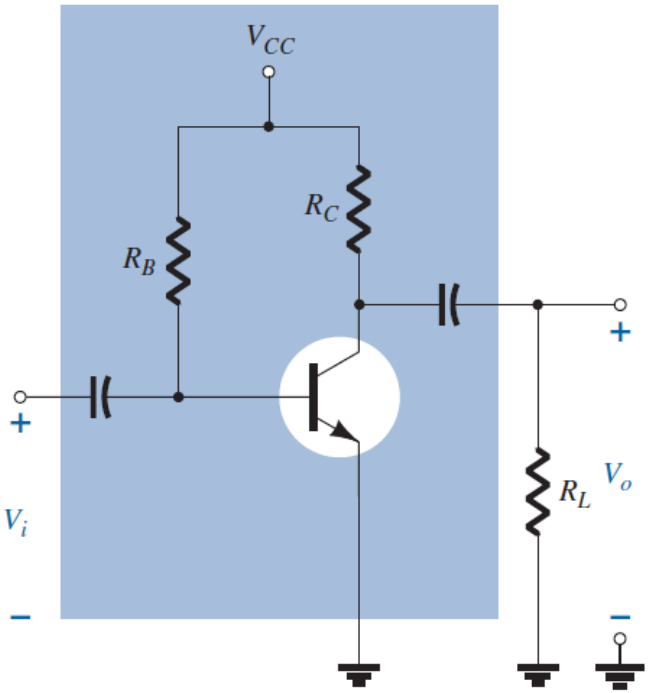
$$\frac{V_o}{V_s} = A_{VSO} = A_{VNL} \frac{R_i}{R_i + R_s}$$

Where A_{VSO} is the gain with the effect of the source resistor alone.

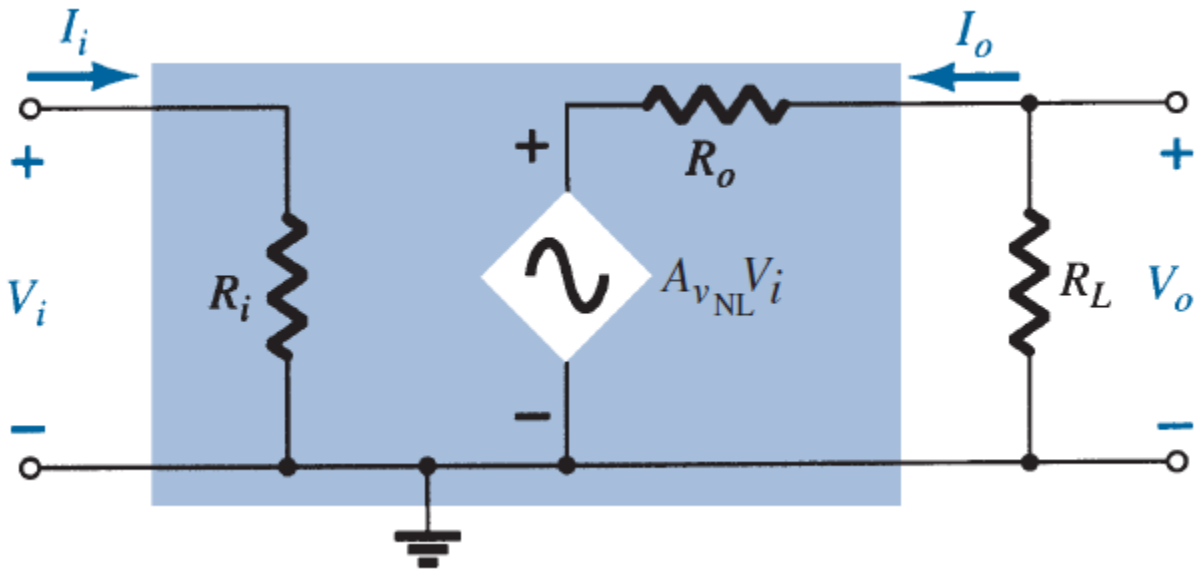


Effect of Source and Load Resistors

- The circuit below will be used to analyze the effects of the load resistance but without the source resistance. The loaded gain will change because the output impedance of the system is in series with R_L. Using the general equation for A_V, the output voltage will now be measured across the load resistor.



$$A_{v_L} = \frac{V_o}{V_i}$$



Effect of Source and Load Resistors

- The voltage across R_L in terms of A_{VNL} is:

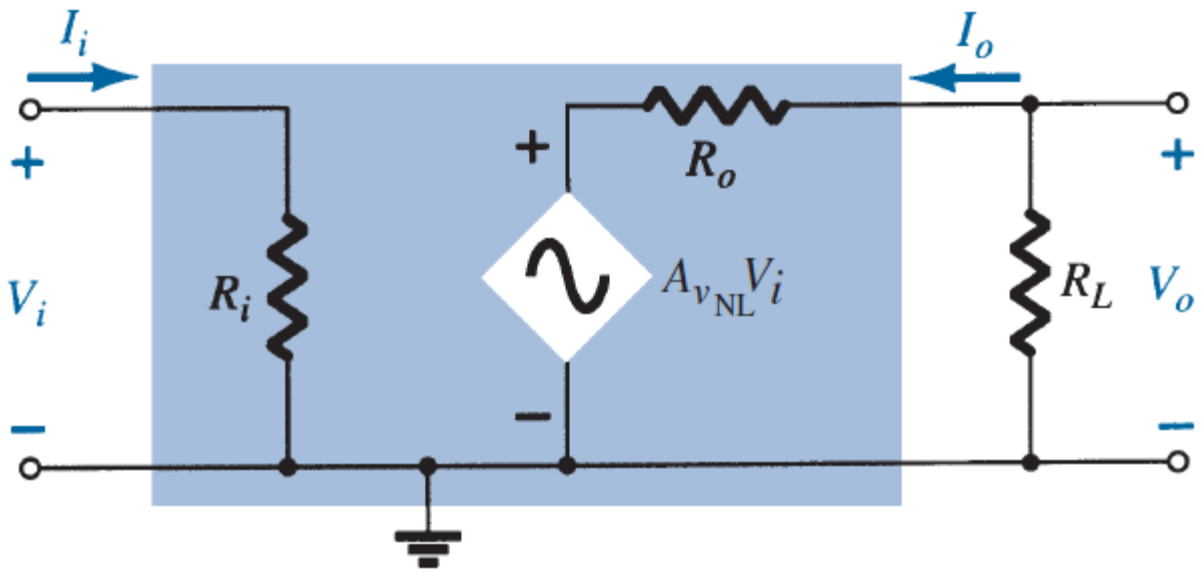
$$V_{R_L} = V_o = A_{VNL}\, V_i \left(\frac{R_L}{R_o + R_L}\right)$$

- Since

$$A_{VL} = \frac{V_o}{V_i} = \frac{A_{VNL}\, V_i \left(\frac{R_L}{R_o + R_L}\right)}{V_i}$$

- The equation for the loaded gain is:

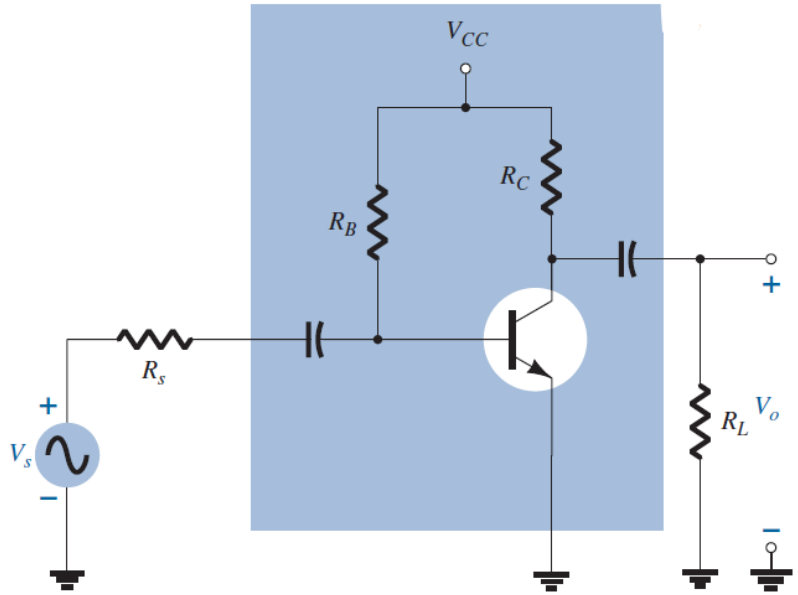
$$A_{VL} = A_{VNL} \left(\frac{R_L}{R_o + R_L}\right)$$



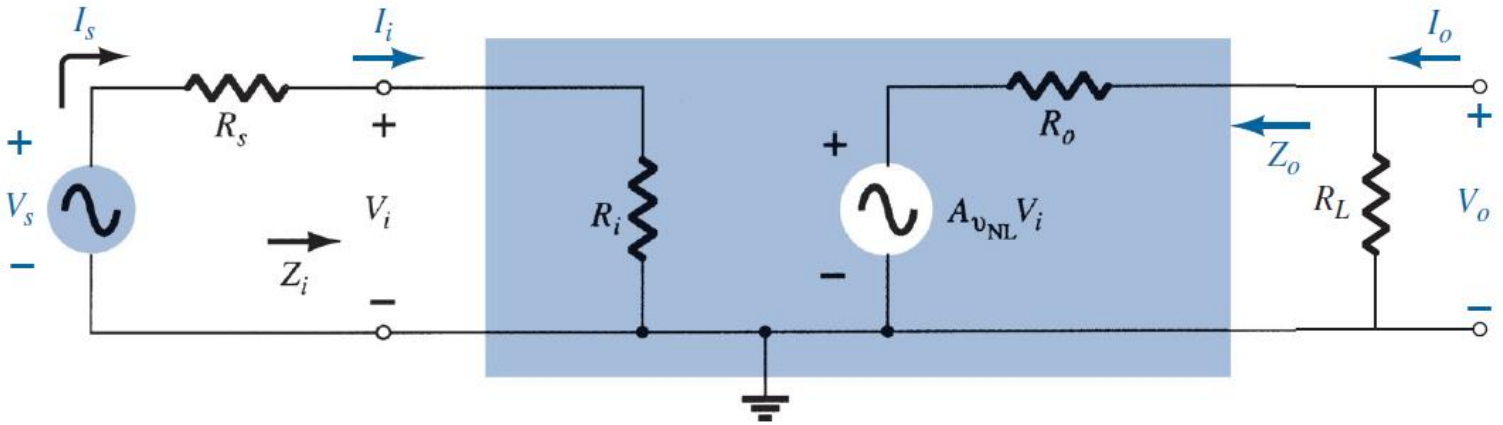
Where A_{VL} is the gain with the effect of the loaded resistor alone/loaded voltage gain

Effect of Source and Load Resistors

- To analyze the effects for both the source and load resistance, the circuit below will be used:



$$A_{v_s} = \frac{V_o}{V_s}$$



Effect of Source and Load Resistors

- Using the general equation for the voltage gain:

$$A_V = \frac{V_o}{V_i}$$

- The output voltage is measured across the load resistance while the input voltage is measured across the input impedance of the AC network from the source voltage. With the effects of both R_L and R_S the voltage gain is:

$$A_{VS} = \frac{V_o}{V_s} = \frac{V_o}{V_i} x \frac{V_i}{V_s}$$

- Since

$$V_o = V_{R_L} = A_{VNL} V_i \left(\frac{R_L}{R_o + R_L} \right)$$

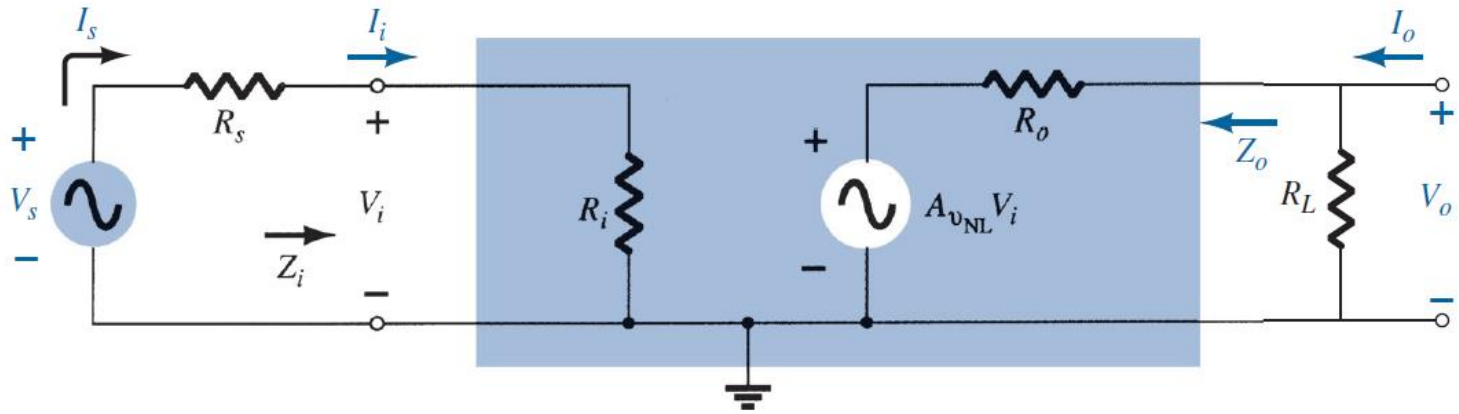
And

$$V_i = \frac{R_i}{R_i + R_S} V_S \; ; V_S = \frac{R_i + R_S}{R_i} V_i$$

Using substitution to determine the overall voltage gain:

$$A_{VS} = \frac{A_{VNL} V_i \left(\frac{R_L}{R_o + R_L} \right)}{\frac{R_i + R_S}{R_i} V_i}$$

$$A_{VS} = A_{VNL} \left(\frac{R_L}{R_o + R_L} \right) \left(\frac{R_i}{R_i + R_S} \right) = \mathrm{A_{VL}} \left(\frac{\mathrm{R_i}}{R_i + R_S} \right)$$

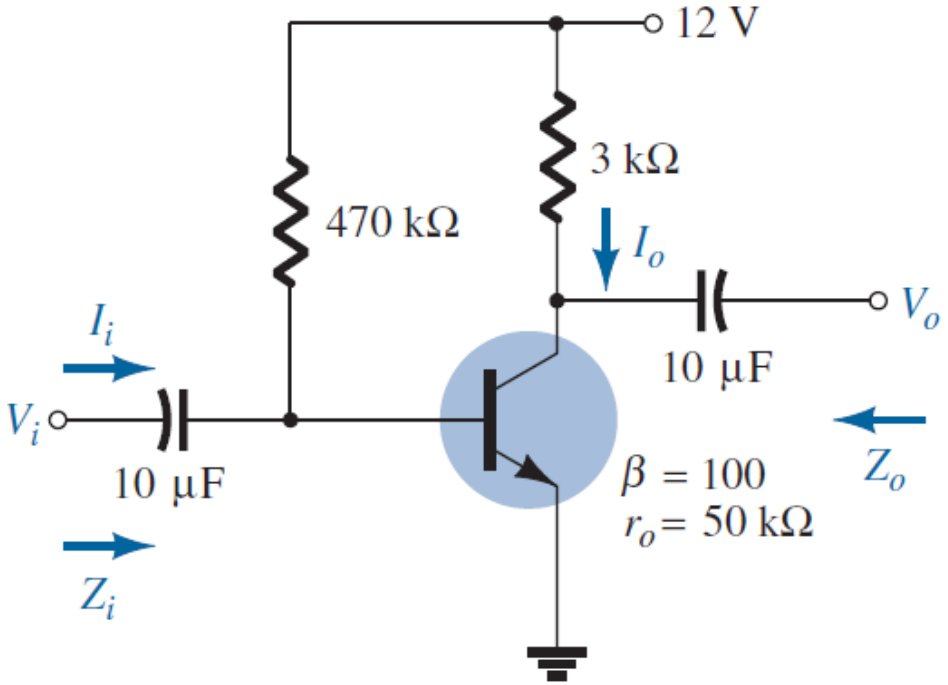


Effect of Source and Load Resistors

- Determine A_{vL} and A_{vs} for the network and compare solutions. Example 1 showed that A_{vNL} = -280, Zi = 1.07 kΩ, and Zo = 3 kΩ. And RL = 4.7 kΩ and Rs = 0.3 kΩ.

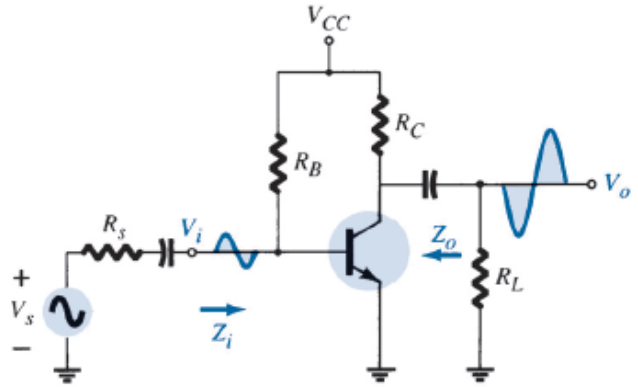
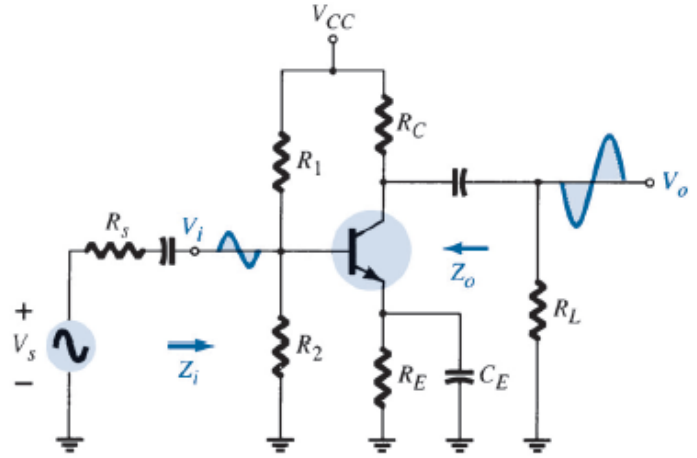
Solution

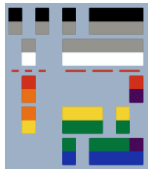
- $A_{VL} = \frac{V_o}{V_i} = \frac{R_L}{R_o+R_L} A_{VNL} = \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega+3\,\text{k}\Omega} * -280$
- $A_{VL} = -170.98$
- $A_{VS} = \frac{R_i}{R_i+R_s} \cdot \frac{R_L}{R_o+R_L} A_{VNL}$
- $A_{VS} = \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega+0.3\,\text{k}\Omega} \cdot \frac{4.7\,\text{k}\Omega}{4.7\,\text{k}\Omega+3\,\text{k}\Omega} * -280$
- $A_{VS} = -133.45$



A_{vNL} = -280, Zi = 1.07 kΩ, and Zo = 3 kΩ

Summary Tables

Configuration	$A_{v_L} = V_o/V_i$	Z_i	Z_o
	$\frac{-(R_L \\| R_C)}{r_e}$	$R_B \\| \beta r_e$	R_C
	Including r_o: $\frac{-(R_L \\| R_C \\| r_o)}{r_e}$	$R_B \\| \beta r_e$	$R_C \\| r_o$
	$\frac{-(R_L \\| R_C)}{r_e}$	$R_1 \\| R_2 \\| \beta r_e$	R_C
	Including r_o: $\frac{-(R_L \\| R_C \\| r_o)}{r_e}$	$R_1 \\| R_2 \\| \beta r_e$	$R_C \\| r_o$



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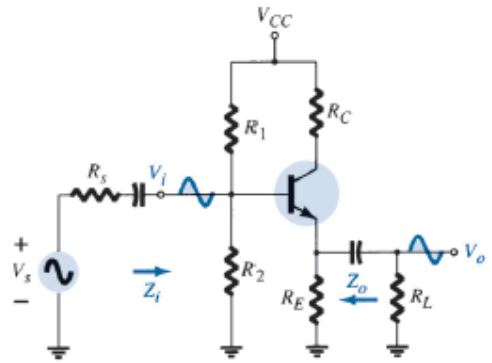
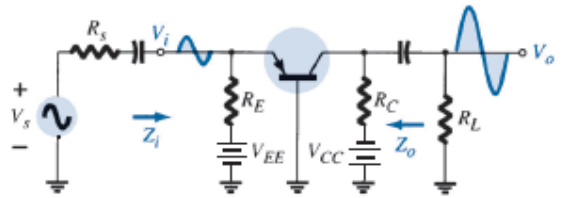
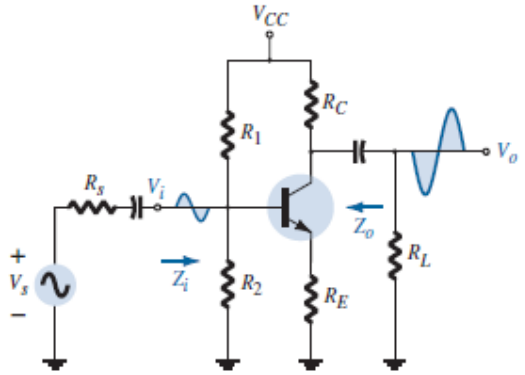
	$\cong 1$	$R'_E = R_L \| R_E$ $R_1 \| R_2 \| \beta(r_e + R'_E)$	$R'_s = R_s \| R_1 \| R_2$ $R_E \| \left(\frac{R'_s}{\beta} + r_e\right)$
	Including r_o: $\cong 1$	$R_1 \| R_2 \| \beta(r_e + R'_E)$	$R_E \| \left(\frac{R'_s}{\beta} + r_e\right)$
	$\cong \frac{-(R_L \| R_C)}{r_e}$	$R_E \| r_e$	R_C
	Including r_o: $\cong \frac{-(R_L \| R_C \| r_o)}{r_e}$	$R_E \| r_e$	$R_C \| r_o$
	$\frac{-(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_E)$	R_C
	Including r_o: $\frac{-(R_L \| R_C)}{R_E}$	$R_1 \| R_2 \| \beta(r_e + R_e)$	$\cong R_C$

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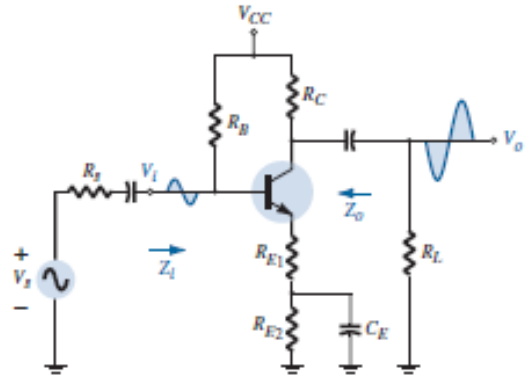
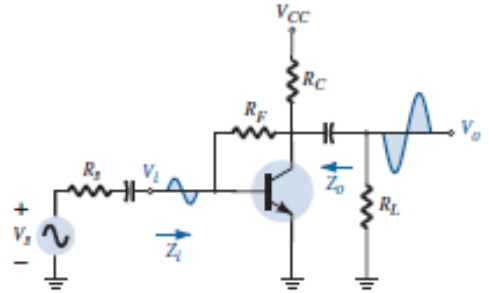
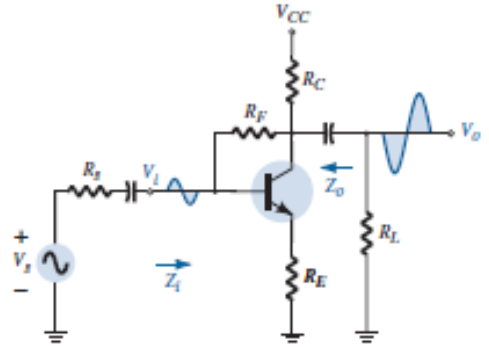
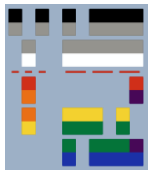
	$\dfrac{-(R_L \| R_C)}{R_{E_1}}$	$R_B \| \beta(r_e + R_{E_1})$	R_C
	Including r_o: $\dfrac{-(R_L \| R_C)}{R_{E_1}}$	$R_B \| \beta(r_e + R_E)$	$\cong R_C$
	$\dfrac{-(R_L \| R_C)}{r_e}$	$\beta r_e \| \dfrac{R_F}{\lvert A_v \rvert}$	R_C
	Including r_o: $\dfrac{-(R_L \| R_C \| r_o)}{r_e}$	$\beta r_e \| \dfrac{R_F}{\lvert A_v \rvert}$	$R_C \| R_F \| r_o$
	$\dfrac{-(R_L \| R_C)}{R_E}$	$\beta R_E \| \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \| R_F$
	Including r_o: $\cong \dfrac{-(R_L \| R_C)}{R_E}$	$\cong \beta R_E \| \dfrac{R_F}{\lvert A_v \rvert}$	$\cong R_C \| R_F$



Effect of Source and Load Resistors

- The R_S mentioned is the internal resistance of the voltage source.
- For FET analysis, we could use the variable R_{sig} for the source resistance.

Note that the load resistance appears in parallel with the drain resistance and the source resistance Rsig appears in series with the gate resistance R.

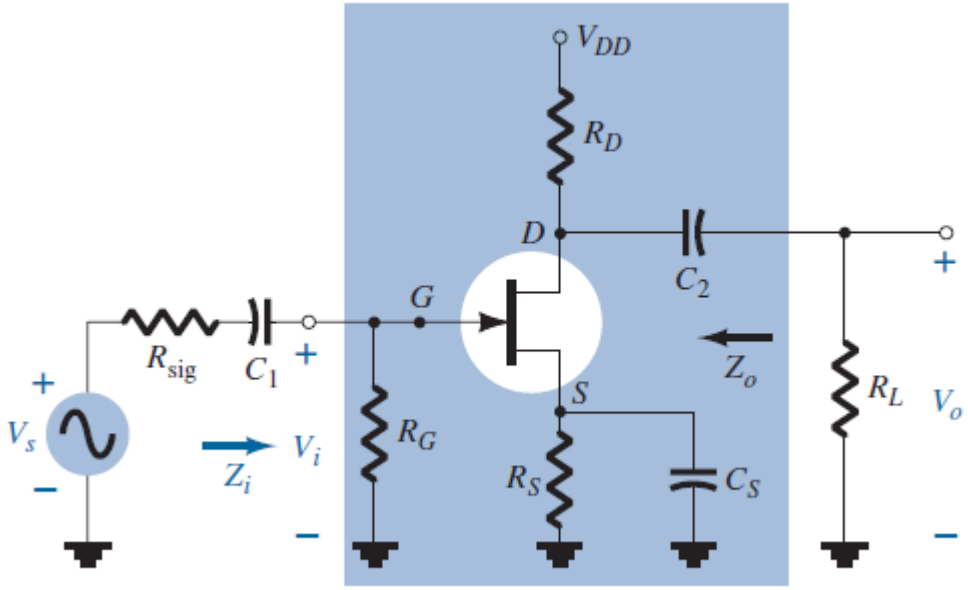
$$A_{VL} = -g_m\,(r_d||R_D||R_L)$$

For the overall gain A_{VS},

$$A_{VS} = \frac{R_G}{R_G+R_{sig}}[-g_m\,(r_d||R_D||R_L)]$$

which for most applications where $R_G >> R_{sig}$ and $R_D||R_L << r_d$ results in

$$A_{VS} \cong -g_m\,(R_D||R_L)$$



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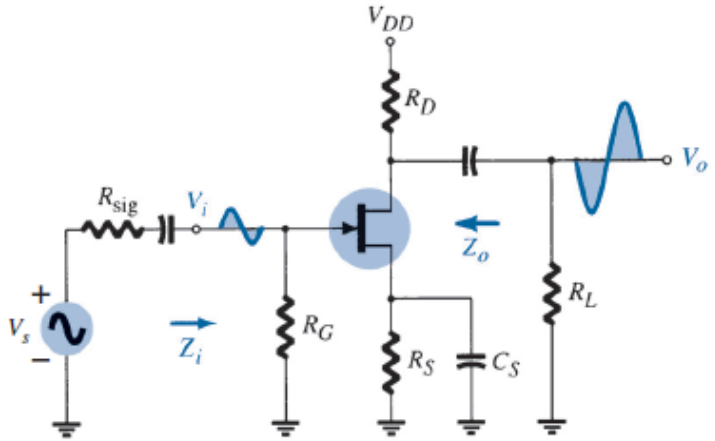
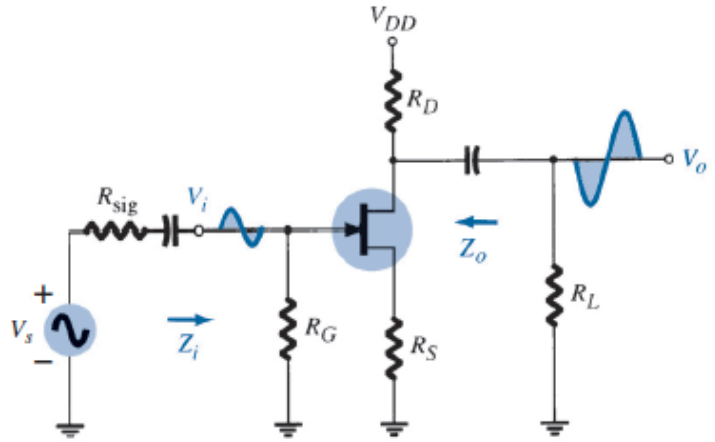
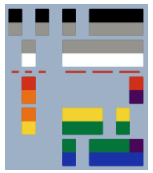
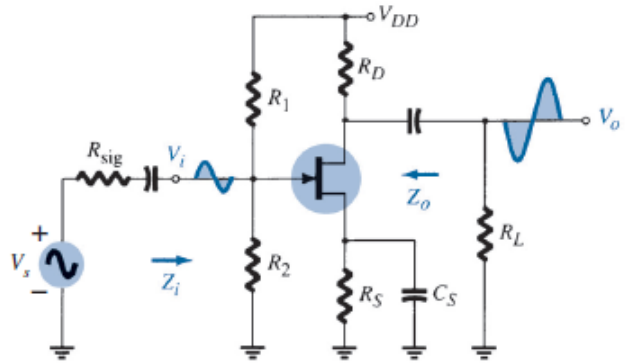
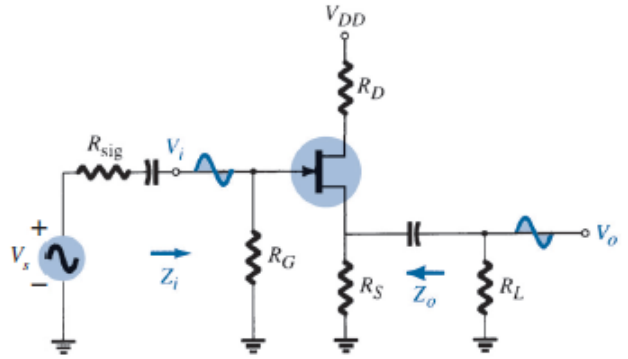
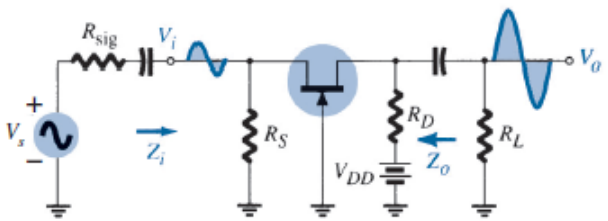
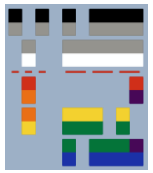
	$-g_m(R_D \| R_L)$ Including r_d: $-g_m(R_D \| R_L \| r_d)$	R_G R_G	R_D $R_D \| r_d$
	$\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S}$ Including r_d: $\dfrac{-g_m(R_D \| R_L)}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}}$	R_G R_G	$\dfrac{R_D}{1 + g_m R_S}$ $\cong \dfrac{R_D}{1 + g_m R_S}$

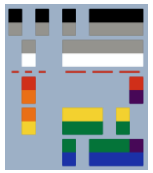


Summary Tables

	$-g_m(R_D \Vert R_L)$ Including r_d: $-g_m(R_D \Vert R_L \Vert r_d)$	$R_1 \Vert R_2$ $R_1 \Vert R_2$	R_D $R_D \Vert r_d$
	$\dfrac{g_m(R_S \Vert R_L)}{1 + g_m(R_S \Vert R_L)}$ Including r_d: $= \dfrac{g_m r_d (R_S \Vert R_L)}{r_d + R_D + g_m r_d (R_S \Vert R_L)}$	R_G R_G	$R_S \Vert 1/g_m$ $\dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D}}$
	$g_m(R_D \Vert R_L)$ Including r_d: $\cong g_m(R_D \Vert R_L)$	$\dfrac{R_S}{1 + g_m R_S}$ $Z_i = \dfrac{R_S}{1 + \dfrac{g_m r_d R_S}{r_d + R_D \Vert R_L}}$	R_D $R_D \Vert r_d$



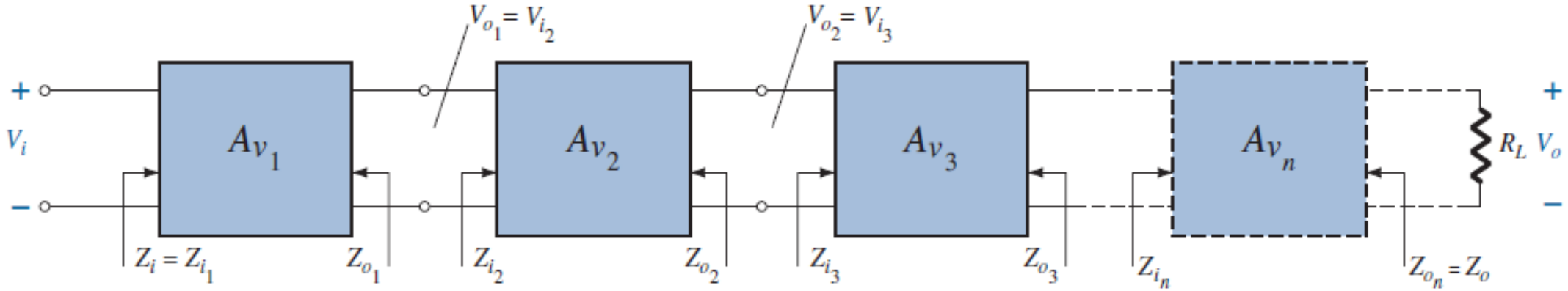
Cascaded Systems

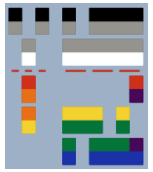


Cascaded Systems

- The two-port systems approach is particularly useful for cascaded systems such as the block diagram shown int the figure.
- The voltage gain of each of the individual stages are $A_{V_1}, A_{V_2}, A_{V_3}$ ... and so on under loaded conditions.
- A_{V_1} is determined with the input impedance of A_{V_2} acting as the load resistance of A_{V_1}(same as A_{V_2} to A_{V_3}, A_{V_3} to A_{V_4} ...)
- The total gain of the system is then determined by the product of the individual gains, that is:

$$A_{V_T} = A_{V_1} A_{V_2} A_{V_3} \ldots A_{V_n}$$

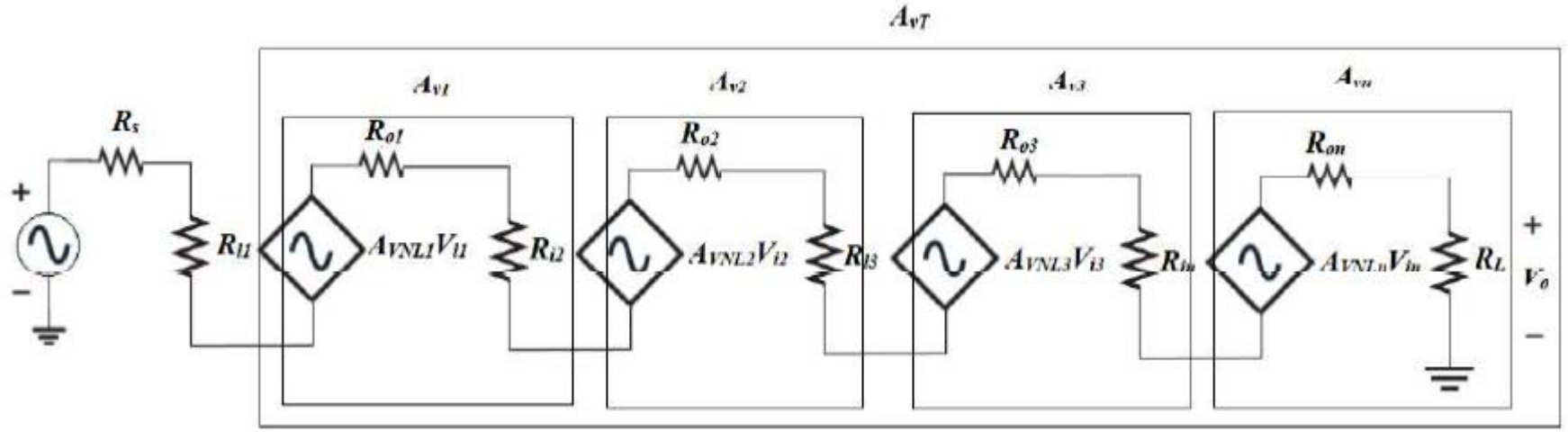




Cascaded Systems

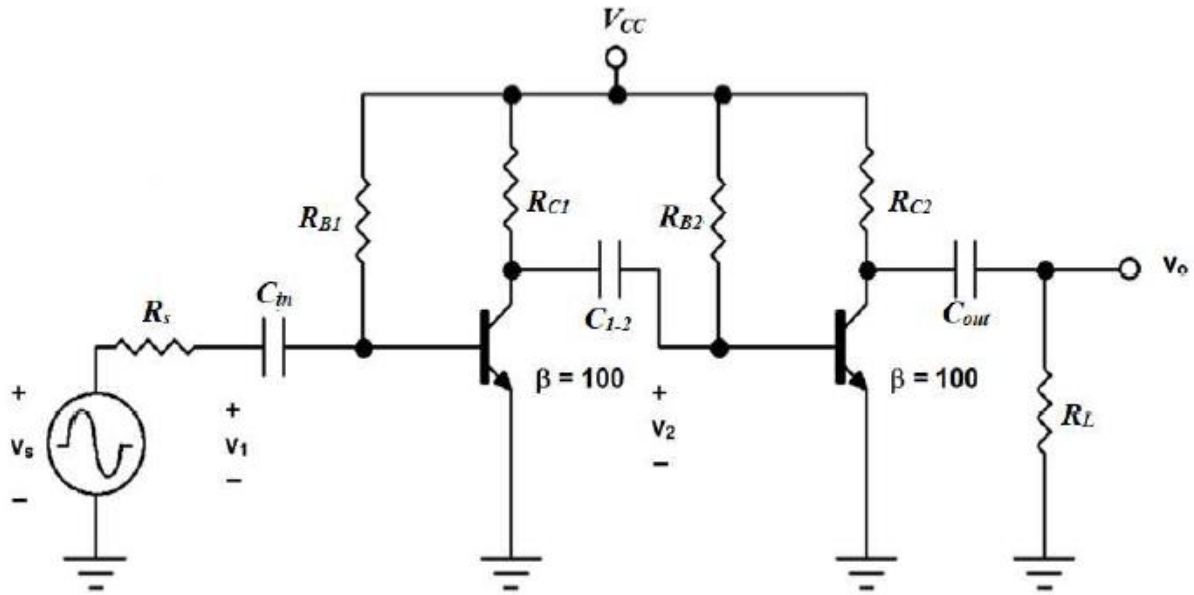
- The equivalent network model shown below will be used for better analysis and getting the overall gain of a cascaded network.
- The overall gain is:

$$A_{V_{S(Total)}} = A_{V_T}\left(\frac{R_i}{R_i + R_s}\right)$$



Cascaded Systems

- Considering the circuit shown, by DC analysis, we can determine the value of each individual I_E to be used on small signal analysis.
  - I_{E1} =emitter current for the first stage
  - I_{E2} =emitter current for the second stage



Cascaded Systems

- By DC analysis, the individual stage parameters are calculated:
  - First stage

$$r_{e1} = \frac{26\ mV}{I_{E1}}$$

Z_{i1} =input impedance (first stage)

Z_{o1}=output impedance (first stage)

A_{VNL1} = voltage gain (first stage)

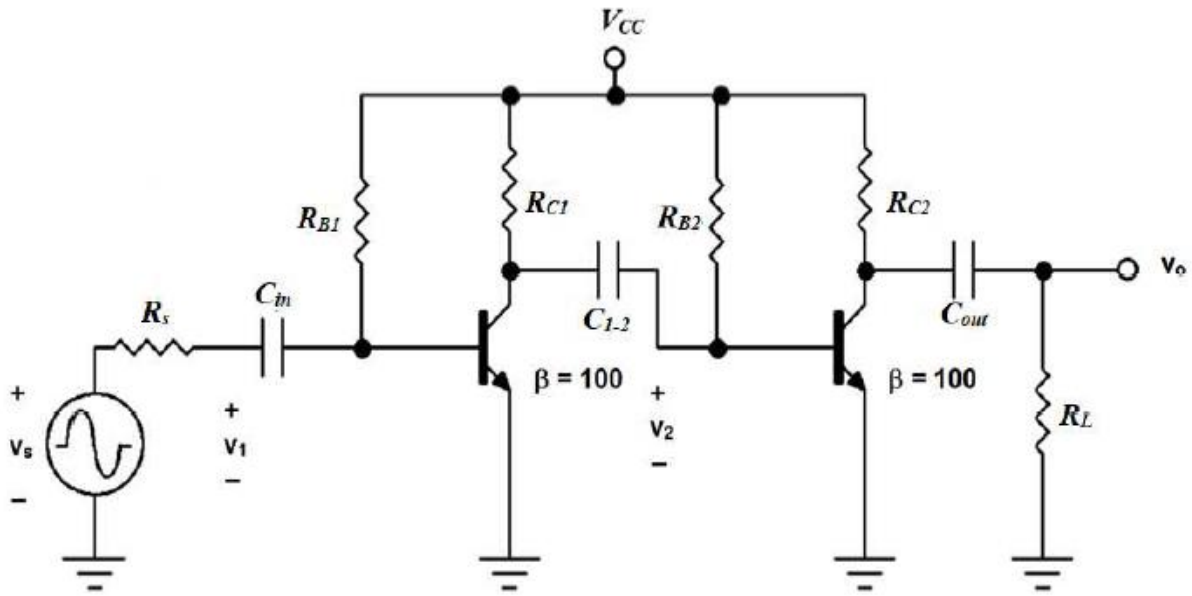
  - Second Stage

$$r_{e2} = \frac{26mV}{I_{E2}}$$

Z_{i2}=input impedance (second stage)

Z_{o2}=output impedance (second stage)

A_{VNL2}=voltage gain (second stage)



Cascaded Systems

- Computing for the individual gain looking at the network with the effects of the load resistors:

$$A_{V_1} = A_{VNL1}\left(\frac{R_{i2}}{R_{o1} + R_{i2}}\right)$$

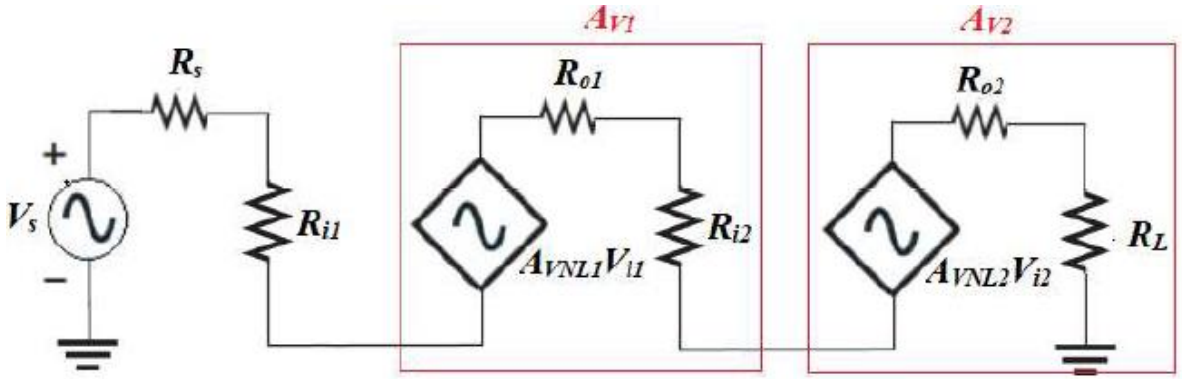
$$A_{V_2} = A_{VNL2}\left(\frac{R_L}{R_{o2} + R_L}\right)$$

- Solving for the total gain for A_V

$$A_{V(Total)} = A_{V_1}A_{V_2}$$

- The overall gain of the cascaded network is:

$$A_{V_{S(Total)}} = A_{V(Total)}\left(\frac{R_{i1}}{R_s + R_{i1}}\right)$$

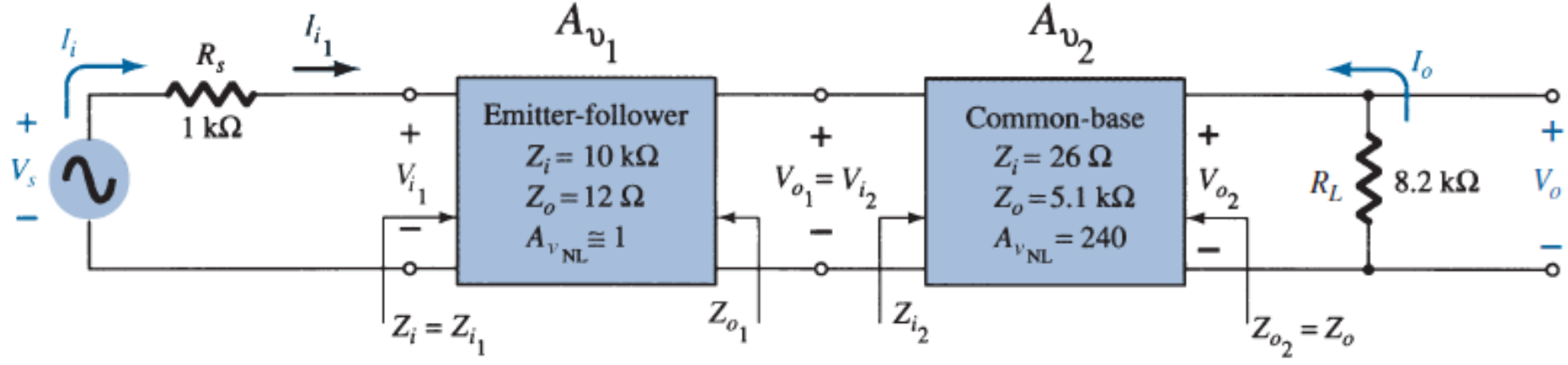


Cascaded Systems

- The two-stage system employs a transistor emitter-follower configuration prior to a common-base configuration to ensure that the maximum percentage of the applied signal appears at the input terminals of the common-base amplifier. In the figure, the no-load values are provided for each system, with the exception of *Zi* and *Zo* for the emitter-follower, which are the loaded values. For the configuration of the figure, determine:

a. The loaded gain for each stage.

b. The total gain for the system, *Av* and *Avs*.



Cascaded Systems

a. For the emitter-follower configuration, the loaded gain is

$$V_{o1} = \frac{Z_{i2}}{Z_{i2}+Z_{o1}} A_{vNL} V_{i1} = \frac{26\Omega}{26\Omega+12\Omega}(1)V_{i1} = 0.684V_{i1}$$

and $A_{v1} = \frac{V_{o1}}{V_{i1}} = 0.684$

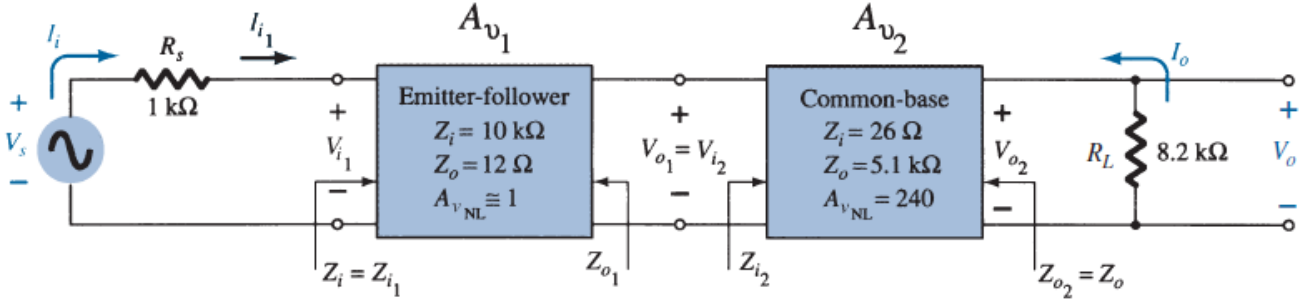
For the common-base configuration,

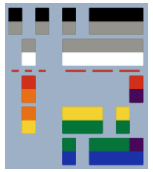
$$V_{o2} = \frac{R_L}{R_o+R_L} A_{vNL} V_{i2} = \frac{8.2\ k\Omega}{8.2\ k\Omega+5.1\Omega}(240)V_{i2}$$

and $A_{v2} = \frac{V_{o1}}{V_{i1}} = 147.97$

b. $A_{vT} = A_{v1} A_{v2} = (0.684)(147.97) = 101.2$

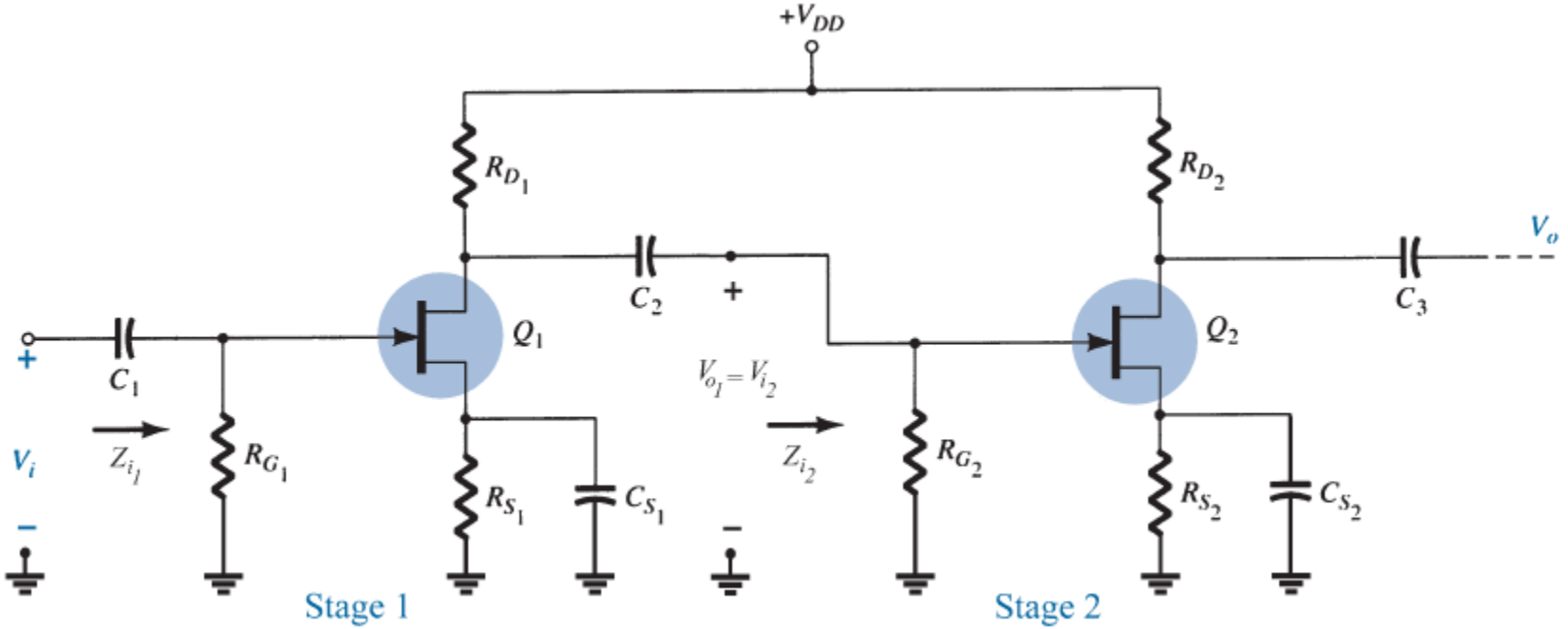
$$A_{vs} = \frac{Z_{i1}}{Z_{i1}+R_s} A_{vT} = \frac{10\ k\Omega}{10\ k\Omega+1\ k\Omega}(101.2) = 92$$





Cascaded Systems

- The total gain is the product of the gain of each stage including the loading effects of the following stage.
- $A_{VT} = A_{V1} \cdot A_{V2} = (-g_{m1}\, R_{D1})(-g_{m2}\, R_{D2}) = g_{m1}\, g_{m2}\, R_{D1}\, R_{D2}$



Important Conclusions and Concepts

- The total gain of a multistage amplifier is the product of the individual gains.
- Single-stage amplifiers can be connected in sequence with capacitively-coupling and direct coupling methods to form multistage amplifiers.
- The gain obtained with a source resistance in place will always be less than that obtained under loaded or unloaded conditions due to the drop in voltage across the source resistance.
- For the same configuration $A_{VNL} > A_{VL} > A_{VS}$
- For a particular design, the larger the level of R_L, the greater is the level of the AC voltage gain.
- For a particular amplifier, the smaller internal resistance of the signal source, the greater is the overall gain.
- For any network that has coupling capacitors, the source and load resistance does not affect the DC biasing levels.