A FIFO is a memory block that works like a queue: the first data in is the first data out.

The depth of the FIFO (number of memory cells) is set by the ***depth_g*** (depth) generic value. The depth is **5** by default.

The data to be written ***data_in*** is written, when the signal ***we_in*** (write enable) is high during the rising edge of the clock signal ***clk*** (clock). The data is stored until it is read away.

The read data ***data_out*** is output, when the signal ***re_in*** (read enable) is high during the rising edge of the clock signal ***clk*** (clock). The data read is the oldest data written into the FIFO.

If the memory is full, the signal ***full_out*** (full) is **high**.

If the memory is empty, the signal ***empty_out*** (empty) is **high**.

If the FIFO has only one data cell to be read, the signal ***one_d_out*** (one data) is **high**.

If the FIFO has only one free space for data to be written, the signal ***one_p_out*** (one place) is **high**.

The FIFO is in reset state when the signal ***rst_n*** (reset) is **low**. The FIFO is empty after the **reset.**

Example block diagram: